Conversion analogique numérique Sigma Delta reconfigurable à entrelacement temporel

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Reconfigurable Parallel Delta Sigma Analog to Digital Converters

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Abstract

Nowadays, communication devices are supporting an increasing number of standards. The diversity of the requirements in terms of speed and resolution, makes the design of a single low power analog to digital converter (ADC) suitable for all the scenarios very problematic. Reconfigurable ADCs are a solution to this problem, where resolution would be exchanged for bandwidth. Classical $\Delta\Sigma$ ADCs offer an easy way to perform this exchange by adjusting their oversampling ratios. However, they are not suitable for wideband applications. Parallelizing $\Delta\Sigma$ ADCs overcomes this problem and in addition, increases the reconfigurability of the ADC.

In this work, a fully reconfigurable Time-interleaved $\Delta\Sigma$ ADC is proposed. Its reconfigurability permits it to perform resolution-bandwidth trade-off as well as power consumption-bandwidth trade-off by adjusting the operation frequency, the number of active channels, the oversampling ratio and the modulator order. A novel interpolation technique is also proposed. It allows to downscale the capacitor sizes that may otherwise reach unreasonable values if large resolutions are required and relaxes the constraints on the anti-alias filter as well.

A prototype of the presented Time-interleaved $\Delta\Sigma$ ADC has been realized in a 1.2 V 65 nm CMOS technology. It was designed to fulfill the requirements of GSM, EDGE, UMTS, DVBT, WiFi and WiMax standards. For the GSM/EDGE scenario, a 80 dB SNR was measured. For the rest of scenarios, the performances were not secured but the functionality was tested successfully.

Contents

List of Abbreviations and Symbols

Abbreviations

ADC	Analog to Digital Converter
AAF	Anti-Alias Filter
$\Delta\Sigma$	Delta Sigma
BP	Band Pass
BPS	Bottom Plate Sampling
CT	Continuous Time
DAC	Digital to Analog Converter
dBFS	dB Full Scale
DR	Dynamic Range
DT	Discrete Time
FBD	Frequency Band Decomposition
FI	Frequency Interleaved
FoM	Figure of Merit
GBW	Gain-bandwidth product
GMSCL	Generalized Multi Stage Closed Loop
HD2	Second Harmonic Distortion
HD3	Third Harmonic Distortion
HFB	Hybrid Filter Bank
HP	High pass
LP	Low Pass
NTF	Noise Transfer Function
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PSD	Power Spectral Density
S/H	Sample and Hold
SC	Switched capacitor
SFDR	Spurious Free Dynamic range
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal To Noise Ratio
SR	Slew Rate
STF	Signal Transfer Function
STHD	Signal to Total Harmonic Distortion ratio
TI	Time Interleaved

Symbols

B	Signal Bandwidth
C_s	Sampling capacitor
C_{int}	Integration Capacitor
$\delta()$	Dirac's delta function
f_{in}	Sinusoidal input signal frequency
f_{op}	Operation frequency of the electrical blocks
f_s	Sampling frequency, two times the signal bandwidth B
$f_{S/H}$	Operating frequency of the S/H in the TI $\Delta\Sigma$ ADCs
f_u	Unitary frequency
G	Quantizer gain
k	The number of CT integrators in a L^{th} order hybrid modulator
K	$\frac{N}{M}$
K_{bol}	Boltzmann constant
L	$\Delta\Sigma$ modulator order
M	Number of channels
n	Number of bits of the quantizer
N	Interpolation factor for TI $\Delta\Sigma$ ADCs
P	Power
σ	Standard deviation
T	Temperature in Kelvin
τ	Time constant
V_p	Peak voltage
V_{pp}	Peak to peak voltage
$Vref$	ADC Reference Voltage
V_{th}	Threshold voltage

Résumé Français

I Introduction

La prolifération d'un grand nombre de normes sans fil et la nécessité d'avoir des dispositifs de communication les supportant tous à la fois ont entraîné une forte demande pour des puces adaptées à la réception multi-standard. Compte tenu des contraintes élevées sur la consommation électrique à l'extrémité mobile, une mise en œuvre efficace de ces puces nécessite la reconfiguration du récepteur pour lui permettre de s'adapter aux différentes normes.
Un élément clé de n'importe quel récepteur et surtout dans un récepteur multi-standard est le convertisseur analogique-numérique (CAN). La diversité des exigences en termes de vitesse et de résolution des normes radio rend la conception d'un CAN multi-standard une tâche difficile. Le CAN Sigma Delta $\Sigma\Delta$ est un bon candidat pour atteindre des hautes résolutions (supérieures à 12 bits) qui sont requises pour certaines normes radio telles que le EDGE et le GSM. En fait, le suréchantillonnage et la mise en forme du bruit qui sont les deux principes fondamentaux du CAN $\Sigma\Delta$ le rendent robuste contre les non-idéalités électroniques et ainsi lui permettent d'atteindre des résolutions plus élevées que les convertisseurs type Nyquist [1] [2]. Par ailleurs, le CAN $\Sigma\Delta$ offre un moyen facile d'effectuer un échange entre vitesse et résolution en ajustant leur rapport de suréchantillonnage (OSR). Cependant, leur bande passante est étroite par rapport aux spécifications de certains standards radio comme le WiMax ou des normes sans fil futures.

Plusieurs techniques basées sur le parallélisme permettent d'augmenter la bande de conversion des CAN $\Sigma\Delta$ classiques: les CAN $\Sigma\Delta$ à entrelacement temporel [3], les CAN $\Pi\Sigma\Delta$ [4], les CAN $\Sigma\Delta$ filtrage de bloc [5] et les CAN $\Sigma\Delta$ à décomposition en bande de fréquence [6]. Par ailleurs, le parallélisme fournit un paramètre supplémentaire de reconfiguration qui est le nombre de canaux actifs. Cela permet de réaliser un échange entre vitesse et consommation de puissance.
Le but de ce travail est de concevoir un CAN $\Sigma\Delta$ parallèle et reconfigurable adapté à la réception multi-standards.

Ce résumé en français est composé de six sections. La section II discute l'utilisation du parallélisme en pointant ses avantages par rapport à une solution à un seul canal et en montrant également ses principaux inconvénients. La section III donne un aperçu du fonctionnement des modulateurs $\Sigma\Delta$. Elle présente aussi deux comparaisons. La première est entre les implémentations temps continu, temps discret et hybride. La seconde compare les modulateurs passe-bas aux modulateurs passe-haut. Ces deux analyses permettront d'expliquer en détail le fonctionnement des modulateurs $\Sigma\Delta$ et de choisir l'implémentation (temps continu, temps discret ou hybride) et la mise en forme de bruit (passe-bas ou passe-haut) les mieux adaptées pour le modulateur qui sera utilisé dans le CAN parallèle. Dans la section IV, on justifie le choix de l'architecture à entrelacement temporel par rapport aux autre architectures paral-

lèles. On présente également les incovénients majeurs de cette architecture et on expose une nouvelle technique d'interpolation qui permet de les réduire considérablement. La section V présente la conception en CMOS 65 nm d'un CAN ΣΔ à entrelacemnt temporel adapté aux normes GSM, EDGE, UMTS, DVB-T, WiFi et WiMax. Ce CAN emploie la technique d'interpolation présentée dans la section IV. Cette section présente les résultats de mesure également. Ce résumé est conclu dans la section VI.

II Parallélisme

II.a Variation de la consommation en fonction de la fréquence

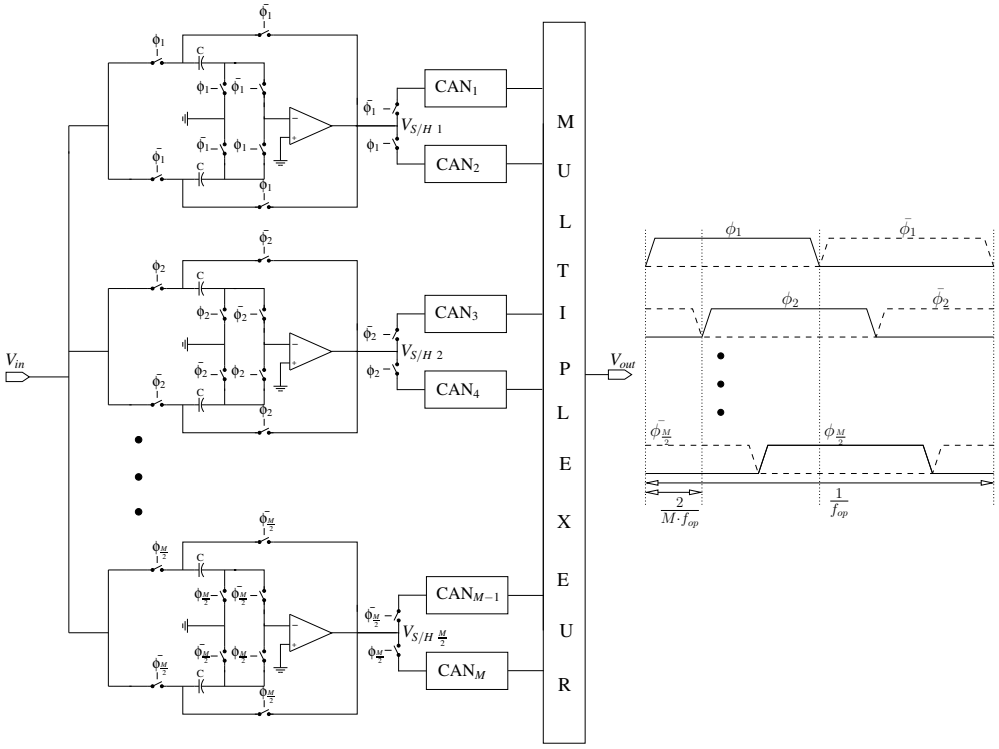


Figure 1: Circuit d'un CAN à entrelacement temporel

Avec la prévalence des applications à haut débit et à haute résolution, les CANs sont considérés comme l'un des éléments clés dans tout système. Deux approches principales pour améliorer leurs vitesses existent. La première consiste à augmenter la performance des blocs du CAN, ceci se paye par une augmentation de la consommation. La deuxième approche est l'utilisation du parallélisme. Afin de comparer ces deux approches, nous proposons d'examiner le comportement de la consommation en fonction de la fréquence. Pour cela, nous considérons le circuit d'un CAN à entrelacement temporel ayant M canaux (figure 1). Chaque canal est constitué d'un échantillonneur bloqueur (S/H) et d'un CAN. Les sorties numériques des différents CANs sont multiplexées pour reformer le signal en sortie. La vitesse global du CAN est donnée alors par:

$$f_s = M \cdot f_{op} \tag{1}$$

Avec f_{op} la fréquence d'opération du canal

Le S/H est un des blocs les plus critiques du CAN car, d'une part, il traite des signaux continus et d'autre part, les erreurs introduites à ce niveau se retrouvent tel quel à la sortie [19]. Ainsi, son optimisation est nécessaire pour atteindre les performances requises. La principale source de consommation de puissance dans le S/H est l'amplificateur opérationnel à transconductance (OTA). Les erreurs introduites par ce dernier apparaissent à la sortie du S/H principalement sous formes de distorsions et peuvent être mesurées en utilisant le rapport signal sur la somme des distorsions harmoniques ($STHD$). Par conséquent, nous allons utiliser la figure de mérite (FoM) de l'équation 2 pour mesurer sa performance:

$$\text{FoM} = \frac{P}{2^{(STHD-1.76)/6.02} \times f_s}, \tag{2}$$

Avec P la consommation de puissance

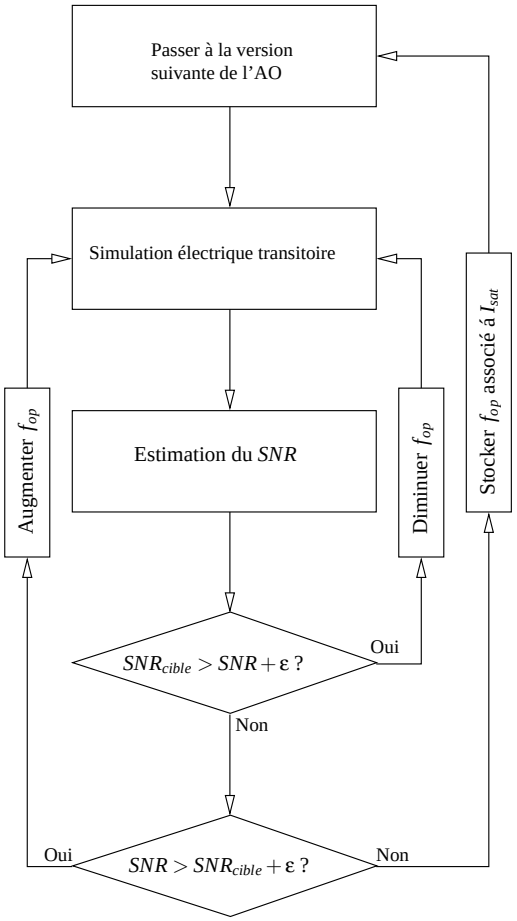


Figure 2: Algorithme utilisé pour trouver f_{op}

Les distortions introduites par l'OTA dépendent principalement de la portion de temps pendant laquelle ce dernier fonctionne dans le régime de saturation (SR). Ainsi, plus on va augmenter la fréquence opération, plus l'effet du SR sera important. La diminution du temps de saturation se fait principalement en augmentant le courant I_{sat} de l'étage de sortie de l'OTA . Ceci cause évidement une augmentation de la puissance consommée. Par conséquent, pour trouver la relation convoitée entre puissance et fréquence, la technique qu'on propose

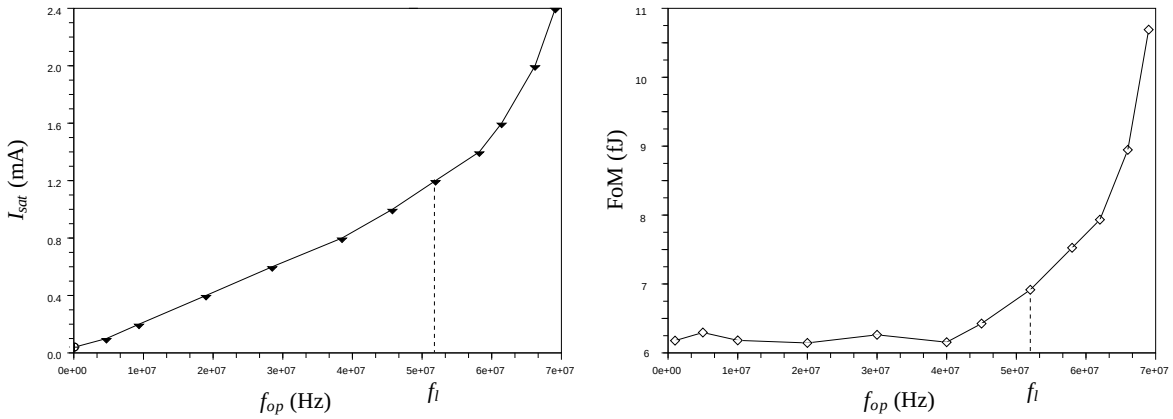


Figure 3: a)I_{sat} en fonction de f_{op} b)FoM en fonction de f_{op}

consiste à trouver les courants I_{sat} nécessaires pour atteindre une résolution donnée pour différentes valeur de f_{op}. Les différentes étapes de la technique sont comme suit:

1. On commence par choisir une architecture d'OTA et en conçoit plusieurs versions qui partagent les mêmes paramètres excepté le courant de saturation I_{sat}.

2. On fixe une valeur de $STHD$ qu'on notera $STHD_{cible}$ qui sera la valeur de linéarité visée. Cette valeur dépendra de la résolution voulue à la sortie du CAN.

3. A l'aide de l'algorithme de la figure 2, pour chaque version de l'OTA, on détermine la fréquence d'opération f_{op} pour laquelle $\mid STHD_{V_{S/H}} - STHD_{target} \mid < \varepsilon$ est trouvée

Et donc ainsi on pourra établir une relation entre courant et fréquence.
Cette technique a été appliquée à une architecture d'OTA cascode replié conçu dans une technologie CMOS 65 nm. Tous les autres composants du S/H ont été implémentés à l'aide de modèles quasi-idéaux pour isoler les erreurs de l'OTA. Douze versions de l'OTA ont été conçues. Leurs courants I_{sat} varient entre 0.1 mA et 2.4 mA. Le $STHD_{cible}$ visé est de 72 dB et ϵ est de 0.5 dB.

Les résultats obtenus sont présentés sur la figure 3 a). On peut noter que la courbe est linéaire pour les basses fréquences et devient exponentielle pour les fréquences élevées. Le comportement linéaire est limitée dans ce cas à 52 MHz. Ce comportement est en fait prévisible, car l'augmentation de f_{op} va diminuer le temps de blocage et ainsi pour préserver le même $STHD$, I_{sat} doit être augmenté afin de réduire la portion de temps pendant laquelle l'OTA est en SR. L'augmentation de I_{sat} se fait par une augmentation des dimensions des transistors des sources de courant. Cette augmentation sera accompagnée par une augmentation des capacités parasites de l'OTA, et ainsi une partie du courant est réservée pour charger de ces capacités.
Dans la figure 3 b), la courbe de la FoM en fonction de f_{op} est tracée en utilisant les résultats de la même simulation. La courbe est caractérisée par une bande de fréquence $f_{op} < f_l$ pour laquelle la FoM est constante et minimale (+10 % du minimum). Pour des fréquences plus élevées, la courbe de la FoM a une allure exponentielle. Par conséquent, pour préserver la plus faible possible FoM, le fonctionnement à des fréquences plus élevées que f_l devrait être évité en utilisant le parallélisme. Idéalement, la consommation électrique du système à entrelacement temporel sera M fois plus élevé que celle d'un seul canal et comme sa bande de conversion est également multipliée par M, son FoM sera minimale, même si $f_s > f_l$. Malheureusement,

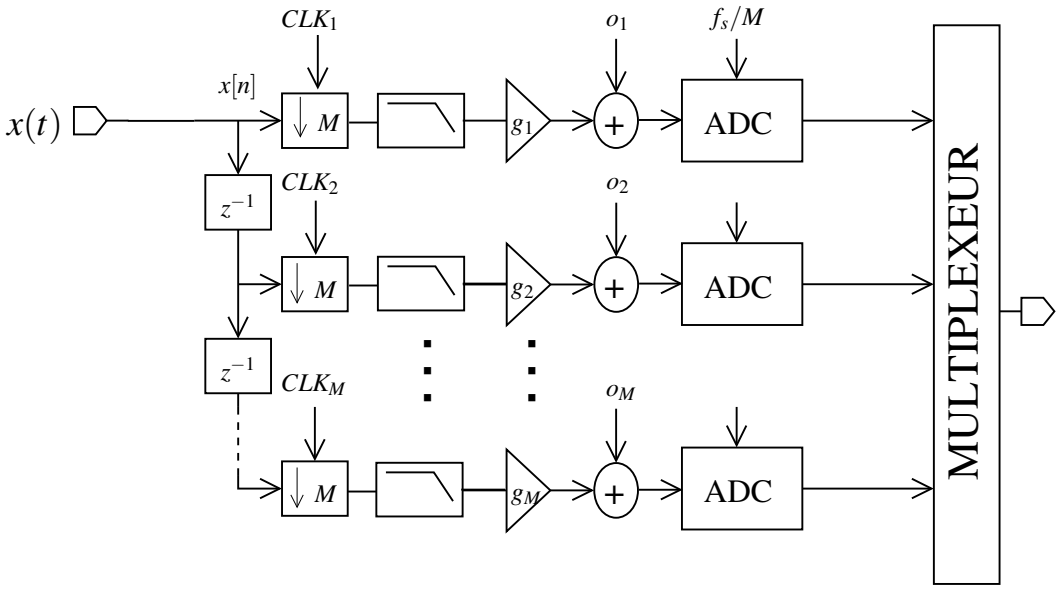


Figure 4: CAN à entrelacement temporel

cette hypothèse n'est pas tout à fait correcte. En fait, le parallélisme introduit de nouvelles erreurs qui doivent être corrigées. Ces erreurs seront discutées dans la sous-section suivante.

II.b Désavantages du parallélisme

Une bonne reconstruction du signal à la sortie d'un CAN à entrelacement temporel requiert que les différents canaux soient identiques. Malheureusement, ceci n'est pas possible en pratique à cause des variations du procédé de fabrication, de température et de tension d'alimentation entre les canaux. Ceci va se traduire par l'apparition de quatre types de désappariements:

- Désappariement de gain
- Désappariement d'offset
- Décalage d'horloge
- Désappariement de bandes

Ces différentes erreurs causent l'apparition de distortions dans la bande passante du signal. Les désappariements de gain et de bande et le décalage horloge génèrent des distortions à $f_s/M \pm i \times f_{in}$ avec $1 < i < M$. Cependant, le désappariement d'offset engendrent des distortions à $i \times f_s/M$ avec $1 < i < M$. La figure 5 représente le spectre en sortie d'un CAN 4 canaux en présence des quatre types de désappariement.

II.c Conclusion

La figure 6 montre une comparaison qualitative de la consommation d'énergie en fonction de f_s. En fait, la consommation d'énergie d'un système multi-canaux est plus élevée que M fois la consommation d'un seul canal à la même fréquence d'opération. Cela est dû à des

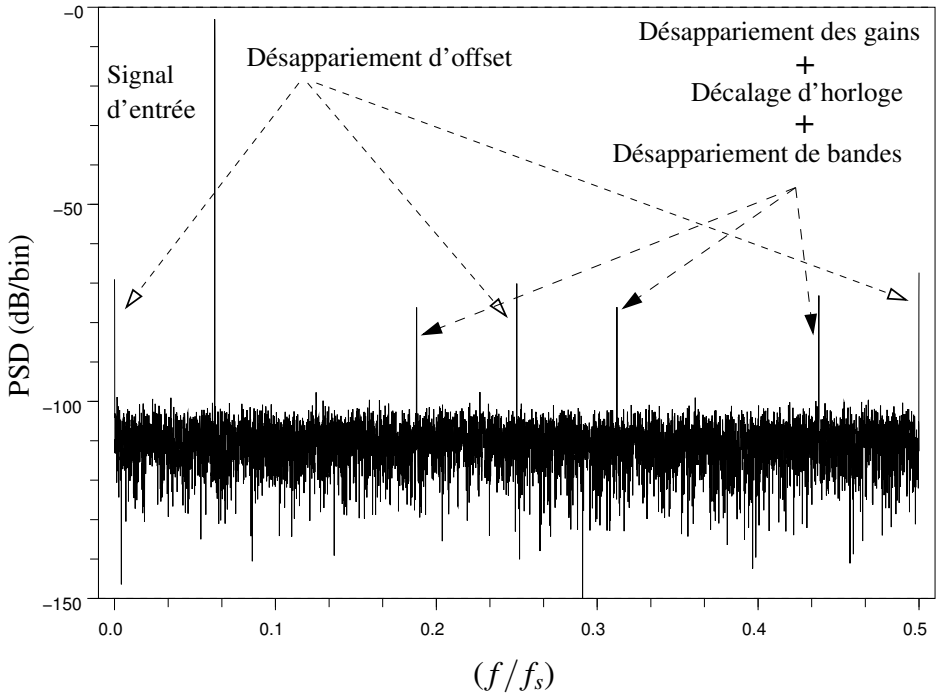


Figure 5: a)I_{sat} en fonction de f_{op} b)FoM en fonction de f_{op}

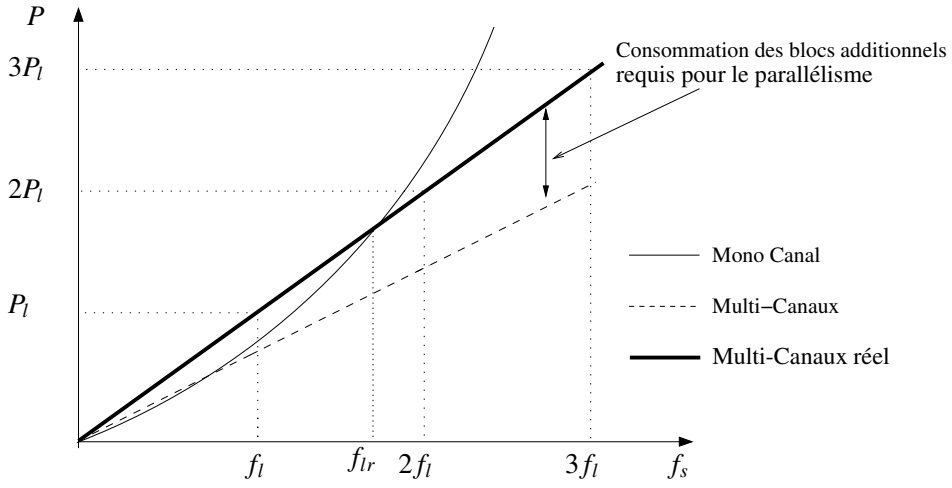


Figure 6: Comparaison de la consommation d'un système mono-canal et d'un système multi-canaux

blocs supplémentaires nécessaires pour le parallélisme. Dans les structures à entrelacement temporel, des blocs analogiques et / ou numériques doivent être ajoutés pour faire face aux désappariements des canaux.
Ainsi, lorsque f_s est égale à f_{lr}, l'utilisation du parallélisme commence à être justifiée, car à ce stade, les structure multi-canaux et canal unique ont la même FoM. Et plus f_s augmente, plus l'intérêt d'utiliser le parallélisme va grandir en raison du fait que contrairement à un seul canal dont la FoM se dégrade avec l'augmentation de f_s, la FoM d'un système parallèle reste presque constante.

III Modulateurs ΣΔ

III.a Principe

Le fonctionnement des modulateurs ΣΔ est caractérisé par deux principes fondamentaux: l'échange entre résolution et vitesse et la mise en forme du bruit de quantification. En effet, dans un CAN ΣΔ, le signal analogique est échantillonné à une cadence f_{op}, OSR fois plus grande que f_s (Avec f_s deux fois la bande du signal utile) et ensuite est quantifié à une résolution n très faible (1 à 5 bits en pratique). Un filtre décimateur placé juste après le modulateur permet le passage du signal n bits@f_{op} à un signal $\log_2(OSR) \times n$ bits@f_s (avec $OSR = \frac{f_{op}}{f_s}$) permettant ainsi de faire l'échange entre résolution et vitesse. En outre, la fonction de bruit du modulateur ΣΔ permet de repousser le bruit de quantification hors de la bande d'intérêt. Pour éclaircir ce point, considérons le modulateur de la figure 7. En utilisant le modèle linéaire du quantificateur et en supposant son gain égal à un, la sortie du modulateur dans le domaine des Z est comme suit:

$$Y(z) = \underbrace{(1)}_{STF(z)} \times X(z) \; + \; \underbrace{(1-z^{-1})^2}_{NTF(z)} \times N(z)$$

Avec $STF(z)$ la fonction de transfert du signal et $NTF(z)$ la fonction de transfert du bruit
En analysant la NTF obtenue, on constate qu'elle présente une caractéristique passe haut ce qui se traduit par une atténuation du bruit de quantification en basse fréquence et une amplification en haute fréquence. Ce résultat est confirmé dans la figure 8 qui montre la sortie du modulateur ainsi que son spectre pour une entrée sinusoïdael. On voit effectivement que le bruit de quantification est rejeté en haute fréquence. Ce bruit, comme indiqué auparavant, sera éliminé par le filtre de décimation.

III.b Comparaison entre implémentation temps continu, temps discret et mixte

Il est possible de concevoir les modulateurs ΣΔ en utilisant soit des circuits temps discret (DT) soit des circuit temps continu (CT) soit des circuits hybrides. Chacune de ses implémentations a ses avantages et ses inconvénients. Dans cette sous section, nous allons faire une analyse comparative pour trouver celle qui sera la plus appropriée pour l'application présentée dans l'introduction.

La figure 9 montre l'architecture générale d'un modulateur DT d'ordre L. Le principe de fonctionnement est le suivant: le signal analogique est échantillonné en entrée avant d'être traîté par L intégrateurs DT dont les implémentations les plus populaires en capacités commutées sont aussi illustrées dans la même figure.

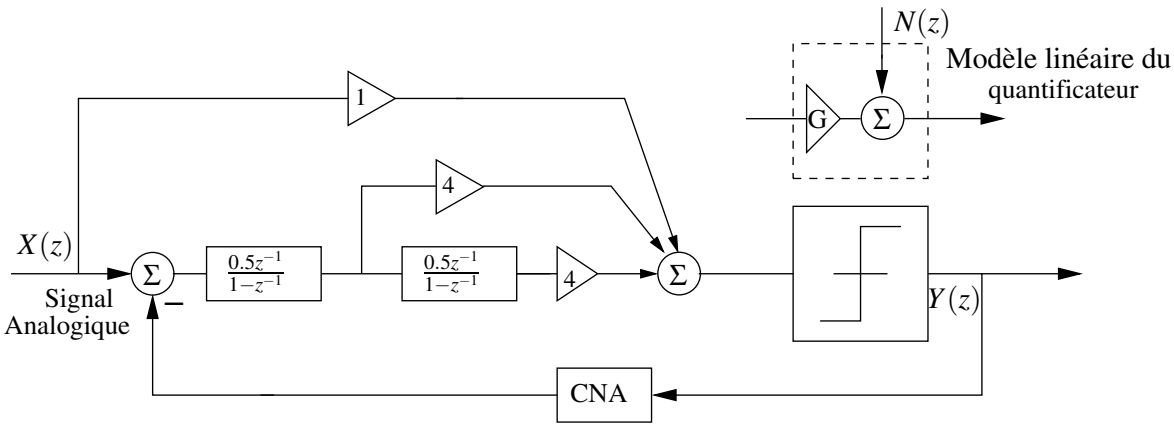


Figure 7: Diagramme bloc d'un modulateur ΣΔ d'ordre 2

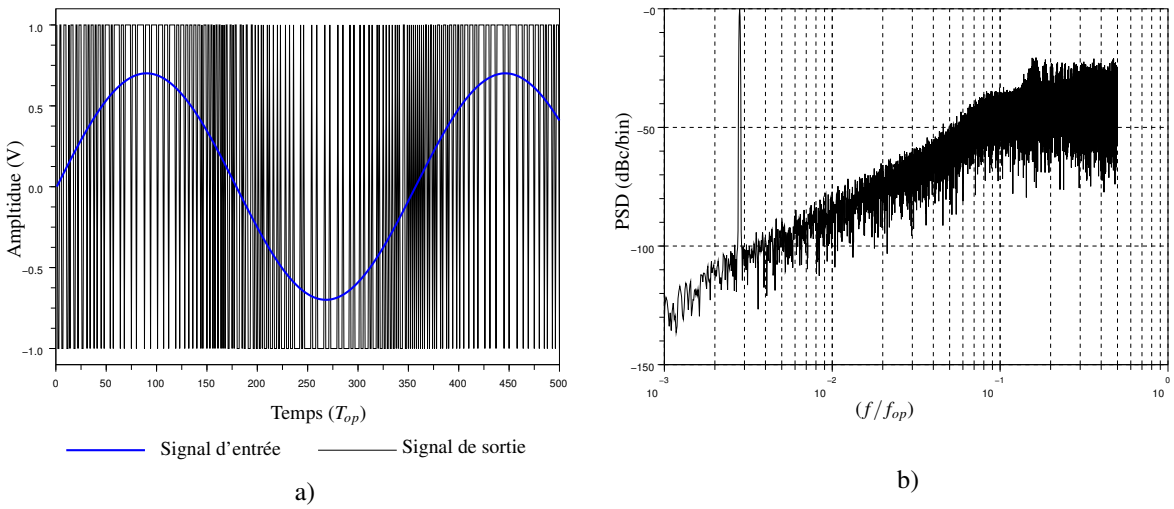


Figure 8: Entrée et sortie d'un modulateur ΣΔ pour une entrée sinusoïdale a)Domaine temporel b)Domaine des fréquences

Dans un modulateur CT (figure 10), le signal n'est échantillonné qu'à l'entrée du quantifica-

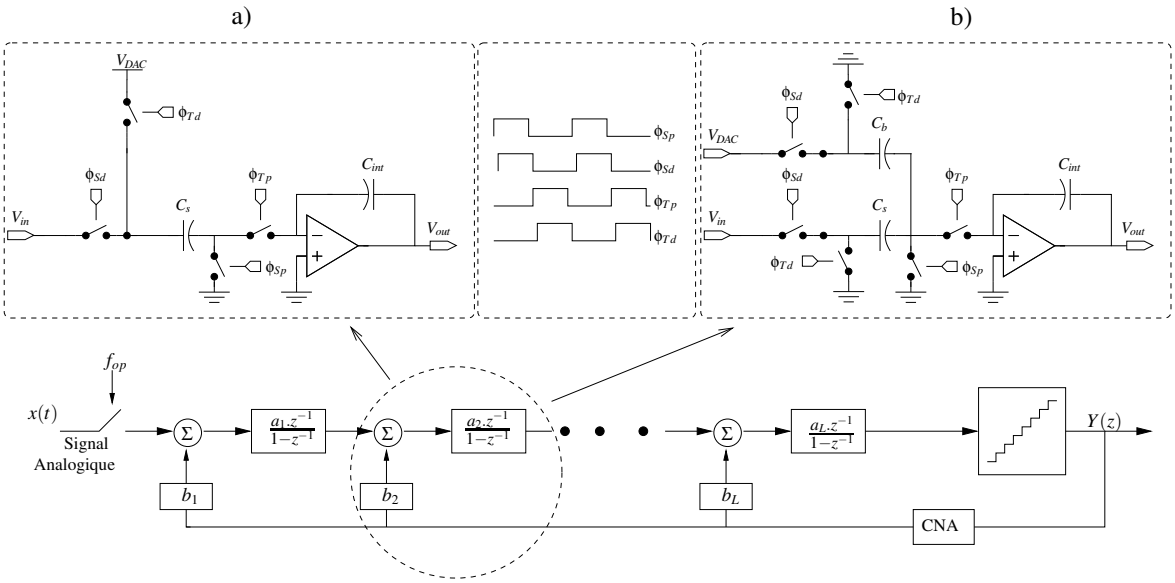


Figure 9: Architecture générale d'un modulateur ΣΔ temps discret

teur après avoir passé L intégrateurs CT. Les deux techniques principales pour les implémenter sont les circuit OTA-RC (figure 10.a)) et les circuits gm-C (figure 10.b)).

Les modulateurs hybrides sont une combinaison de modulateurs DT et CT. Le principe est

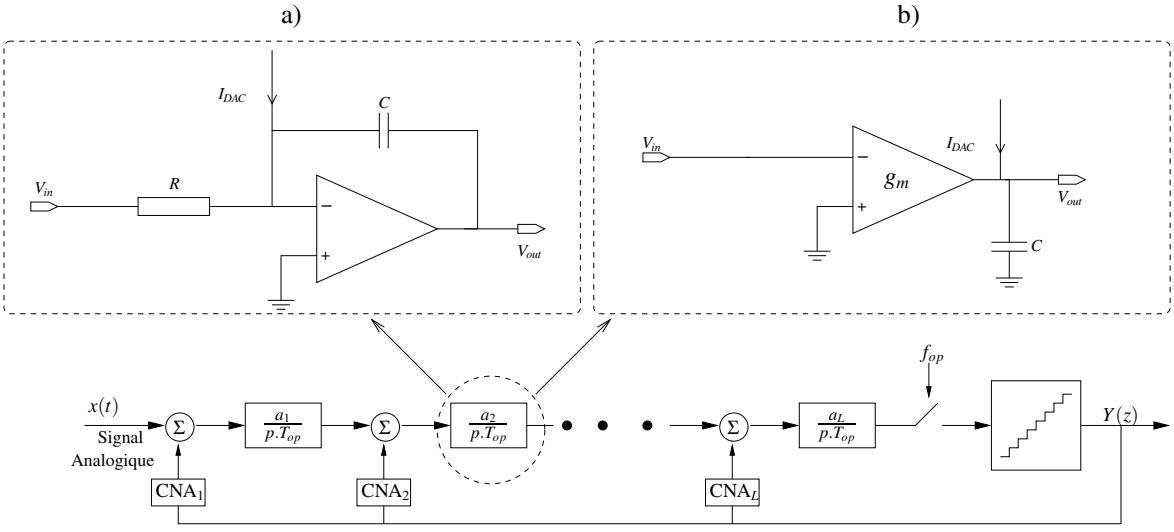


Figure 10: Architecture générale d'un modulateur ΣΔ temps continu

d'aligner k intégrateurs CT suivis $L-k$ intégrateurs DT dans le but de tirer les avantages des deux architectures. La table 1 résume une comparaison faite entre les trois implémentations. Cette comparaison a été réalisée en modélisant les différentes imperfections des modulateurs ΣΔ et en analysant leurs impacts sur chacune des implémentations. Cette étude est détaillée dans la partie en anglais du manuscrit.

Bien qu'elle nécessite une plus grande consommation de puissance que les modulateurs CT et hybrides, une implémentation DT a été préférée car elle est plus robuste face à la gigue

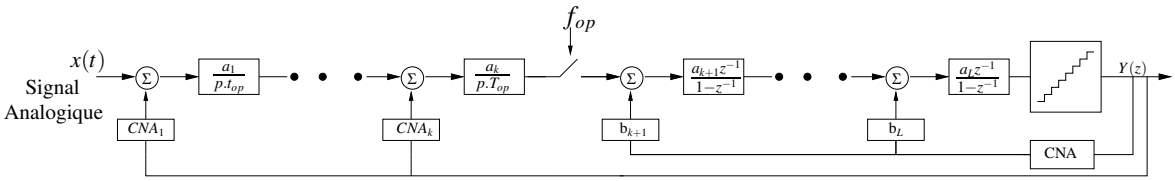


Figure 11: Architecture générale d'un modulateur ΣΔ hybride

	Modulateurs DT	Modulateurs hybrides	Modulateurs CT
Consommation	☺	☺☺	☺☺☺
Vitesse	☹	☺	☺
Variation des coefficients	☺☺	☹	☹☹
Adaptation des coefficients avec f_{op}	☺☺	☹	☹☹
Filtrage anti-repliement	☹☹	☺	☺☺
Bruit thermique	☺	☺	☺
Bruit de gigue	☺☺	☹	☹
Linearités des commutateurs	☹	☺☺	☺☺
Délai de boucle	☺☺	☹☹	☹☹

Table 1: CT vs DT vs Hybrid

d'horloge et le délai de boucle et est surtout plus adaptée à la reconfiguration. En fait, les modulateurs DT s'adaptent automatiquement avec le changement de la fréquence d'opération et sont plus adaptés aux architectures cascades. En outre, les modulateurs DT sont plus adaptés à la plupart des structures parallèles.

III.c Comparaison entre modulateurs passe bas et passe haut

Les CAN ΣΔ peuvent être divisées en 3 catégories principales: les modulateurs passe-bas (LP), les modulateurs passe-haut (HP) et les modulateurs passe-bande (BP). Le signal analogique est en bande de base pour les modulateurs LP, à $f_{op}/2$ pour les modulateurs HP et à une fréquence intermédiaire pour les modulateurs BP. C'est la NTF du modulateur qui caractérise le type de modulateur. La figure 12 montre la NTF pour les trois types de modulateurs. Comme on peut le constater, la NTF est conçue d'une manière à pousser le bruit de quantification hors de la bande d'intérêt. On voit aussi que le bruit dans la bande diminue lorsque l'on augmente l'ordre du modulateur ce qui va permettre d'atteindre des résolutions plus élevées, mais en même temps en augmentant l'ordre du modulateur, le bruit de quantification hors bande augmente imposant ainsi un filtrage plus sévère par le filtre de décimation et en conséquent un ordre plus élevé.

Après avoir discuté le choix de l'implémentation dans la sous-section précédente, une comparaison entre modulateur LP et HP est effectuée dans cette sous-section. La même approche considérée pour la comparaison entre CT, DT et hybride sera adoptée. Les non-idéalités de tous les blocs de base à savoir l'OTA, quantificateur, interrupteurs et horloges sont prises en considération. Cette comparaison nous permettra de choisir la mise en forme la plus adaptée (LP ou HP) pour notre conception. Les modulateurs ΣΔ BP ont été écartés de cette analyse comparative en raison de la complexité de l'implémentation des résonateurs BP en DT.

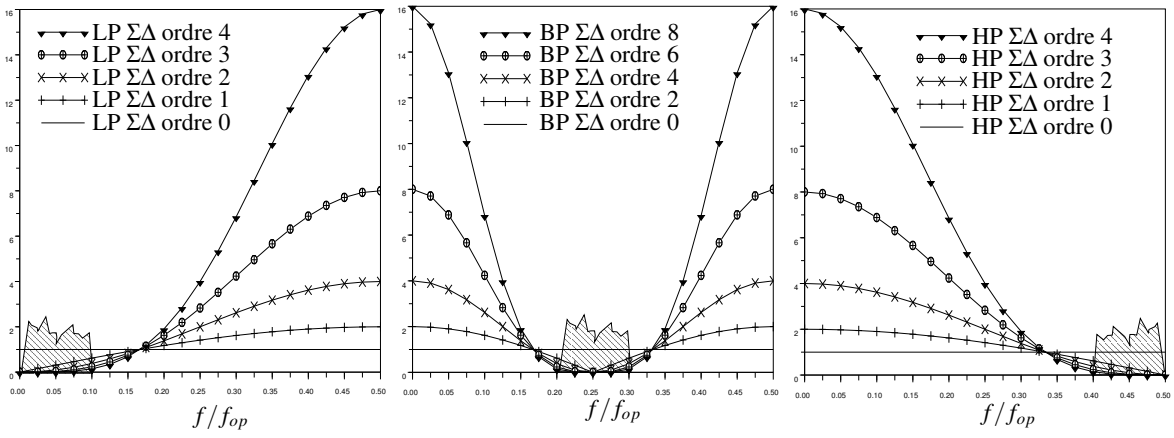


Figure 12: Mise en forme du bruit

La table 2 résume les résultats de cette comparaison dont les détails se trouvent dans la partie en anglais du manuscrit. Il a été montré que les modulateurs HP sont plus robuste contre l'offset de l'OTA et du bruit 1/f que leurs homologues LP. Cette caractéristique est très importante car elle permet de réduire les dimensions des transistors de l'OTA vu que les exigences en termes de bruit et d'appariement sont plus faibles et va leur permettre d'être bien adaptés à la numérisation des signaux à bande étroite.
D'autre part, les exigences en termes de gigue et de la linéarité des commutateurs sont signi-

ficativement plus faibles dans le modulateur LP que le modulateur HP. La grande sensibilité à la gigue d'horloge dans ce dernier ainsi que le problème de linéarité des interrupteurs peuvent devenir très critique si f_{op} est élevée. Pour cela, l'architecture choisie est la LP. Les problèmes de bruit 1/f et d'offset de l'OTA seront traités avec une conception soignée et par l'utilisation de techniques d'appariement adaptées pendant le dessin du masque.

	Modulateurr LP	Modulateur HP
Saturation de l'OTA	☺	☺
Gain DC de l'OTA	☺	☺
SR de l'OTA	☺	☺
Bruit 1/f de l'OTA	☹	☺
Bruit thermique de l'OTA	☺	☺
Offset de l'OTA	☹	☺
Offset du comparateur	☺	☹
Métastabilité du comparateur	☺	☺
Hysteresis du comparateur	☹	☺
Gigue d'horloge	☺	☹
Linéarité des commutateurs	☺	☹

Table 2: LP vs HP

IV ΣΔ parallèle

Plusieurs techniques employant le parallélisme pour élargir la bande passante des CANs ΣΔ ont été proposées: la décomposition en bande de fréquence (FBD) [**?**] [**?**], les sigma-delta à modulation Hadamard (ΠΣΔ) [4], et les sigma-delta à filtrage de block [62] [63] et les sigma delta à entrelacement temporel [3] [68] [69] [70].

L'architecture FBD utilise des modulateurs ΣΔ BP distribués dans la bande utile. Cette architecture est adaptée aux récepteurs hétérodynes et est très robuste en cas désappariements analogiques. Toutefois, elle est la plus complexe parmi les quatre architectures considérées car elle nécessite la mise en œuvre de différents modulateurs sigma-delta passe-bande.

La solution ΠΣΔ, basée sur la modulation Hadamard est moins complexe que la FBD car elle utilise le même modulateur ΣΔ pour tous les canaux, mais elle a besoin de filtres numériques avec des ordres élevés pour atteindre les performances théoriques. En plus, l'obtention d'une haute résolution en utilisant cette technique nécessite l'utilisation d'un grand nombre de canaux ce qui la rend inadaptée à l'application désirée.

La solution ΣΔ à filtrage de bloc proposée dans [62] [63] a également l'avantage d'utiliser le même modulateur pour tous les canaux. En outre, les ressources numériques nécessaires au démultiplexage du signal en entrée ainsi qu'à sa reconstruction en sortie sont très faibles. Cependant, cette technique souffre d'un inconvénient majeur. En fait, pour réaliser la fonction de transfert de bruit souhaitée, la sortie du i^{eme} intégrateur de chaque canal doit être appliquée à l'entrée des $i+1^{eme}$ intégrateurs de tous les canaux avec un gain et un retard appropriés. Ces signaux inter-canaux entraînent une augmentation de la complexité dans le dessin du masque, des désappariements supplémentaires et des couplages entre les différents signaux en particulier si le nombre de canaux et d'intégrateurs par canal sont grands.

La solution ΣΔ à entrelacement temporel proposée dans [3] [68] [69] [70] utilise le même modulateur pour tous les canaux et nécessite des ressources numériques raisonnables pour la reconstruction du signal et son démultiplexage [71]. Par ailleurs, aucun signal analogique nécessite de transiter entre les canaux ce qui élimine les contraintes sur le nombre de canaux et surtout les contraintes sur le choix de l'architecture du modulateur desquelles souffrent l'architecture à filtrage de bloc.

IV.a Sigma Delta à entrelacement temporel avec la technique classique d'interpolation

La figure 13 montre le schéma bloc d'un CAN ΣΔ à entrelacement temporel. Le principe de fonctionnement est le suivant: le signal analogique temps continu $x(t)$ est tout d'abord échantillonné à une fréquence f_s deux fois la bande utile; le signal discrétisé est ensuite distribué entre les canaux, ce qui se traduit mathématiquement par une décimation par M; le signal de chaque canal est par la suite interpolé par un facteur N pour créer un signal suréchantillonné à l'entrée du modulateur ΣΔ, ceci se fait par l'insertion de $N-1$ zéros entre deux valeurs utiles du signal; le signal interpolé est ensuite numérisé et reconstruit dans le domaine numérique en appliquant un filtrage adéquat présenté dans [71]. Cette technique d'interpolation qui consiste à insérer $N-1$ zéros entre deux échantillons du signal a l'avantage d'être simple à implémenter d'une part et de réduire la complexité du traitement numérique pour reconstruire le signal d'autre part . Cependant, elle présente le défaut de réduire la puissance du signal d'entrée d'un facteur N en comparaison à une implémentation mono-canal. En conséquent, pour pouvoir atteindre la résolution visée en sortie du CAN, il faudra aussi réduire la puissance du bruit thermique par ce même facteur N. Ceci se fait par une

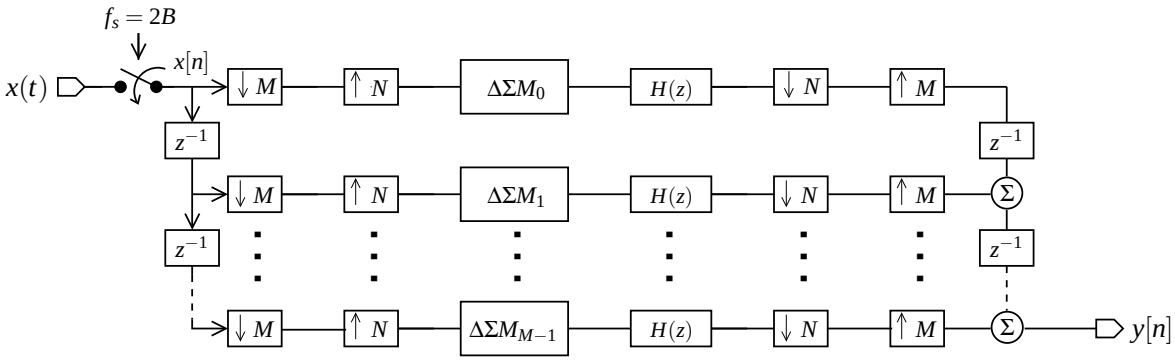


Figure 13: Architecture du CAN ΣΔ à entrelacement temporel

augmentation de la taille des capacités par N et donc pourra conduire à des valeurs de capacités non-raisonnables. Par exemple, dans un scénario UMTS en utilisant 2 canaux et un N de 52, l'obtention d'un rapport signal à bruit thermique de 83 dB requiert des capacités de 15.4 pF!!

IV.b Sigma Delta à entrelacement temporel avec la nouvelle technique d'interpolation

Pour répondre auproblème de sensibilité au bruit thermique des CANs ΣΔ à entrelacement temporel, une nouvelle technique d'interpolation a été proposée. Cette technique est basée sur le sur-échantillonnage du signal d'entrée $x(t)$ à une cadence supérieure à f_s tel que f_{op}. Les échantillons additionnels résultants du sur-échantillonnage permettront d'augmenter la puissance du signal et donc de réduire les contraintes en termes de bruit thermique et en conséquent de diminuer les tailles des capacités.
La figure 14 montre cette technique pour $M = 2$ et $N = 12$. Les lignes en pointillées correspondent aux échantillons acquis à la cadence de Nyquist f_s et les lignes en trait plein correspondent aux échantillons additionnels acquis à une cadence f_{op}, N/M fois supérieure à f_s. La distribution de ces échantillons additionnels entre les différents canaux est un point important et capital pour assurer une bonne reconstruction du signal en sortie. En se basant sur des développements mathématiques et sur des résultats de simulations détaillés dans la partie en anglais du rapport, la distribution retenue consiste à allouer au premier canal les N/M premiers échantillons, au deuxième canal les N/M échantillons suivant et ainsi de suite. Au bout de N échantillons, on reviendra au premier canal. Ceci peut être vu sur l'exemple de la figure 14, ainsi, on a alloué les 6 (12/2) premiers échantillons au premier canal et les 6 échantillons suivants au deuxième canal et on a complété le reste avec des zéros.
La puissance du signal utile avec la nouvelle technique d'interpolation est N/M fois supérieure à celle de la technique classique et donc les tailles capacités peuvent être réduites par ce même facteur tout en assurant le rapport signal à bruit thermique visé.
Un autre avantage de cette nouvelle technique d'interpolation est la réduction des contraintes sur le filtre anti-repliement. En effet, vu que le signal sera sur-échantilonné en entrée, les premiers bloqueurs qui vont se replier dans la bande sont à un offset de $2 \times \frac{N}{M} \times B$ comparé à un offset de B en utilisant la technique classique. Ceci va permettre de réduire considérablement l'ordre du filtre anti-repliement.
Les inconvénients de cette nouvelle technique sont une augmentation de la complexité du circuit de génération d'horloge nécessaire pour les opérations de décimation et d'interpolation

qui sera présenté dans la section suivante. En plus, l'ordre du filtre d'égalisation requis augmente d'un ordre 10 à un ordre 30. Néanmoins, ces inconvénients sont négligeables par rapport aus avantages acquis.

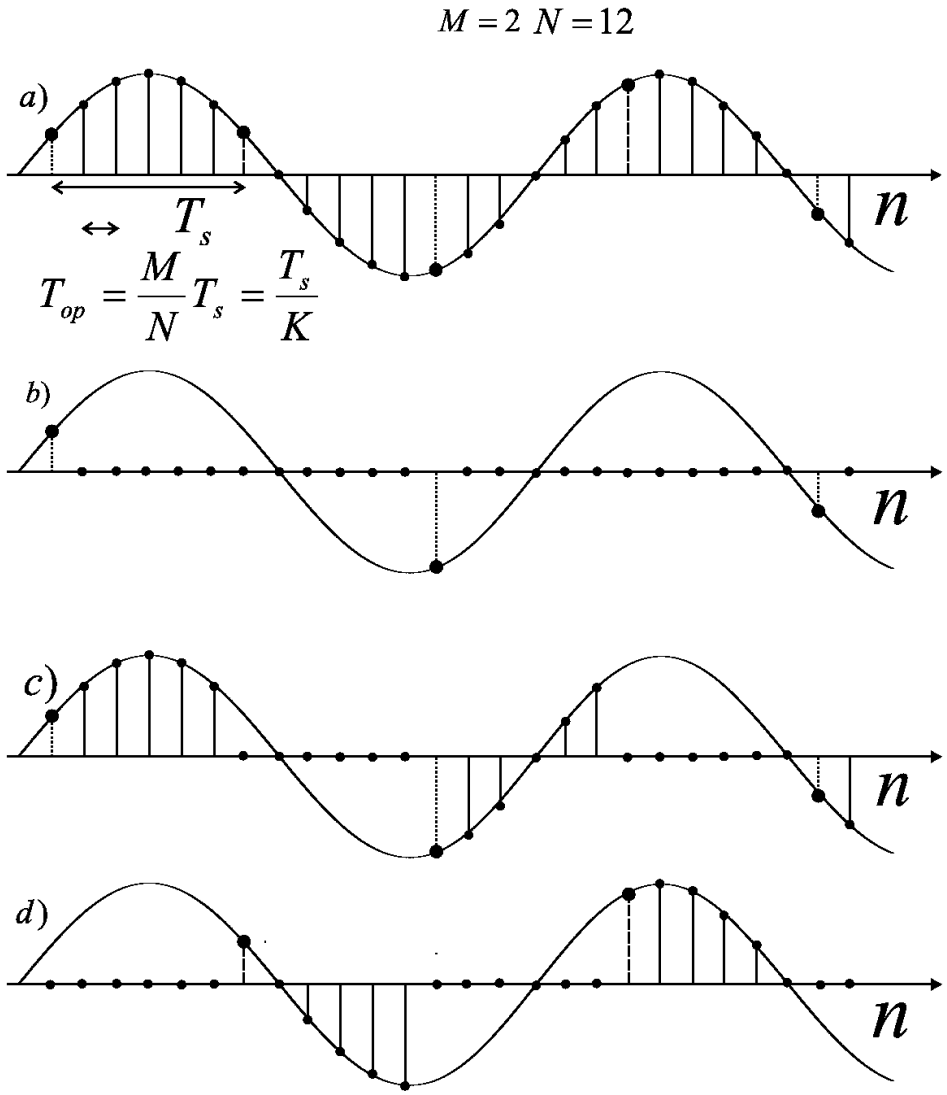


Figure 14: Exemple illustrant la nouvelle technique d'interpolation a) Signal d'entrée échantillonné à f_{op}, b) Signal du canal 1 avec la technique classique d'interpolation , c),d) Signaux des canaux 1 et 2 avec la nouvelle technique d'interpolation

V Prototype

Versanum, (pour numérisation à large bande versatile), est un projet financé par l'agence nationale de recherche française (ANR) [83]. L'objectif de ce projet est d'étudier le concept de numérisation large bande versatile. Notre travail est de concevoir un CAN pour un récepteur multimode à conversion directe adapté pour les normes GSM, EDGE, UMTS, DVB-T, WiFi et WiMax. Le cahier des charges des standards ciblés est donné dans le tableau 3. Par souci de simplification de la conception, les spécifications de certaines normes ont été fusionnées.

Table 3: Spécifications des standards visés

Modes	B	SNR
GSM/EDGE	135 KHz	80 dB
UMTS/DVBT	4 MHz	80 dB
WiFi/WiMax	12.5 MHz	52 dB

Dans cette section, la conception du prototype Versanum est présenté. Certaines des caractéristiques de ce CAN ont été discutées dans les sections précédentes. En fait, il a été décidé que le CAN sera implémenté en temps discret. Le modulateur utilisé sera un passe-bas. L'architecture du CAN parallèle est l'architecture à entrelacement temporel avec la nouvelle technique interpolation qui a été présentée dans leasection précédente. Les autres aspects de la conception seront abordés dans cette section.

V.a Etude système

Pour le mode GSM/EDGE, un seul canal avec un modulateur d'ordre 2 est suffisant. En fait, puisque la bande dans ce mode est étroite, un OSR très important peut être réaliser tout en maintenant une fréquence de fonctionnement assez faible. Par conséquent, il n'y a ni besoin d'utiliser un CAN multi-canaux, ni un modulateur d'ordre supérieur. La Figure 15 montre l'architecture du modulateur employé. Un quantificateur 1.5 bit a été préféré à un quantificateur 1 bit, car il permet d'augmenter la résolution de 3 dB et le DR de près de 3 dB ainsi. En plus, le quantificateur 1.5 bit rend la STF plus plate comparé à un quantificateur 1 bit. Les coefficients du modulateur sont choisis comme un compromis entre la stabilité du modulateur, la suppression du bruit de quantification et une STF unité. Le spectre de sortie pour un signal d'entrée à -3 dBFS est représenté sur la figure 16. Le SQNR obtenu pour un OSR de 96 est de 87 dB.

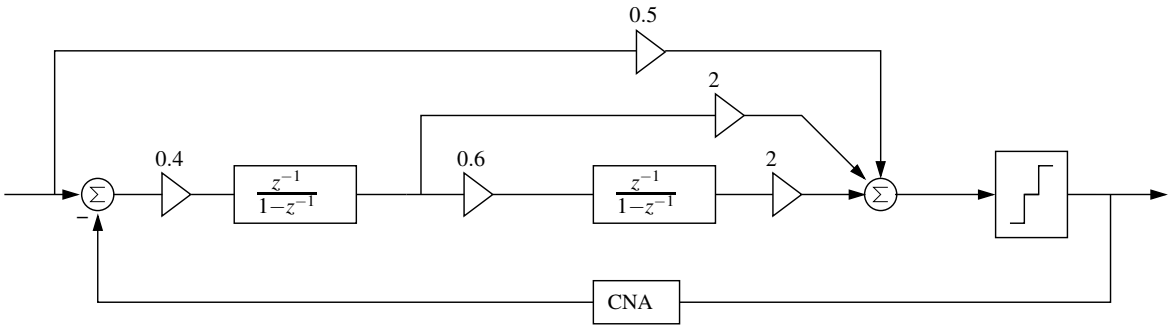


Figure 15: Architecture du modulateur ordre 2

Dans les modes UMTS / DVB-T et WiFi / WiMax, le taux de conversion ciblé est nettement plus élevé que dans le mode GSM / EDGE. Par conséquent, un modulateur d'ordre supérieur est nécessaire parce que les OSR réalisables sont plus faibles. Le modulateur utilisé est illustré dans la figure 17. C'est un modulateur ordre 4 avec une boucle de contre-réaction globale. L'avantage d'une telle architecture comparée à une architecture cascade classique est qu'elle ne requiert pas une annulation du bruit pour la reconstruction du signal en sortie. Une solution ($M = 2$, $N = 52$) est utilisée pour le mode UMTS/DVB-T et une solution ($M = 4$, $N = 32$) pour le WiFi / WiMax mode. Ces couples de (M, N) permettent

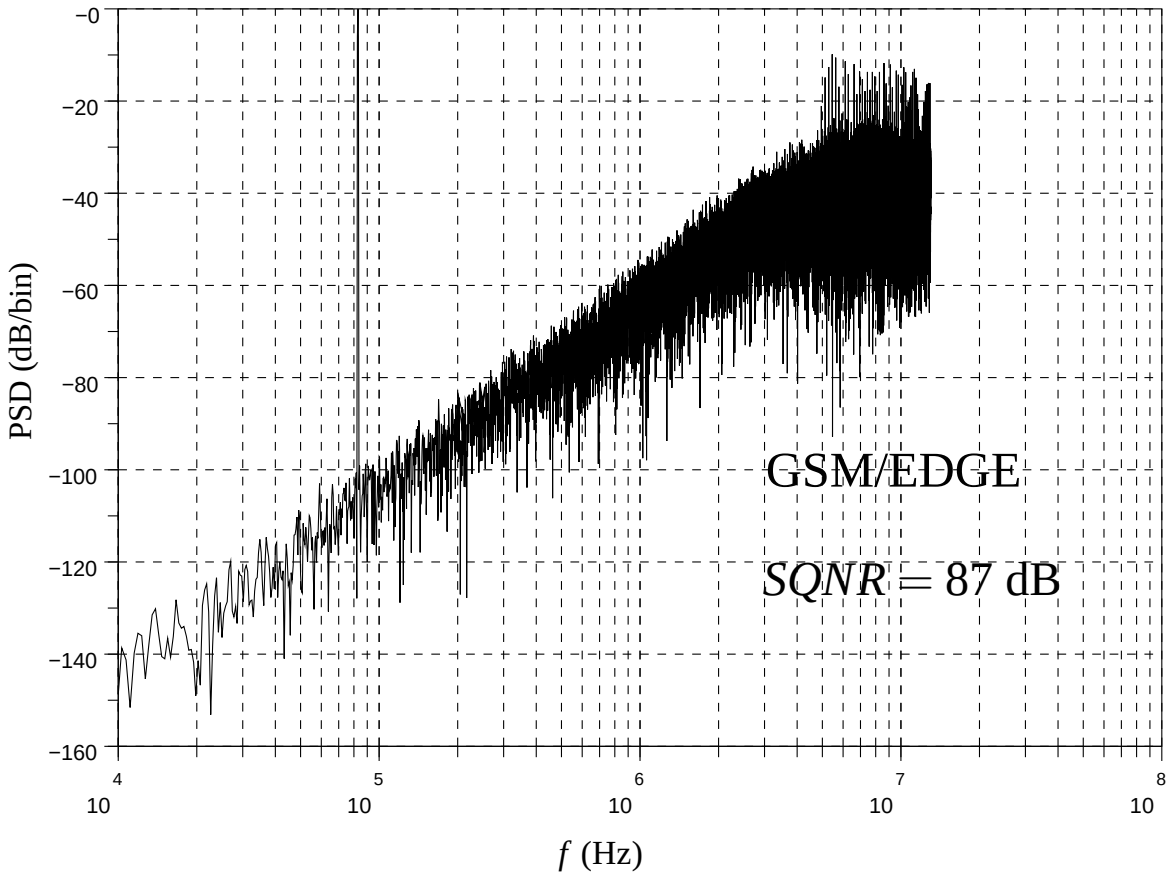


Figure 16: Spectre de sortie dans le mode GSM/EDGE

d'atteindre le SQNR requis pour les deux modes ainsi que d'utiliser le même f_{op} ce qui permet de simplifier la conception.
La figure 18 montre les spectres des signaux reconstruits à la sortie du CAN ΣΔ à entrelacement temporel dans les modes UMTS/DVBT et WiFi/WiMax. Le SQNRs respectifs sont de 89 dB et 63 dB .

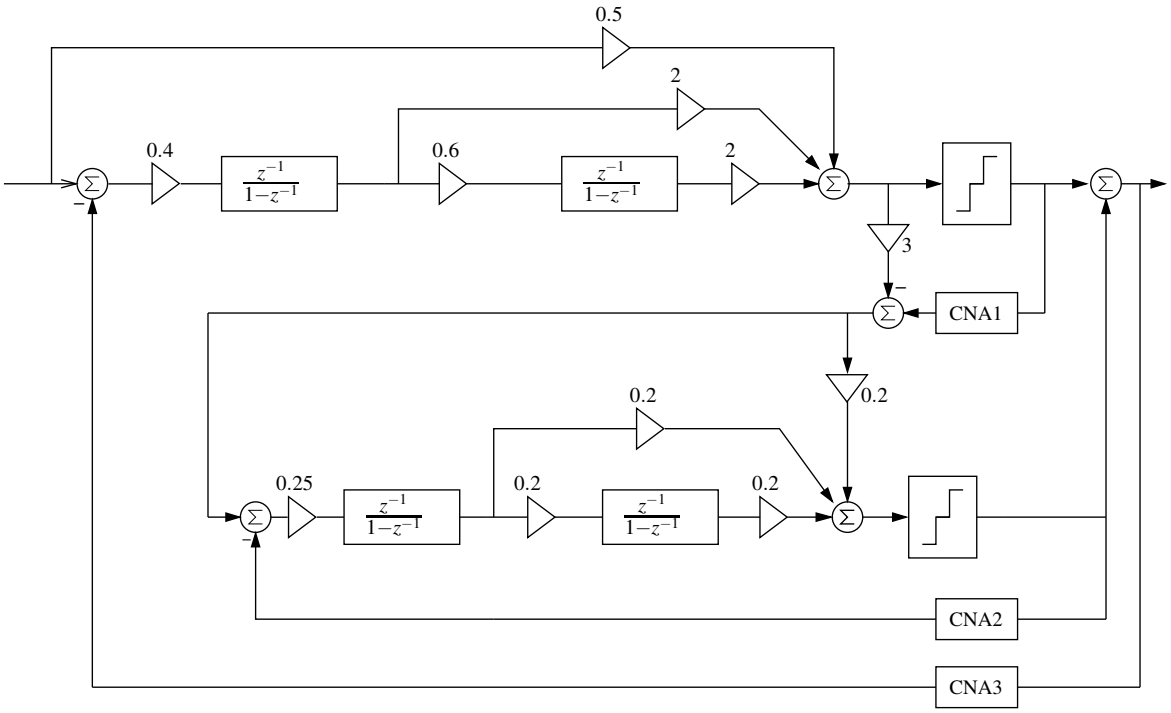


Figure 17: Architecture du modulateur ordre 4

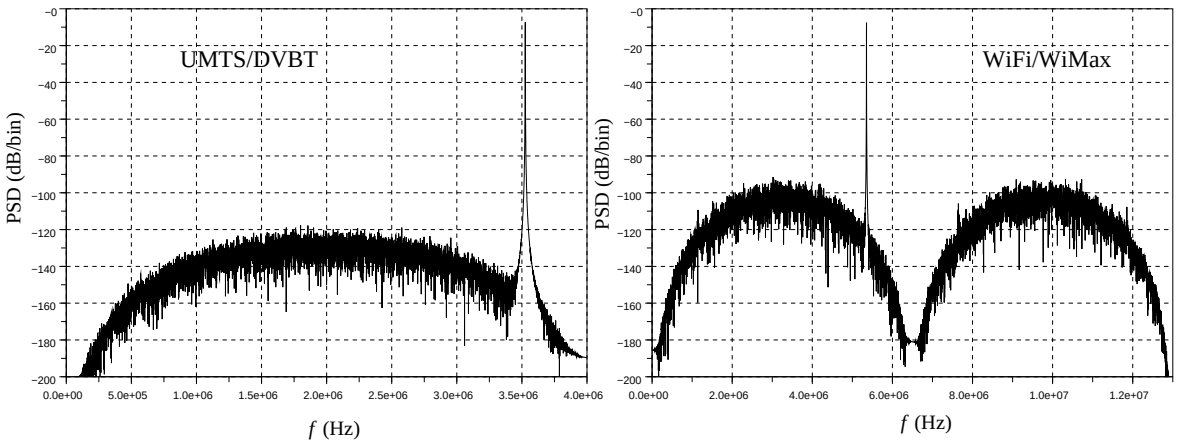


Figure 18: Spectres de sortie dans les modes UMTS/DVB-T et WiFi/WiMax

V.b Conception

La figure 19 montre l'implémentation en capacité commutées d'un canal du CAN. Notez qu'un échantillonneur bloqueur (S/H) a été placé en amont de tous les canaux pour éviter

les problèmes de décalage d'horloge et de désappariement de bandes. En ce qui concerne les désappariements de gain et d'offset, elles sont corrigées en utilisant les algorithmes présentés dans [81]. Un bit de contrôle auquel on se référera par $ULAN$ permet de passer du modulateur ordre 2 (Figure. 15) au modulateur ordre 4 (Figure. 17) . Ce bit contrôle d'une part, le circuit de polarisation principal qui fournit les courants de référence pour les OTA et les pré-amplificateurs des comparateurs. Ainsi, si le circuit est configuré en tant que modulateur ordre 2, les courants de référence de blocs du deuxième étage sont mis à zéro pour éviter la consommation inutile du courant et les courants de référence des blocs du premier étage sont fixées à des valeurs qui optimiseront le fonctionnement à un f_{op} de 26 MHz, utilisé en mode GSM / EDGE ($\underbrace{96}_{OSR} \times 2 \times \underbrace{135\text{ kHz}}_{\text{Bande}} = 26$ MHz).
Le bit $ULAN$ contrôle également les OTA du premier étage. En fait, ces OTA ont besoin de fonctionner à 26 MHz en mode GSM/EDGE et à 208 MHz dans les modes UMTS/DVB-T et WiFi/WiMax ($\underbrace{\overbrace{\frac{52}{2}}^{N}}_{M} 2 \times \underbrace{4\text{ MHz}}_{\text{Bande}} = \underbrace{\overbrace{\frac{32}{4}}^{N}}_{M} 2 \times \underbrace{13\text{ MHz}}_{\text{Bande}} = 208$ MHz). Par conséquent, étant donné la grande différence entre les deux fréquences, un simple changement du courant de référence ne permet pas un fonctionnement optimisé dans les deux cas et donc une reconfiguration de l'OTA lui-même est nécessaire. Ceci est réalisé en permettant un changement, contrôlé par $ULAN$, de la taille de certains transistors des OTA.

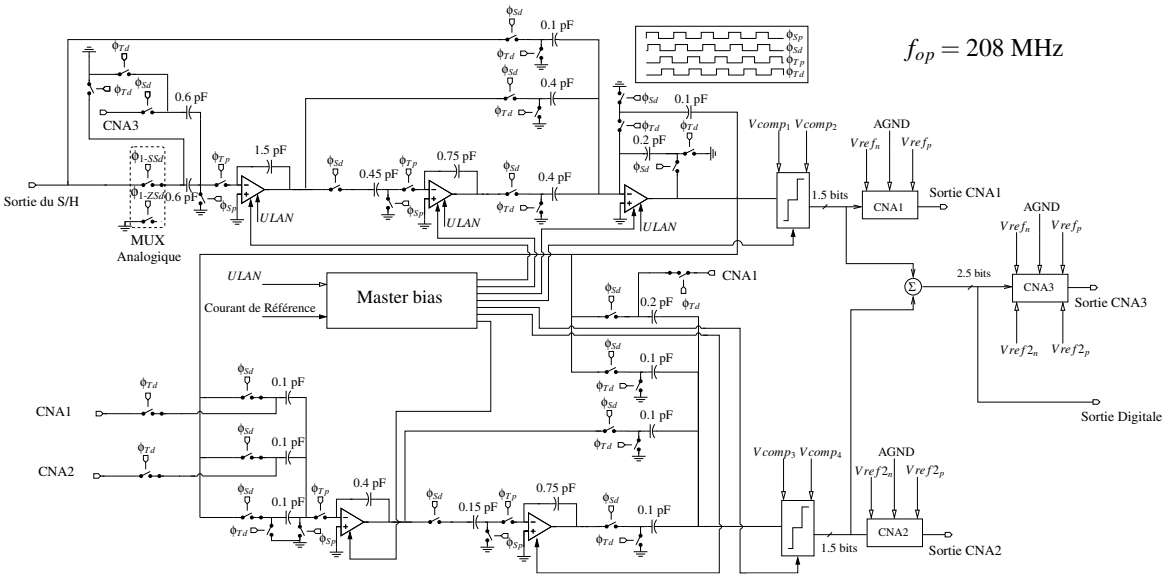


Figure 19: Ciruit d'un canal du CAN ΣΔ

Une architecture à deux étages avec une compensation Miller est utilisée pour les OTAs du premier étage car ces derniers nécessite un grand gain DC et une grande dynamique de sortie. Pour les OTAs du deuxième étage, vu que les contraintes sont relaxées à ce niveau, des OTAs à un seul étage sont préférés pour diminuer la consommation.
Le quantificateur 1.5 bit de chaque étage est implémenté comme un CAN flash. Ses niveaux de comparaison sont générés hors puce.
Le diagramme de l'horloge est représentée sur la figure 19. Les deux versions retardées de l'horloge permettent de décaler les instants d'ouverture du commutateur d'entrée par rapport

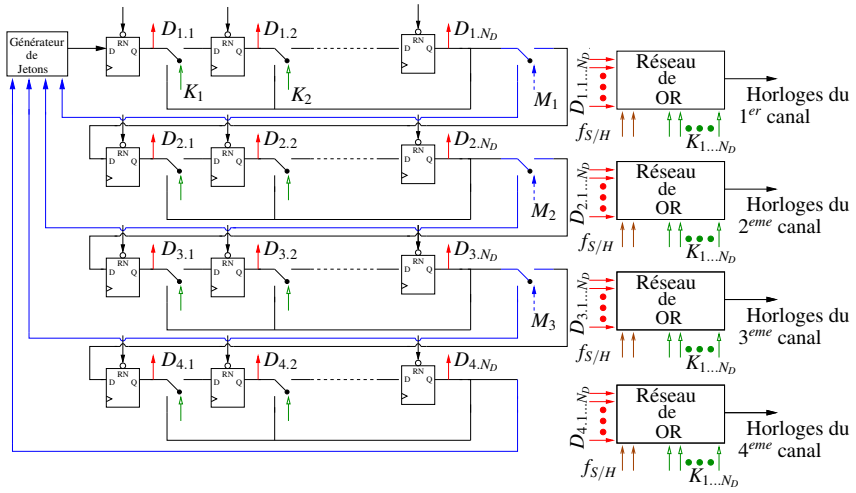


Figure 20: Architecture du circuit d'interpolation

au commutateur d'échantillonnage, ce qui permet de réduire considérablement les effets des injections de charge .
Les opérations de décimation par M et d'interpolation par N sont réalisés grâce aux multiplexeurs analogiques qui se trouvent à l'entrée de chaque canal. Ces multiplexeurs consiste en deux interrupteurs dont l'un permet d'acquérir des échantillons utiles et l'autre d'acquérir des zéros. Leurs horloges ϕ_{i-SSd} et ϕ_{i-ZSd} sont générées à l'aide du circuit d'interpolation présenté dans la figure 20.
Le mode UMTS/DVB-T présente le plus de contraintes en termes de bruit thermique et fixe ainsi la valeur de la capacité d'échantillonnage. Grâce à la nouvelle technique d'interpolation, une capacité de 600 fF est nécessaire pour atteindre un rapport signal à bruit thermique de 83 dB à 363 K (90 ^{o} C) comparée à une valeur de 15.6 pF requise en utilisant la technique d'interpolation classique.

Table 4: Caractéristiques du CAN $\Sigma\Delta$ 4 canaux conçu

Standard	f_s (MHz)	M	N	ordre du modulateur	f_{op} (MHz)	P (mW)
GSM/EDGE	0.27	1	96	2	26	1.74
UMTS/DVBT	8	2	52	4	208	55.2
WiFi/WiMax	25	4	32	4	208	110.4

V.c Test

Le CAN conçu a été fabriqué en une technologie CMOS 65 nm 1p7M. La figure 21 montre une photo du circuit. Sa surface est de 3mm^2 et a été paqueté dans un CQFP à 100 pattes. Notez qu'un canal isolé a été ajouté pour augmenter la flexibilité du test.

Résultats en mode GSM/EDGE

La figure 22 montre le SNR et le SNDR mesuré pour une sinusoïde d'entrée à 10 KHz et un f_{op} de 26 MHz. Le pic de SNR et SNDR sont respectivement de 80 dB et 78.5 dB. La DR du

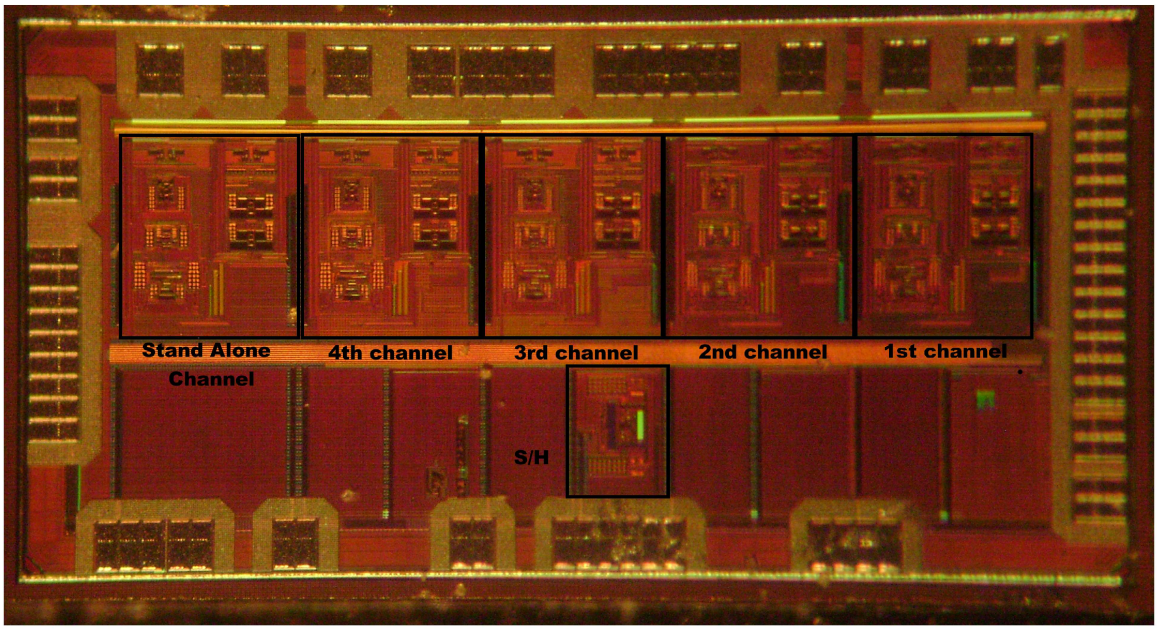


Figure 21: Photo de la puce fabriquée

CAN en mode GSM/EDGE est de 82 dB.

La figure 23 montre la STF du modulateur pour deux amplitudes d'entrée différentes. L'ondulation dans la bande est inférieure à 0.01 dB. A 2 MHz, un pic de 4 dB est observé. Ce pic est dû principalement au nombre réduit de palier du quantificateur. Cette ondulation doit être prise en considération lors de la conception du filtre anti-repliement pour éviter de saturer le modulateur en raison de l'amplification d'interféreur qui pourrait exister à cette fréquence.

La table 5 résume les autres paramètres du modulateur en mode GSM/EDGE et le compare à d'autres réalisations de l'état de l'art. Comme on peut le constater, notre ADC présente une FoM très compétitive.

Ref	B	f_{op}	Entrée	SNDR	DR	P	FoM	Alimentation	Technologie
[97]	100 KHz	50 MHz	1.6 Vpp	77 dB	85 dB	3.43 mW	2.86 pJ/conv	1.2 V	90 nm
[98]	100 KHz	26 MHz	1.4 Vpp	85 dB	88 dB	2.9 mW	0.99 pJ/conv	1.2/3.3 V	130 nm
[99]	100 KHz	48 MHz	1.6 Vpp	84 dB	85 dB	3.3 mW	1.27 pJ/conv	1.2 V	65 nm
[100]	100 KHz	39 MHz	0.8 Vpp	81 dB	82 dB	2.4 mW	1.31 pJ/conv	1.2 V	130 nm
This work	135 KHz	26 MHz	1.6 Vpp	78.5 dB	82 dB	1.74 mW	0.94 pJ/conv	1.2 V	65 nm

Table 5: Comparaison du CAN à l'état de l'art dans le mode GSM/EDGE

Résultats des modes UMTS/DVBT et WiFi/WiMax

Dans les modes UMTS/DVBT et WiFi/WiMax, les performances n'ont pas été atteintes à cause deux problèmes majeurs:

1-Problème du CNA (convertisseur numérique analogique): Dans les deux modes considérés, le modulateur ordre 4 est utilisé. La contre-réaction globale du modulateur (CNA 3 de la Figure 17.) est un CNA multi-bits et donc ses problèmes de désappariements doivent être traitées pour éviter de dégrader la résolution du modulateur. Ceci peut être réalisé en utilisant des

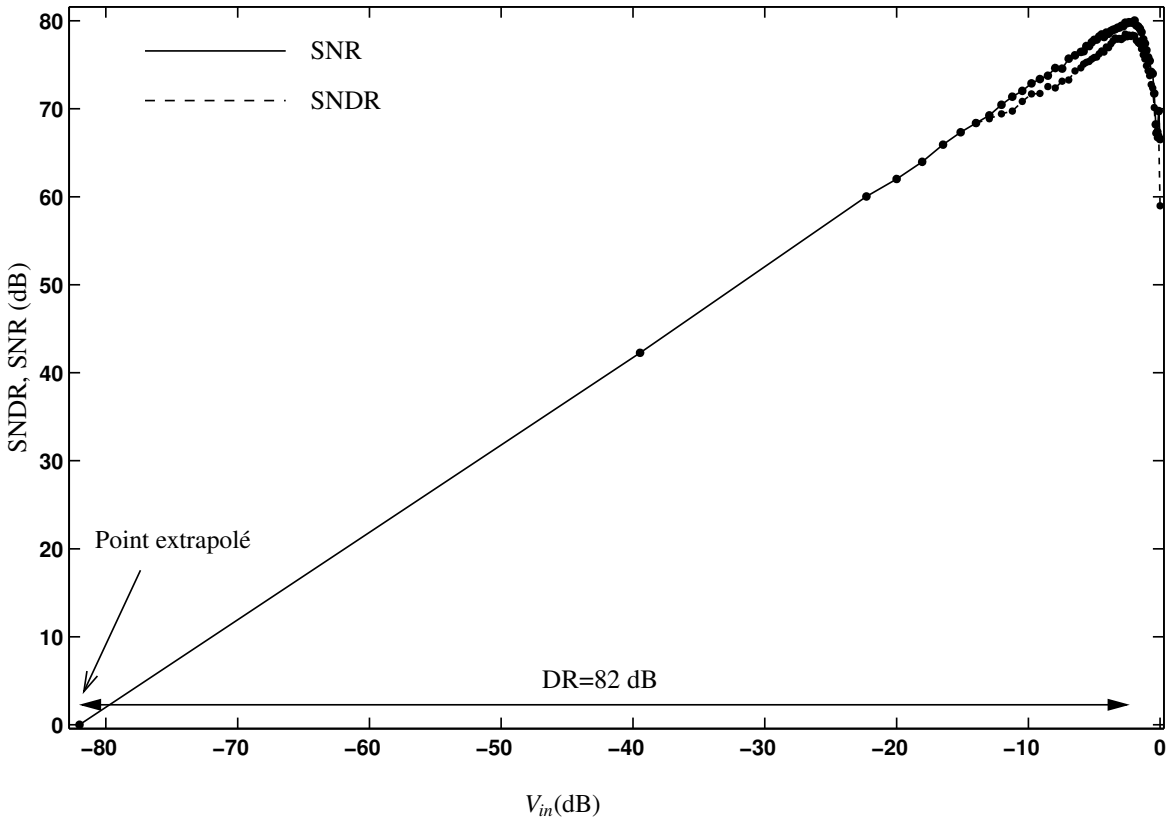


Figure 22: SNR and SNDR en fonction de V_{in}

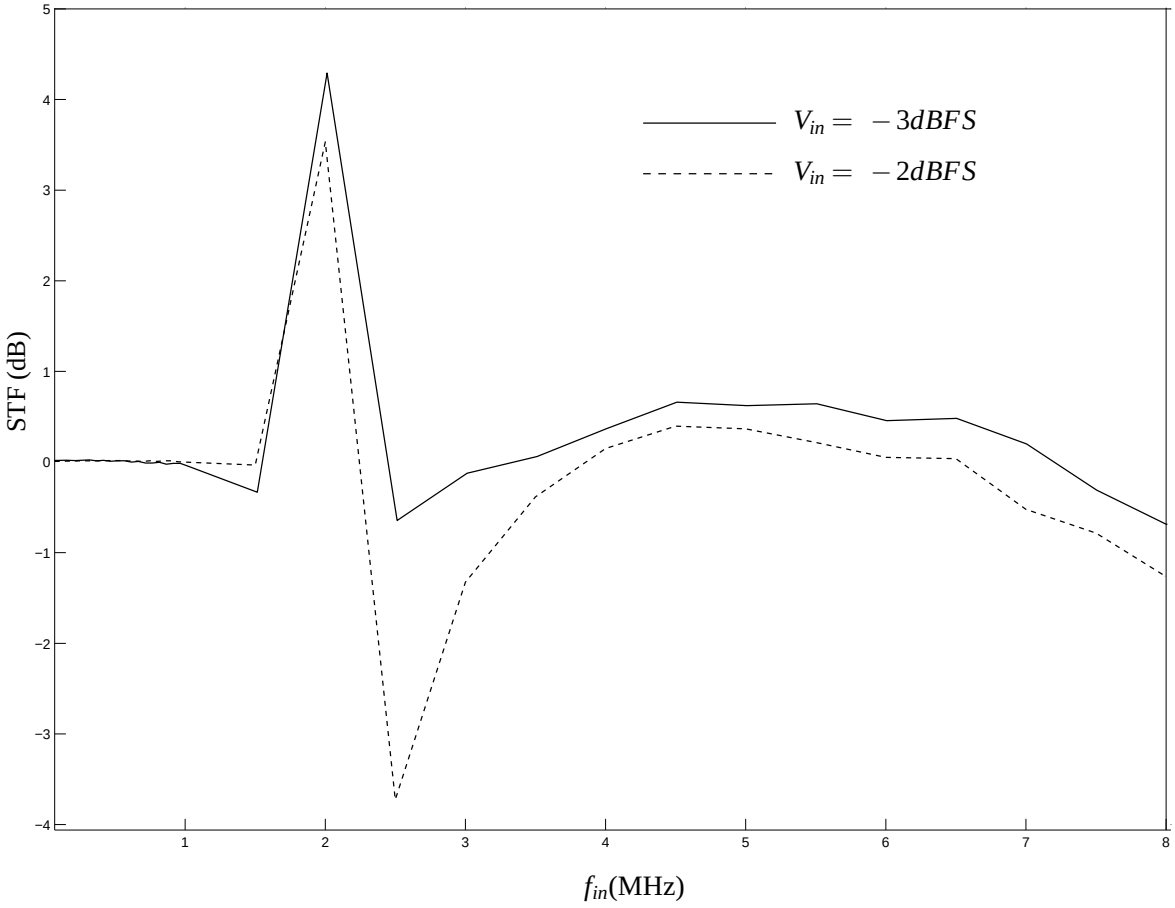


Figure 23: STF du modulateur ordre 2

techniques de calibration ou de corrections [92] [93] [94]. Toutefois en raison du temps limité de conception, nous avons décidé de traiter ce problème en réglant de l'extérieur du circuit les tensions de référence du CNA. Malheureusement, aucune technique n'a été trouvée pour définir ces valeurs de façon précise et donc des distortions très importantes ont été observées dans le spectre de sortie.

2-Problème du S/H: Le deuxième problème a été observé au niveau de l'échantillonneur bloqueur. En effet, idéalement, la sortie du canal isolé et du CAN multi-canaux en n'activant qu'un seul canal doivent donner des résultats identiques. Malheureusement, une chute très importante (de l'ordre de 60 dB) de la puissance du signal d'entrée du CAN multi-canaux a été détecté. Des enquêtes ont été menées pour comprendre les causes du problème. La réponse est venue de l'extraction des parasites du dessin de masque du S/H. Cette opération n'a pas été faite lors de la phase de conception du circuit parce que l'outil n'était pas disponible à ce moment-là. L'extraction a permis de mettre un évidence un problème de polarisation de l'étage de sortie de l'OTA du S/H en raison d'un rail métallique très résistif. Ceci provoque une chute de tension au niveau de la source du transistor PMOS du deuxième étage de l'OTA et le fait passer dans la région linéaire.
Cependant, des test additionnels détaillés dans la partie en anglais du manuscrit ont permis de vérifier la fonctionnalité du CAN $\Sigma\Delta$ à entrelacement temporel et de la nouvelle technique d'interpolation.

VI Conclusion

La conception d'un CAN $\Sigma\Delta$ à entrelacement temporel a été présentée. Ce CAN utilise une nouvelle technique d'interpolation qui permet de réduire considérablement les tailles des capacités du modulateur et l'ordre du filtre anti-repliement requis.

Un prototype à 4 canaux a été fabriqué en une technologie CMOS 65 nm. L'ordre du modulateur P, le nombre de canaux actif M et le facteur d'interpolation N sont reconfigurables. Cela permet au CAN d'effectuer des échanges entre bande passante, résolution et consommation de puissance le rendant ainsi approprié pour les normes GSM, UMTS, EDGE, WiFi et WiMax.

Le test a donné des résultats très promettants pour le scénario GSM/EDGE avec un SNR pic de 80 dB pour une consommation de 1.74 mW. Malheureusement, une erreur de layout nous a empêché d'atteindre les performances visées dans les modes UMTS/DVB-T et WiFi/WiMax. Cependant, la fonctionnalité a été testée avec succès.

Une perspective de ce travail est de proposer une méthode permettant de déterminer avec précision la fréquence seuil de f_{lr} pour les CAN $\Sigma\Delta$. Cette méthodologie pourrait être basée sur l'approche présentée dans le section 2 ou sur une autre approche. La difficulté pour les CAN $\Sigma\Delta$ réside dans la diversité des possibilités de mise en œuvre d'un modulateur adapté pour un scénario donné. En fait, plusieurs degrés de liberté tels que l'architecture du modulateur, son ordre, le taux de suréchantillonnage et le nombre de bits du quantificateur sont des paramètres de conception. Tous ces paramètres interviennent dans l'établissement de la relation entre la consommation d'énergie et la bande de conversion et doivent donc être pris en considération pour déterminer une valeur optimisée de f_{lr}.

Chapter 1

Introduction

1.1 Motivations

The proliferation of a large number of wireless standards and the need for all in one communication devices have resulted in a demand for chipsets suited for multi-standard reception. Given the high constraints on power consumption at the mobile end, an efficient implementation of these chipsets requires the reconfiguration of the receiver to allow it to adapt to the different standards.
A key component in any receiver and especially in a multi-standard receiver is the analog to digital converter (ADC). Its operation comprises two steps: 1) Sampling, which makes the signal discrete in time and thus determines the ADC's speed; 2) Quantization, which makes the signal discrete in amplitude and thus determines the ADC's resolution. The diversity of the requirements in terms of speed and resolution of radio standards makes the design of a multi-standard ADC a challenging task.
Fig. 1.1 shows a selection of state of the art ADCs from 2000 to 2010. Four types of ADCs are considered: flash, pipeline, Successive approximation (SAR) and Delta Sigma ($\Delta\Sigma$). As it can be seen, this latter is a good candidate for high resolution conversion (higher than 12 bits) which is required for some radio standards such as EDGE and GSM. In fact, oversampling and noise shaping make $\Delta\Sigma$ ADCs robust against circuit errors and thus allow them to reach higher resolutions than Nyquist rate converters [1] [2]. Besides, $\Delta\Sigma$ ADCs offer an easy way to perform a speed to resolution exchange by adjusting their oversampling ratios. However, their bandwidth is narrow compared to some radio standards specifications such as WiMax or some LTE standards.
Several techniques based on parallelism allow to increase conversion bandwidth of classical $\Delta\Sigma$ ADCs: time interleaved $\Delta\Sigma$ [3], $\Pi\Delta\Sigma$[4], block filtering $\Delta\Sigma$[5] and frequency band decomposition [6]. Moreover, parallelism provides an additional parameter of reconfiguration which is the number of active channels. This allows to perform speed to power consumption exchange.
The goal of this work is to design a reconfigurable parallel $\Delta\Sigma$ ADC suited for multi-standards reception. An advanced 1.2 V 65 nm CMOS process will be used for this design thereby making it more challenging [7]. In fact, using an older process such as 0.13 μm or 0.18 μm relaxes the constraints on the analog design compared to a 65 nm process. Nevertheless, this latter was retained to profit from the scalability of the $\Delta\Sigma$'s digital blocks such as the decimation filter or calibration blocks or other digital signal processing blocks that could be included on the same chip.

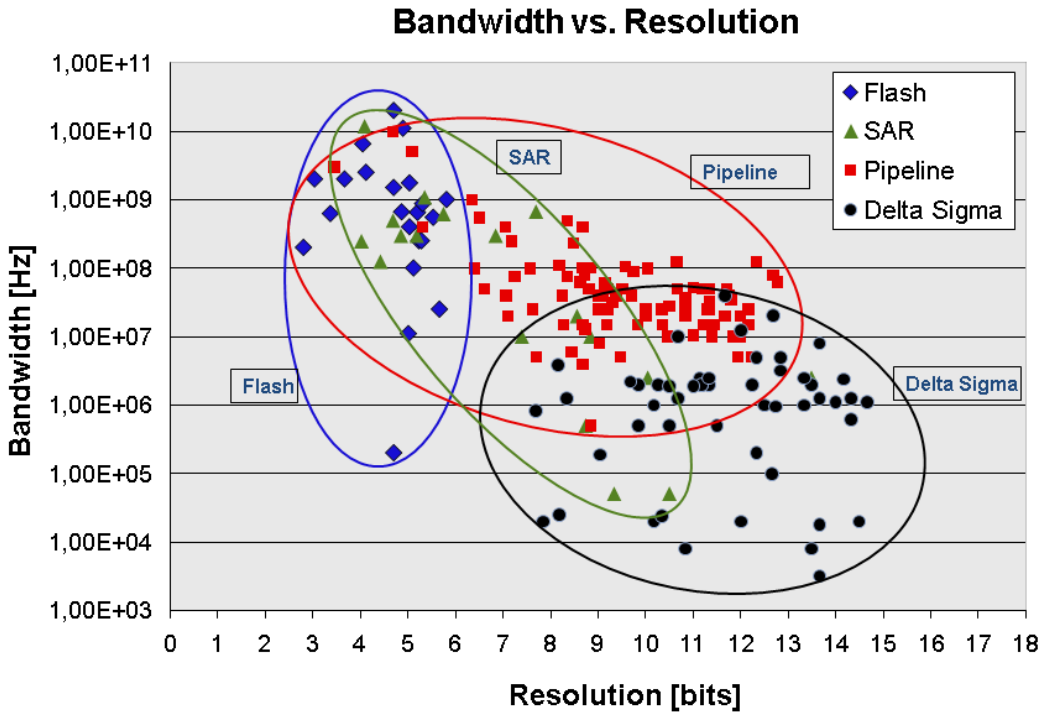


Figure 1.1: Selection of ADCs placed in the bandwidth vs resolution space

1.2 Organization

The organization of the thesis is as follows:

Chapter 2 discusses the use of parallelism. Its sheds light on the advantages of employing parallelism compared to a one channel solution. It also reviews the main drawbacks of this technique specially the channel mismatch that arises due to process variation.

Chapter 3 gives an overview of the operation of $\Delta\Sigma$ modulators. It presents also two comparative analyses. The first compares continuous time to discrete time and hybrid modulators. The second compares low pass to high pass modulators. These two analyses will allow to explain in details the operation of $\Delta\Sigma$ modulators and to choose the most suited implementation (continuous time, discrete time or hybrid) and noise shaping style (low pass or high pass) for the modulator employed in the parallel ADC.

Chapter 4 explains, in a first place, the choice of the time interleaved architecture over the other parallel architectures. Afterwards, it expounds a novel interpolation technique for time interleaved $\Delta\Sigma$ ADC that reduces their high sensitivity to thermal noise. Finally, the retained solutions for channel mismatch are presented.

Chapter 5 presents the design of a four channels time interleaved $\Delta\Sigma$ ADC in a 1.2 V 65 nm CMOS process suited for the GSM, EGDE, UMTS, DVBT, WiFi and WiMax standards. This ADC employs the novel interpolation technique presented in chapter 4. This chapter presents the measurement results as well.

Chapter 6 shows conclusions and presents perspectives and future research directions.

1.3 Contributions

The main contributions of this work are as follows:

1. A novel technique to establish the relation between the power consumption and frequency for analog blocks [8]
2. An extended comparative analysis between high pass and low pass $\Delta\Sigma$ modulators
3. A novel technique to reduce the impact of Hysteresis in $\Delta\Sigma$ ADCs [9]
4. A novel interpolation technique for time-interleaved $\Delta\Sigma$ ADCs [10] [11]
5. The implementation of four channels time interleaved $\Delta\Sigma$ ADC in a 1.2 V 65 nm process suited for multi-standards conversion [12] [13] [14].
6. An extended analysis of CMOS switch operation [15]
7. An extended overview of the analog layout considerations and matching techniques

Chapter 2

Parallelism

2.1 Power consumption vs frequency

With the prevalence of high data rate applications, high-speed high-resolution low-power ADCs are considered to be one of the key components in a system. Two main approaches to improve ADC's speed exist. The first consists of increasing the performance of ADC's blocks which is paid by a power consumption increase. The second approach is the use of parallelism. In order to compare these approaches, we propose to examine the behaviour of consumption with frequency change. Therefore, let us consider the circuit of a time-interleaved (TI) M channels ADC shown in Fig. 2.1 [16]. Each channel consists of a switched capacitor (SC) double-sampled Sample and Hold (S/H) [17] and an ADC. The digital outputs of the ADCs are multiplexed to obtain the final overall output. Regarding the S/Hs, an operational transconductance amplifier (OTA) is shared by two channels. This architecture known as OTA sharing or double-sampling avoids the idle time of the OTA and minimizes the die area and power consumption [18]. In fact, for a pair of channels sharing the same OTA, when the first one is in the sampling phase, the other is in the hold phase and *vice versa*. Therefore, for a M-channels S/H, $M/2$ OTAs are required. The ADC overall sampling frequency f_s is given by:

$$f_s = M \cdot f_{op} \tag{2.1}$$

where f_{op} is the operation frequency.

The operation of the S/H is one of the most restraining part of ADCs because it deals with continuous signal. Moreover, errors introduced at this level are propagated to all succeeding levels [19]. Thereby, optimizing this stage is necessary to achieve the required performance of the ADC. The main power consuming element of the S/H is the OTA. Its induced errors appear at the S/H output mainly as distortions and can be measured thereby using Signal to total harmonic distortion ($STHD$). Therefore, we will use the following Figure of Merit (FoM) to measure its performance:

$$\text{FoM} = \frac{P}{2^{(STHD-1.76)/6.02} \times f_s}, \tag{2.2}$$

where P is the power consumption

The THD added by the OTA depends mainly on the portion of the time while it is working in the slew rate (SR) regime. It arises whenever the circuit current sink is greater than OTA saturation current (I_{sat}). The OTA continues to provide this maximum current until the current sink becomes lower than I_{sat}. The settling error corresponds to the difference

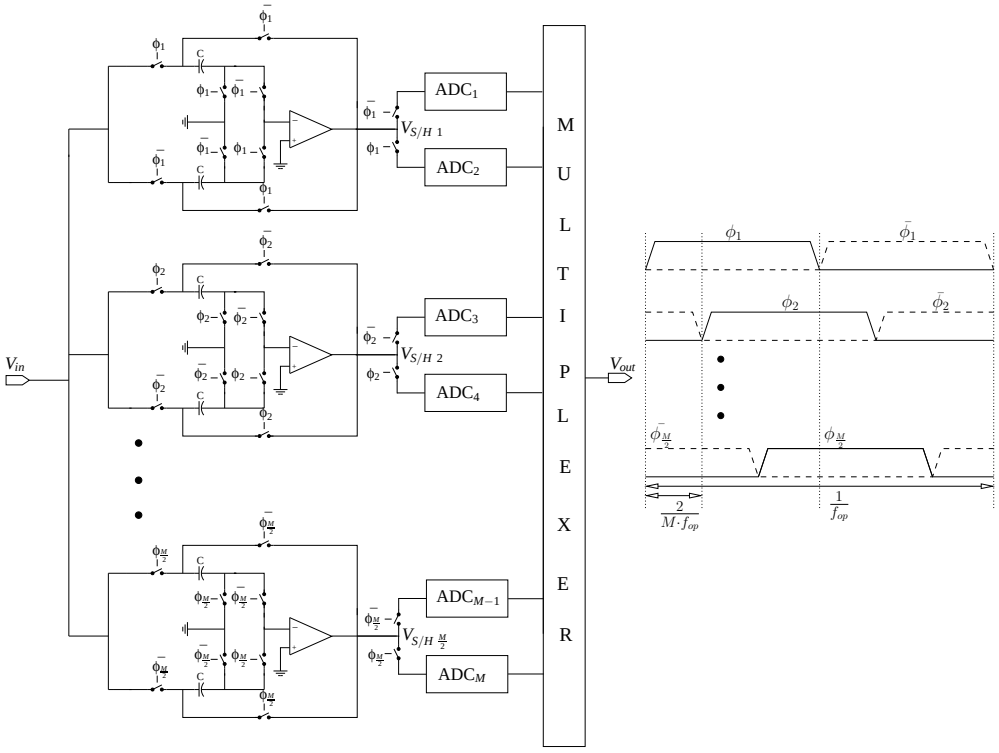


Figure 2.1: Circuit of a TI ADC

between V_{final} and $v(t)$ at the end of the settling time, where V_{final} is the value taken by $v(t)$ if the settling time was infinite. As it is shown in Fig. 2.2, this error exists even if I_{sat} is greater than the current sink. Its effect on the hold sample can be seen just as a linear gain. Meanwhile, when the SR portion of time is significant, harmonic distortions appears in the frequency domain.

To find the sought-after relation between the power consumption and frequency, the technique that we propose is to find the power consumption required for different f_{op}s to achieve a given resolution. It can be summarized by the following steps. A transient electrical simulation of one double-sampled S/H circuit is performed and since the main source of consumption in the S/H is the OTA, all other components are implemented using quasi-ideal models. Then, for a given OTA topology, several versions of OTA are designed forming what we call a family. The difference between these versions is that each one has a different saturation current I_{sat}, while the other OTA characteristics such as gain and phase margin are kept the same. Afterwards, a target signal to total harmonic distortion ($STHD_{target}$) is fixed. It is measured for the output $V_{S/H}$ of the S/H. The value of $STHD_{target}$ could depend on the required specifications of the ADCs. Then, for each version of the OTA, the operation frequency f_{op} for which the $\mid STHD_{V_{S/H}} - STHD_{target} \mid < \varepsilon$ is found. This is done by means of a simple trial-and-error algorithm summarized by the diagram shown in Fig. 2.3. The value of ε is chosen as a compromise of the accuracy and the simulation runtime.

The proposed extraction technique has been applied on the gain boosted folded cascode OTA shown in Fig. 2.4 implemented in a 1.2 V 65 nm CMOS technology. As it has been previously mentioned, all the circuit components are quasi-ideal models except the OTA. The switch is modelled by a 100 Ω resistance when on and by a 10 MΩ resistance when off. The capacitive load on the S/H is 4 pF. The input signal is a sinusoid of 0.5 V peak to peak (Vpp)

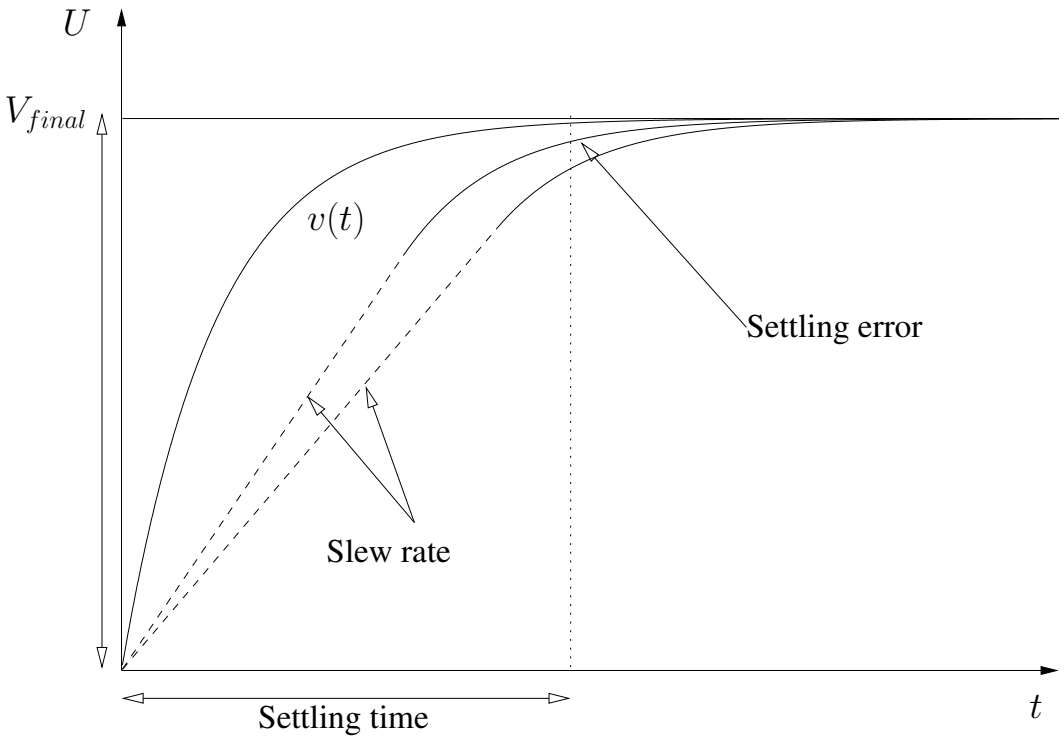


Figure 2.2: Slew rate

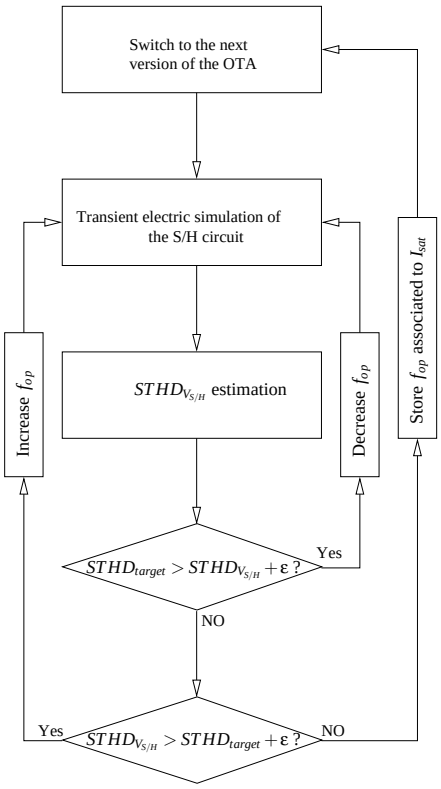


Figure 2.3: f_{op} search algorithm

Vdd	1 V
DC Gain	60 dB
f_t	266 MHz
PM	65^0

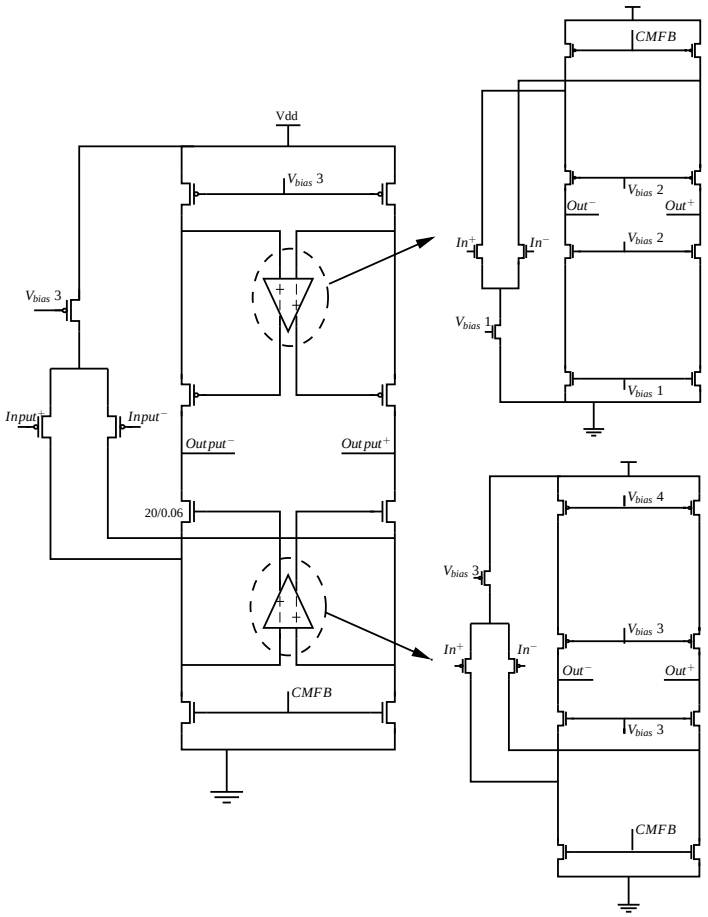


Figure 2.4: OTA circuit

differential amplitude and the $STHD_{target}$ is equal to 72 dB.

Twelve versions of this OTA have been realized. Their I_{sat} vary between 100 μA and 2.4 mA. All the OTA versions have a gain around 60 dB for a 1 V differential excursion and a $65^o \pm 1^o$ phase margin. The f_{op} search algorithm was implemented with Scilab and interfaced with an electric simulator (Spectre). The simulations are carried out in a 64 bits Linux server with two 3.6 GHz Intel Xeon CPUs and 4.6 GB memory. The simulation runtime was 10 hours for an ε of 0.5 dB.

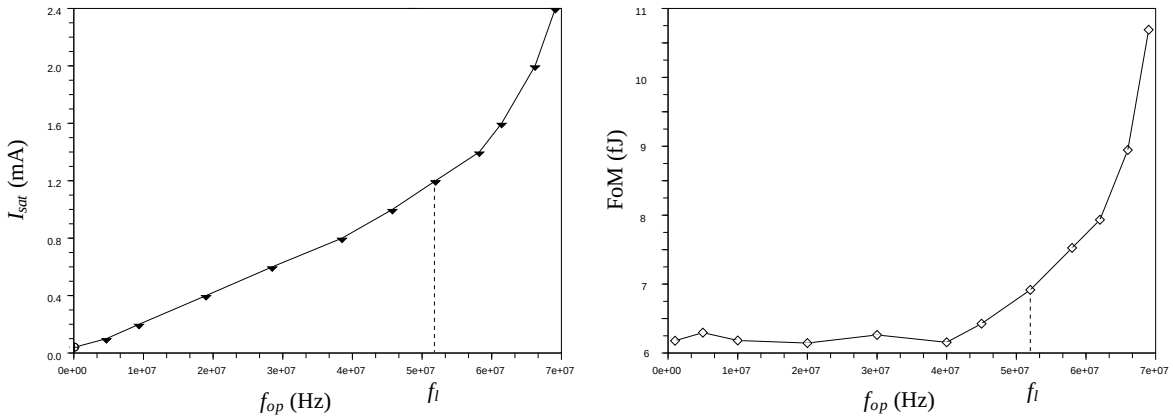


Figure 2.5: a)I_{sat} vs f_{op} b)FoM vs f_{op}

The obtained results are presented in Fig. 2.5.a). It can be noted that the curve is linear at low frequencies and is exponential at high frequencies. The linear behaviour is limited in this case at 52 MHz. This behaviour is predictable. In fact, increasing f_{op} will decrease the settling time and to preserve the same THD, I_{sat} must be increased to reduce the portion of time while the OTA is operating in the slew rate regime. The increasing of I_{sat} is made by scaling-up the dimensions of the transistors of the current source. This increasing will be accompanied by an augmentation of the parasitic capacitances of the OTA and then a portion of the current is reserved to charge these capacitances. In Fig. 2.5 b), the FoM vs f_{op} curve is plotted using the same simulation results. The curve is characterized by a frequency band $f_{op} < f_l$ for which the FoM is constant and minimal (+10% of the minimum). For higher frequencies, the FoM increases. Therefore, to preserve the lower FoM possible, operating at frequencies higher than f_l should be avoided by using parallelism. Ideally, the power consumption of the TI system will be M times higher than a single channel and since its conversion bandwidth is also multiplied by M, its FoM will be minimal even if $f_s > f_l$. Unfortunately, this assumption is not perfectly correct. In fact, parallelism introduces new errors that must be dealt with. These errors will discussed in next section.

2.2 Drawbacks of parallel circuits

2.2.1 Time-interleaved circuits

Theoretically, if all circuit components were ideal, ADC input referred offset will be null and its input referred gain will be one. Unfortunately, due to circuit imperfections, they deviate from their theoretical values. Since all samples suffer from the same error, this problem is not very critical in single path ADCs. It causes a variation in signal power and a DC offset. These imperfections could be easily corrected during digital signal processing. However, in a multi

path ADC, each channel has its own input referred gain and offset. This causes significant errors during signal reconstruction. The impact of these errors in addition to clock skew and bandwidth mismatch will be discussed in this subsection.

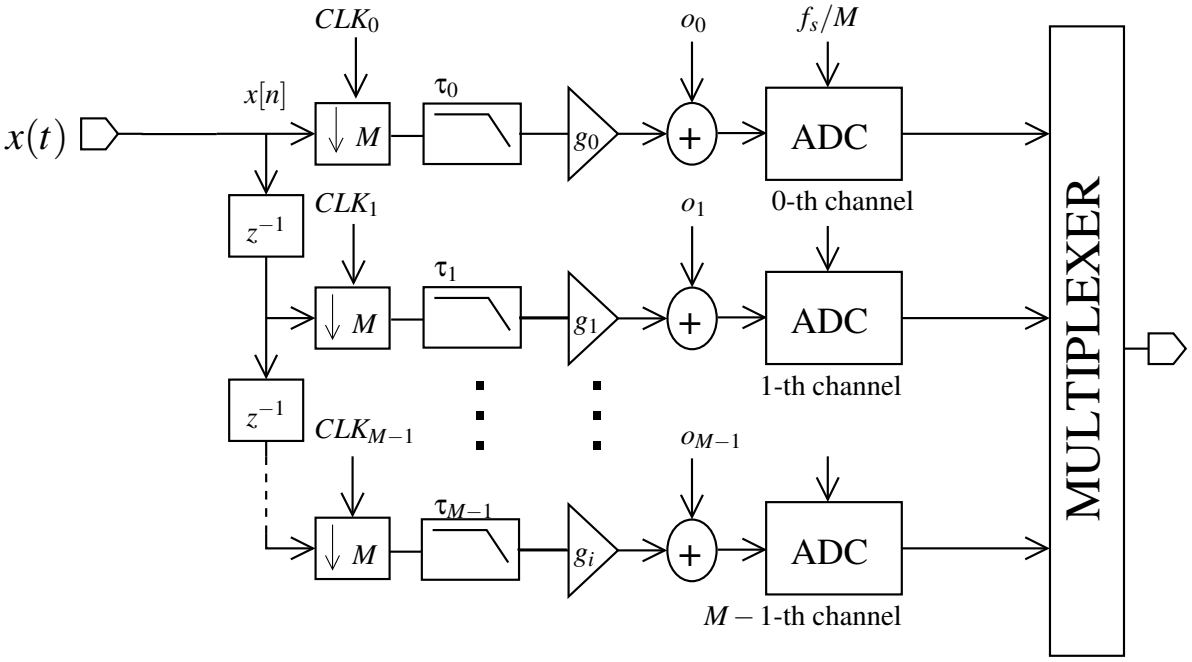


Figure 2.6: TI ADC

2.2.1.1 Gain mismatch

The impact of gain mismatch on signal spectrum if no other error sources were considered is given by [20]:

$$Y(e^{j2\pi f}) = \frac{1}{MT_s}\sum_{i=0}^{M-1}\sum_{k=-\infty}^{+\infty} g_i e^{-j2\pi\frac{ik}{M}} X(2\pi f - \frac{2\pi}{MT_s}k) \tag{2.3}$$

To simplify Eqn.2.3, let us consider that $M = 2$ and X is a sinewave. The digital spectrum between -$f_s/2$ and $f_s/2$ is then given by:

$$Y(e^{j2\pi f}) = \frac{1}{2T_s}[\underbrace{(g_0 + g_1)\frac{\delta(f-f_{in})-\delta(f+f_{in})}{2}}_{A} + \underbrace{(g_0 - g_1)\frac{\delta(f-(\frac{f_s}{2}-f_{in}))-\delta(f+(\frac{f_s}{2}-f_{in}))}{2}}_{B}]$$

The two terms of the equation are sine waves. The term A whose frequency is equal to f_{in} corresponds to the input sine. Meanwhile, the term B corresponds to a parasitic tone that arises due to gain mismatch at the frequency $f_s/2 - f_{in}$. If $g_0 = g_1$ which corresponds to the no error scenario, the parasitic tone is cancelled. Meanwhile if $g_0 = -g_1$, the term A is nullified and all the power will be concentrated in B. This operation known as chopping could be done in purpose to transpose the signal from f_{in} to $f_s/2 - f_{in}$.
Fig. 2.7 shows the output spectrums of a two and four channels ADCs in the presence of gain mismatch. As it can be seen, for $M = 4$, two additional tones arise at $f_s/4 \pm f_{in}$. In general, for a M channels ADC, parasitic tones arise at at $\frac{i.f_s}{M} \pm f_{in}$ with $0 < i < M$.

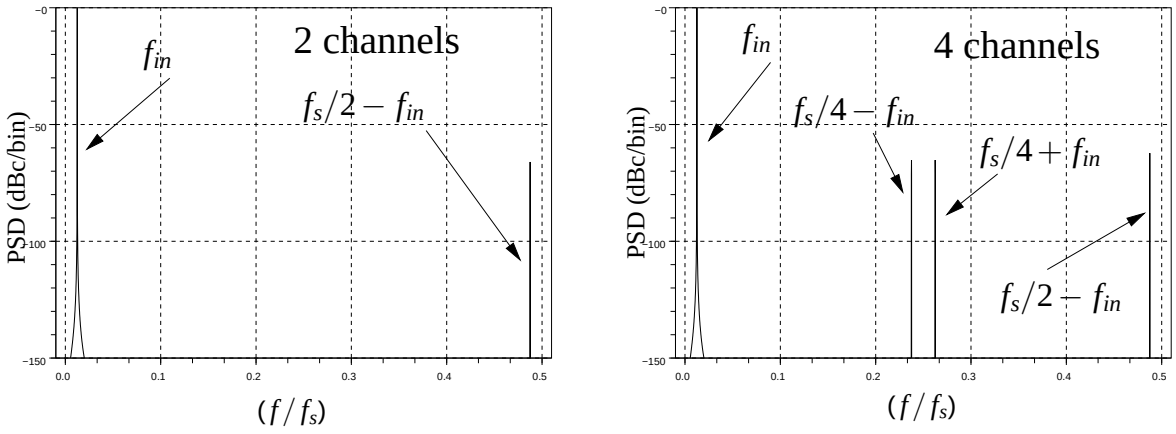


Figure 2.7: Output spectrums for a 2 and 4 channels ADCs in the presence of gain mismatch

If channels' gain g_i were assumed to be Gaussian random variables with one mean and σ_g^2 variance, the SNDR loss caused by gain mismatch is given by the Eqn.2.4 [20].

$$SNDR \simeq 10Log(\frac{g}{\sigma_g}) - 10Log(1 - \frac{1}{M}) \tag{2.4}$$

2.2.1.2 Offset mismatch

The impact of offset mismatch on signal spectrum if no other error sources were considered is given by [20]:

$$Y(e^{j2\pi f}) = \frac{1}{T_s}\sum_{k=-\infty}^{+\infty} X(2\pi f - \frac{2\pi}{T_s}k) + \frac{2.\pi}{M}\sum_{i=0}^{M-1}\sum_{k=-\infty}^{+\infty} o_i e^{-j2\pi\frac{ik}{M}}\delta(2\pi f - \frac{2\pi}{MT_s}k) \tag{2.5}$$

To simplify Eqn.2.5, let us consider that $M = 2$ and X is a sinewave. The digital spectrum between -$f_s/2$ and $f_s/2$ is then given by:

$$Y(e^{j2\pi f}) = \frac{1}{T_s}\underbrace{(\frac{\delta(f - f_{in}) - \delta(f + f_{in})}{2}}_{A} + \underbrace{\pi(o_0 + o_1)\delta(f)}_{B} + \underbrace{\pi(o_0 - o_1)(\delta(f - \frac{f_s}{2}) + \delta(f + \frac{f_s}{2}))}_{C}$$

As it can be seen, in a M=2 scenario, the impact of offset mismatch is the arising of parasitic tones at 0 and at $f_s/2$. In general, in a M channels scenario, M tones are created at $\frac{i.f_s}{M}$ with $0 < i < M - 1$. These results are confirmed in Fig. 2.8.
If offset values o_i were assumed to be Gaussian random variables with zero mean and σ_o^2 variance, the SNDR loss caused by offset mismatch is given by the Eqn.2.6 [20].

$$SNDR \simeq 10Log(\frac{A_{in}^2}{2\sigma_o^2}) \tag{2.6}$$

2.2.1.3 Clock skew

The sampling clocks of two successive channels must be separated by exactly T_s to preserve the same operation as a single path circuit. Unfortunately, due to channels mismatches, the

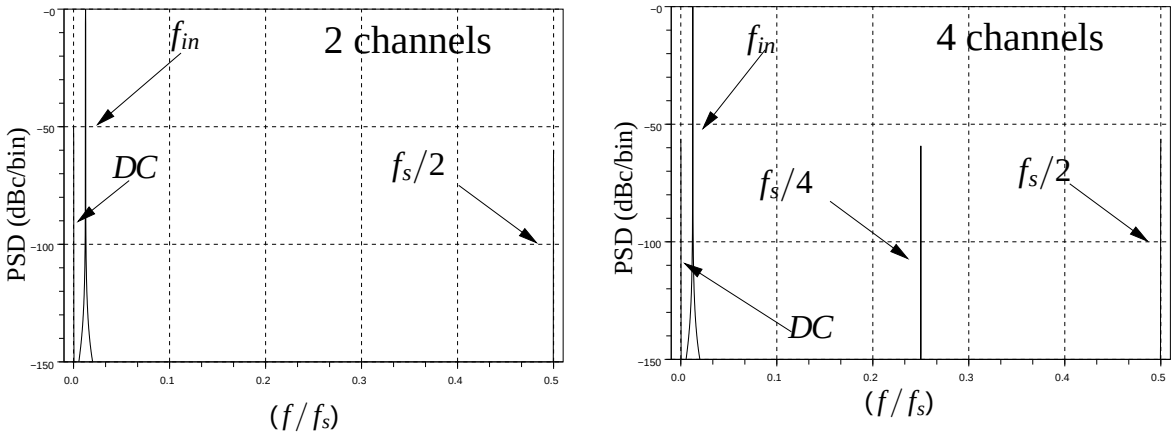


Figure 2.8: Output spectrums for a 2 and 4 channels ADCs in the presence of offset mismatch

delay between clock edges is not exactly as predicted. In fact, the process and environment variations on components that process the clock signal in each channel such as clock rails and digital gates deviates the practical delay from the theoretical one. As shown in Fig. 2.9, the jitter can be seen as a Gaussian distribution of the sampling instant. While, the clock skew is a constant deviation of the Gaussian distribution mean from the theoretical instant. The

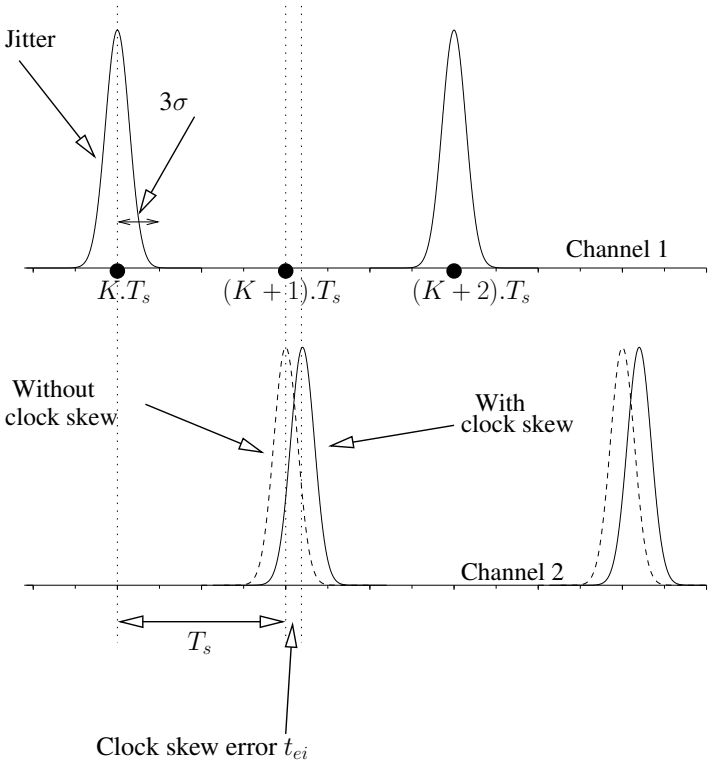


Figure 2.9: Clock skew modelization

impact of clock skew on signal spectrum if no other error sources were considered is given by

[21]:

$$Y(e^{j2\pi f}) = \frac{1}{MT_s}\sum_{i=0}^{M-1}\sum_{k=-\infty}^{+\infty} e^{j(2\pi f - \frac{2\pi k}{M})\frac{t_{ei}}{T_s}} e^{-j2\pi\frac{ik}{M}} X(2\pi f - \frac{2\pi}{MT_s}k) \tag{2.7}$$

To simplify Eqn.2.7, let us consider that $M = 2$ and X is a sinewave. The digital spectrum between -$f_s/2$ and $f_s/2$ is then given by:

$$Y(e^{j2\pi f}) = \frac{1}{2T_s}[\underbrace{(1 + e^{j2\pi f_{in}\frac{t_{e1}}{T_s}})\frac{\delta(f - f_{in}) - \delta(f + f_{in})}{2}}_{A} + \underbrace{(-1 + e^{j2\pi f_{in}\frac{t_{e1}}{T_s}})\frac{\delta(f - (\frac{f_s}{2} - f_{in})) - \delta(f + (\frac{f_s}{2} - f_{in}))}{2}}_{B}]$$

The impact of clock skew on the output spectrum is the arising of a parasitic tone (term B) at $f_s/2 - f_{in}$ similarly to gain mismatch. Nevertheless, in this case, the error power is f_{in} dependent. This can be seen in the SNDR Eqn. 2.8 [21]. The timing errors t_{ei} were assumed to be Gaussian random variables with zero mean and σ_{te}^2 variance.

$$SNDR \simeq 20Log(\frac{1}{2\pi\sigma_{te}f_{in}T_s}) - 10Log(1 - \frac{1}{M}) \tag{2.8}$$

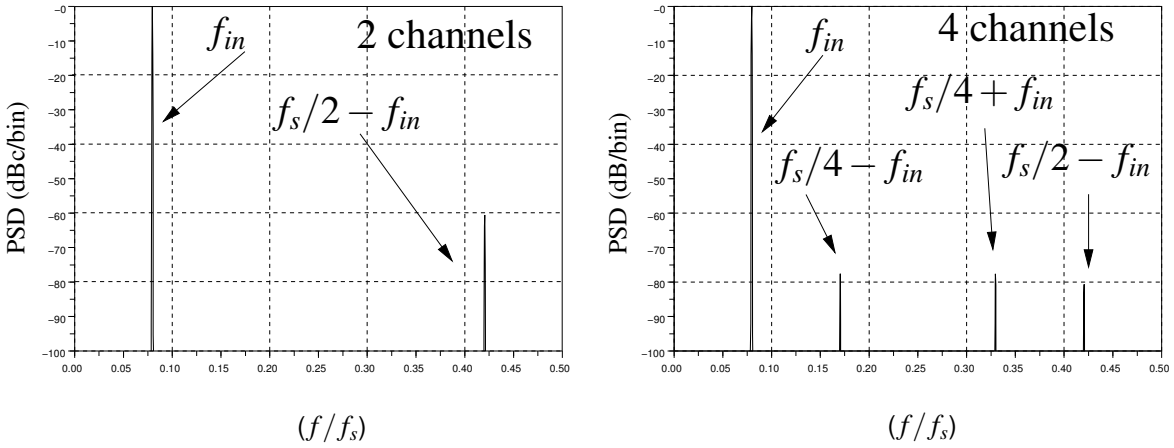


Figure 2.10: Output spectrums for a 2 and 4 channels ADCs in the presence of clock skew

2.2.1.4 Bandwidth mismatch

In SC ADCs, the sampling circuit behaves as low pass filter whose characteristics depend on the values of the sampling capacitor and the resistances of the switches (section A.2). In a TI ADC, if all channels are identical, this low pass behaviour creates a small ripple inside the band that can be corrected in the digital domain. Unfortunately, due to the spacing between channels, the process variation is different in each channel thereby leading to a mismatch between the channels' frequency responses.
The impact of this error, known as bandwidth mismatch, on signal spectrum if no other errors were considered is given by [22]:

$$Y(e^{j2\pi f}) = \frac{1}{MT_s}\sum_{i=0}^{M-1}\sum_{l=0}^{M-1}\sum_{k=-\infty}^{+\infty} H_l(f)e^{-j2\pi\frac{i.l}{M}} X(2\pi f - \frac{2\pi}{MT_s}k - \frac{2\pi}{T_s}i) \tag{2.9}$$

Where $H_l(f)$ is the frequency response of the l^{th} channel

To simplify Eqn. 2.9, let us consider that $M = 2$ and X is a sinewave. The digital spectrum between -$f_s/2$ and $f_s/2$ is then given by[22]:

$$Y(e^{j2\pi f}) = \frac{1}{2T_s}[\underbrace{(\frac{1}{1+j2\pi f_{in}\tau_1} + \frac{1}{1+j2\pi f_{in}\tau_2})\frac{\delta(f-f_{in})-\delta(f+f_{in})}{2}}_{A} + \underbrace{(\frac{1}{1+j2\pi f_{in}\tau_1} - \frac{1}{1+j2\pi f_{in}\tau_2})\frac{\delta(f-(\frac{f_s}{2}-f_{in}))-\delta(f+(\frac{f_s}{2}-f_{in}))}{2}}_{B}]$$

Where τ_l is the time constant of the l^{th} channel

The impact of bandwidth mismatch on the output spectrum is quite similar to the impact of clock skew. In fact, it causes the arising of tones at $if_s/M \pm f_{in}$ and the error magnitude is also f_{in} dependent.
If τ_l were assumed to be Gaussian random variables with a mean equal to τ and σ_τ^2 variance, the SNDR loss caused by bandwidth mismatch is given by the Eqn. 2.10 [23] .

$$SNDR \simeq 20Log(\frac{1}{2\pi\sigma_\tau f_{in}\tau}) + 10Log(1+(2\pi f_{in}\tau)^2) - 10Log(1-\frac{1}{M}) \tag{2.10}$$

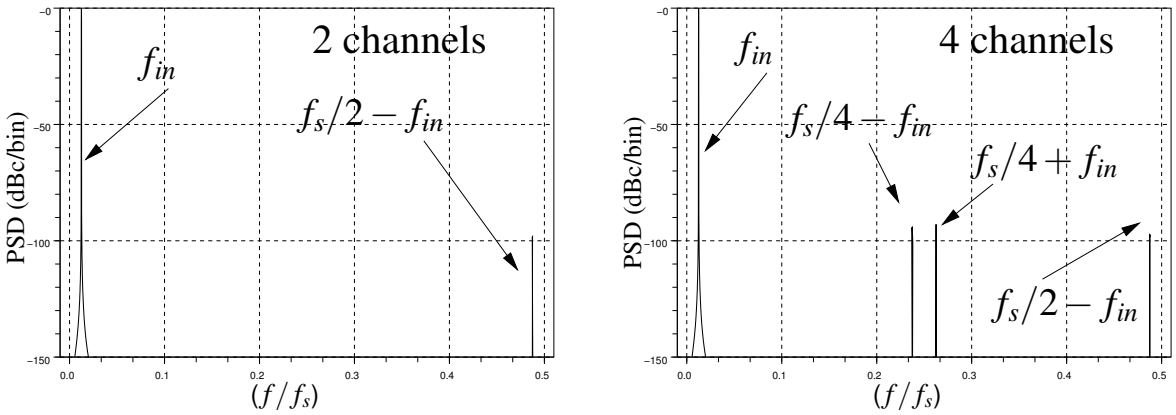


Figure 2.11: Output spectrums for a 2 and 4 channels ADCs in the presence of bandwidth mismatch

2.2.2 Frequency interleaved circuits

The operation of a TI ADC consists of allocating one out of M samples to each channel, allowing thereby to reduce the operation frequency by M. Meanwhile, in frequency interleaved (FI) architectures, the operation is based on allocating one over M of the conversion bandwidth to each channel which will also result in a reduction by M of the operation frequency. Fig. 2.12 shows the architecture of a FI ADC. Each channel has an analysis filter that selects its conversion band. If this filter has a frequency response that approaches the ideal frequency response shown in Fig. 2.13, the downsampling by M will only alias the channel sub-band

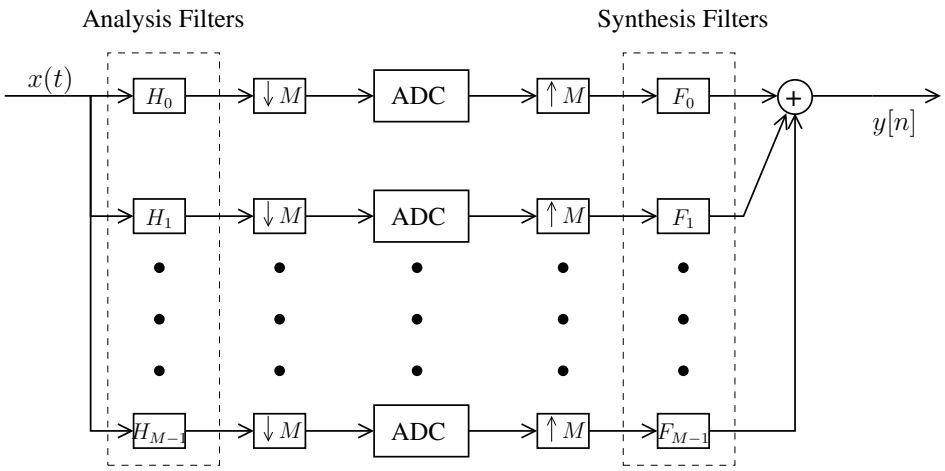


Figure 2.12: FI ADC

into baseband. Afterwards, since the conversion band was divided by M, the signal will be digitized at a M times lower frequency.

In this architecture, apart from the first channel, the offset is filtered by the synthesis filter. Therefore, offset mismatch has no impact. The gain mismatch causes a small ripple magnitude in the band that can be tolerated. Since it has very low sensibility to both gain and offset mismatch, this architecture seems to be very interesting. However, very sharp response filters have a very large power consumption which degrades considerably the FoM of the ADC and limits its use. A more appropriate approach is the one used for hybrid filter banks (HFB) [24] [25]. It consists of degrading the analysis filters' frequency response deliberately as shown in Fig. 2.13 and correcting their non-idealities in the synthesis filters by employing adapted algorithms. These algorithms compensate the filter impact by applying an inverse filtering and combine channels' outputs to reconstruct the signal in recovered bands. Therefore, there is a need to know the exact filtering of each channel which imposes the synthesis filters to deal with ADCs' gain mismatch and process variation on analysis filters, as well.
The impact of this approach is, thus, the transfer of the complexity from the analysis filters to the synthesis filters. Nevertheless, since they are digital, the price in terms of power consumption and die area is significantly lower than the former approach.

2.3 Conclusion

Fig. 2.14 shows a qualitative comparison of power consumption vs f_s. In fact, the power consumption of a multi-channel system is higher than M times the consumption of one channel operating at the same frequency. This is due to the additional blocks required for parallelism. In FI structures, analysis and synthesis filters are needed. While, in TI structures, analog or/and digital blocks must be added to deal with channel mismatch and clock skew. The architectures of these blocks depend on ADC's architecture and therefore will be discussed later. It was assumed that the overall power consumption of the parallel ADC is linear with frequency increase. This assumption is not always absolutely true due to the fact that the complexity of some correction algorithms may have a square or a cubic increase when the number of channels increases. Nevertheless, specially with technology advance that leads to significantly higher decrease in the power consumption of the digital part with respect to the analog part, the difference can be considered negligible compared to the overall power

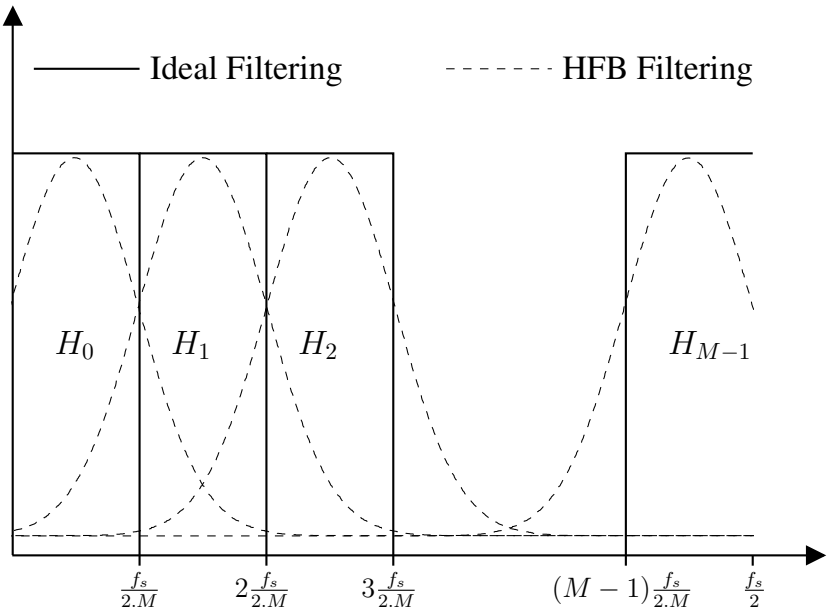


Figure 2.13: Frequency response of analysis filters

consumption of the ADC.

When f_s equals f_{lr}, the use of parallelism begins to be justified because at this point, the multi-channel and the single channel structures have the same FoM. And as f_s increases, the interest of using parallelism will increase due to the fact that in contrary to a single channel whose FoM degrades with f_s increase, a multi-channel ADC has a almost constant FoM.

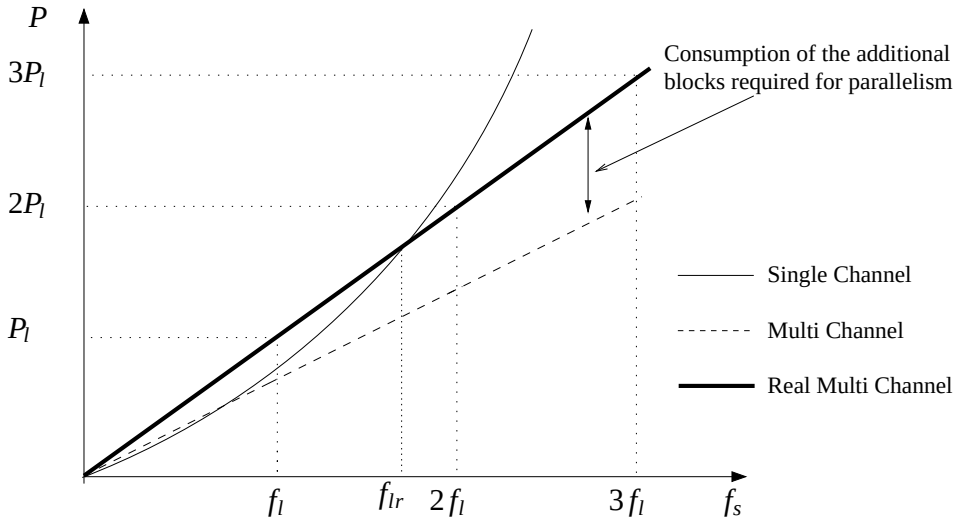


Figure 2.14: Power consumption vs frequency comparison between a single channel and a multiple channel

Chapter 3

$\Delta\Sigma$ Modulators

3.1 $\Delta\Sigma$ operation

$\Delta\Sigma$ modulation is an improvement of Δ modulation. As its name indicates, it consists of placing an integrator before the Δ modulator. Its operation is based on making the average of the digital output converge to the average of the analog input. $\Delta\Sigma$ ADCs are characterized by two main points: speed to resolution exchange and noise shaping. In fact, in a $\Delta\Sigma$ ADC, the analog signal is oversampled at a rate f_{op}, OSR times faster than f_s (where f_s is equal to two times the signal bandwidth B) but is quantized with a low resolution (1 to 4 bits usually). A decimation filter follows the $\Delta\Sigma$ modulator and ensures the switch-over from the high speed low resolution code to the desired code at the Nyquist rate. The noise transfer function of $\Delta\Sigma$ modulators shapes the quantization noise in a manner to force it out of the band of interest.
As it will pointed out later at different points of this work , these two characteristics relaxe the constraints on the analog blocks of the modulator and the requirements on the Anti-Alias filter (AAF) that precedes it thereby making $\Delta\Sigma$ ADCs a go-to solution for high resolution low power applications.

3.1.1 General

To have a better idea of $\Delta\Sigma$ modulator operation, let us consider the second order modulator of Fig. 3.1 [26].
Using the quantizer linear equivalent model, the modulator output in the Z-domain can be determined:

$$Y(z) = \underbrace{\frac{1}{(G-1)z^{-2}+(2G-1)z^{-1}+1}}_{STF(z)} \times X(z) \; + \; \underbrace{\frac{(1-z^{-1})^2}{(G-1)z^{-2}+(2G-1)z^{-1}+1}}_{NTF(z)} \times N(z)$$

Where STF stands for signal transfer function and NTF for noise transfer function.
If the quantizer gain G is assumed to be one, $Y(z)$ becomes:

$$Y(z) = \underbrace{(1)}_{STF(z)} \times X(z) \; + \; \underbrace{(1-z^{-1})^2}_{NTF(z)} \times N(z)$$

The frequency response of the NTF presents the characteristic of a High pass filter. As a consequence, the quantization noise is attenuated for low frequencies and amplified for high

frequencies. This result is confirmed in Fig. 3.2 b) and Fig. 3.3 b) which show the ΔΣ output spectrums for a sinusoidal input and for a DC input of 0.2 $Vref$ respectively (Where $Vref$ is the reference voltage of the quantizer and of the feedback digital to analog converter (DAC). For all system simulations, $Vref$ is equal to 1 V). The tones in Fig. 3.3 b) are due to the fact that the input is a DC signal. They arise at $i\frac{A_{DC}}{Vref}f_{op}$ where A_{DC} is the DC input value and with $i \epsilon \mathbb{N}$ [1].

Fig. 3.2 a) and Fig. 3.3 a) show the output of the 1-bit DAC in time domain for the same inputs. It can be noted in Fig. 3.2 a) that as the input signal amplitude increases, the number of ones in the surrounding output samples increases with respect to the number of minus ones. For example, when the signal is near to the maximum, the output is mainly plus ones, when the signal is near to the minimum the output is mainly minus ones and it is equally distributed when the input signal is around zero. Hence it can be seen that the average of the output follows the average of the input.

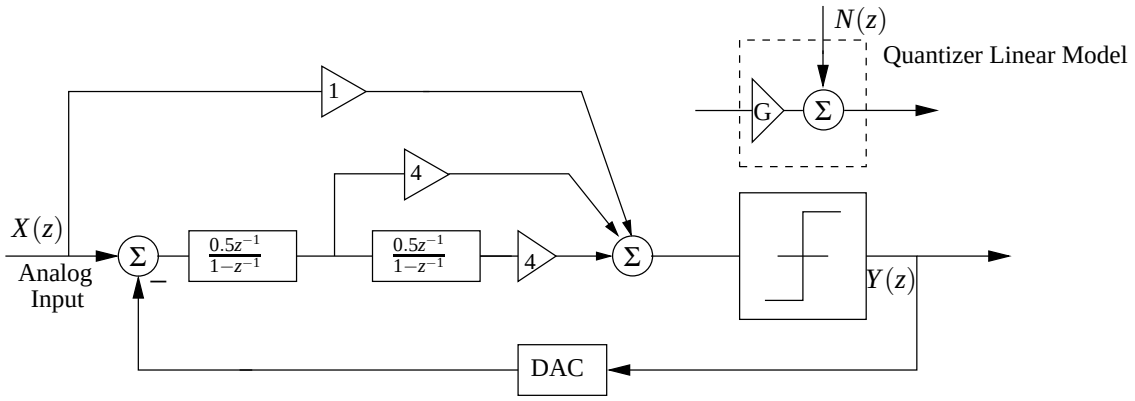


Figure 3.1: Block diagram of a 2^{nd} order ΔΣ modulator

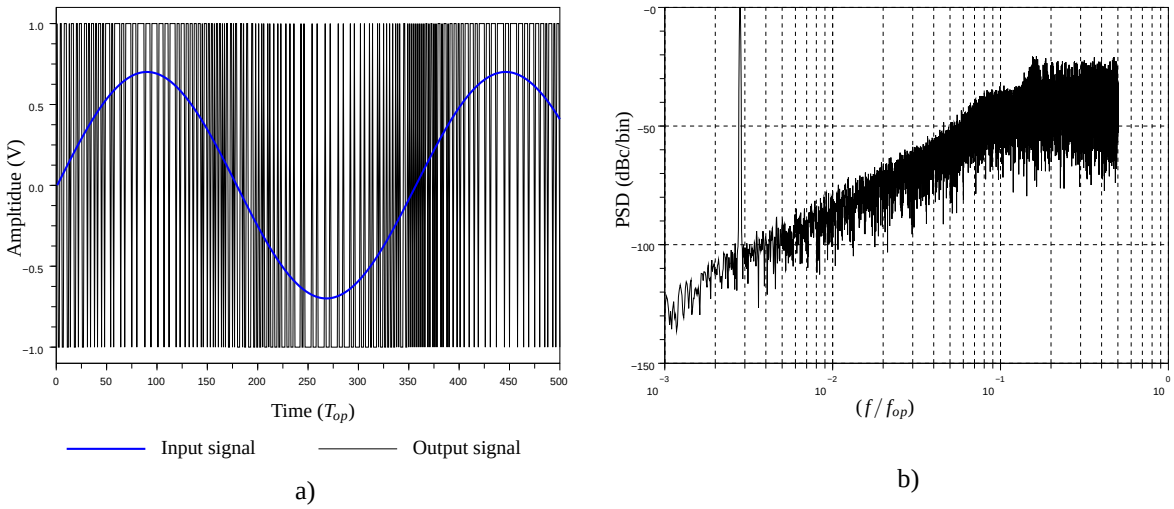


Figure 3.2: ΔΣ modulator input and output for a sine input a)time domain b)frequency domain

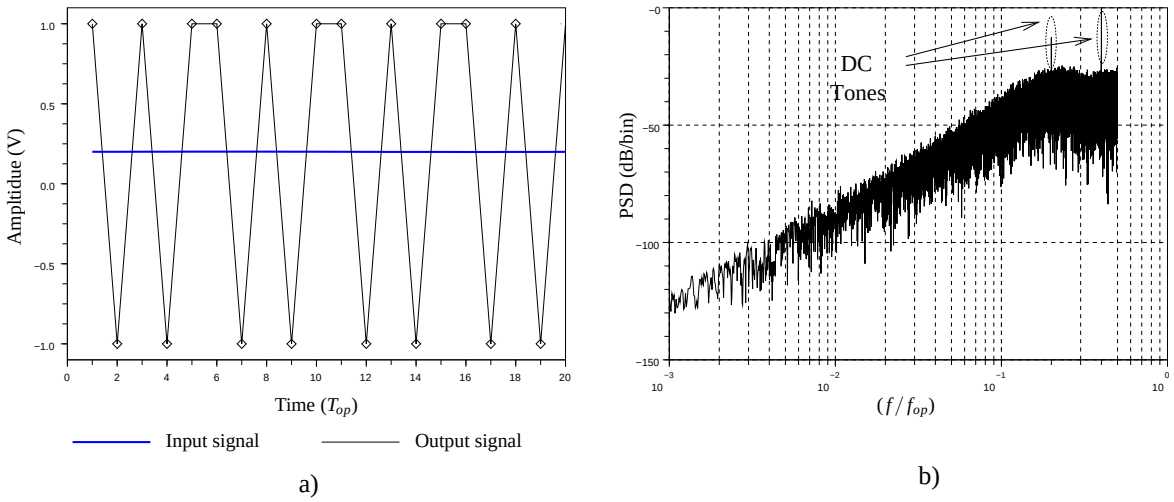


Figure 3.3: $\Delta\Sigma$ modulator output for a DC input a)time domain b)frequency domain

3.1.2 Noise shaping

$\Delta\Sigma$ ADCs can be divided into 3 main categories: low pass (LP) modulators, high pass (HP) modulators and band-pass (BP) modulators. The analog signal is at baseband for LP modulators, at $f_{op}/2$ for HP modulators and at an intermediate frequency for BP modulators. It is the modulator NTF that characterizes the modulator type. Fig. 3.4 shows the NTF for the three types of modulators. As it can be seen, the NTF is designed to push the quantization noise out of the band of interest. It can be seen also that the in-band noise decreases when the modulator order increases but at the same time the out of band quantization noise increases imposing thus a more severe filtering by the decimation filter and consequently a higher order.

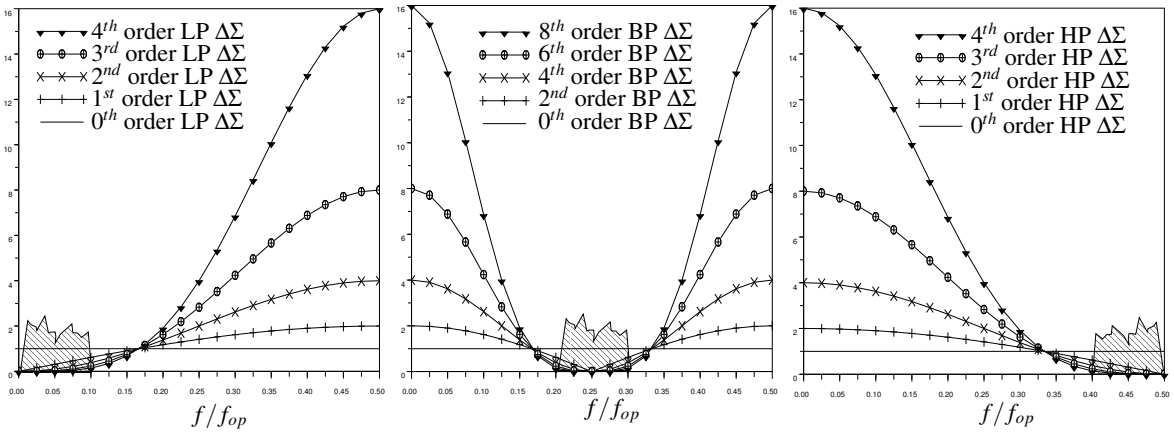


Figure 3.4: Noise shaping

Generally the NTFs for a L^{th} order modulator are given by:

$$NTF = (1 - z^{-1})^L \quad \text{for a LP} \tag{3.1}$$

$$NTF = (1 + z^{-1})^L \quad \text{for a HP} \tag{3.2}$$

$$NTF = (1 + z^{-2})^{L/2} \quad \text{for a BP at } f_{op}/4 \tag{3.3}$$

The LP and the HP NTFs have an L^{th} order zero at dc and at $f_{op}/2$ respectively. While, the BP NTF has 2 $(L/2)^{th}$ order zeros: the first at $f_{op}/4$ and the second at -$f_{op}/4$. Consequently, the BP order is always even and a L^{th} order BP modulator has the same noise rejection as a $(L/2)^{th}$ order LP modulators or HP modulators as it can be noted in Fig. 3.4. BP modulator central frequency could be at any frequency between 0 and $f_{op}/2$. The NTF of a L^{th} order BP modulator with central frequency equal to f_c, can be deduced from the $L/2$ order LP modulators NTF using the transformation:

$$z \longrightarrow -z\frac{z - cos(2\pi\frac{f_c}{f_{op}})}{-cos(2\pi\frac{f_c}{f_{op}})z + 1} \tag{3.4}$$

The NTFs exposed are not the only way to realize ΔΣ modulators. In fact, it is possible to have multiple zeros of lower order than having one higher order zero (or two in the case of BP modulator). In fact, if the zeros' position is optimized, the in-band noise can be reduced. For example, for a 2^{nd} order LP modulator, if the zeros were placed at $\pm\frac{f_b}{\sqrt{3}}$ instead of placing both of them at the frequency zero, the SNR is increased by 3.5 dB[1].

3.1.3 Resolution and stability

In order to evaluate the achievable resolution by a ΔΣ ADC, let us calculate the in-band quantization noise power at the output of this later.
If the quantization noise $N(z)$ is assumed to be white, its power spectral density (PSD) is then given by:

$$PSD_N(f) = \frac{q^2}{12.f_{op}} = \frac{Vref^2}{2^{2n-2}12.f_{op}} \tag{3.5}$$

This noise is shaped by the modulator NTF that is equal to $(1 - z^{-1})^L$ for a typical LP modulator. Hence the quantization noise PSD at the modulator output is:

$$PSD_Q(f) = \frac{Vref^2}{2^{2n-2}12.f_{op}} \mid NTF(f) \mid^2 = (2sin(\pi f T_{op}))^{2L} \tag{3.6}$$

The in-band quantization noise can be determined by integrating $PSD_Q(f)$ over the band of interest. For an $OSR >> 1$, the approximation $sin(\pi f T_{op}) \approx \pi f T_{op}$ is valid which gives us:

$$P_Q = \int_{-B}^{B} PSD_Q(f)df \approx \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}\frac{Vref^2}{2^{2n-2}12} \tag{3.7}$$

If the STF is unitary, the SQNR at the modulator output is found by:

$$SQNR = 10Log\frac{P_{signal}}{P_Q}$$

$$SQNR \approx 1.76 + 20Log(\frac{A}{Vref}) + 6.02n + 10Log(2L+1) - 9.9L + (6L+3)ln_2(OSR) - 20Log(\pi) \tag{3.8}$$

Where A is the input signal amplitude
Equation 3.8 shows that the SQNR at the output of a ΔΣ modulator is fixed by three parameters: the modulator order L, the number of bits of the quantizer n and the oversampling

ratio OSR. Consequently, achieving a certain $SQNR$ can be realized by different sets of these three parameters and it is the designer duty to find the set that reduces the most the overall complexity of the modulator. In fact, increasing n requires an exponential increase of the number of comparators. Besides, a larger n leads also to an increase of the number of bits of the feedback DAC. As a consequence, the matching or calibration algorithm required to deal with the sensitivity of the DAC to component mismatch will become more complex, hence more consuming. While increasing the OSR increases f_{op} and consequently the speed requirements on the OTAs. Whereas the selection of the modulator of a higher order has an impact of the stability of the modulator. In fact, the quantization model used in Eqn. 3.5 is based on the assumption that the quantizer gain is constant and that its input signal does not exceed $Vref$. However, for large input values, the quantizer input is frequently higher than $Vref$ and its gain decreases significantly thereby leading to instability as shown in Fig. 3.5. When the modulator order L is increased, the overall quantization noise power increases as shown in Fig. 3.4. This causes a higher excursion at the quantizer input leading to a lower maximum stable amplitude (MSA) hence to a lower $SQNR$.

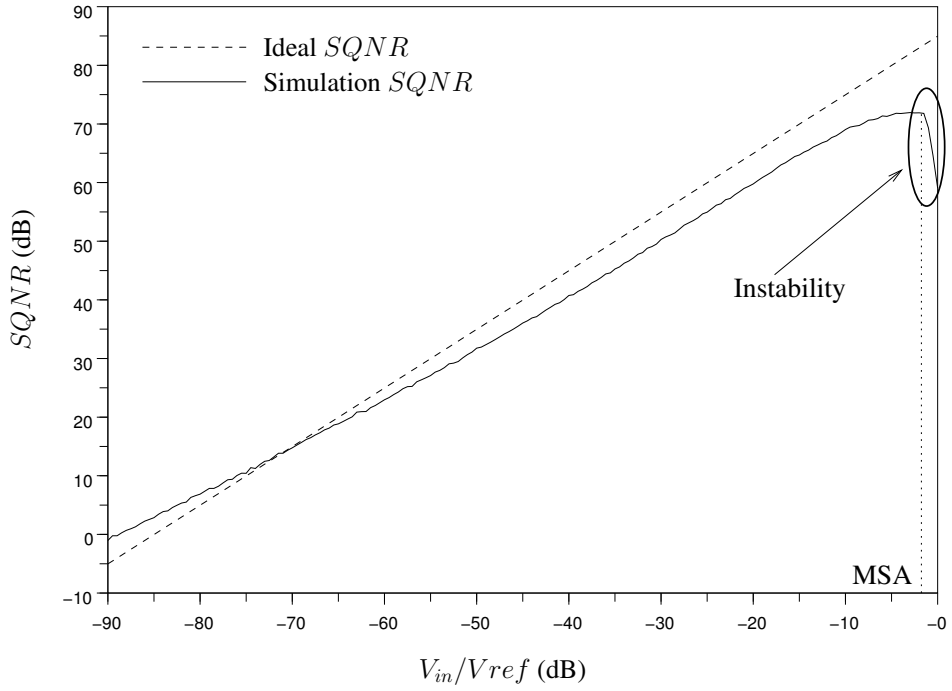


Figure 3.5: Dynamic range

3.2 Discrete time vs continuous time vs Hybrid

It is possible to design ΔΣ modulators using either discrete time (DT) circuits, continuous time (CT) circuits, or Hybrid circuits. Each implementation has its advantages and disadvantages. In this section, we will make a comparative analysis of these implementations to figure out the most suited one for the considered application presented in the introduction.

3.2.1 Operation

3.2.1.1 Discrete Time Modulators

Fig. 3.6 shows the general architecture of a L^{th} order feedback discrete time ΔΣ modulator. The signal is sampled at the ADC input and then processed through L DT integrators implemented using the SC technique before being applied to the quantizer. If b_i is equal one, the i^{th} integrator can be implemented using the circuit Fig. 3.6 a). If not, the circuit of Fig. 3.6b) that uses an additional capacitor must be used.

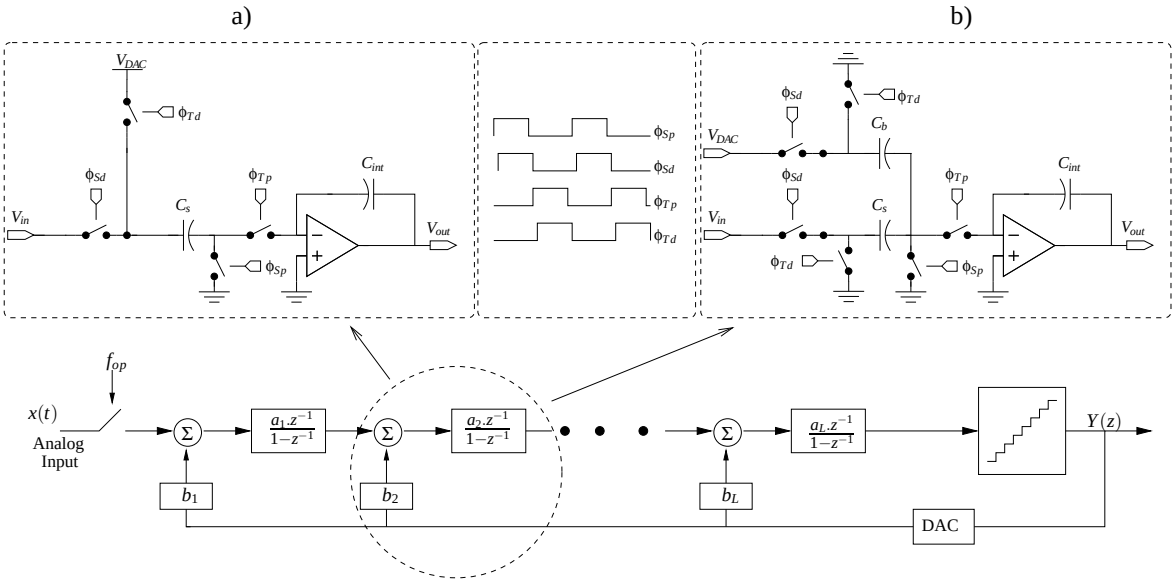


Figure 3.6: General Architecture of a feedback discrete time ΔΣ modulator

3.2.1.2 Continuous Time Modulators

Fig. 3.7 shows the general architecture of an L^{th} order feedback continuous time ΔΣ modulator. In this case, the signal is sampled at the input of the quantizer after being processed by the CT integrators. Two main techniques exist for the implementation of a CT integrator. The first converts the voltage to a current using a resistor before integrating it in a capacitor. The second uses a transconductance to achieve the voltage to current conversion. The OTA-RC implementation is more linear than the gm-C implementation but requires a higher power consumption [27] [28]. A good compromise to reduce power consumption while preserving good linearity is to implement the first stage as an OTA-RC integrator and the following integrators as gm-C integrators[29].

3.2.1.3 Hybrid Modulators

The operation of Hybrid ΔΣ modulators combines CT integrators and DT integrators. This architecture [30] [31] [32][33] [34] tries to extract the advantages of both implementations but unfortunately suffers also from the disadvantages of both of them as well. Its working principle shown in Fig. 3.8 is as follows: the signal is processed by k CT integrators, then sampled and afterwards processed by $L-k$ DT integrators.

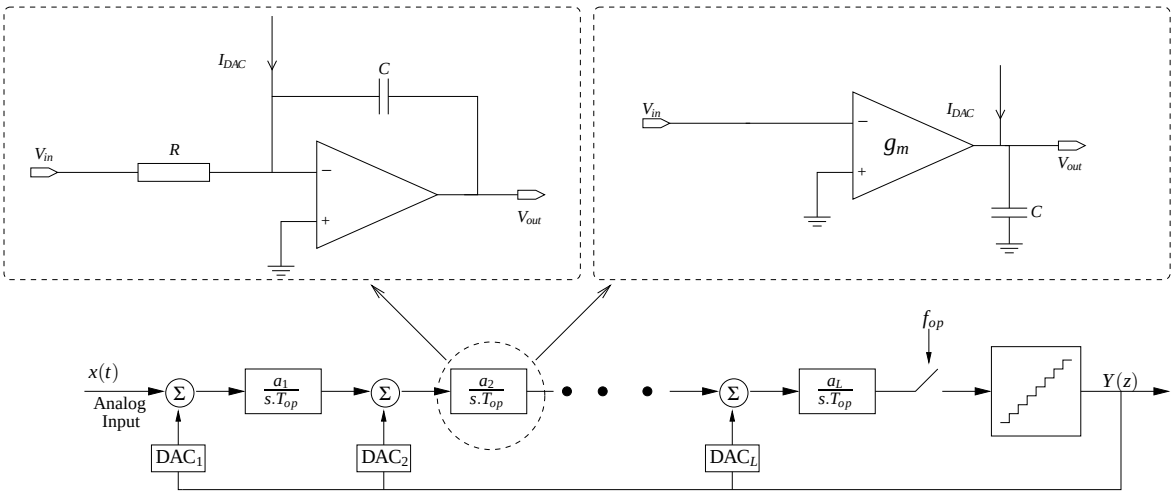


Figure 3.7: General Architecture of a feedback continuous time $\Delta\Sigma$ modulator

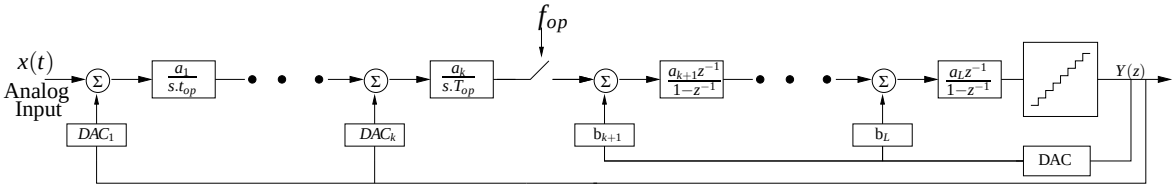


Figure 3.8: General Architecture of a feedback hybrid $\Delta\Sigma$ modulator

3.2.2 Coefficient sizing and trimming with frequency

The charge transfer analysis of DT integrators a) and b) gives respectively:

$$V_{out}(z) = \underbrace{\frac{C_s}{C_{int}}}_{a_i} \frac{z^{-1}}{1-z^{-1}}(V_{in}(z) - V_{DAC}(z)) \tag{3.9}$$

$$V_{out}(z) = \frac{z^{-1}}{1-z^{-1}}(\underbrace{\frac{C_s}{C_{int}}}_{a_i} V_{in}(z) - \underbrace{\frac{C_b}{C_{int}}}_{b_i} V_{DAC}(z)) \tag{3.10}$$

For CT integrators, the transfer functions are:

$$H(s) = \frac{1}{R.C.s} = \frac{\underbrace{\frac{T_{op}}{R.C}}_{a_i}}{s.T_{op}} \tag{3.11}$$

$$H(s) = \frac{g_m}{C.s} = \frac{\underbrace{\frac{g_m.T_{op}}{C}}_{a_i}}{s.T_{op}} \tag{3.12}$$

Analysing equations 3.9, 3.10, 3.11 and 3.12 leads to two main observations concerning integrators' gain. First, it can be seen that the value of CT integrators' coefficient depends

linearly on T_{op}. This means that a CT integrator should be reconfigured by adjusting the value of one of its components to allow it to operate on a different f_{op}. This problem does not occur for a DT integrator that scales automatically with frequency. This problem can be seen from a different angle. In fact, the operation of a DT integrator consists of simulating the behaviour of a resistor using a SC network as it can be seen in Fig. 3.9. The value of the simulated resistance depends on T_{op} and consequently the DT integrator coefficient a_i will scale automatically with f_{op}.

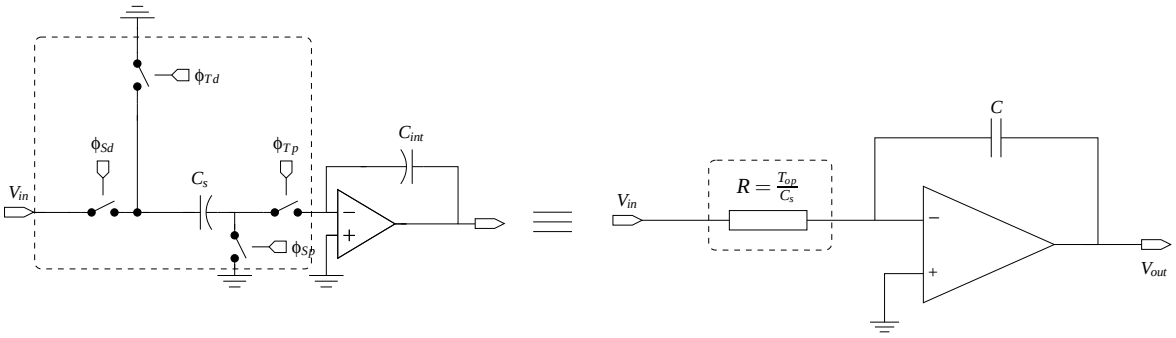


Figure 3.9: The simulation of a resistor with SC circuits

The second point concerns the coefficient precision. In fact, for CT integrators, coefficients' values are set by a R-C product or a gm-C ratio. In the latest technologies, the process variation on capacitors, resistors and tranconductances range from 20 to 40% depending on the technique used for implementation. Besides, the variation on each of these components is uncorrelated from the two others because they are fabricated in different steps of the chip manufacturing. This leads to a coefficient deviation of the same order of the variation on the components. However, coefficients are defined by capacitor ratios in DT circuits. Although their respective values suffer from 20 to 40% variation, their ratio can be set accurately specially if the two capacitors were matched carefully allowing to have precisions higher than 99% [35].

In order to evaluate the impact of integrator gain variation on ΔΣ ADCs, the modulator

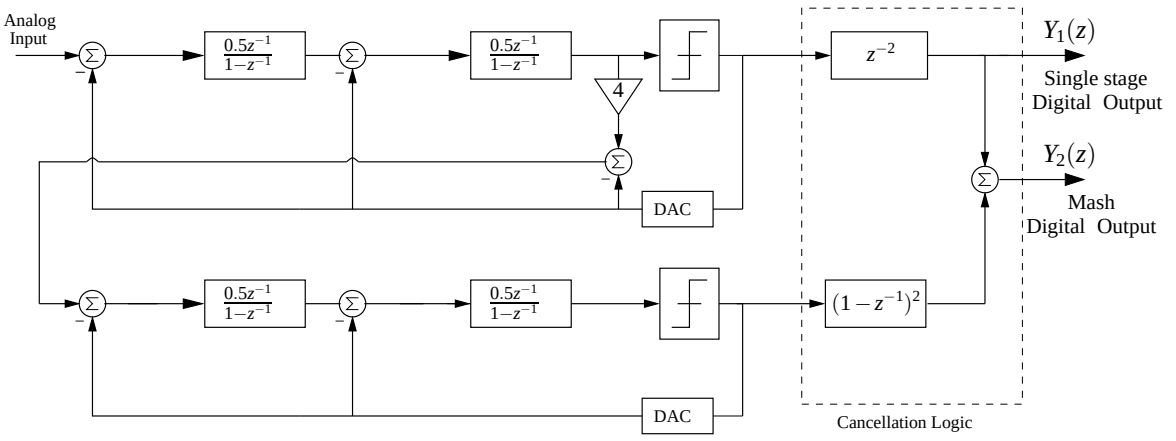


Figure 3.10: Cascaded Boser modulator

of Fig. 3.10 is considered. It is a cascaded 2-2 feedback modulator. Its operation consists of

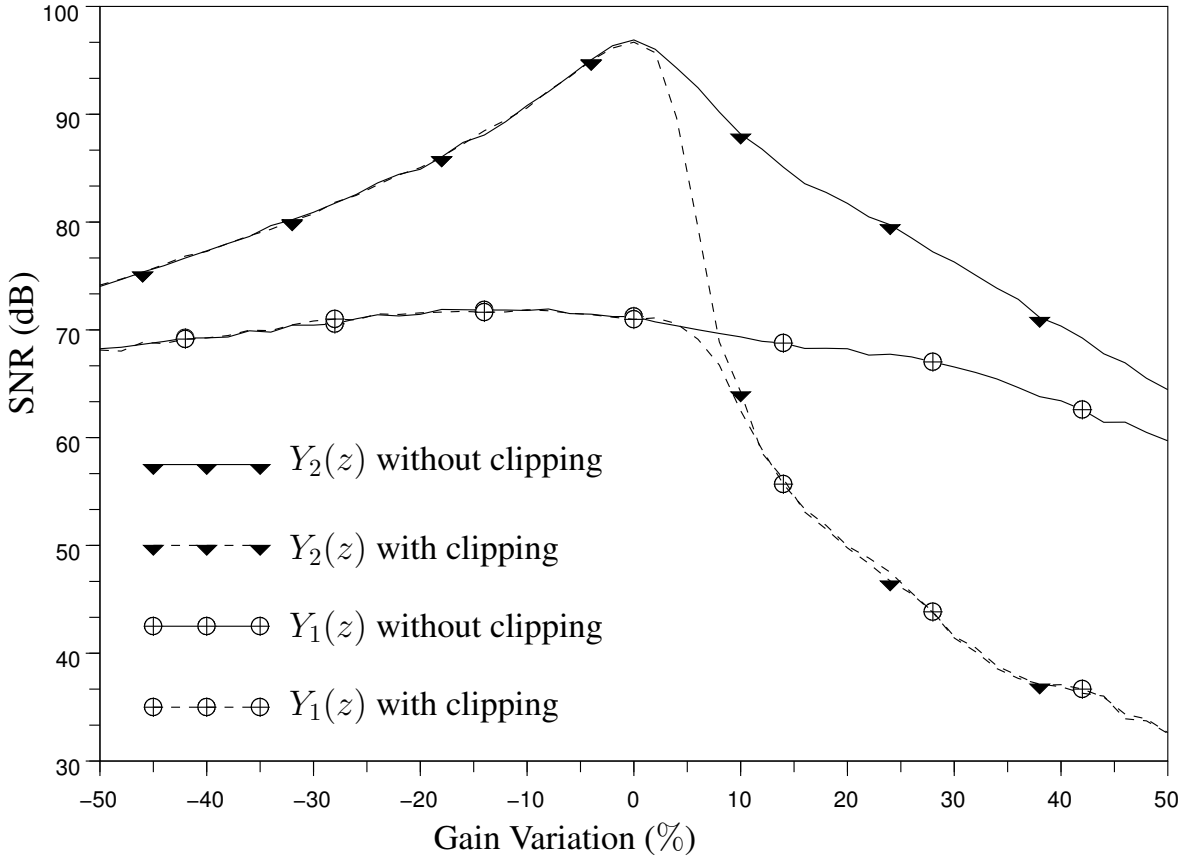


Figure 3.11: SNR vs gain variation

feeding the quantization error of the first stage to the second stage and ideally the order of the complete modulator will be sum of the stages' order while beneficiating of the stability of a second order modulator [36] [37]. Fig. 3.11 shows the SNR at the output of the first stage output $Y_1(z)$ and the cascaded output $Y_2(z)$ with respect to the gain variation of the first stage first integrator for an input sine at -3 dB below the full scale (dBFS). The SNR was simulated for an OSR of 64.
First let us consider the case where the integrators are not clipped, it can be observed that single stage modulators are much more robust in the face of gain variation than cascaded modulators. Nevertheless, they suffer from some SNR degradation when the gain deviates from its original value. In fact, if the gain is smaller than expected, the noise shaping will be less aggressive leading to a higher noise power hence a lower SNR. While, when the gain increases, the modulators begins to be unstable which lead also to a SNR loss. Cascaded modulators suffer also from these two effects but their performance degradation is caused mainly by the mismatch between the first stage NTF and the transfer function of the second stage noise cancellation digital filter. This mismatch arises due to first integrator's gain variation. This is one of the main reasons for which it is preferred to implement CT modulators using a single stage architecture and not a cascaded one.
Furthermore, when the integrator clipping is taken into consideration, the impact of gain variation becomes very critical even for single loop architectures. The problem occurs if the gain is larger than expected which would increase the excursion of integrators' output and since they are clipped, the probability of saturation increases which causes a SNR loss. Two approaches can be used to deal with this problem. The first consists of taking some margin during the design by reducing $Vref$ with respect to the clipping voltage. This solution is efficient in terms of design time but it is not optimized in terms of power consumption and die area. In fact, as it will be shown later, reducing $Vref$ leads to higher contribution of thermal noise and restoring it back to its original level with respect to signal power requires a lower resistor. Consequently, to preserve the same time constant, the capacitor value should be augmented causing an increase in power consumption and die area. The second approach is to tune the time constants by using a trimming circuit [38] [28]. Its operation is usually based on measuring the time constant after fabrication and to correct it using a digitally controlled resistor bank or capacitor bank.

3.2.3 Anti-alias filter considerations

The simulations of CT integrators need to be realized using a continuous time simulator. Computers and servers are, as all digital machines, discrete time and consequently the computation time required to simulate a continuous time behaviour is very high. To avoid this problem, an equivalent DT modulator of the considered CT or Hybrid modulator can be used instead thereby reducing considerably the simulation time. Some techniques to realize this transformation are presented in [39] [40] [41].
The equivalent DT modulator will have the same behaviour with respect to the noise shaping. However, additional filters must be added to ensure the authenticity of the STF. In fact, CT integrators achieve a low pass filtering of the input and depending on the order, the architecture and the coefficient values of the modulator, the frequency response of the STF is fixed. For example, a L^{th} order distributed feedback CT modulator has sinc^L filtering. While a L^{th} order CT modulator for which the 1^{st} integrator output is fed forward to the quantizer, has a sinc^1 filtering only [42].
This low pass response of the STF is very interesting because it relaxes the constraints

on the anti-alias filter and even in some cases, it removes its necessity. Fig. 3.12 shows the STF of a 2^{nd} order feedback DT modulator($a_1 = a_2 = b_1 = b_2 = 1$), a 2^{nd} order feedback Hybrid modulator ($a_1 = a_2 = b_1 = 1$ $b_2 = 2$) and 2^{nd} order feedback CT modulator($a_1 = a_2 = b_1 = 1$ $b_2 = 1.5$). The simulations were carried out using the "scicos" simulator of scilab, an equivalent of Matlab Simulink. To have an idea of the order of magnitude of the simulation time, the computation times were measured. 2.7 seconds are required to perform a 10000 cycles simulation of the considered CT modulator coded in scicos with respect to 4.5 milli-seconds for its DT equivalent coded in C language. This means that simulations are almost 600 times faster when using the DT models rather than its CT counterparts.

The simulation results are shown in Fig. 3.12. As expected, the DT modulator has all-pass STF response. While, the CT modulator has a 2^{nd} order low pass filtering. The hybrid modulator has only one CT integrator, hence its STF performs a sinc^1 filtering.

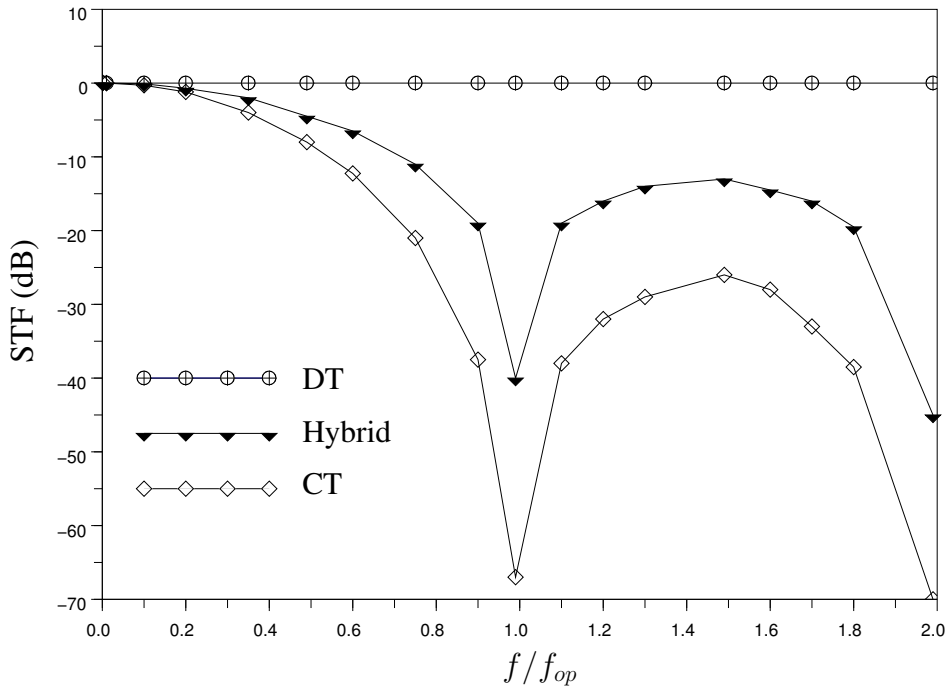


Figure 3.12: CT, hybrid and DT modulators' STF

For $\Delta\Sigma$ ADCs, the interferes that might corrupt the useful signal are those that have power at $if_{op} \pm B$. The inherent AAF of CT and hybrid modulators attenuates strongly these interferes because it has a zero for all f_{op} multiples. Nevertheless, another problem persists. In fact, if the scenario of Fig. 3.13 is considered. Interferes 2 and 3 are filtered by the inherent AAF and Interferer 1 will not alias into the useful band. However, this latter is almost unfiltered and its remaining power will reduce strongly the dynamic range of the ADC. This problem can be dealt with either at the preceding AAF level by adapting its frequency response to ensure a considerable attenuation of Interferer 1, either at the modulator level by adding notches in the STF at the frequencies that it is desired to attenuate [43] [29]. This approach increases the complexity of the modulator but relaxes the constraints on the AAF. Therefore, the choice of one approach over the other must be done by comparing the complexity of the overall solution.

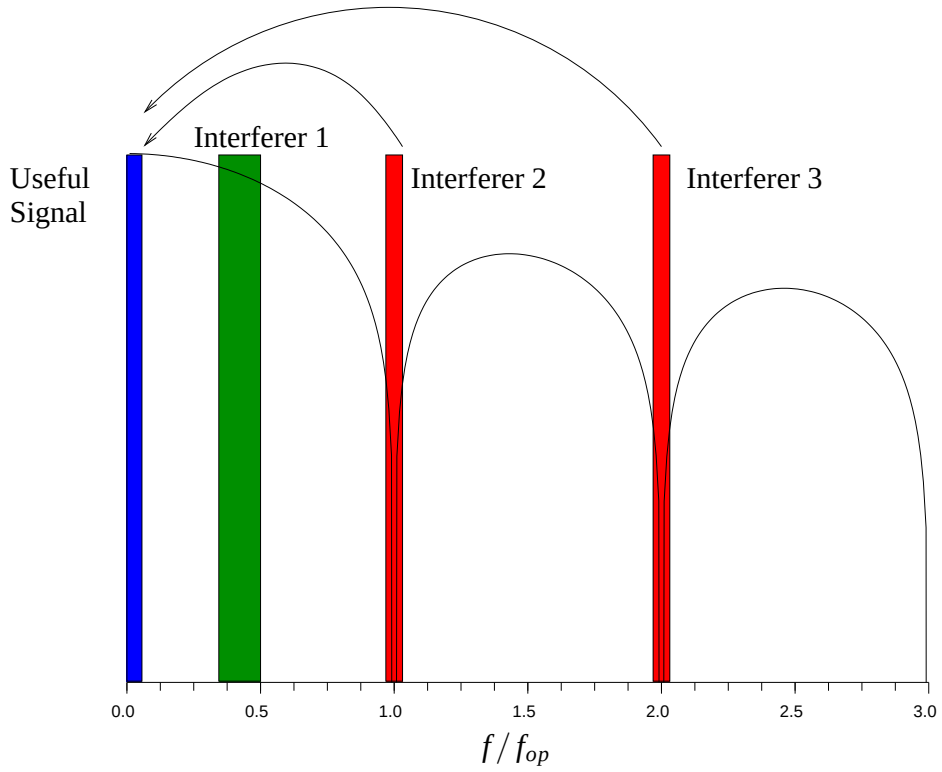


Figure 3.13: Dynamic range considerations

3.2.4 Power consumption

In ΔΣ modulators, OTAs commonly have the lion's share of the overall power consumption of the analog part. Besides, they are one of the main limiting points of the operation frequency. One of the main benefits of CT integrators over DT integrators is that they relax the constraints on OTAs speed. In fact, for CT integrators, the OTA limited bandwidth induced error increases linearly when the ratio of the unitary frequency (f_u) to f_{op} decreases. However, for DT integrators, this error increases exponentially with $\frac{f_u}{f_{op}}$ decrease. Hence, the requirements in terms of the gain-bandwidth product on DT integrators' OTA are higher than on CT integrators' OTA. In practice and depending on the targeted resolution, DT integrators' OTAs must have a $\frac{f_u}{f_{op}}$ around 5 compared to $\frac{f_u}{f_{op}}$ of 2 to 3 for CT integrators [2].

This gives two advantages for CT modulators over DT modulators. 1) for the same conversion bandwidth, the power consumption will be lower for a CT modulator; 2) the possible conversion bandwidth is larger for a CT implementation.

3.2.5 Thermal noise

In high resolution applications such as ΔΣ ADCs, thermal noise is often one of the main limiting points[44]. Moreover, with technology advance, transistors' transition frequencies are becoming higher and supply voltages are becoming lower. As it will be pointed out in this subsection, these two effects render the thermal noise more problematic and thereby amplify the constraints on the ADC blocks .
In ΔΣ ADCs, an error introduced in the i^{th} integrator is shaped by the $i-1$ previous integrators [1]. Consequently, thermal noise is a serious concern just in the first integrator.

Since Hybrid modulators and CT modulators have a CT integrator as their first integrator, the impact of thermal noise is similar on both of them. Its PSD for an R-C integrator if the OTA contribution is neglected, can be expressed as follows [27]:

$$PSD = 4K_{bol}T(R + R_{DAC}) \tag{3.13}$$

where K_{bol} is the Boltzmann constant, T the temperature in Kelvin and R_{DAC} the resistor of the feedback DAC.
If it is assumed that the decimation filter cancels all out of band noise, the thermal noise is then given by:

$$Pth_{inband} = (4K_{bol}T(R + R_{DAC}))2B \tag{3.14}$$

Let $SNR_{th\ R}$ be the targeted signal to first integrator thermal noise ratio that usually constitutes the main thermal noise contribution. The maximal value of R for which the thermal noise is lower than its allocated budget is:

$$R = \frac{A^2.OSR}{8K_{bol}T.10^{(SNR_{th\ R})/10}.f_{op}} \tag{3.15}$$

Equation 3.15 shows that R must be lower than a certain value in order to achieve the desired signal to thermal noise ratio. The problem is that when R is decreased, C must be increased by same factor in order to preserve the same integrator gain. This will amplify the constraints in terms of GBW and SR on the OTA. Besides, in very high speed very high resolution implementations, the maximum value of R becomes very small. Consequently, the resistance of the wire connecting the input to the resistor will not be anymore negligible with respect to resistor's value. This will obligate the designer to allocate a larger portion of the overall noise to thermal noise and to reduce the wire resistance as much as possible by using larger rails.

In DT integrators, the thermal noise is generated by the switches. Subsection A.2.1.1 shows that the PSD of the thermal noise is:

$$PSD = \frac{4K_{bol}T}{C_s.f_{op}} \tag{3.16}$$

Similarly, if it is assumed that the decimation filter cancels all out of band noise, the thermal noise is then given:

$$Pth_{inband} = \frac{4K_{bol}T}{C_s.OSR} \tag{3.17}$$

Let $SNR_{th\ sw}$ be the targeted signal to thermal noise ratio. The minimal value of C_s is then given by:

$$C_s = \frac{8K_{bol}T.(10^{(SNR_{th\ sw})/10}}{A^2.OSR} \tag{3.18}$$

Equation 3.18 shows that reducing thermal noise requires to increase C_s value. Since $\frac{C_s}{C_{int}}$ fixes the integrator gain, increasing C_s value leads to an increase of C_{int} value which causes, similarly to CT integrator, an increase of the die area and the constraints on the OTA.

3.2.6 Jitter

Although its impact is the same in the three considered implementations (an added white noise), the main error due to jitter occurs at different points of the $\Delta\Sigma$ modulator for each of them.
In fact, jitter affects all clocked components which are: the switches, the quantizer and the DAC.

3.2.6.1 Switches

The main concern is the switches that process the continuous signal. For all other switches, the signal at the output of the switch converges exponentially to a value V_{final} that is constant during a complete clock phase (the sampling phase or the hold phase). If the clock is ideal, the sampled value will be V_{final} affected by a settling error that depends mainly on the time constant of the sampling circuit (Section 2.1). Thus, when the jitter is considered, the error at the end of the phase will not be exactly as predicted but the difference will be very small as it can be seen in Fig. 3.14 because it will be an error on the value of the settling error.
For CT and Hybrid modulators, the sampling operation occurs after k and L integrators respectively. Therefore, the sampling jitter error is shaped by the previous stages and can be neglected. While for DT integrators, since the sampling operation is performed at the ADC input, this error must be taken into consideration. In subsection A.2.6, the value of the jitter

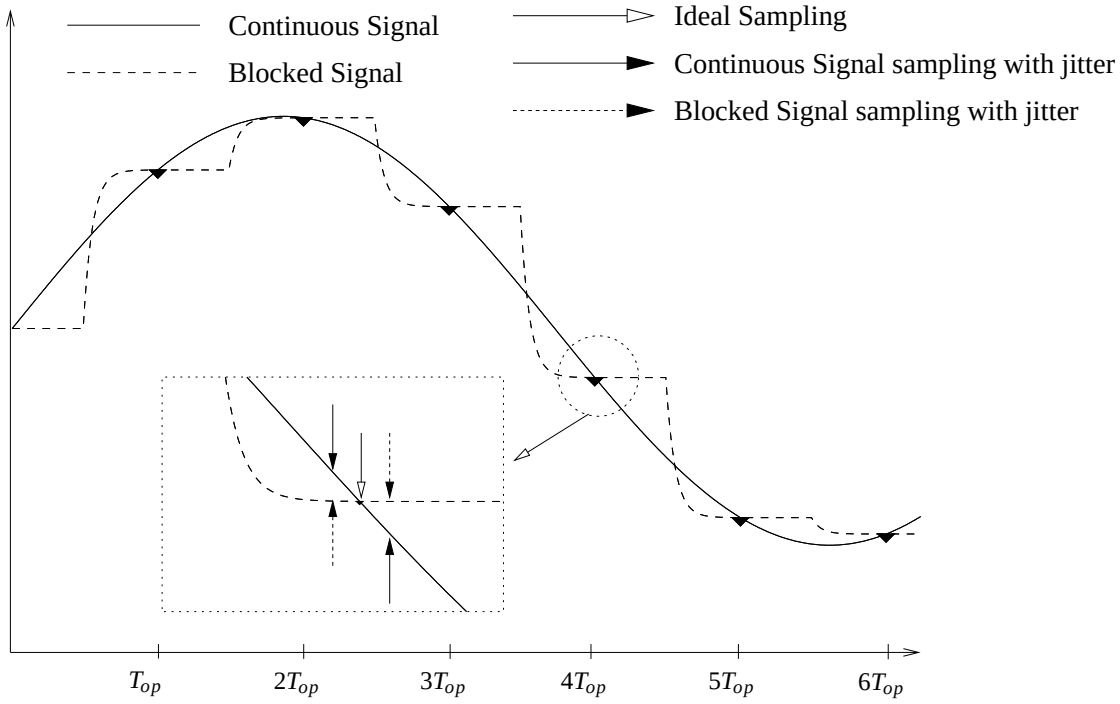


Figure 3.14: Impact of jitter on a continuous signal and on a blocked signal

error amplitude is determined as follows

$$A_{jittnoise} \approx (2A\pi f_{in}\sigma_t) \tag{3.19}$$

where σ_t is the clock jitter value.
In the worst case for which all the signal power is concentrated at B, the signal to jitter noise ratio becomes:

$$SNR_{jit} = 10Log\frac{P_s}{\frac{P_{jittnoise}}{OSR}} \approx 10Log\frac{\frac{A^2}{2}}{\frac{(2A\pi B\sigma_t)^2}{2OSR}} = 20Log\frac{OSR\sqrt{OSR}}{2\pi f_{op}\sigma_t} = 20Log\frac{OSR\sqrt{OSR}}{f_{op}\sigma_t} - 15.9 \tag{3.20}$$

3.2.6.2 Quantizer

In the three implementations, the quantizer digitizes signal samples that are processed by L integrators. Therefore, the jitter induced error of the quantizer is shaped by the previous

stages and can be neglected.

3.2.6.3 DAC

There are several ways to implement the DAC of $\Delta\Sigma$ modulators. The choice of the implementation depends on many parameters such as power consumption, inter symbol interference and jitter sensibility. Fig. 3.15 shows the current shape at the output of four popular DAC implementations . The SC implementation has the lowest sensibility to jitter. However, large current peaks need to be generated in the cycle beginning. In DT integrators, the charge transfer between C_s and C_{int} has a similar shape and therefore the OTA is designed to deal with large currents which makes it suitable for a SC DAC. While, the operation of CT integrators does not require dealing with large current. Consequently the use of a SC DAC affects the operation requiring higher OTA slew rate hence a higher consumption. Therefore, it is preferable to avoid this type of DACs for CT integrators in order to preserve their low power consumption.
The three other DACs are current mode DACs. RTZ, HRZ and NRZ stand for return to zero, half return to zero and none return to zero, respectively. Their jitter induced error power for a 1 bit DAC is expressed by:

$$err_{jittnoise} = \frac{\sigma_t}{T_{width}} Vref.n_{rz} \tag{3.21}$$

where T_{width} is the pulse width and n_{rz} is the number of transition per cycle. It is equal for RTZ and HRZ and it depends on the output for the NRZ
Based on Eqn. 3.21, it can be deduced that HRZ has the highest sensibility to jitter. Besides, it requires higher power consumption than the RTZ and the NRZ implementations. Nevertheless, the HRZ relaxes the constraints in terms of loop delay since it gives the quantizer $T_{op}/2$ to settle. This time is not offered in the RTZ and the NRZ implementations and therefore additional feedbacks must be added to reduce the impact of loop delay [45]. The NRZ implementation has the lowest sensibility to jitter. However, it suffers from inter-symbol interference. In fact, due to component mismatches, the rising edge and falling edge of the DAC are not equal. This makes integrated voltages of equivalent codes data dependent. For example, let us consider the codes 0101 and 1001, their integrated voltages must be equal but they are not due to the difference between the DAC rise and fall times. This will cause an SNR loss but it can be mitigated by the use of a differential feedback circuit [46].
To compare the jitter impact on the SNR, let us consider a 1 bit RTZ DAC.

$$SNR_{jit} = 10Log\frac{P_s}{\frac{P_{jittnoise}}{OSR}} = 10Log\frac{\frac{A^2}{2}}{\frac{\sigma_t^2}{T_{op}^2 OSR} Vref^2.2^2} \tag{3.22}$$

For an input amplitude of -3 dBFS which is considered usually the maximum stable amplitude, SNR_{jit} becomes:

$$SNR_{jit} = 20Log\frac{\sqrt{OSR}}{\sigma_t f_{op}} - 15.03 \tag{3.23}$$

It can be seen by comparing equations 3.23 and 3.20 that the impact of jitter is significantly higher on CT modulators than on DT modulators. Using a multi-bit quantizer, hence a multi-bit DAC decreases the impact of jitter for current mode DAC but nevertheless it remains significant. In fact, jitter is one of the main concerns in CT $\Delta\Sigma$ Modulators. Their implementation requires frequently the use of a on-chip phase locked loop (PLL) especially for wideband applications [38] [47].

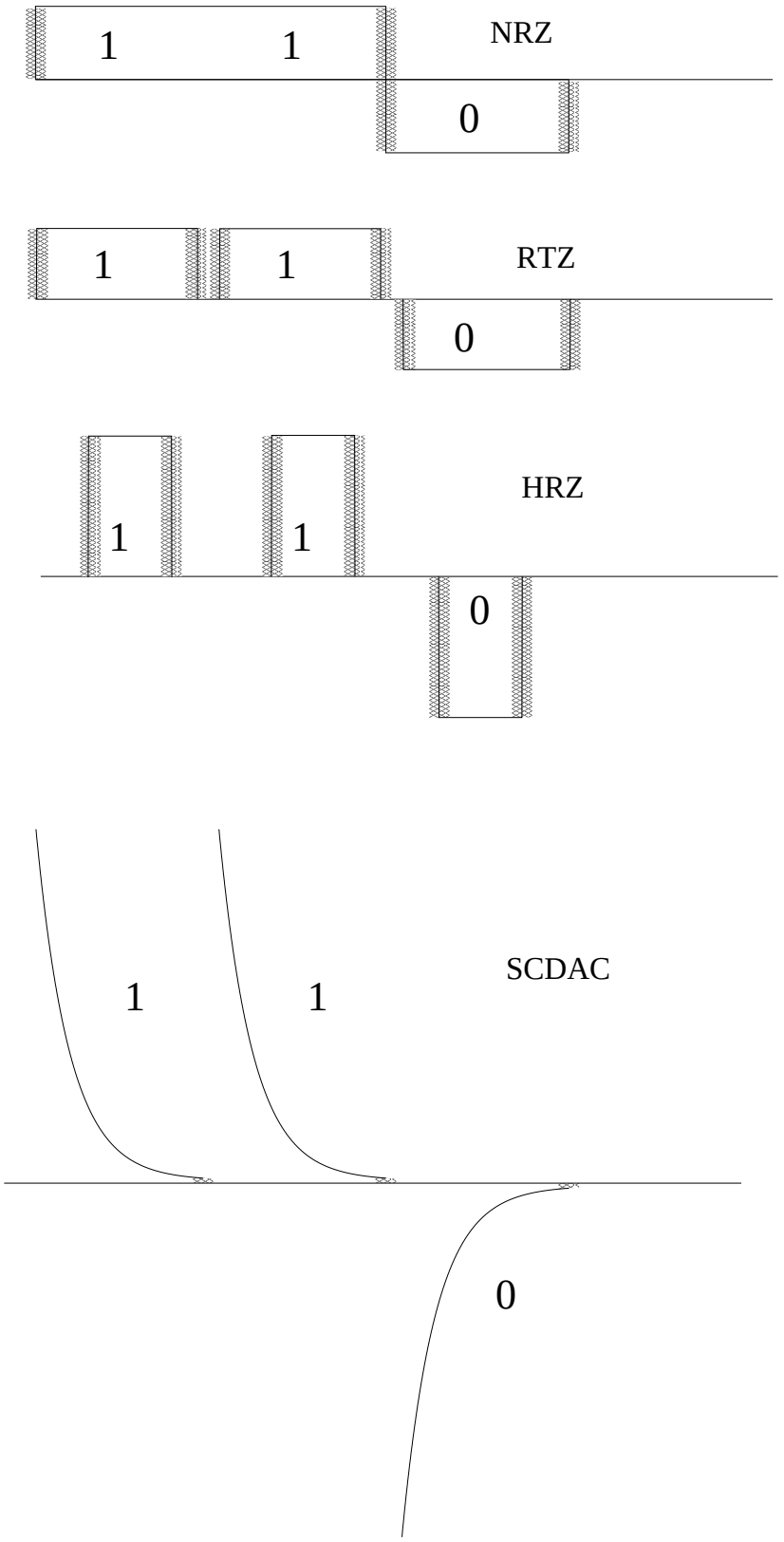


Figure 3.15: Different DAC Implemenations

3.2.7 Switch linearity requirements

In DT integrators, the sampling operation is realized at the ADC input. This means that any signal deformation introduced at this level due to the sampling operation, will appear at the output. Therefore, there is need to use correction techniques such as bootstrapping, bottom plate sampling or dummy switch addition to preserve a good SNDR at the ADC input (section A.2). These techniques increase the power consumption, the die area and the design time of the chip.
While in hybrid and CT modulators, the sampling operation occurs after k and L integrators respectively. As it was said before, any error introduced at this level will be shaped by the previous stages thereby reducing the constraints on the sampling switch.

3.2.8 Conclusion

	DT Modulators	Hybrid Modulators	CT Modulators
Power consumption	☺	☺☺	☺☺☺
Speed	☹	☺	☺
Coefficient variation	☺☺	☹	☹☹
Coefficient scaling with f_{op}	☺☺	☹	☹☹
Anti-alias Filtering	☹☹	☺	☺☺
Thermal noise	☺	☺	☺
Jitter noise	☺☺	☹	☹
Switch linearity requirements	☹	☺☺	☺☺
Loop delay	☺☺	☹☹	☹☹

Table 3.1: CT vs DT vs Hybrid

Table 3.2.8 summarizes the comparison between the three implementations. Although it requires a higher power consumption than CT and Hybrid modulators, a DT implementation

was preferred because it is more robust against jitter and loop delay and especially is more prone to reconfigurability. In fact, as it was pointed in subsection 3.2.2, DT modulators scale automatically with the operating frequency and are more suited for multi-stage architecture. In addition, as it will be explained later, DT modulators are more adapted to most of the parallel structures.

3.3 Low Pass vs High Pass modulators

After discussing the choice of the implementation in the previous section, a comparative analysis of high-pass and low-pass ΔΣ modulators is carried out in this section. The non-idealities of all the basic blocks i-e OTA, Quantizer, Switches and Clocks are considered. This comparison will allow us to choose the most suited architecture (LP or HP) for our design and to explain in details the operation of SC ΔΣ modulators. BP ΔΣ modulators have been left out of this comparative analysis because of the complexity of BP resonators. In fact, their implementation is achieved either using two integrators with a feedback either using the circuit of Fig. 3.16 [48]. Both solutions require high power consumption and large die area.

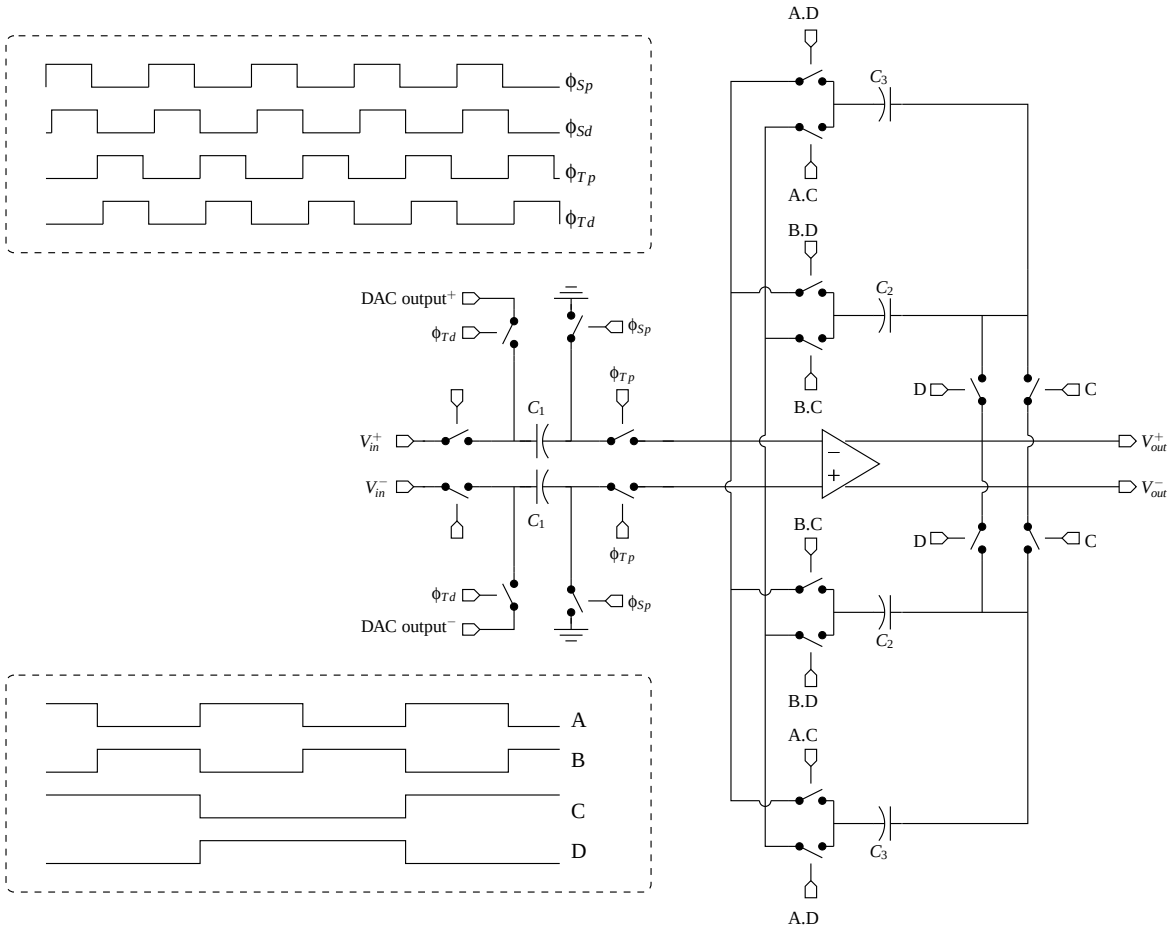


Figure 3.16: Band pass resonator implemented using one OTA

Extensive simulations have been performed on various architectures to compare the high-pass and low-pass operation, and interestingly the results are more or less independent of

the modulator architecture. For the sake of simplicity, the feedforward second-order single-loop architecture presented in [26], has been selected for showing comparative analysis. Its low-pass and high-pass versions are shown in Fig. 3.17

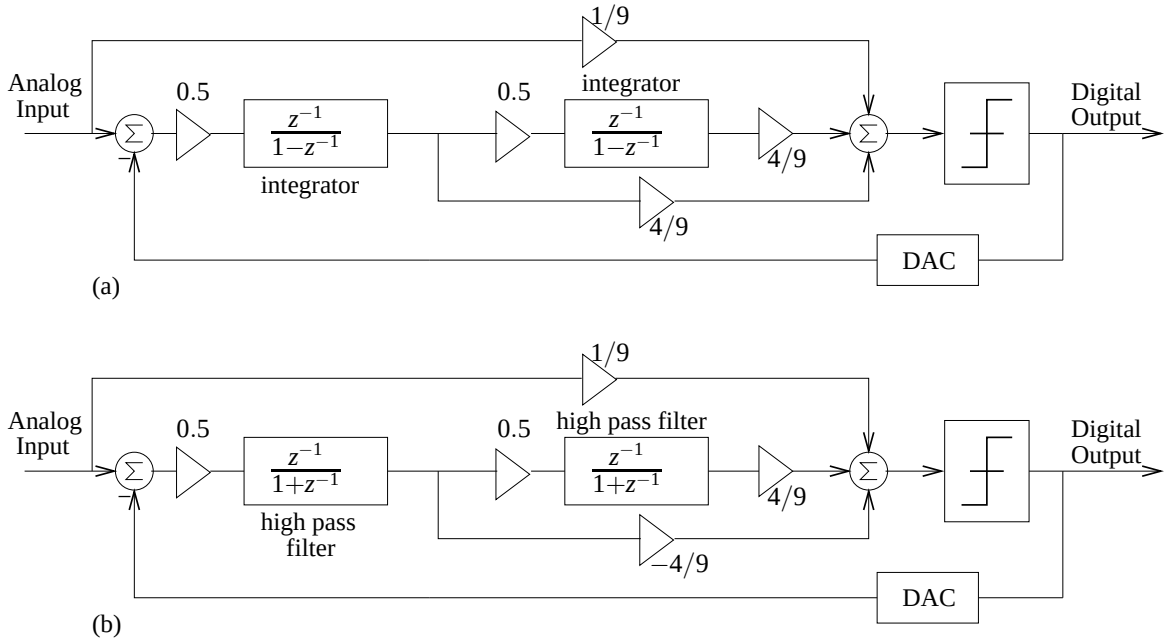


Figure 3.17: Optimized version of Silva-based Structure for (a) LP operation, (b) HP operation

In this topology, input signal is fed directly to the quantizer and thus does not have to traverse the integrators/high-pass filters. As a result, the non-linearities of the op-amps constituting the integrators/high-pass filters do not distort the input signal. This is why, this architecture is also called low-distortion architecture. It is important to mention here that the adder before the comparator is implemented as a passive adder and hence the value of the feedforward coefficients are scaled in consequence (section A.4).

3.3.1 High-Pass Filter/Mirrored-Integrator Implementation

The working principle of HP $\Delta\Sigma$ modulator is the same as that of LP $\Delta\Sigma$ modulator, i.e. the quantization noise is shaped away from the signal band by a loop filter. The difference lies in the placement of the signal band. In the case of HP $\Delta\Sigma$ modulator, it is located at $f_{op}/2$. High pass filter has the same role in HP $\Delta\Sigma$ modulators as integrator has in LP $\Delta\Sigma$ modulators. Its z-domain transfer function is given by Eqn. 3.24. It can be derived from the LP integrator transfer function by applying the $z \rightarrow -z$ transformation.

$$H_{hp}(z) = a\frac{-z^{-1}}{1+z^{-1}} \tag{3.24}$$

HP filter design has been a major bottle neck in the development of HP modulators. In the absence of an efficient HP filter little progress could be made in HP modulators. But in the recent past, an innovative design has been proposed which has opened the gates for research in HP modulators.

Traditional HP filters were designed using the SC integrator as the basic component [49, 50]. It must be noted that the HP filters are used in [49] and [50] to implement the resonators

for BP ΔΣ modulator. This results in a wastage of resources, as twice the number of HP filters are required to achieve the same order of noise-shaping. In the following subsections, the most widely used of the classical topologies called "Integrator-based HP filter" [50], and the lately introduced "Improved HP filter" [51] are exposed and compared.

3.3.1.1 Integrator Based High-Pass Filter

The integrator-based HP Filter is based on the approach of introducing an extra feedback loop around the integrator. This feedback loop is realised by adding a feedback capacitor which is twice the size of the integrating capacitor around the integrator as illustrated in Fig. 3.18.

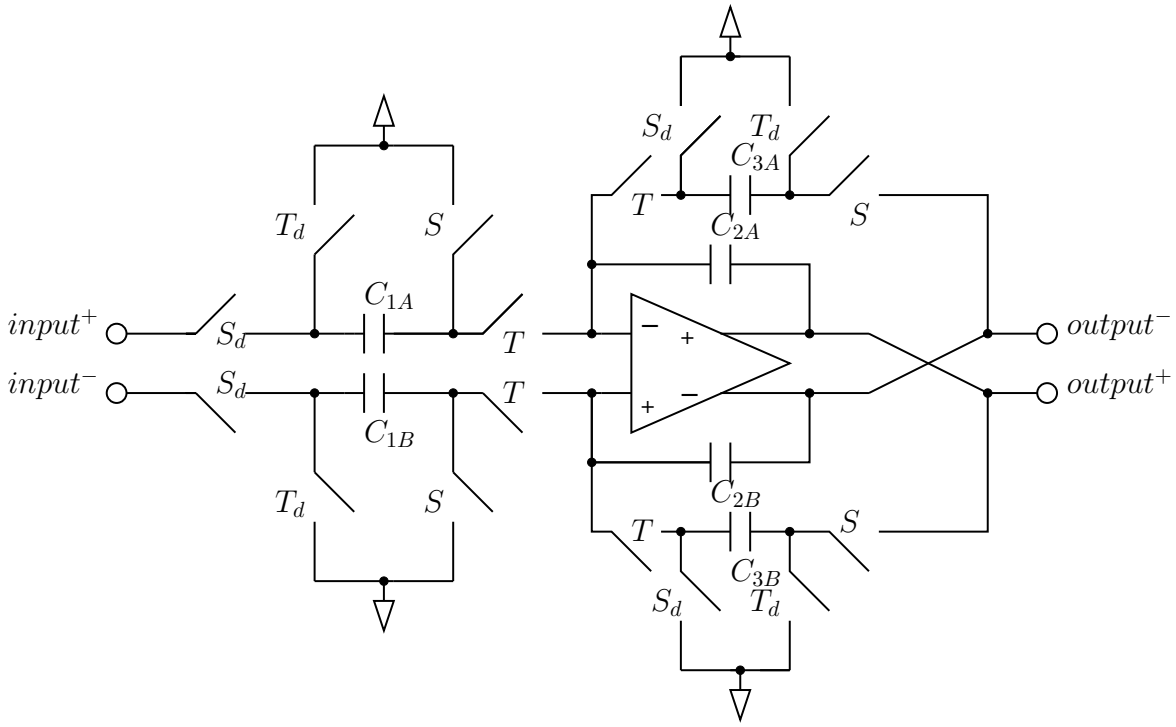


Figure 3.18: Integrator-based HP Filter

This implementation suffers from increased sensitivity to the amplifier noise [49] as the extra feedback loop results in the amplifier noise being captured by both the integrating capacitor and the extra feedback capacitor. There is increased matching requirement to avoid placing the pole outside the unit circle, resulting in the filter going unstable [50].

3.3.1.2 Improved High-Pass Filter

An ingenious implementation of HP filter is presented in [51]. This filter along with its associated timing diagram is presented in Fig 3.19. The timing diagram is modified from its original version in [51] because it was faulty and did not achieve the functioning of HP filter. This implementation is free from the drawbacks associated with the previous implementations. The basic operation is such that the charge is sampled onto C_{1A}, during phase S. On phase T, this charge is transferred to C_{2A} on odd clock cycles and to C_{2B} on even clock cycles. C_{1B} functions in a similar manner.

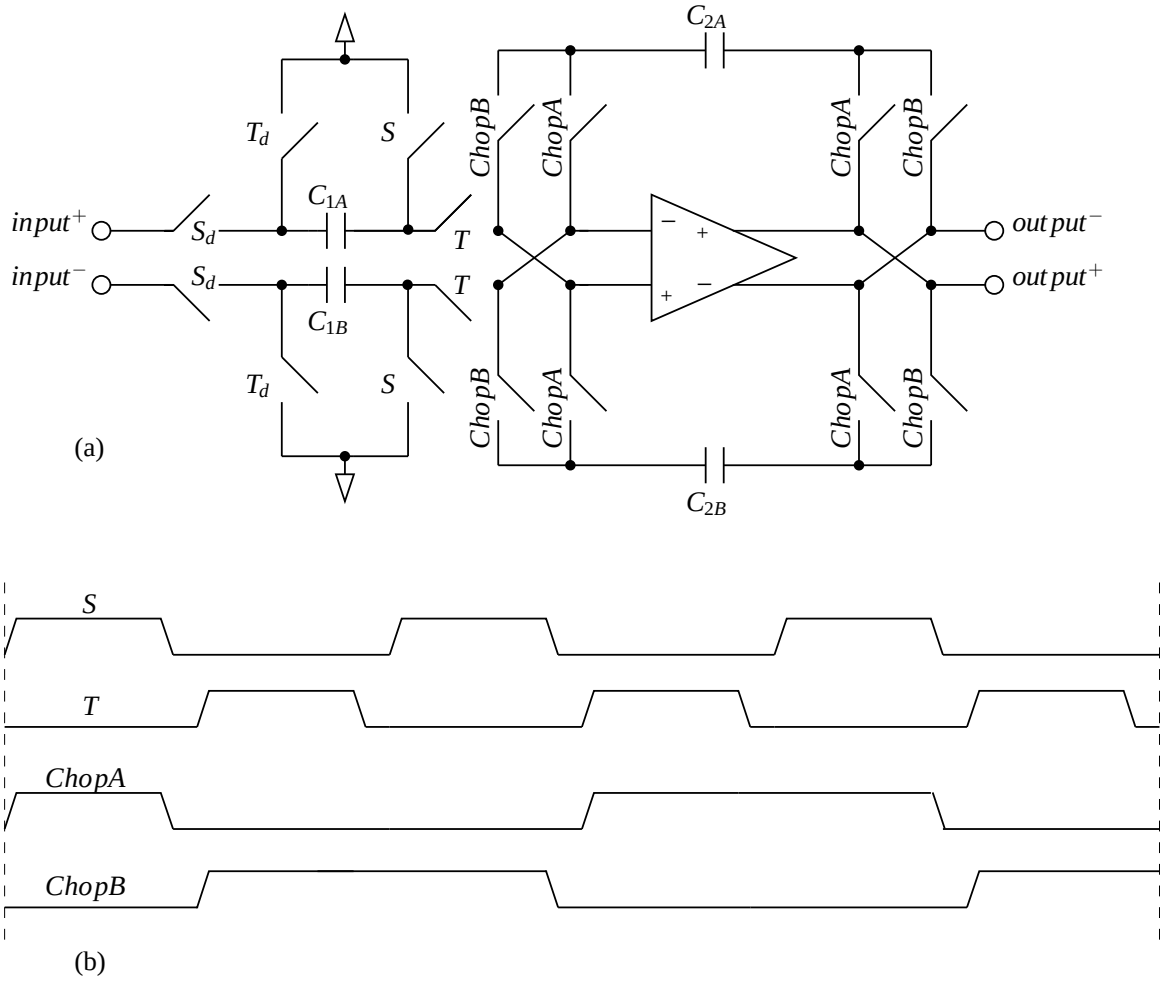


Figure 3.19: Improved HP Filter

An interesting feature of the improved implementations is that if the chopping mechanism is switched off (i.e. *ChopA* remains high and *ChopB* remains low, or vice versa) the high pass filter reduces to being a SC integrator. This feature can be exploited to design a reconfigurable ADC as the same modulator can work as both HP and LP by just changing the chopping clocks.

3.3.1.3 Comparative Analysis

The parameters that we have selected for comparing the two HP filter structures are power consumption, switch noise, OTA noise and die area.

Sampling capacitances are $C_{1A} = C_{1B} = C_S$, and for an HP filter gain of 0.5, feed-back capacitances are $C_{3A} = C_{3B} = 4 \times C_S$ to achieve the HP filter transfer function. With these values, the total noise power due to switches in integrator-based filter can be calculated to be:

$$\overline{e^2_{switch,filter1}} = \frac{5K_{Bol}T}{C_S} \tag{3.25}$$

While for the improved filter, solving the charge-transfer equations, the total input referred

switch noise power is:

$$\overline{e^2_{switch,filter2}} = \frac{4K_{Bol}T}{C_S} \tag{3.26}$$

Thus, comparing Eqns. 3.25 and 3.26, it can be shown that improved-structure provides 20% improvement in switch-noise over integrator-based structure.

Assuming the input-referred amplifier noise power to be $\overline{e^2_{amp}}$ consisting purely of white noise component, the power of the amplifier noise present in the signal band while using the integrator-based filter in the modulator architecture of Fig. 3.17 is approximately:

$$\begin{aligned} \overline{e^2_{amp,inband}} &\approx [S_{amp1,inband}(f) + S_{amp2,inband}(f)] \times B \\ &= 41 \times \frac{\overline{e^2_{amp1}}}{f_{op}} \times B \end{aligned} \tag{3.27}$$

where B is the bandwidth of the useful signal. Similarly the power of the amplifier noise present in the signal band in the event of using improved HP filter in the modulator can be approximated by:

$$\begin{aligned} \overline{e^2_{amp,inband}} &\approx [S_{amp1,inband}(f) + S_{amp2,inband}(f)] \times B \\ &= 1 \times \frac{\overline{e^2_{amp1}}}{f_{op}} \times B \end{aligned} \tag{3.28}$$

Comparing Eqns. 3.27 and 3.28, it becomes evident that the improved-filter has much better noise performance than the other topology, when used in the feedforward HP modulator.

For the purpose of comparing power consumptions of the two HP filters, behavioural modelling of finite GBW and SR of the OTAs has been performed [52]. Then, the simulations are carried out by varying the values of SR at fixed GBW and observing the output SNDR. The operation frequency is normalized to one and the input signal is a sinusoid of amplitude -3 dBFS and frequency $(0.5 - 0.0013)f_{op} = 0.4987$. The OSR is chosen to be 64. The result is illustrated in Fig. 3.20:

The result shows that the minimum SR of $2.1 \times f_{op}(V/sec)$ is needed to reach an SNDR of 70 dB for the proposed modulator architecture implemented with the improved filter to establish the required performance at the GBW of $5f_{op}$. On the other hand, the minimum SR of $5.1 \times f_{op}(V/sec)$ is required , if the proposed architecture is built with integrator-based filter. Thus, clearly the integrator-based filter requires more power consuming OTA.

The integrator-based filter also suffers from a high surface area because of the feedback capacitor which is twice the size of the integrating capacitor. This capacitor also increases the capacitive loading on the amplifier thus increasing the power consumption. Thus because of its reduced power consumption, reduced die area and improved noise immunity, the Improved HP filter is chosen for the HP modulator.

3.3.2 OTA Non-Idealities

OTAs' non-idealities including finite and nonlinear dc-gain, finite GBW and finite SR cause incomplete transfer of charge in the SC implementation of filters (integrators and high-pass

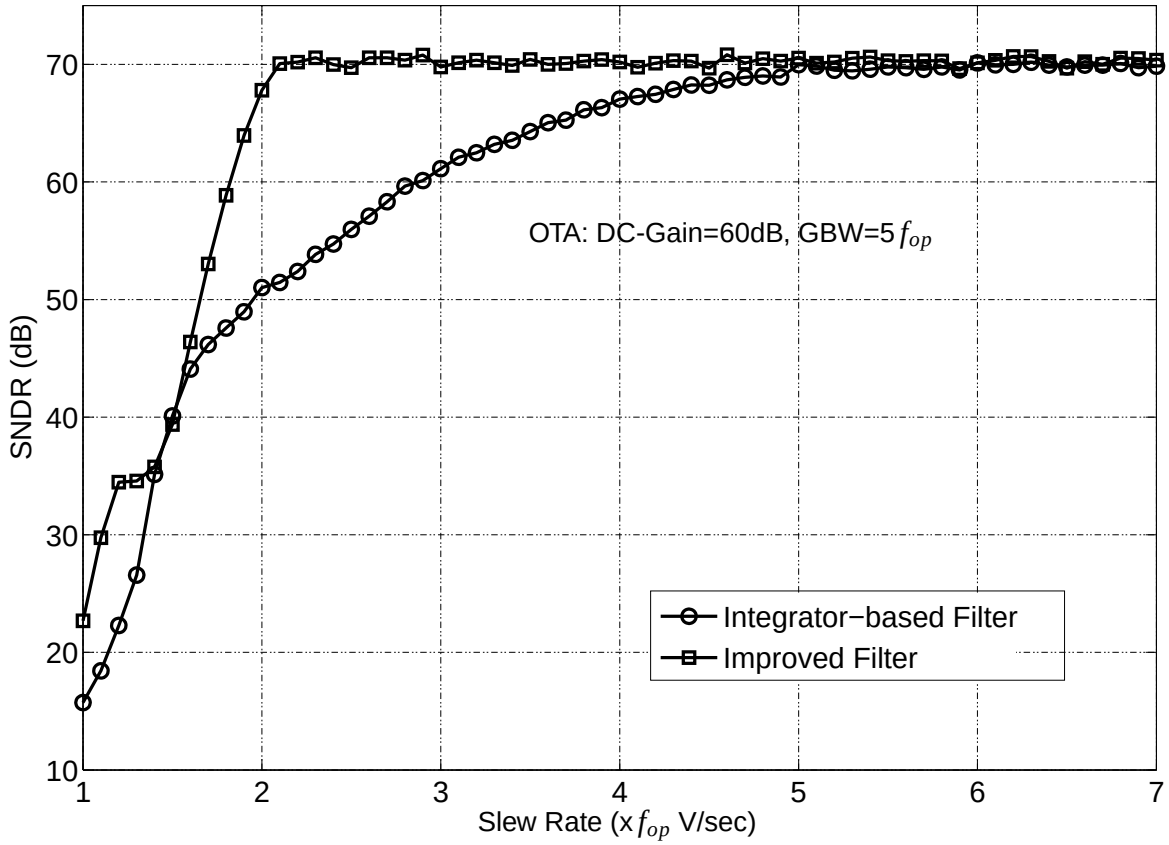


Figure 3.20: SNDR vs OTA SR

filters) which is a major cause of performance degradation in $\Delta\Sigma$ modulators. Several articles in the literature have discussed these effects and established their behavioural models to study their effect on integrators [53, 54, 55], which form the basis of traditional low-pass (LP) $\Delta\Sigma$ modulators. Here, we compare the OTA non-idealities' effect on a LP modulator comprising the integrator and on a HP modulator made up of improved HP filter. All system simulations of the OTA behaviour are carried out for an input sine at 0.0013 f_{op} for LP ($(0.5-0.0013)f_{op}$ for HP) and an amplitude of -3 dBFS and the OSR is chosen to be 64.

3.3.2.1 Clipping

OTA clipping or saturation happens due to limited voltage-swing available at the OTA output. The simulation result showing the influence of clipping on both LP and HP modulators is presented in Fig. 3.21. This figure presents the SNDR performance as a function of first integrator (or HP filter) clipping level.

This shows that both LP and HP structures perform equally good in the presence of OTA saturation. They require at least an output swing of $0.8Vref$ to achieve the required performance. The reason for this is explained by having a look at the histogram of the output signal of first integrator (or HP filter) in Fig. 3.22.

It shows that both the integrator and the HP filter have the same output excursion and hence the same number of samples undergo the clipping; therefore the same performance in the presence of OTA clipping or saturation.

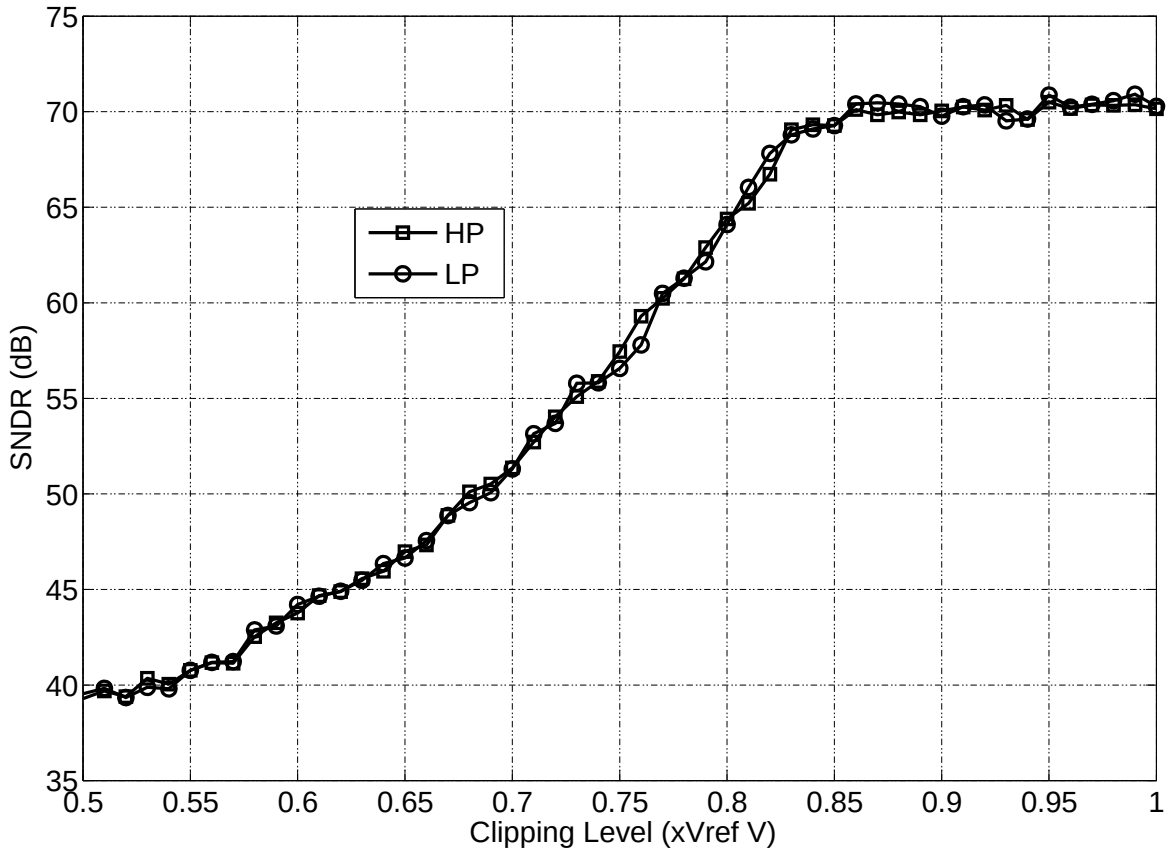


Figure 3.21: Effect of OTA clipping on LP and HP Modulators

3.3.2.2 DC-Gain

Finite DC-Gain of the OTAs introduces static errors in the charge-transfer transient. For an integrator made up of OTA with finite open-loop dc-gain A_O, the transfer function is transformed into:

$$H_{practical,int}(z) = b\frac{\alpha_{int}z^{-1}}{1-\beta_{int}z^{-1}} \tag{3.29}$$

where α_{int} and β_{int} are less-than-unity quantities and represent gain degradation and filter leakage (or gain and pole location perturbation) respectively. Gain degradation results in only a fraction of the input signal being added to the output and filter leakage results in only a fraction of the last output being added to the input.

After doing the necessary calculations [52], their values are found to be:

$$\alpha_{int} = \frac{A_0}{A_0+1.5}, \quad \beta_{int} = \frac{A_0+1}{A_0+1.5} \tag{3.30}$$

Similarly for a HP filter, the OTA finite open-loop dc-gain A_O introduces errors in its ideal transfer function. This effect can be represented mathematically by:

$$H_{practical,hp-filter}(z) = b\frac{\alpha_{hp-filter}z^{-1}}{1+\beta_{hp-filter}z^{-1}} \tag{3.31}$$

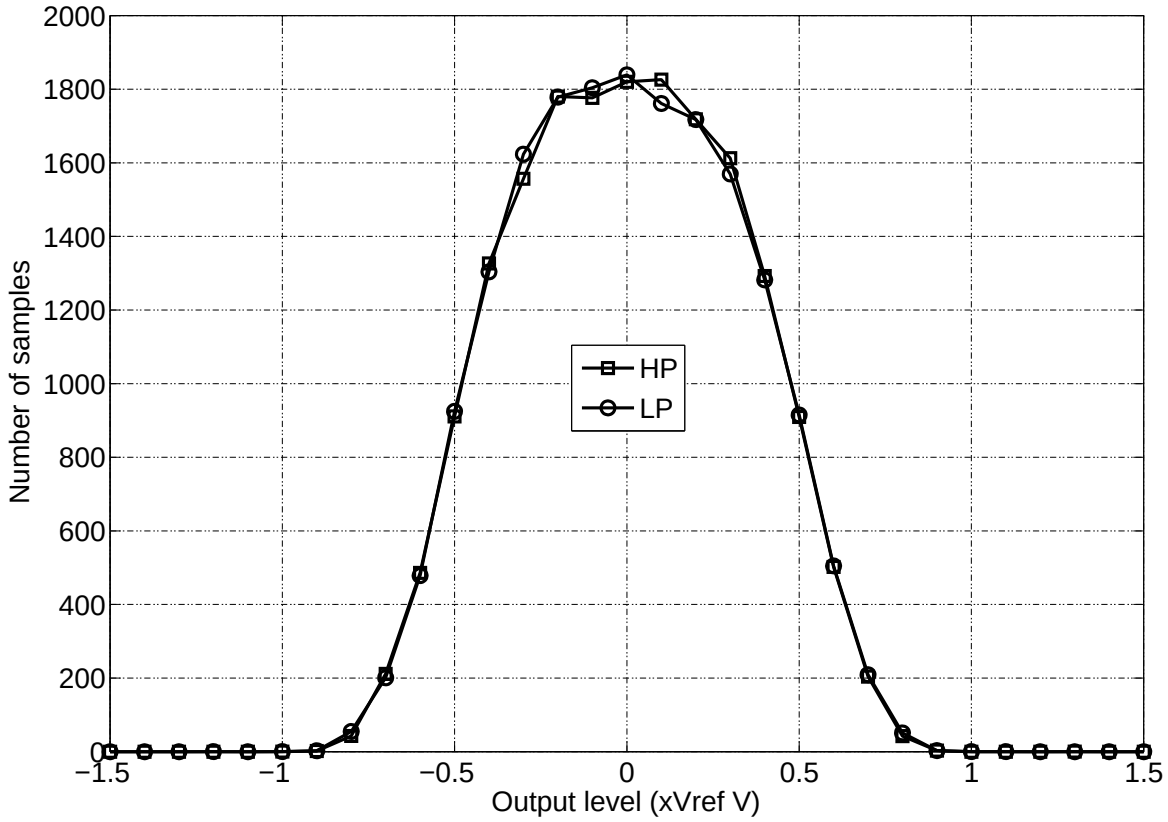


Figure 3.22: Output Excursions

Gain degradation $\alpha_{hp-filter}$ results in only a fraction of the input signal being added to the output while the filter leakage $\beta_{hp-filter}$ results in only a fraction of the last output being subtracted from the input.

Solving the charge transfer equations [52] gives the values of $\alpha_{hp-filter}$ and $\beta_{hp-filter}$ as:

$$\alpha_{hp-filter} = \frac{A_0}{A_0 + 1.5}, \quad \beta_{hp-filter} = \frac{A_0 + 1}{A_0 + 1.5} \tag{3.32}$$

Using Eqns. 3.30 and 3.32 as the transfer function for the first integrater and the first HP filter respectively, the modulator is simulated at a range of values of A_0 to identify the effect of this non-ideality.

The result in Fig. 3.23 shows that both LP and HP modulators require OTA with a minimum dc-gain of 30 dB to reach an SNDR of 70 dB.

3.3.2.3 Gain Bandwidth Product and Slew Rate

In contrast to the finite dc-gain, finite GBW and finite SR of the OTAs generate dynamic errors in the charge-transfer transient. For a given OTA, the maximum operation frequency is limited due to this non-ideal settling behaviour. To compare the performances of HP and LP modulators in the presence of finite GBW and SR, circuit schematics have been made in CADENCE-VIRTUOSO editor. Schematics for HP and LP modulators are shown in Figs. 3.24 and 3.25 respectively.

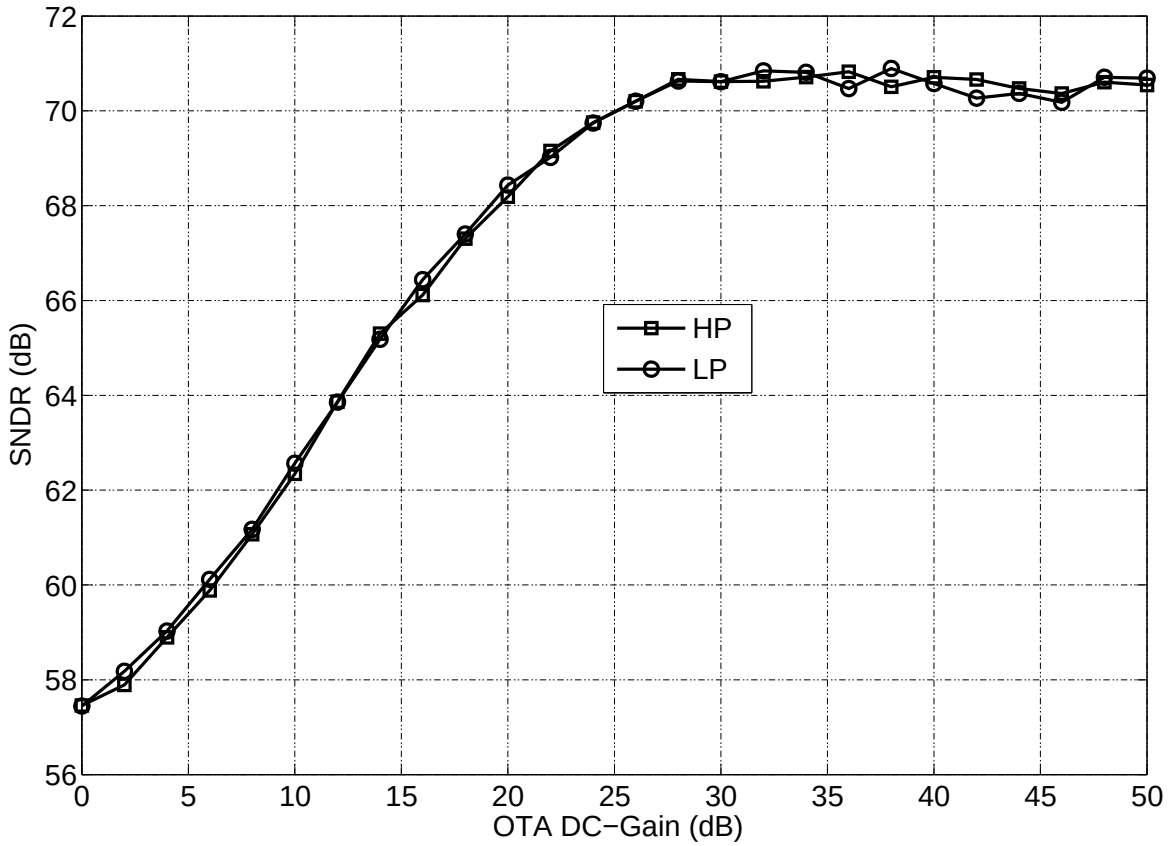


Figure 3.23: SNR vs OTA DC-Gain

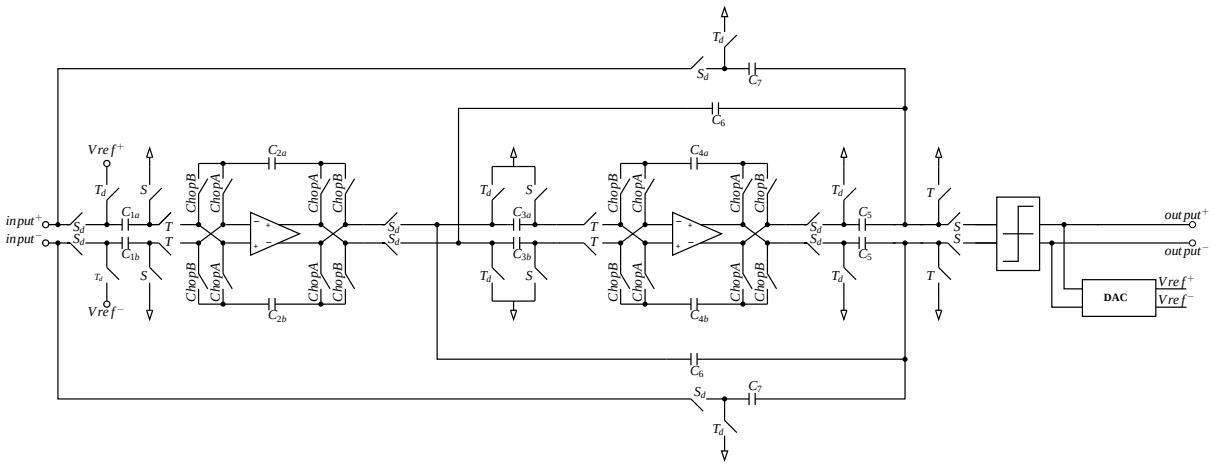


Figure 3.24: Silva HP Circuit

All components are implemented as quasi-ideal models except the OTA of the first high-pass filter (or integrator) that was implemented at the transistor level to gauge the relative effect of finite OTA performances on HP and LP modulators. The employed OTA has a two stages architecture with a Miller compensation as shown in Fig. 3.26. The first-stage provides the major portion of gain and the second-stage acts as a buffer to provide high voltage-swing. This OTA architecture has been chosen as it has to be used in the first HP filter where

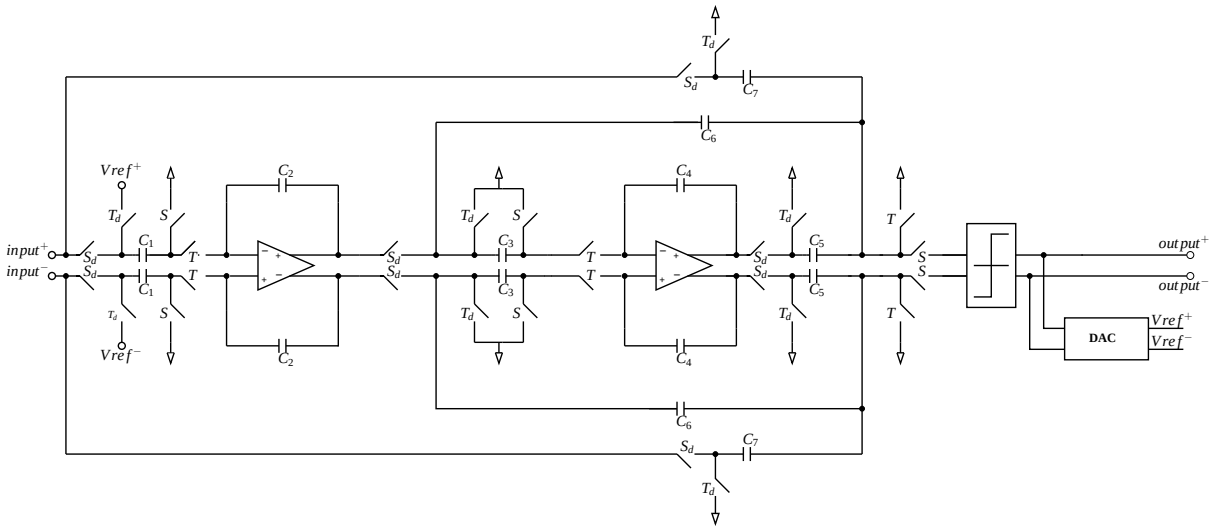


Figure 3.25: Silva LP Circuit

voltage-swing requirement is high as shown in the histogram of Fig. 3.22. The trade-off is increased power consumption as both the stages need to be biased with currents.

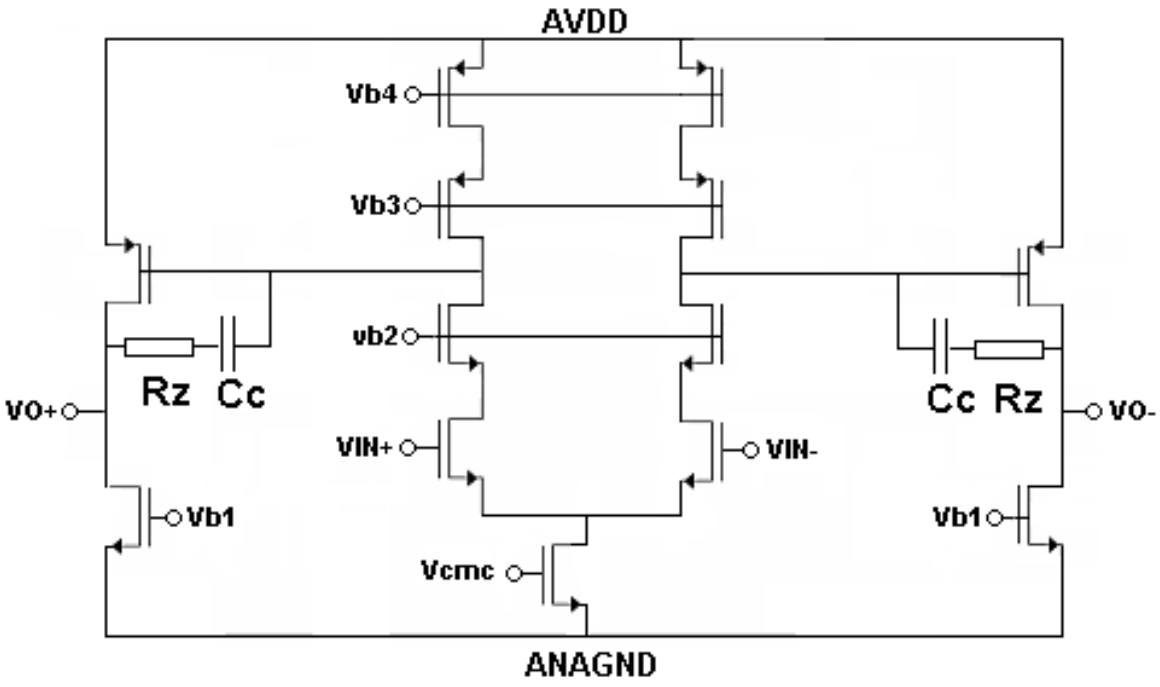


Figure 3.26: OTA Configuration

These circuits have been simulated at various operation frequencies using SPECTRE and 65nm CMOS process. The results are illustrated in Fig. 3.27.

The LP and HP modulators perform equally good in the presence of finite GBW and SR. The two SNDR curves are within 2dB of each other.

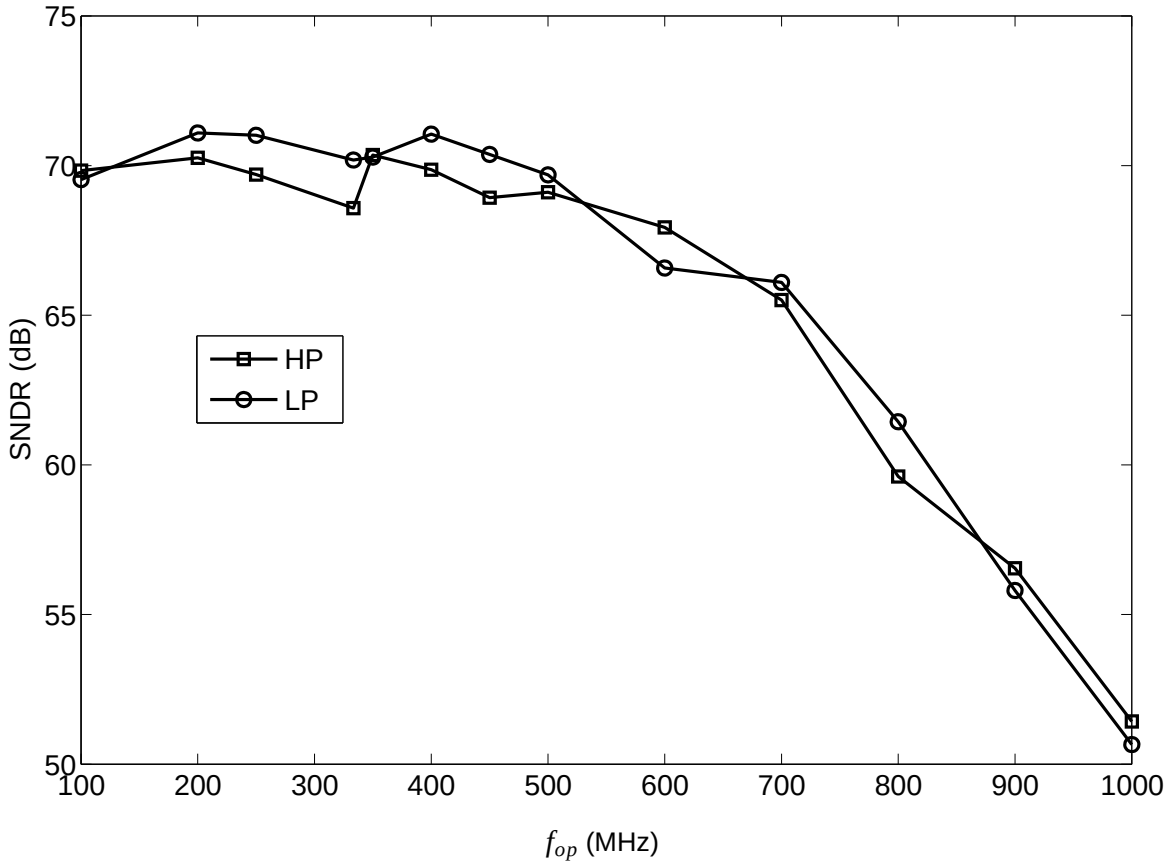


Figure 3.27: Impact of finite SR and finite GBW

3.3.3 DC-Offset, 1/f Noise and Thermal Noise

Dc-offset arises in OTA due to mismatches between the transistors[56]. The random motion of charge carriers in silicon is responsible for the thermal noise and the random trapping and releasing of charge carriers at the interface between gate oxide and silicon gives rise to flicker noise.

For the purpose of noise analysis, the input referred OTA noise is generated in MATLAB which is the sum of dc-offset, thermal noise and flicker noise. Thermal noise consists of random values with normal distribution at mean 0 and variance equal to the power required of the noise source which has been set at 0.01. The time interval between two samples has been set at $T_{op}/10$ which enables to model the noise as a continuous time source [57].

Flicker noise (1/f noise), on the other hand, is generated in MATLAB by passing white noise through a filter with a transfer function [58]:

$$H_f(z) = \frac{1}{(1 - z^{-1})^{\alpha/2}} \tag{3.33}$$

Input referred noise of the OTA generated in the MATLAB is injected in the circuit by adding a voltage source at each input of the OTA as presented in Fig. 3.28. The values of these voltage sources are read from MATLAB.

The OTA1 in Figs. 3.24 and 3.25 is replaced by noisy OTA of Fig. 3.28. The simulation result of noise-injection in both HP and LP modulators is shown in Fig. 3.29.

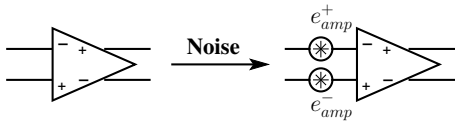


Figure 3.28: Noise injection in OTA

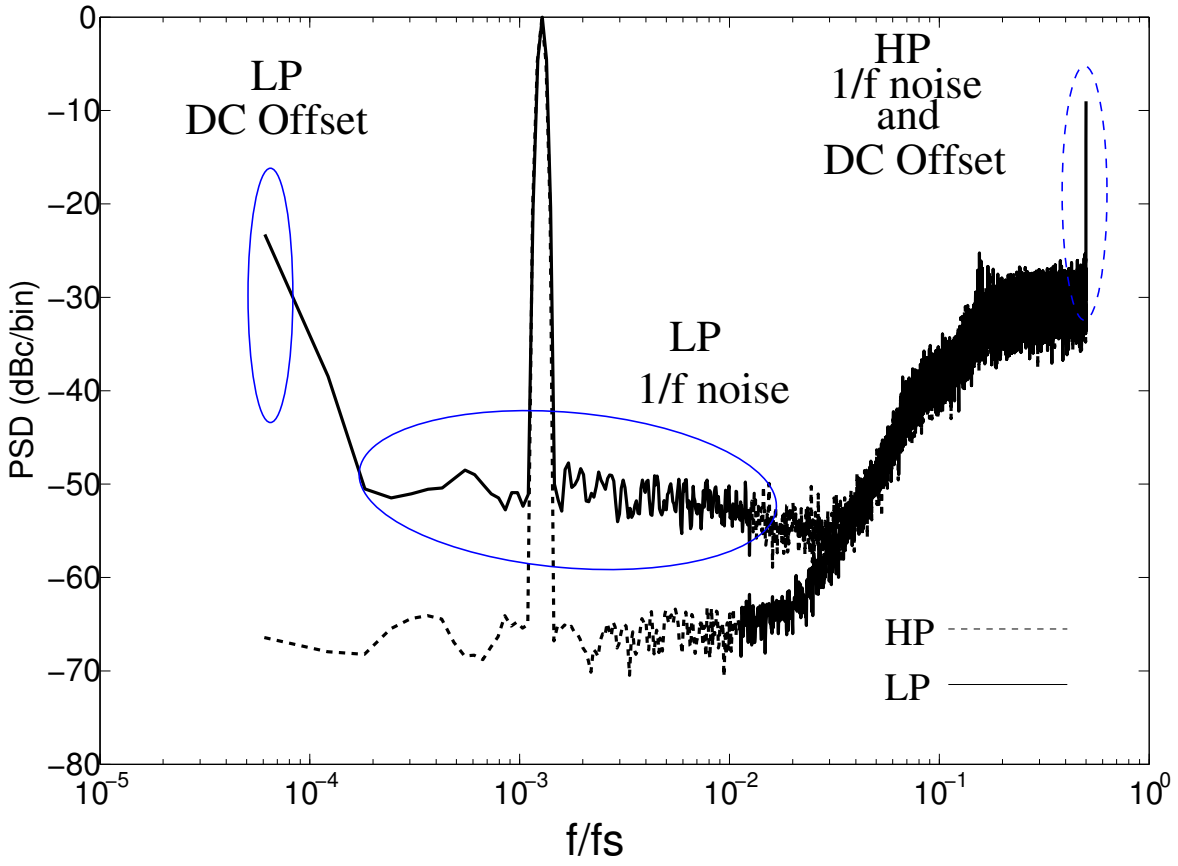


Figure 3.29: Output PSD of the LP and HP modulator in the presence of a flicker noise, a thermal noise and a DC offset

This figure shows that the HP modulator succeeds in avoiding the low frequency-Flicker noise and DC-offset, while in LP modulator, the DC-offset and 1/f noise corrupt the signal band and result in considerable reduction of SNR. This immunity against low-frequency noises is one of the main advantages of HP modulators.

3.3.4 Quantizer Non-Idealities

3.3.4.1 Offset

Offset can be seen as an added voltage to the latch input signal. It is caused mainly by mismatches of dynamic latch transistors and mismatches of switches that are connected to the comparator input [59].

Fig. 3.30 shows the SNDR with respect to offset for both the LP and HP modulators with and without OTA clipping. It can be noticed that in contrast to LP modulators that are almost insensitive to offset, HP modulators suffer from a significant SNDR degradation when

the offset increases. Fig. 3.31 shows the histograms of the different points of both modulators in the presence of an offset of $0.15Vref$. For LP modulators, the quantizer input's average is equal to the offset which minimizes the quantization noise power (Fig. 3.31). While, for HP modulators, the average of the comparator input is almost unchanged compared to the ideal case. Consequently, since the distribution of the samples is not centered around the threshold voltage of the comparator, the quantization noise increases with offset increase which explains $Degradation_1$.

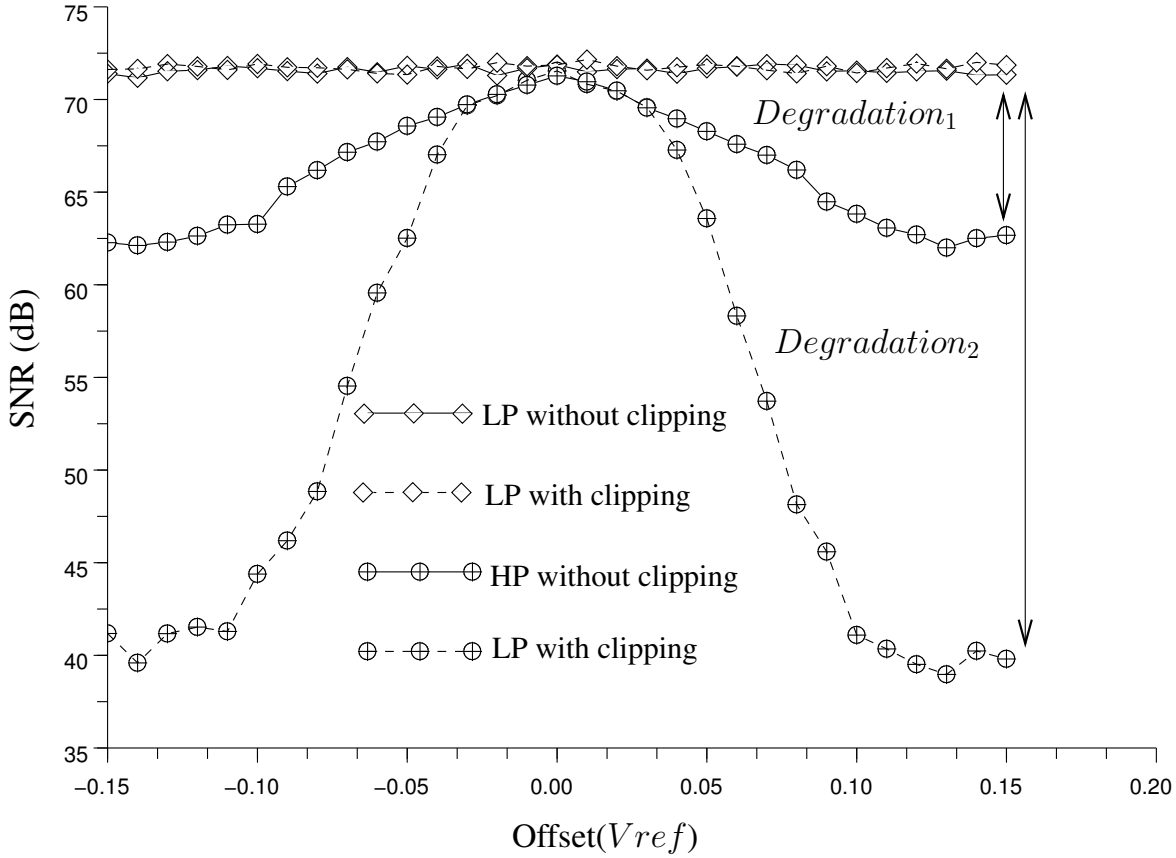


Figure 3.30: SNDR vs Offset

On the other hand, it can be noticed that the output excursions of the HP modulator stages are larger than the corresponding excursions in LP modulator. In fact, the comparator offset causes the arising of even order distortions. This error is added at the quantizer level and as a consequence it will be filtered by the modulator NTF. For LP modulators, the harmonics arise at low frequencies hence they will be strongly attenuated by the NTF filtering. For HP modulators, the signal is at $f_{op}/2 - f_{in}$. Its even order harmonics appear at $i(f_{op} - 2f_{in})$ (where $i \epsilon \mathbb{N}$). These harmonics will alias at $2if_{in}$ and since the HP NTF has a low pass behaviour, they will be amplified as it can be seen in Fig. 3.32. These harmonics are not in the signal bandwidth but nevertheless they cause an increase of the signal power at the modulator input and consequently the HP filters' excursion. Besides, the higher the offset, the higher the harmonics' power and consequently the HP filters' excursion. Therefore, when OTAs' clipping is considered, the number of samples affected by saturation increases with offset which explains $Degradation_2$.

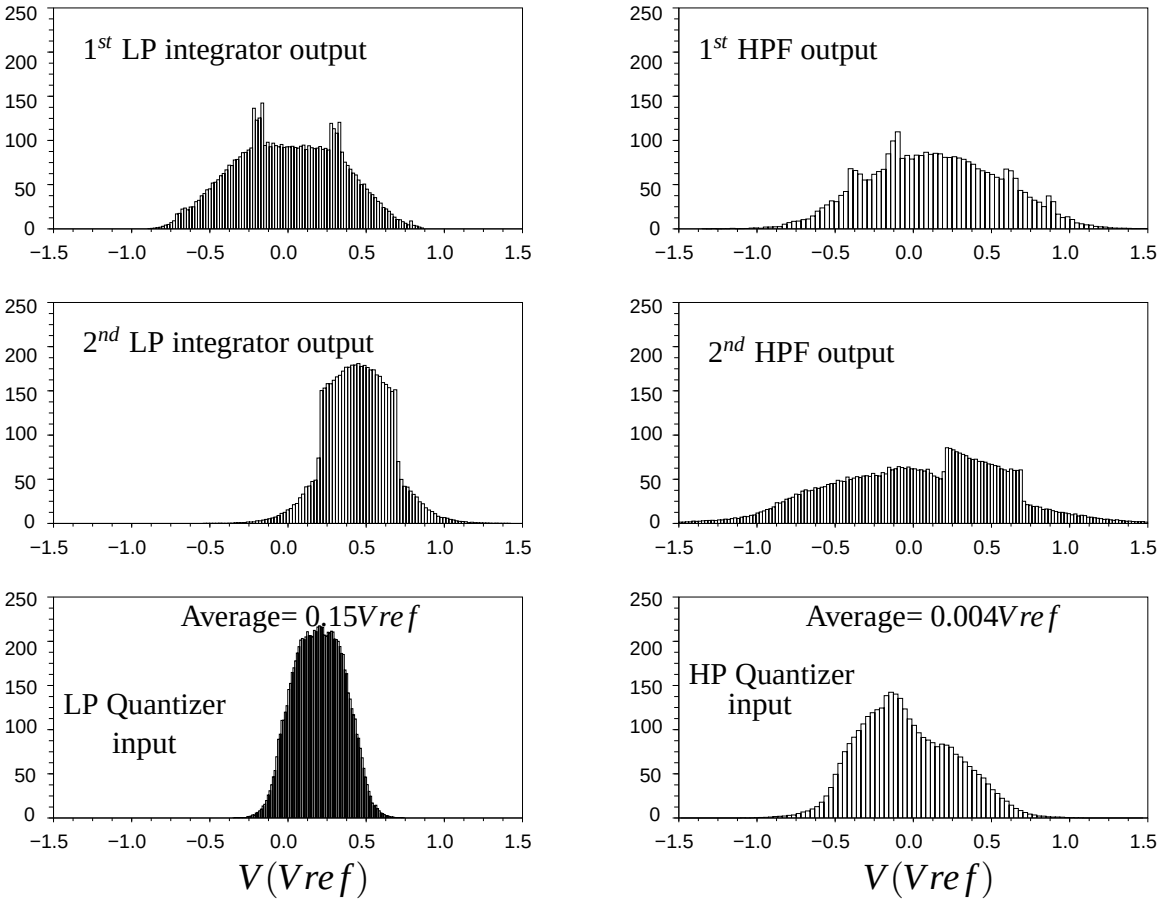


Figure 3.31: Histograms of the HP and the LP Modulators

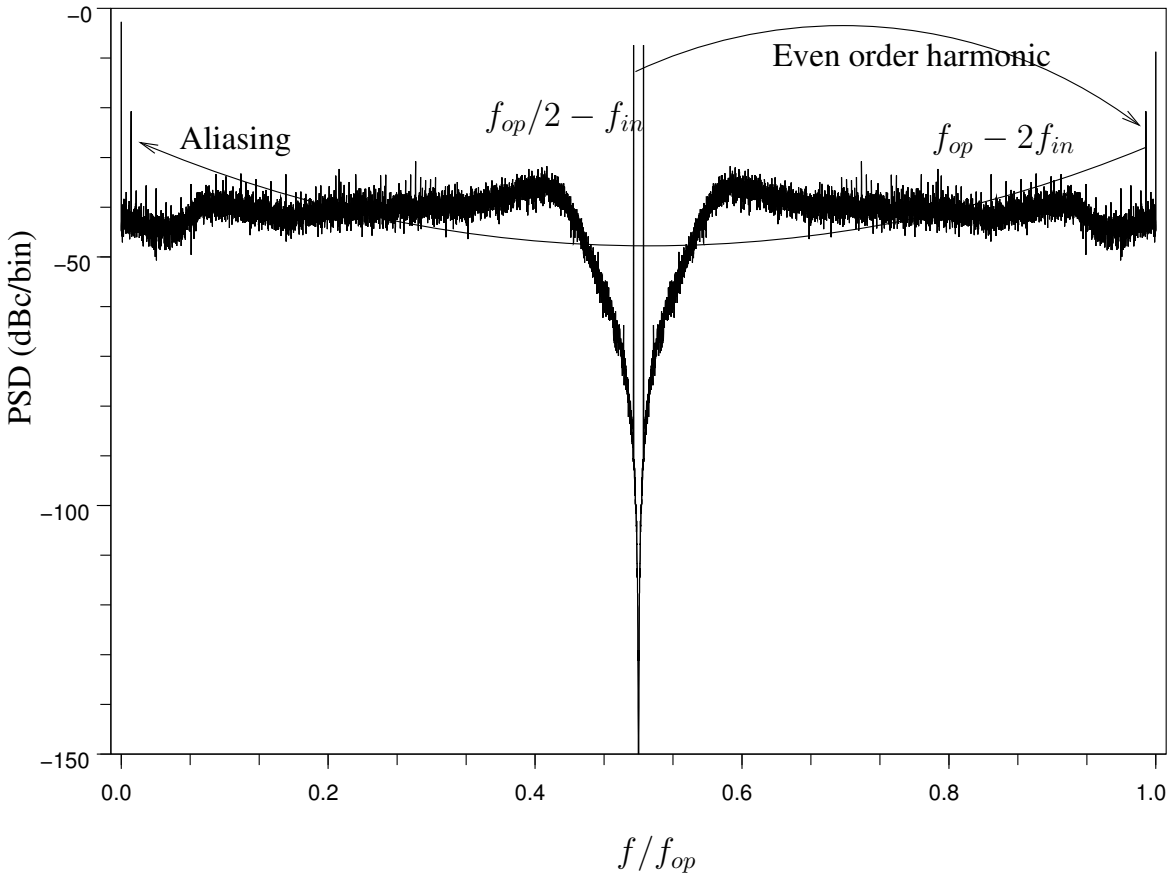


Figure 3.32: HP modulator spectrum with an offset of 0.15 $Vref$

3.3.4.2 Metastability

A comparator is called metastable if its decision time exceeds the length of the latch phase. Its output will be then an undetermined value [42]. The decision time depends mainly on the gain of the dynamic latch, the gain of the pre-amplifying stage that may precede it and on the input value. In fact, the lower the quantizer input and gain and the higher the operation frequency, the higher the metastability impact.

The signal distribution of the quantizer input of LP and HP modulators is almost identical

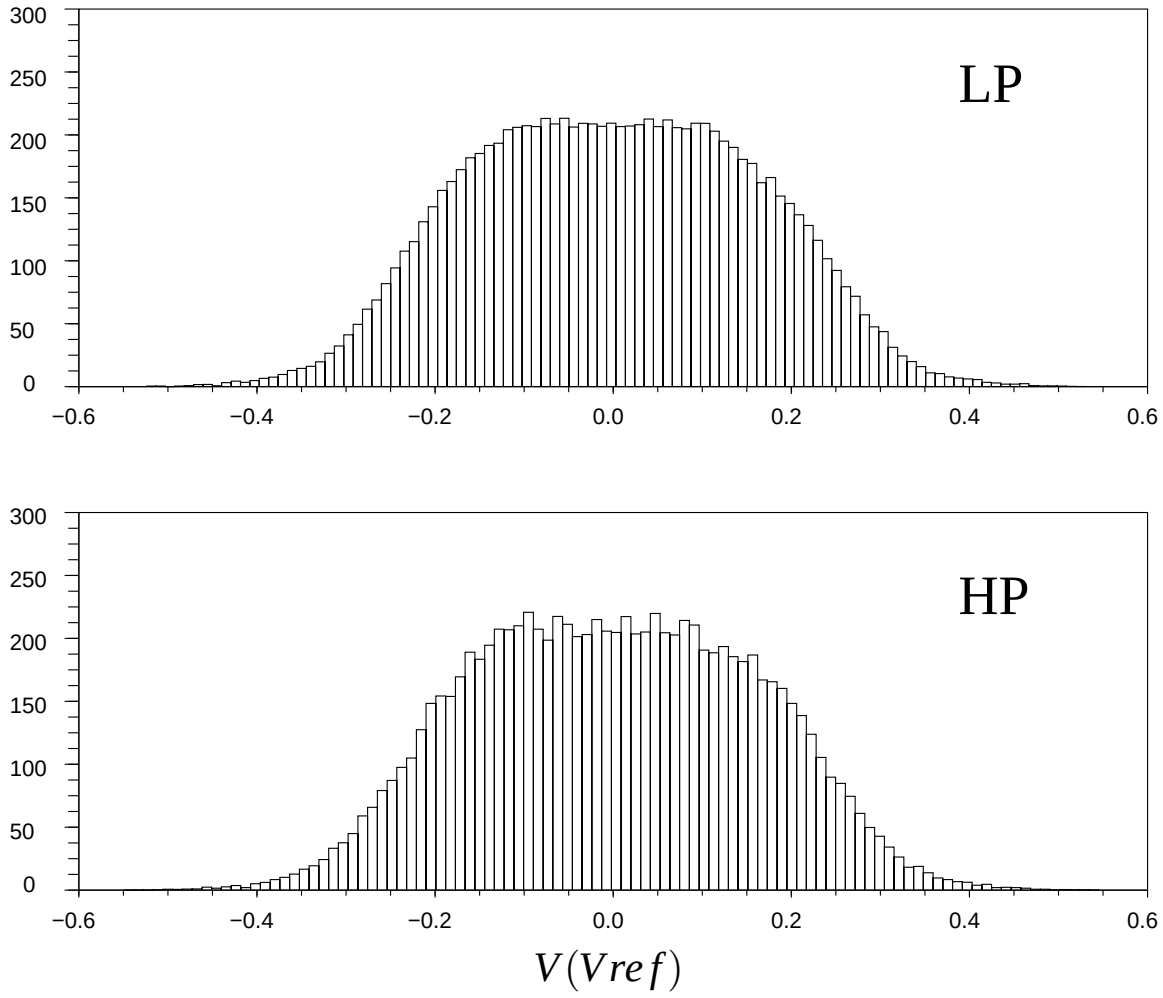


Figure 3.33: Histogram of the comparator input

as it can be seen in Fig. 3.33. As a result, for an identical comparator, the probability of metastability occurrence is equal for LP and HP modulators. Besides, its impact is a white noise arising [42], therefore the SNR degradation due to metastability will be the same for both architectures. This result is confirmed in Fig. 3.34

3.3.4.3 Hysteresis

During its off-phase, the dynamic latch forces its output nodes to a pre-determined voltage. However when the operation frequency increases, these voltages can not be reached exactly and their value will depend on the previous state of the latch. This creates a memory effect

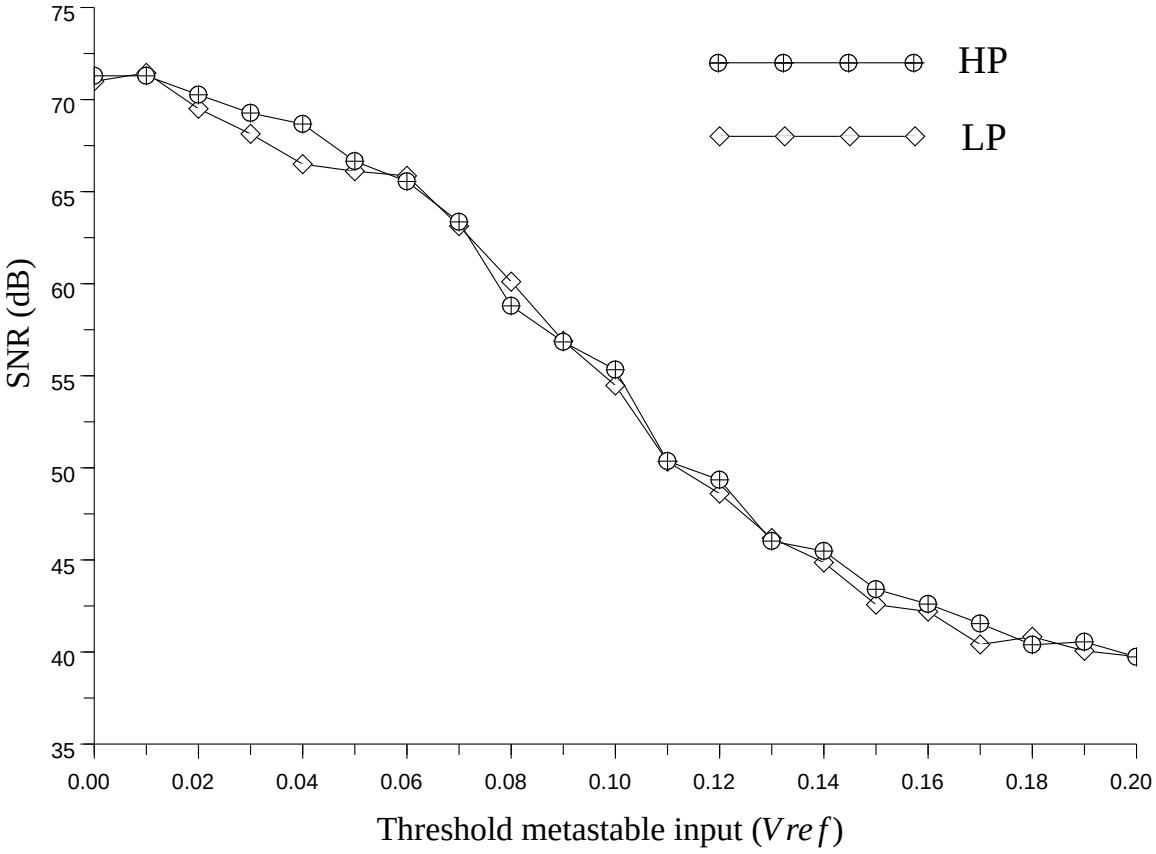


Figure 3.34: SNR vs metastability threshold V_{in}

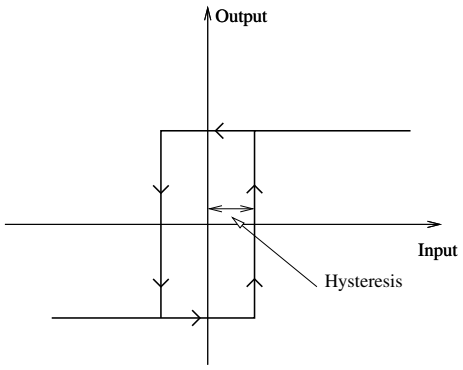


Figure 3.35: Comparator output vs input with hysteresis

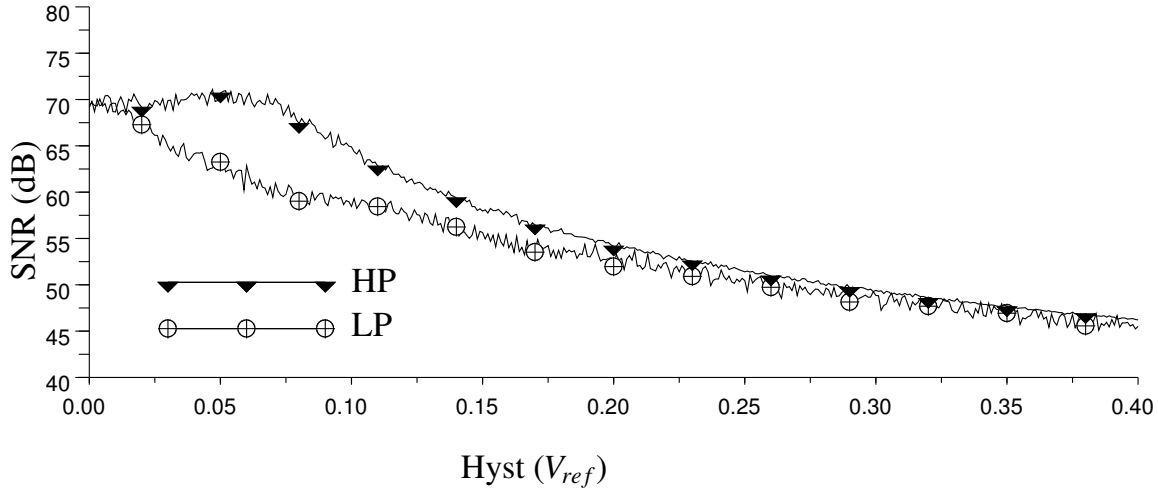


Figure 3.36: SNR vs hysteresis

known as hysteresis that causes a variation of the threshold voltage of the comparator as a function of its previous state as shown in Fig. 3.35.

The impact of hysteresis on $\Delta\Sigma$ modulator can be seen as an added white noise [60]. Fig. 3.36 shows the SNR with respect to hysteresis for both modulators. As it can be seen, for small values of hysteresis, no SNR degradation occurs because the hysteresis noise is dominated by the quantization noise. On the other hand, it can be observed that SNR degradation for HP modulators occurs for higher values. In order to understand the reason of this observation, the 3D histograms of the couples (previous state , transition) were traced. Previous state is the comparator input value in the previous clock cycle and transition is the difference between actual value and previous one. The red (dark) bars represent the samples that have suffered from an hysteresis of $0.1Vref$. It can be noted that the number of these samples is much larger in the case of LP modulator. This explains the higher robustness of HP modulators against hysteresis.

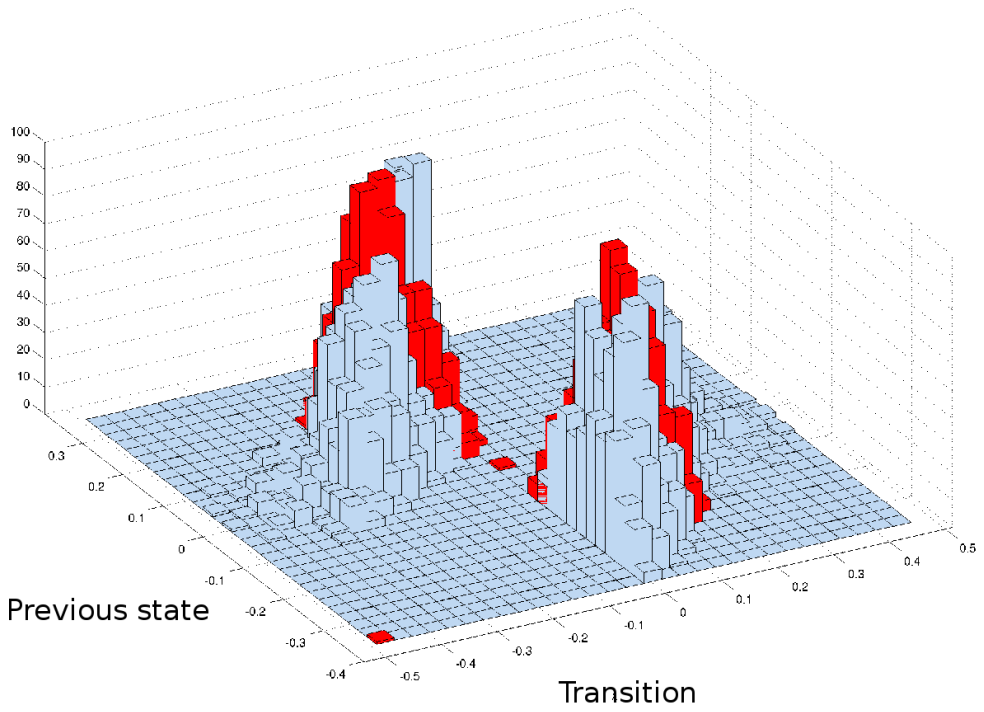


Figure 3.37: 3D Histogram for a LP modulator

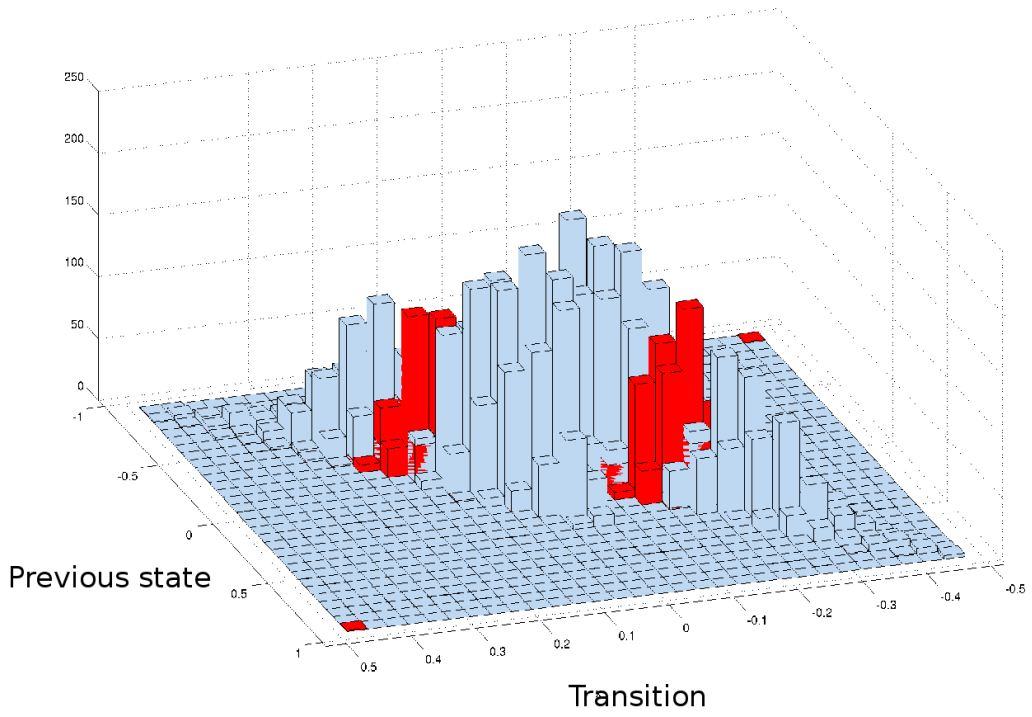


Figure 3.38: 3D Histogram for a HP modulator

Novel correction technique for LP modulators against hysteresis

Since HP modulator is robust face to hysteresis, the main problem remains for LP modulator. Interestingly, this latter is more robust to a negative hysteresis than the former as it can be seen in Fig. 3.39. The proposed technique to reduce the hysteresis effect is based on this result. Although that a negative hysteresis does not occur in reality, a positive hysteresis can be changed into negative one.

Fig. 3.41 shows one way to implement the feedforward LP modulator. Two chopping circuits were added on the circuit of the classical modulator before and after the comparator. The first converts the positive hysteresis into a negative one. The second chopping circuit corrects the effect of the first chopping operation to preserve the same noise shaping.
To isolate as much as possible the hysteresis impact, OTAs, capacitors and switches were implemented using quasi-ideal models. In fact, the OTAs were implemented as a one pole model which has a DC gain of 60 dB and a slew rate of 500 V/μs. The switches were modelled as 100 Ω resistance when On and 100 MΩ resistance when off. The dynamic latch, the RS latch and the two chopping circuits were implemented in a 65 nm CMOS process. The dynamic latch was implemented using the circuit of Fig. B.14, it is controlled by clock T_d. Its hysteresis is equal to 27 mV for an operation frequency of 220 MHz. The RS latch consists of four NAND gates and it is controlled by clock S_d. The two additional switches were implemented as regular CMOS switchs. The generation of clocks $S1$, $S2$ and $S3$ is shown

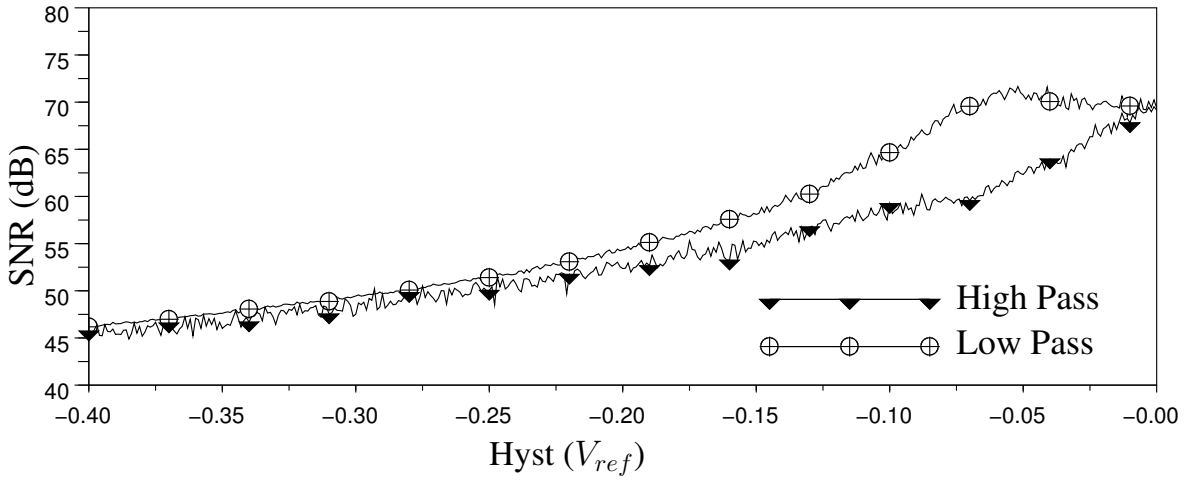


Figure 3.39: SNR vs negative hysterisys

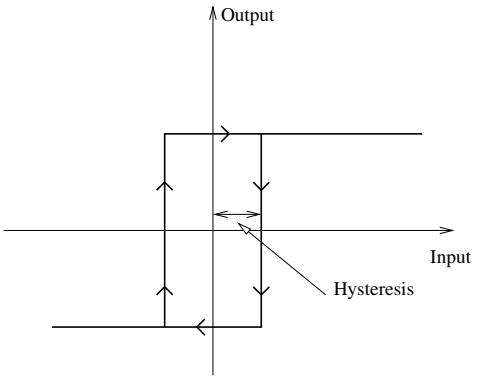


Figure 3.40: Comparator output vs input with negative hysterisys

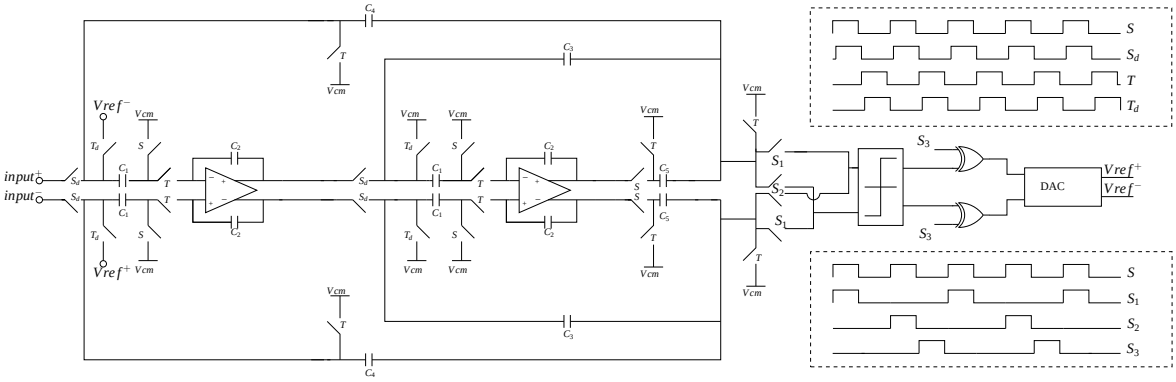


Figure 3.41: Switched capacitor implementation of a 2^{nd} order feedforward $\Delta\Sigma$ modulator with the proposed technique for hysterisys degradation reduction

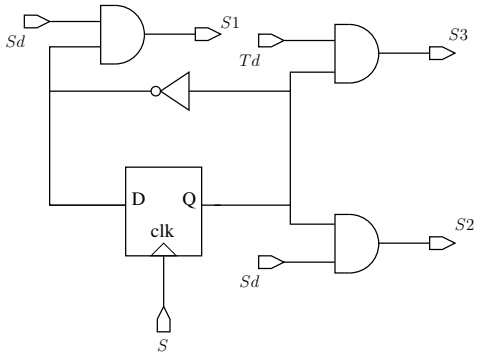


Figure 3.42: Clock generation circuit

in Fig. 3.42.

Two electrical simulations were carried out. The first was performed using the classical circuit without the chopping technique and the second using the circuit of Fig. 3.41. The input signal amplitude is equal to $0.6Vref$ for both simulations. The output spectrums are shown in Fig. 3.43. For an OSR of 64, the measured SNRs are 63 dB and 72 dB for the classical technique and for the proposed technique respectively.
Using the proposed technique has allowed to reduce the degradation due to hysteresis by 9 dB. The power consumption required for the two chopping circuits with their clock generation is equal to 40.8 μW.

3.3.5 Sampling requirements

3.3.5.1 Switch considerations

The SNDR degradation at the output of a $\Delta\Sigma$ modulator due to switch errors depends on many parameters such as the operation frequency, the input signal amplitude and the input signal frequency. Since this last parameter is different for LP and HP modulators, its impact on the SNDR was studied. To achieve this, the circuit of the considered LP and HP modulators were implemented using ideal models for all components except the switches that were implemented as regular CMOS switches in 65 nm CMOS process with $W_p = W_n = 20$ μm and $L_p = L_n = 60$ nm. The modulators were sampled at 100MHz and the input signals were

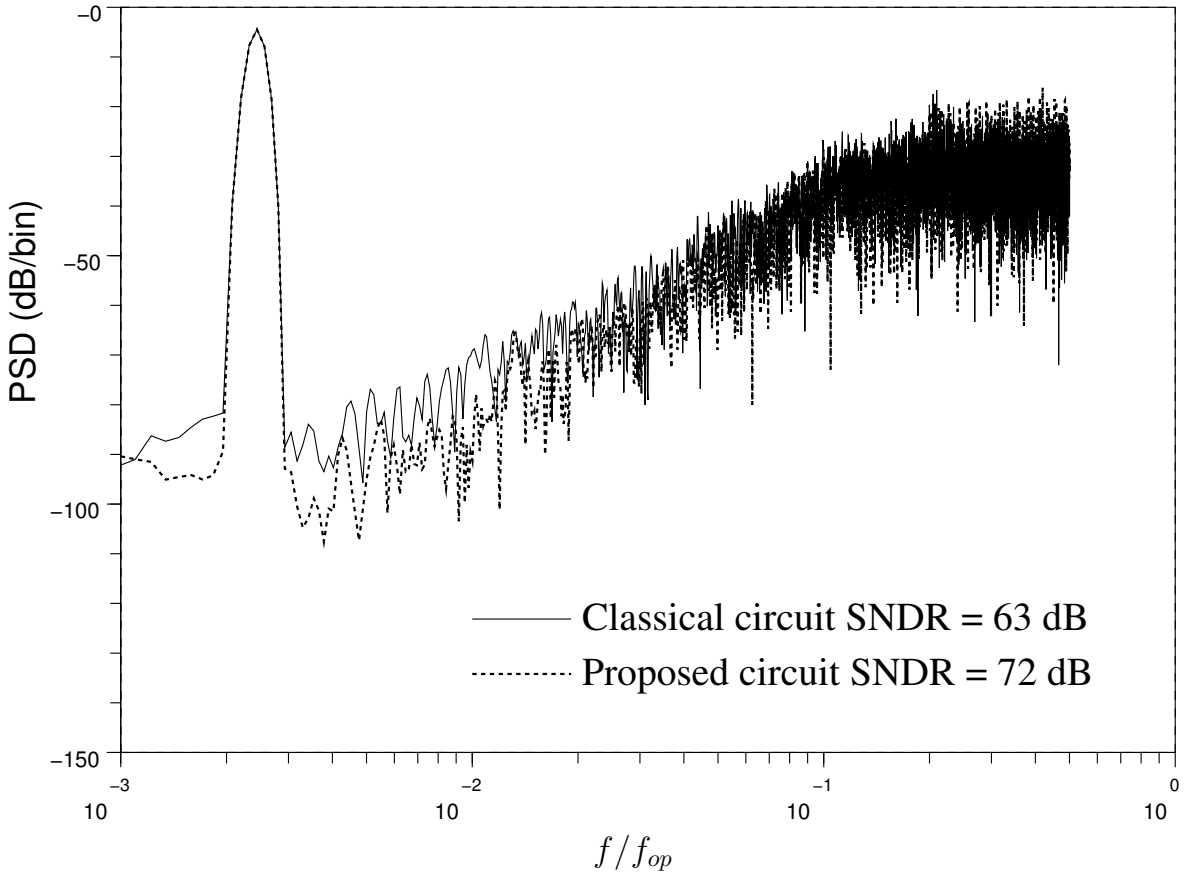


Figure 3.43: ΔΣ modulator output Spectrums with and without hysterisys degradation reduction

at 230KHz for the LP modulator and at $50MHz - 230KHz$ for the HP one. The results are shown in Fig. 3.44. It can be noticed that the distortions and the noise floor are higher for the HP modulator. The SNDR measured for an OSR of 64 is 8 dB lower for this latter. This is due mainly to the higher impact of signal feedtrough and charge injection in HP modulator since the input signal frequency is higher than in LP modulator.

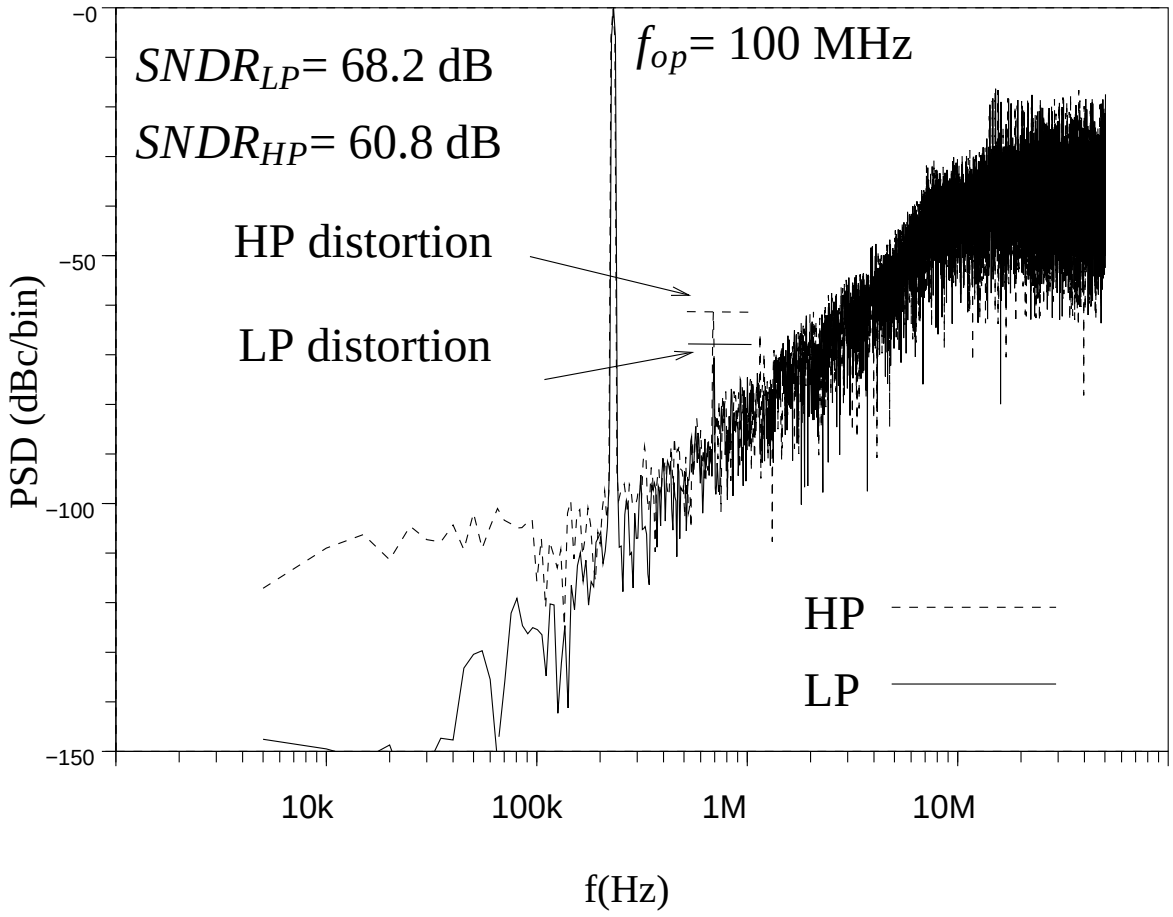


Figure 3.44: Output spectrum with real switches

3.3.5.2 Jitter

The edges of the clock suffer from a random variation known as time jitter. It can be modelled as a Gaussian distribution whose mean is equal to zero and its standard deviation to σ_t. The impact of the clock jitter on the sampled signal can be seen as an additive white noise(section A.2.6). Its power for an sinusoidal input is given by:

$$P_{jitt} \simeq \frac{(2A\pi f_{in}\sigma_t)^2}{2} \tag{3.34}$$

Assuming that the decimation filter eliminates all out of the band noise, the signal power to jitter noise power ratio for an input sine at the edge of the band is then given by:

$$SNR_{jitt-LP} = \frac{P_{signal}}{P_{jitt}/OSR} \simeq 20Log\frac{OSR\sqrt{OSR}}{\pi f_{op}\sigma_t} \tag{3.35}$$

$$SNR_{jitt-HP} \simeq 20Log\frac{OSR\sqrt{OSR}}{(OSR-1)\pi f_{op}\sigma_t} \tag{3.36}$$

Hence, the impact of clock jitter on HP modulator is $20Log(OSR-1)$ times higher than for LP modulators. This result is confirmed in Fig. 3.45 that shows the output spectrums of a LP and HP modulators with a σ_t of 20 ps, an OSR of 64 and a signal at the edge of the band . It can be seen that the noise floor is almost 35dB higher for the HP modulator which corresponds to $20Log(64-1)$.

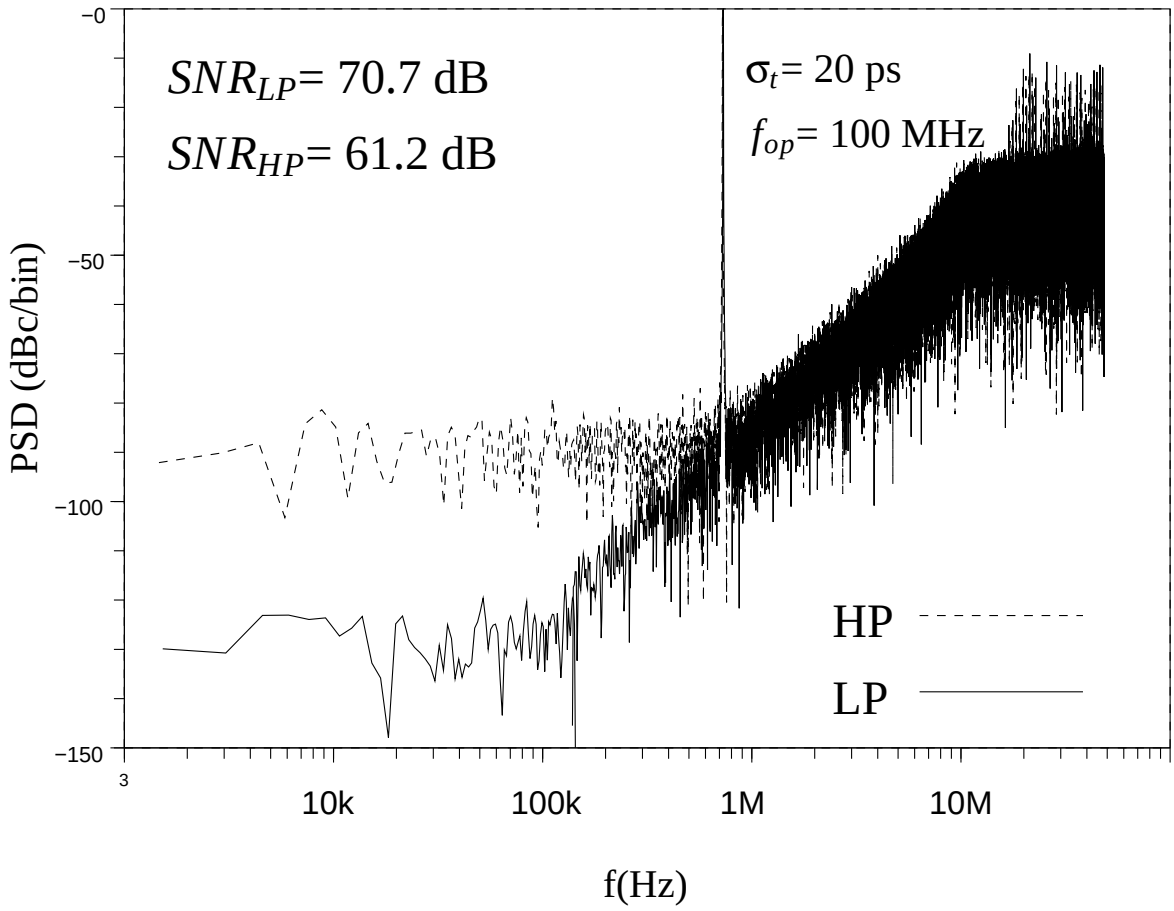


Figure 3.45: Output spectrum with jitter

3.3.6 Conclusion

Table 3.3.6 summarizes the comparative analysis between LP and HP architectures. This analysis was carried out using an improved architecture of high-pass filter that overcomes a large number of drawbacks from which suffered the classical high-pass filter such as high

	LP Modulator	HP Modulator
OTA clipping	☺	☺
OTA DC gain	☺	☺
OTA SR	☺	☺
OTA 1/f noise	☹	☺
OTA thermal noise	☺	☺
OTA offset	☹	☺
Comparator offset	☺	☹
Comparator metastability	☺	☺
Comparator hysteresis	☹	☺
Jitter	☺	☹
Switch requirements	☺	☹

Table 3.2: LP vs HP

power consumption, high thermal noise and high die area.
During this comparison, it has been shown that HP modulators are more robust against OTA's offset and 1/f noise than their LP counterparts. This characteristic is very important because it allows to reduce OTA transistors' dimensions as the requirements in terms of noise and matching are lower. Besides, the offset immunity of HP modulators makes the layout of their OTAs less critical than in LP modulators.
On the other hand, the requirements in terms of jitter and switch linearity are significantly lower in the LP modulator than the HP modulator. The high sensitivity to clock jitter in this latter, may require the use of an on-chip PLL. While the switch problem requires the use of switch linearization techniques such as bootstrapping and clock feedthrough reduction techniques such as dummy switch addition. Besides, section 2.2 showed that increasing the input frequency leads to a higher impact of clock skew and bandwidth mismatch. Therefore, the architecture chosen is the LP. The problems of 1/f noise and OTA's offset will be dealt with careful design and the use of layout matching techniques exposed in section B.2.

Chapter 4

Parallel ΔΣ Modulators

4.1 Parallel ΔΣ Modulators Architectures

Several possibilities to widen the bandwidth of ΔΣ ADCs using parallelism exist : Block filtering ΔΣ, Frequency Band Decomposition, Parallel ΔΣ, and Time Interleaved ΔΣ. The major benefit of all of these approaches is that they increase the conversion bandwidth with a linear increase of the power consumption whereas with a single Delta Sigma modulator, the power consumption increases exponentially as shown in chapter 2.
In this section, each of these architectures is reviewed and their design tradeoffs are discussed in order to determine the most suited architecture for our design.

4.1.1 Block filtering ΔΣ ADC

Fig. 4.1 shows the general architecture of a block filtering structure[61]. Its operation consists of achieving the relation $H(z)$ between the input signal $X(z)$ and the output signal $Y(z)$ by the means of a MxM matrix transfer function $\overline{H}(z)$ shown below:

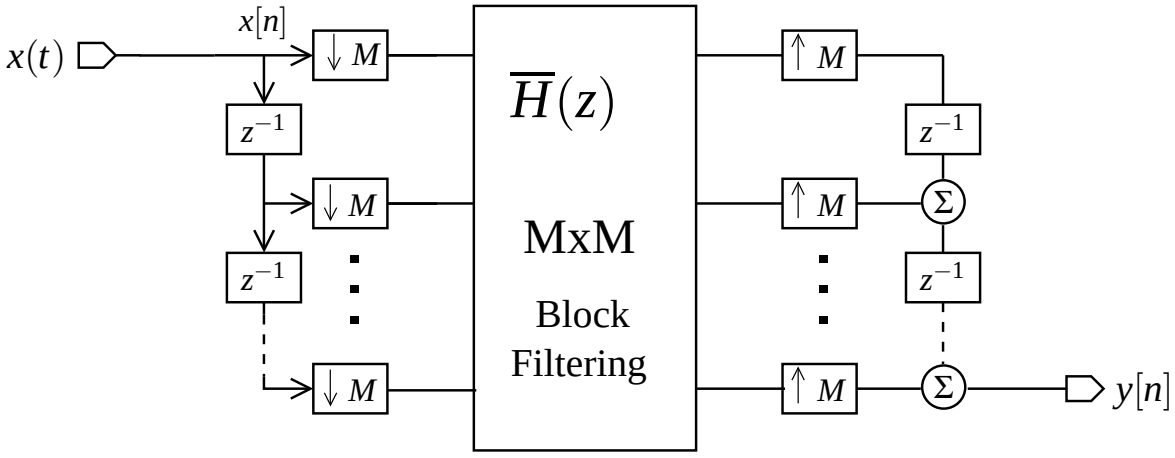


Figure 4.1: Block filtering structure

$$\overline{H}(z) = \begin{bmatrix} E_0(z) & E_1(z) & E_2(z) & \cdots & E_{M-1}(z) \\ z^{-1}E_{M-1}(z) & E_0(z) & E_1(z) & \cdots & E_{M-2}(z) \\ z^{-1}E_{M-2}(z) & z^{-1}E_{M-1}(z) & E_0(z) & \cdots & E_{M-3}(z) \\ \vdots & \vdots & \vdots & & \vdots \\ z^{-1}E_1(z) & z^{-1}E_2(z) & z^{-1}E_3(z) & \cdots & E_0(z) \end{bmatrix}.$$

The term $\overline{H}_{ij}$ of the matrix corresponds to the transfer function between the j^{th} input and the i^{th} output.

The block filtering technique can be used to parallelize ΔΣ modulators[5][62][63]. The OSR of the resultant ADC will be M times higher than the OSR of a single path modulator. This allows to increase the resolution of the ADC or to increase its conversion bandwidth.
The first step in the design of a block filtering ΔΣ ADC is to choose an architecture for the ΔΣ modulator. The corresponding $\overline{H}(z)$ should be derived afterwards. Then, some topological changes must be carried out to implement $\overline{H}(z)$. This last step is very critical because it must be achieved while trying to use as much as possible the circuitry of the modulator to avoid adding components.
For sake of simplicity, an M=2 scenario with a 2^{nd} order distributed Feedback modulator is considered. The equivalent block filter is chosen to be the integrator. Therefore the operation must be repeated twice. This solution was preferred to a whole modulator equivalent block filter solution because it needs less additional circuitry. The equivalent $\overline{H}(z)$ is shown below:

$$H(z) = 0.5\frac{z^{-1}}{1-z^{-1}} \Longrightarrow \overline{H}(z) = \left| \begin{array}{cc} z^{-1} & 1 \\ z^{-1} & z^{-1} \end{array} \right| \frac{0.5}{1-z^{-1}}.$$

The architecture of the parallel ADC is derived from the expression of $\overline{H}(z)$. An optimized architecture is shown in Fig. 4.2. As it can be seen, the implementation of $\overline{H}(z)$ has just required the addition of four paths between channels (The dashed lines in the figure). In a differential DT implementation, this requires two additional sampling capacitor per path to achieve the summing operation.

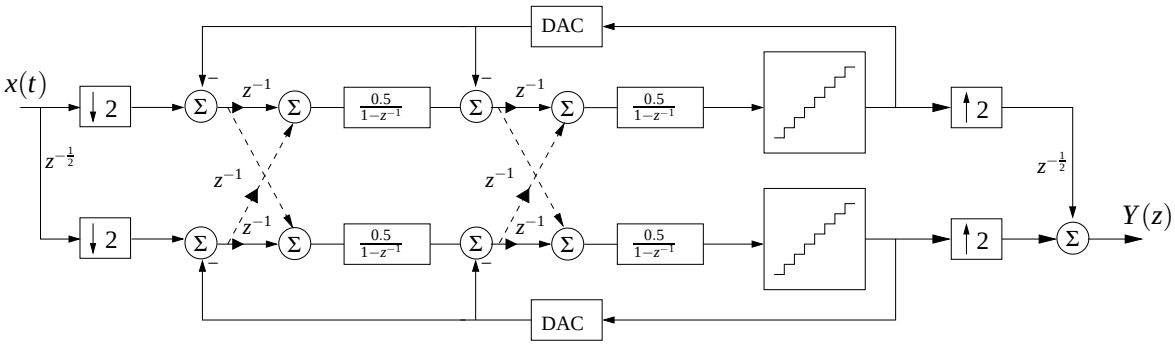


Figure 4.2: Block filtering ΔΣ ADC

The advantages and disavantages of the block filtering architecture are:
Advantages:

- The signal demultiplexing at the input and reconstruction at the output are very simple
- All the channels are identical

- Channel mismatch does not generate tones. It causes just an increase of the noise floor [62]

Disadvantages:

- The summing operation requires additional capacitors which increases the die area and the load on the OTAs
- The paths between channels must be protected from coupling which makes the layout critical
- Practical implementation for ADCs with M>2 is very complex due to the previous reasons [62]
- The implementation of some architectures of $\Delta\Sigma$ modulators is impractical due to the high complexity of the equivalent $\overline{H}(z)$

4.1.2 $\Pi\Delta\Sigma$ ADC

Fig. 4.3 shows the architecture of a $\Pi\Delta\Sigma$ ADC[4][64]. In this architecture, the input signal is applied to all channels simultaneously. Then the signal in each channel is multiplied by a ±1 sequence that is specific to each channel. The ±1 sequence is derived from a MxM Hadamard

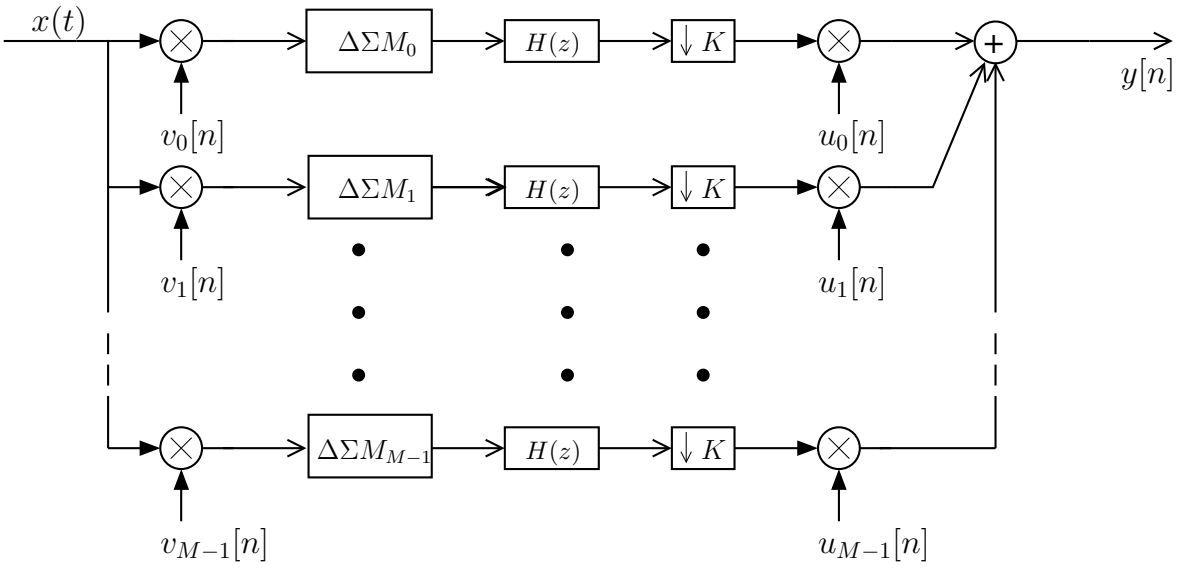


Figure 4.3: $\Pi\Delta\Sigma$ ADC

matrix that has two main properties: 1)it is composed of just ±1; 2) its multiplication by its transpose gives an identity matrix. The first property allows to achieve simpler multiplications at the input. In fact, in differential circuits, this multiplication is implemented by adding two switches at the input and then depending on the current term of $v[n]$, the input is either passed or crossed. While the second property is important for the digital signal reconstruction.
The matrix below shows $v[n]$ for M=4 and OSR=16 scenario. The terms in bold are the terms of a 4x4 Hadmard matrix. The other terms are derived by repeating the Hadamard term k

times, where k=OSR/M.

$$v[n] = \left| \begin{array}{cccccccccccccccc} \mathbf{1} & 1 & 1 & 1 & \mathbf{1} & 1 & 1 & 1 & \mathbf{1} & 1 & 1 & 1 & \mathbf{1} & 1 & 1 & 1 \\ \mathbf{1} & 1 & 1 & 1 & \mathbf{-1} & -1 & -1 & -1 & \mathbf{1} & 1 & 1 & 1 & \mathbf{-1} & -1 & -1 & -1 \\ \mathbf{1} & 1 & 1 & 1 & \mathbf{1} & 1 & 1 & 1 & \mathbf{-1} & -1 & -1 & -1 & \mathbf{-1} & -1 & -1 & -1 \\ \mathbf{1} & 1 & 1 & 1 & \mathbf{-1} & -1 & -1 & -1 & \mathbf{-1} & -1 & -1 & -1 & \mathbf{1} & 1 & 1 & 1 \end{array} \right|.$$

The modulated signal by $v[n]$ is then digitized by a ΔΣ modulator. There are no constraints on the architecture of the modulator. The filter $H(z)$ that follows the modulator is an important block of this architecture because it must ensure the signal reconstruction and a maximum quantization noise cancellation. The filter output is then brought back to the Nyquist rate by a decimator by k and then demodulated by multiplying it by the sequence $u[n]$ that is equal to the Hadamard matrix(The terms in bold of $v[n]$).
The advantages and disavantages of the ΠΔΣ architecture are:
Advantages:

- All the channels are identical
- A coding gain of 3 dB is achieved for every M doubling [65]

Disadvantages:

- High sensitivity to channel mismatch
- The digital reconstruction is complex [65]
- Two switches must be added at the input of each modulator and since they process the signal, they might have to be implemented as bootstrapped switches (section A.2)

4.1.3 Frequency band decomposition

The frequency band decomposition (FBD) architecture is derived from the concept of the HFB[6][66] [67]. The conversion bandwidth is divided into M sub bands. Each sub band is converted by a ΔΣ modulator that operates at OSR$\times f_s/M$ instead of OSR$\times f_s$.

Fig. 4.4 shows the bloc diagram of a FBD ADC. The signal is first fed to an input filter. Unlike HFB in which the input filters' purpose is to minimize the aliasing, in FBD the input filters' purpose is to reduce the out of band power in order to increase as much as possible the dynamic range of the ADC. In fact, the decimation operation is achieved at the digital back-end and therefore the rejection of the aliasing between sub-bands can be realized at this level which will simplify its implementation compared to an analog rejection operation. The filtered signal is then applied to a bandpass ΔΣ modulator. The NTF of each channel is different to reject the quantization noise out of the considered sub band. Fig. 4.5 shows the NTFs for M=4 and OSR=32 scenario. The digital signal is then decimated and reconstructed.

The advantages and disavantages of the FBD architecture are:
Advantages:

- The architecture is almost insensitive to channel mismatch
- Apart from the first channel, the channels are immune to offset and 1/f noise

Disadvantages:

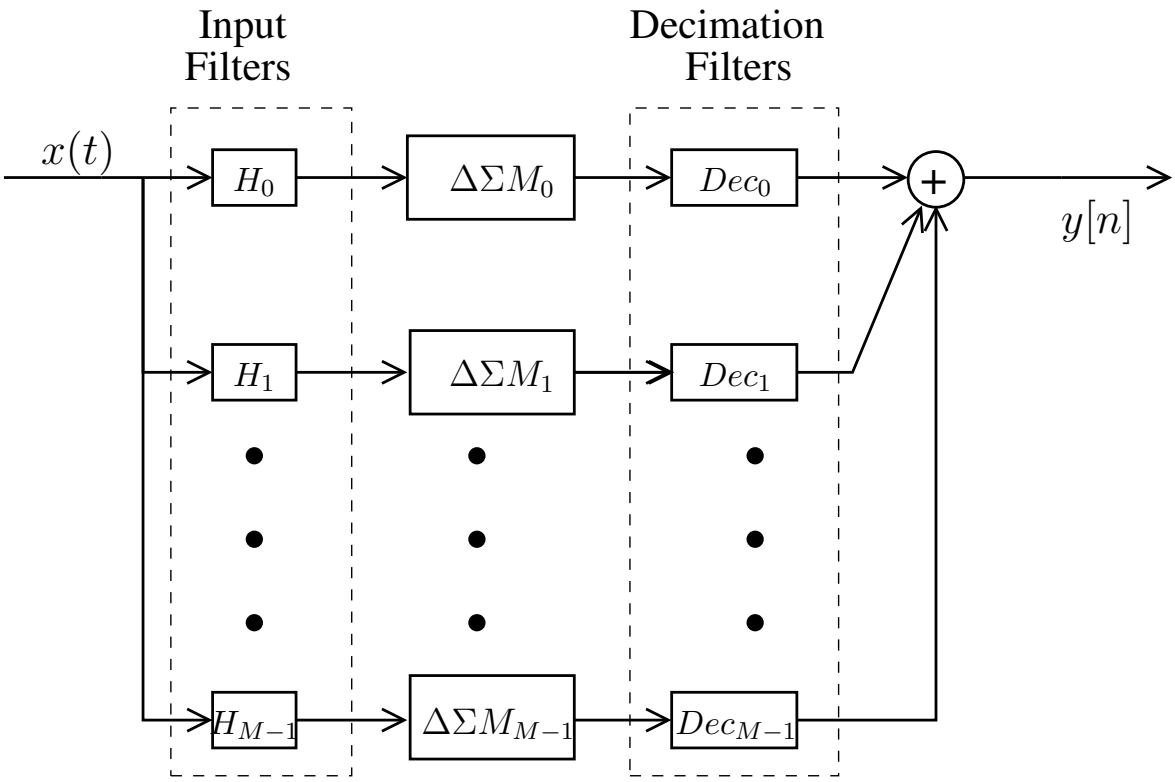


Figure 4.4: FBD Architecture

- The channels are different from each other which complicates the design
- The architecture is more suited for CT implementations because their inherent AAF could achieve the input filtering. In a DT implementation, input filters are required. Besides, DT resonators have a high power consumption and occupy a large area (section 3.3).

4.1.4 Time interleaved $\Delta\Sigma$ ADC

The block diagram of a Time interleaved (TI) $\Delta\Sigma$ ADC is shown in Fig 4.6 [3] [68][69][70]. It should be noted that the architecture of subsection 4.1.1 is named also TI $\Delta\Sigma$ ADC but for the sake of distinction, the block filtering name was used for it. The analog input signal is first sampled at the Nyquist rate f_s. Then it is distributed among the M channels. Afterwards, the signal in each channel is interpolated by a factor N. This operation is performed by adding N-1 zeros between each two signal samples. The interpolation operation permits to have the oversampling ratio needed for $\Delta\Sigma$ modulators that are clocked at a rate f_{op}, N/M times faster than f_s. At the digital back-end, the $\Delta\Sigma$ modulator outputs are filtered by low-pass filters to eliminate the out-of-band quantization noise and then decimated by a factor N and multiplexed allowing thereby the signal reconstruction. The advantages and disavantages of the TI $\Delta\Sigma$ architecture are:
Advantages:

- All the channels are identical
- The signal demultiplexing at the input is very simple

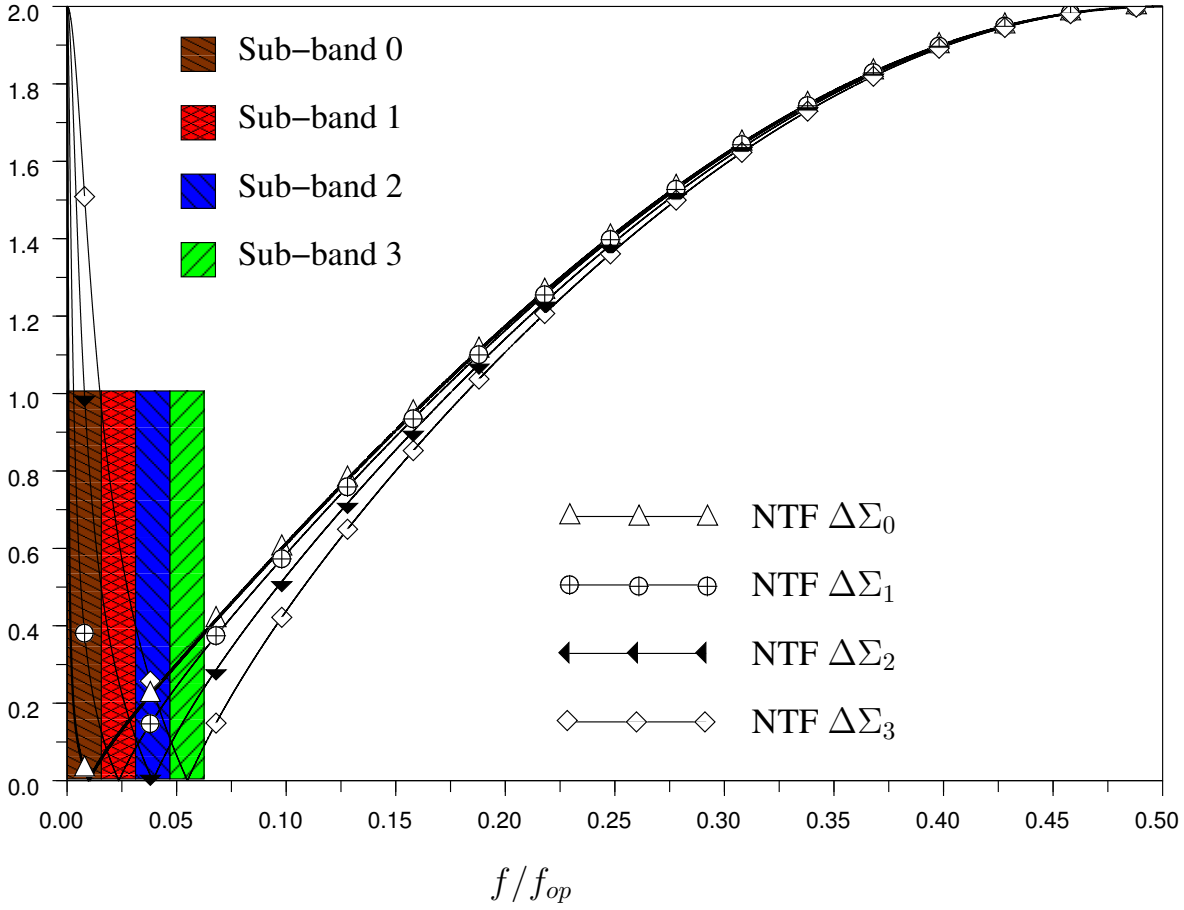


Figure 4.5: ΔΣ modulators' NTFs

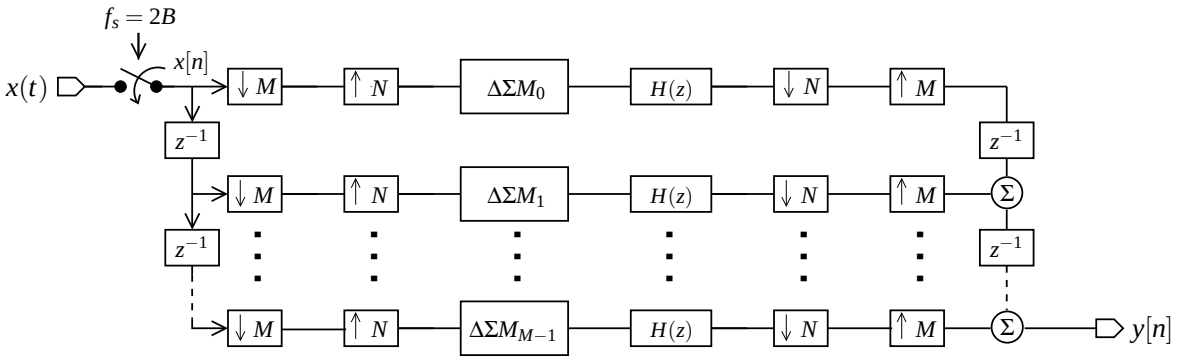


Figure 4.6: TI ΔΣ ADC architecture.

- The signal reconstruction requires reasonable digital resources

Disadvantages:

- High sensitivity to thermal noise
- High sensitivity to channel mismatch

4.1.5 Conclusion

The operation of the four types of parallel $\Delta\Sigma$ ADCs has been presented and their positive and negative points have been discussed. The TI $\Delta\Sigma$ architecture seems to offer the best trade-off between the four architectures. In fact, unlike FBD for which a CT implementation is preferred, the TI $\Delta\Sigma$ ADC is suited for a DT implementation. It uses the same modulator for all channels and requires reasonable digital resources for signal demultiplexing and signal reconstruction. Besides, it does neither put constraints on the modulator's architecture nor on the number of channels as in the block filtering architecture. Furthermore, TI $\Delta\Sigma$ ADCs offer various possibilities of reconfiguration which is a main concern in our design.
The two main drawbacks of TI $\Delta\Sigma$ ADC are its sensitivity to thermal noise and to channel mismatch. In the following two sections, these drawbacks will be discussed and solutions to overcome them will be proposed.

4.2 Time interleaved ΔΣ ADC with novel interpolation technique

4.2.1 Classical Time interleaved ΔΣ ADC

Before discussing the thermal noise problem of the Time interleaved ΔΣ ADC, let us first explain in details the operation of this architecture.

4.2.1.1 Signal transfer function of the Time interleaved ΔΣ ADC

The STF of a DT ΔΣ modulator is commonly a delay that can take any value between zero and the modulator order L depending on its architecture. For sake of simplicity, let us consider in a first time that the STF of the ΔΣ modulator is unitary. The architecture of the TI ΔΣ ADC seen by the useful signal will then become as in Fig. 4.7.

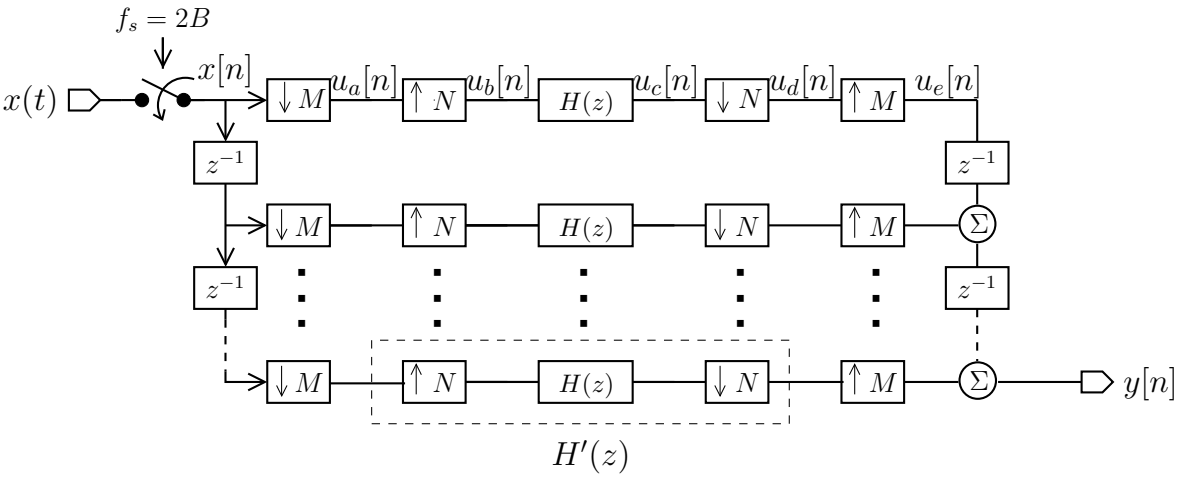


Figure 4.7: TI ΔΣ ADC architecture.

In order to determine the overall transfer function of the architecture, let us first determine the expression of $H'(z)$ that corresponds to a interpolator by a factor N followed by the the filter $H(z)$ and a decimator by N.
$U_b(z)$ is obtained by a interpolation by N of the signal $U_a(z)$. Its expression can be determined by applying to $U_a(z)$ the $z \Longrightarrow z^N$ transformation.

$$U_b(z) = U_a(z^N) \tag{4.1}$$

$$U_c(z) = U_a(z^N)H(z) \tag{4.2}$$

The output of the filter $U_c(z)$ is decimated by N. Its expression is then given by:

$$U_d(z) = \frac{1}{N}\sum_{i=0}^{N-1} U_c(z^{\frac{1}{N}}W_N^i) \qquad with \;\; W_N = e^{-j\frac{2\pi}{N}} \tag{4.3}$$

The terms W_N^i correspond to the aliasing due the decimation operation.

$$U_d(z) = \frac{1}{N}U_a(z)\sum_{i=0}^{N-1} H(z^{\frac{1}{N}}W_N^i) \tag{4.4}$$

The expression of $H'(z)$ is then:

$$H'(z) = \frac{U_d(z)}{U_a(z)} = \frac{1}{N}\sum_{i=0}^{N-1} H(z^{\frac{1}{N}} W_N^i) = \frac{1}{N}\sum_{i=0}^{N-1}\sum_{j=-\infty}^{\infty} h[j] z^{-\frac{j}{N}} W_N^{-ij} \tag{4.5}$$

By inverting the two sums, $H'(z)$ becomes:

$$H'(z) = \sum_{j=-\infty}^{\infty} h[j] z^{-\frac{j}{N}} \underbrace{\frac{1}{N}\sum_{i=0}^{N-1} W_N^{-ij}}_{C_N[j]} \tag{4.6}$$

The sequence $C_N[j]$ fulfils the following:

$$C_N[j] = \frac{1}{N}\sum_{i=0}^{N-1} W_N^{-ij} = \begin{cases} 1 & \text{if } j \text{ is multiple of } N \\ 0 & \text{if not} \end{cases} \tag{4.7}$$

Based on equations 4.6 and 4.7, it can be concluded that the coefficients of $h[n]$ that interfere in the useful signal processing are those whose indices is a multiple of N. Therefore, to ensure that the input signal is not deformed, the impulse response of the filter must fulfil the following condition:

$$h[j] = \begin{cases} 1 & \text{if } j = 0 \\ 0 & \text{if } j \text{ is a multiple of } N \end{cases} \tag{4.8}$$

The other terms of $h[n]$ are calculated in order to minimize the quantization noise power at the output of the TI $\Delta\Sigma$ ADC.
If the condition of Eqn. 4.8 is fulfilled, $H'(z)$ becomes unitary. The signal $U_a(z)$ in the i^{th} channel is obtained by decimating a z^{-i} delayed version of the input signal $X(z)$

$$U_{ai}(z) = \frac{1}{M}\sum_{k=0}^{M-1} z^{-\frac{k}{M}} W_M^{-ik} X(z^{\frac{1}{M}} W_M^i) \tag{4.9}$$

Since $H'(z)$=1, $U_{ei}(z)$ is the result of interpolation by M of the signal $U_{ai}(z)$

$$U_{ei}(z) = \frac{1}{M}\sum_{k=0}^{M-1} z^{-k} W_M^{-ik} X(z W_M^i) \tag{4.10}$$

The output of the TI $\Delta\Sigma$ ADC is the sum of the $U_{ei}(z)$ with the corresponding delays

$$Y(z) = \sum_{i=0}^{M-1} z^{-M-1-k} u_{ei}(z) = \sum_{i=0}^{M-1} z^{-M-1-k} \frac{1}{M}\sum_{k=0}^{M-1} z^{-i} W_M^{-ik} X(z W_M^k)$$

$$Y(z) = \frac{1}{M} z^{-(M-1)} \sum_{k=0}^{M-1} X(z W_M^k) \sum_{i=0}^{M-1} W_M^{-ik} = z^{-(M-1)} \sum_{k=0}^{M-1} C_M[k] = z^{-(M-1)} X(z) \tag{4.11}$$

To take into account the STF of the $\Delta\Sigma$ modulator, the term A should be added to the expression of $Y(z)$. It corresponds to the signal delay in the modulators. This delay is identical in all channels and consequently it can be added as in Eqn. 4.12.

$$Y(z) = z^{-(M-1)} \underbrace{z^{-(0 \longrightarrow L)}}_{A} X(z) \tag{4.12}$$

Hence, if the condition of Eqn. 4.8 is fulfilled, the TI $\Delta\Sigma$ ADC will behave as an all-pass filter and no signal aliasing due to the decimation operation will occur.

4.2.1.2 Noise transfer function of the Time interleaved ΔΣ ADC

To evaluate the performance of the TI ΔΣ ADC, let us derive the expression of the quantization noise power after the signal reconstruction. Fig. 4.8 shows the TI architecture as seen by the quantization noise.

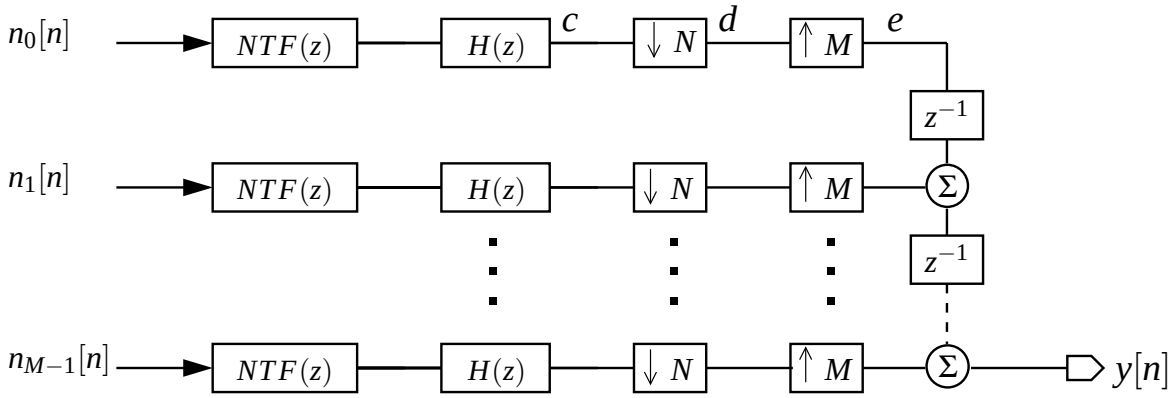


Figure 4.8: TI ΔΣ ADC architecture.

If the quantization noise $N_i(z)$ is supposed white, its PSD at the output of the ΔΣ modulator is given by:

$$PSD_{\Delta\Sigma M}(e^{jw}) = \frac{q^2}{12 f_{op}} \mid NTF(e^{jw}) \mid^2 \tag{4.13}$$

After the filtering operation, its PSD becomes:

$$PSD_c(e^{jw}) = \frac{q^2}{12 f_{op}} \mid NTF(e^{jw}) \mid^2 \mid H(e^{jw}) \mid^2 \tag{4.14}$$

The decimation by N yields:

$$PSD_d(e^{jw}) = \frac{q^2}{12 f_{op} N} \sum_{i=0}^{N-1} \mid NTF(e^{\frac{jw}{N}} W_N^i) \mid^2 \mid H(e^{\frac{jw}{N}} W_N^i) \mid^2 \tag{4.15}$$

The decimated signal is then interpolated by M to allow the signal multiplexing at the output.

$$PSD_e(e^{jw}) = \frac{q^2}{12 f_{op}} \frac{1}{MN} \sum_{i=0}^{N-1} \mid NTF(e^{\frac{jwM}{N}} W_N^i) \mid^2 \mid H(e^{\frac{jwM}{N}} W_N^i) \mid^2 \tag{4.16}$$

The quantization noise power of each channel can be calculated by integrating the PSD

$$P_e = \frac{1}{2\pi} \frac{q^2}{12} \frac{1}{MN} \sum_{i=0}^{N-1} \int_{-\pi}^{\pi} \mid NTF(e^{\frac{jwM}{N}} W_N^i) \mid^2 \mid H(e^{\frac{jwM}{N}} W_N^i) \mid^2 \; dw \tag{4.17}$$

If the quantization noise sources are assumed to be uncorrelated, the overall quantization noise power is then given by:

$$P_Q = M \times P_e = \frac{1}{2\pi} \frac{q^2}{12} \frac{1}{N} \sum_{i=0}^{N-1} \int_{-\frac{\pi}{N}}^{\frac{\pi}{N}} \mid NTF(e^{\frac{jwM}{N}} W_N^i) \mid^2 dw \tag{4.18}$$

If it is assumed that $H(z)$ is an ideal low pass filter with a cut-off frequency of $\frac{f_{op}}{2N}$ and that $NTF_{\Delta\Sigma M} = (1 - z^{-1})^L$, P_Q is then given by:

$$P_Q \approx \frac{1}{2L+1}\frac{q^2}{12}\frac{1}{N}(\frac{\pi}{N})^{2L} \tag{4.19}$$

For a n bits quantizer, the expression of P_Q becomes:

$$P_Q(f) \approx \frac{\pi^{2L}}{(2L+1)N^{2L+1}}\frac{Vref^2}{2^{2n-2}12} \tag{4.20}$$

Comparing Eqn. 3.7 and Eqn. 4.20, it can be noted that the theoretical resolution of a TI $\Delta\Sigma$ ADC is identical to a single channel $\Delta\Sigma$ while converting a M times larger bandwidth.

4.2.1.3 Digital filter

An optimal filter topology which fulfils the perfect reconstruction constraints (4.8) is proposed in [4]. As mentioned earlier, the other coefficients not expressed in (4.8) are calculated in order to minimize the quantization noise power at the output of the TI $\Delta\Sigma$ ADC. It has been shown in [71] that a 310^{th} order optimal low-pass filter is required to reach an SNDR of 81 dB. This filter length requires the implementation of 155 multiplications and 300 additions operating at the operating frequency f_{op}. This is a very huge computing resource requirement.

In order to reduce hardware complexity, a new digital reconstruction method based on Comb-filters was proposed in [71]. The Comb-filters can operate at high sampling rates while minimizing hardware complexity. The transfer function $C(z)$ of a Comb-filter is defined by :

$$C(z) = \left(\frac{1}{N}\sum_{i=0}^{N-1} z^{-i}\right)^{K_f} = \left(\frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}}\right)^{K_f} \tag{4.21}$$

where K_f is the order of the Comb-filter

According to Eqn. 4.21, a Comb-filter can be efficiently implemented using only integrators and differentiators as shown in Fig. 4.9. However, its impulse response does not satisfy the

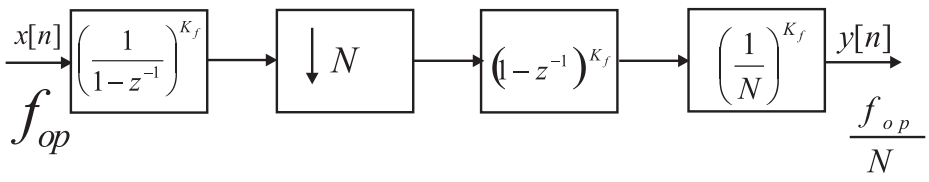


Figure 4.9: Comb-filter architecture.

perfect reconstruction conditions in (4.8). The overall output signal component is not a delayed version of the input signal. It is a filtered version as shown in the following equation:

$$Y_x(z) = H'(z^M)z^{-(M-1-L)}X(z) \tag{4.22}$$

where

$$H'(z) = \sum_{i=d}^{J} h_c\,[iN]\,z^{-i} \quad \text{with} \quad JN \leq L \tag{4.23}$$

with $h_c[n]$ is the impulse response of the Comb-filter and d the decimation delay of the impulse response $h_c[n]$.

The filtering effect ($H'(z^M)$) appears as equiripples on the magnitude of the output spectrum. To correct this effect, an equalization filter $Eq(z)$ is applied at the output of the TI ΔΣ ADC based on a least mean square (LMS) FIR filter. The order of this equalization filter depends on the equiripple magnitudes introduced by $H'(z^M)$ and the equiripple magnitude depends on both the order of the Comb-filter and on the decimation delay d. It has been shown in [71] that, for a L^{th} order ΔΣ modulator , the optimal Comb-filter order reducing aliasing terms (due to the decimation) and equalization filter complexity must be the first even number higher than $L+1$ with zero delay.

Fig. 4.10 shows the magnitude response of $H'(z^M)$, $Eq(z)$ and the result of equalization. For a 6^{th} order Comb-filter, the ripple magnitude is about 14 dB so a 30^{th} order equalization filter is enough to equalize ripples with a maximum error of 3×10^{-4} dB. While for a 2 dB inband ripple magnitude, a 10^{th} order equalization filter is enough.

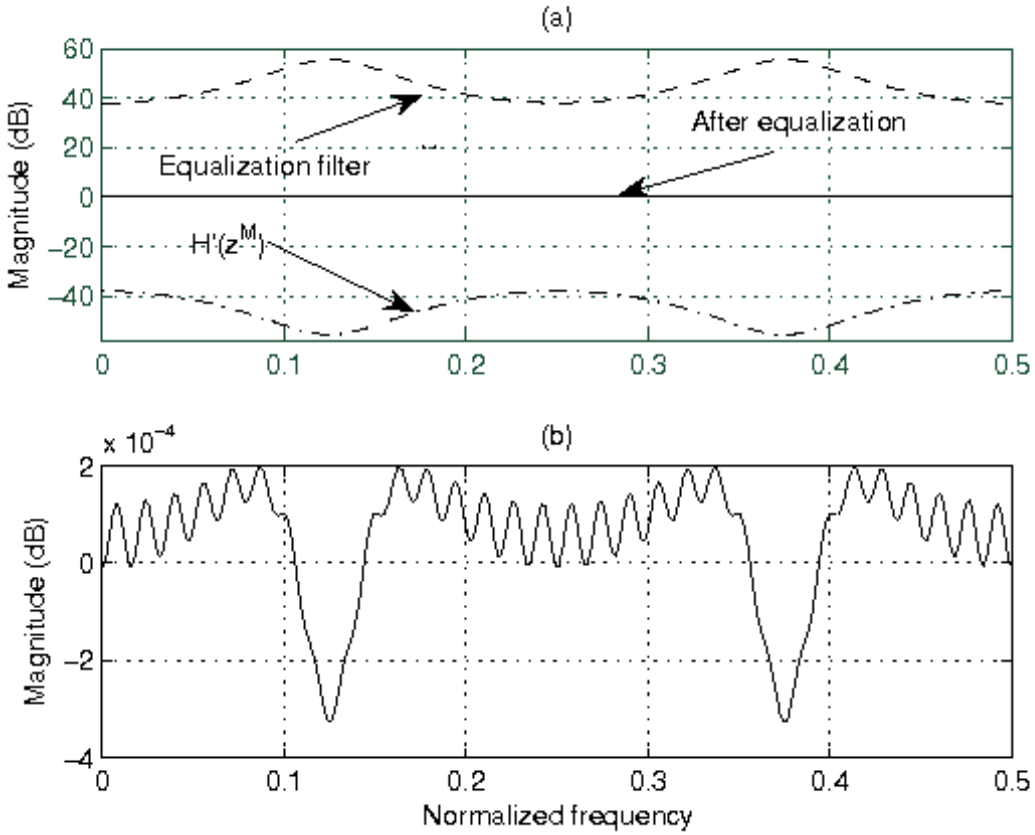


Figure 4.10: (a) Magnitude of $H'(z^M)$ transfer function and equalization filter $Eq(z^M)$ (b) zoom of the magnitude error.

4.2.1.4 Analog front-end implementation

Fig. 4.11 shows one way to implement the frond-end of a TI ΔΣ ADC using switched capacitor technology [14]. For the sake of simplicity, a single-ended representation is illustrated. In Fig. 4.11, the S/H and 1^{st} channel analog multiplexer and 1^{st} integrator are illustrated. The S/H was placed before all channels to avoid clock-skew. The choice of this solution will be

discussed in the following section.

One of the characteristics of the TI $\Delta\Sigma$ ADC is the capacity to perform a Nyquist conversion. However, in high resolution applications, it requires very high value of sampling capacitors because the thermal noise must be lower than the quantization noise defined by the converter resolution. In fact, the sampling capacitor $C_{sS/H}$ of the S/H and C_{sI} of the 1^{st} integrator are sized to get the thermal noise level lower than the expected resolution. Let SNR_{th} be the required signal to thermal noise ratio for the converter, P_s the signal power and P_{th} the thermal noise power, then

$$10Log(\frac{P_s}{P_{th}}) = SNR_{th} \tag{4.24}$$

where

$$P_{th} = \frac{4.K_{Bol}T}{C} (4.25) \qquad P_s = \frac{A^2}{2} (4.26)$$

with K_{Bol} the Boltzman constant, T the temperature in Kelvin and with A the sinusoidal input signal amplitude.
This give us :

$$C_{sS/H} = \frac{8K_{Bol}T.10^{SNR_{th}/10}}{A^2} \tag{4.27}$$

At the input of the $\Delta\Sigma$ modulator, the signal is oversampled by a factor N and if the digital filter removes the out of band noise without any amplification, the effective thermal noise power will be then reduced by a factor N. On the other hand, since the interpolation is performed by adding zeros, and the digital filter has no amplification gain, the signal power is decreased by N also.

$$P_{th} = \frac{4.K_{Bol}T}{C.N} (4.28) \qquad P_s = \frac{A^2}{2.N} (4.29)$$

It results in

$$C_{sI} = \frac{8K_{Bol}T.10^{SNR_{th}/10}}{A^2} \tag{4.30}$$

For example, for a 2 channels scenario with an input signal amplitude of 0.6 Vp and a thermal SNR budget of 83 dB at 300 Kelvin, the required sampling capacitors are 18 pF which occupy an unreasonable die area.

4.2.2 The proposed interpolation technique

4.2.2.1 Principle

In order to overcome the disadvantages of classical TI $\Delta\Sigma$ ADC, a new solution is proposed which consists of oversampling the input signal of the bank of modulators at the operation frequency $f_{op} = \frac{N}{M} f_s$, where f_s is the Nyquist sampling frequency. Then, extra samples behind each "Nyquist sample" (obtained with Nyquist sampling rate) will be used instead of zeros in the interpolation by a factor N. The added extra samples will increase the signal power and consequently allow to reduce the sampling capacitor size while maintaining the same signal power to thermal noise power ratio.

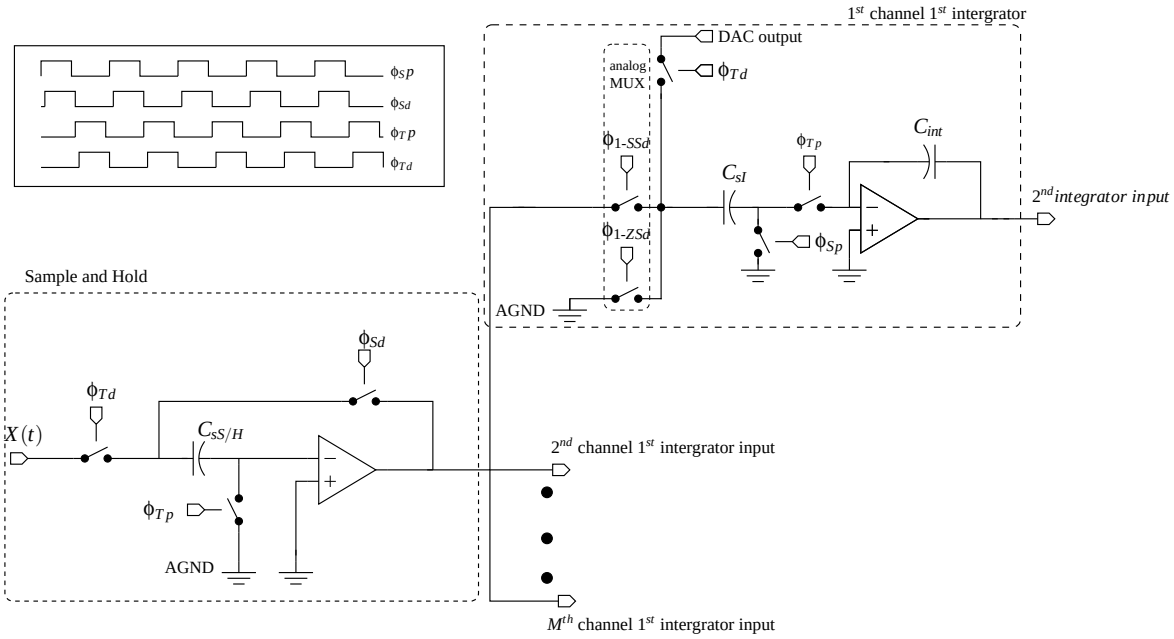


Figure 4.11: TI ΔΣ ADC circuit front-end.

The number of inserted samples N_s at each channel varies between 0 and $N-1$. Fig. 4.12 demonstrates the new interpolation technique with $M=2$, $N=12$ and $N_s=K-1$ where K is the ratio defined by $K=\frac{N}{M}$. The dashed vertical lines represent the samples obtained at the Nyquist rate ("Nyquist samples") and multiplexed in time between the two channels. The sampling at f_{op} (Fig. 4.12 a)) creates $(K-1)$ extra samples between two adjacent "Nyquist samples" (5 in this example). The interpolation with the classical technique is performed by inserting $N-1$ zeros between "Nyquist samples" at the input of the modulator (Fig. 4.12 b)). While, the interpolation with the proposed technique uses the $K-1$ extra samples after each "Nyquist sample" and completes the rest with zeros to reach the $N-1$ values to perform the interpolation by N (Fig. 4.12 c) and d)).
As it will be shown during this section, this distribution of the extra samples has the advantage of cancelling the signal aliasing due to the decimation operation. This characteristic is very important for the digital signal reconstruction operation.

To evaluate the theoretical performance, Fig. 4.13 presents the equivalent mathematical model of the TI ΔΣ ADC using the proposed interpolation technique. The transfer function $F_i(z)$ presents the effect of the new interpolation on the input signal $X(z)$ in the i^{th} channel before the ΔΣ modulator. Fig. 4.15 shows in details the structure of $F_i(z)$ where N_s samples are used. For the example presented in Fig. 4.12, Fig. 4.14 shows the different steps to build the signal of the first channel. Based on this simple example, we can define the general form of $F(z)$ for the i^{th} channel as presented in Fig. 4.15.

First, let us express the output $Y_1(z)$ of the transfer function $F_i(z)$. The transfer function is composed of N_s channels. In each channel, an appropriate delay is applied to the input signal before being decimated and interpolated by N. Then, another delay is applied to each channel before reconstructing the output signal. The different intermediate signals and the

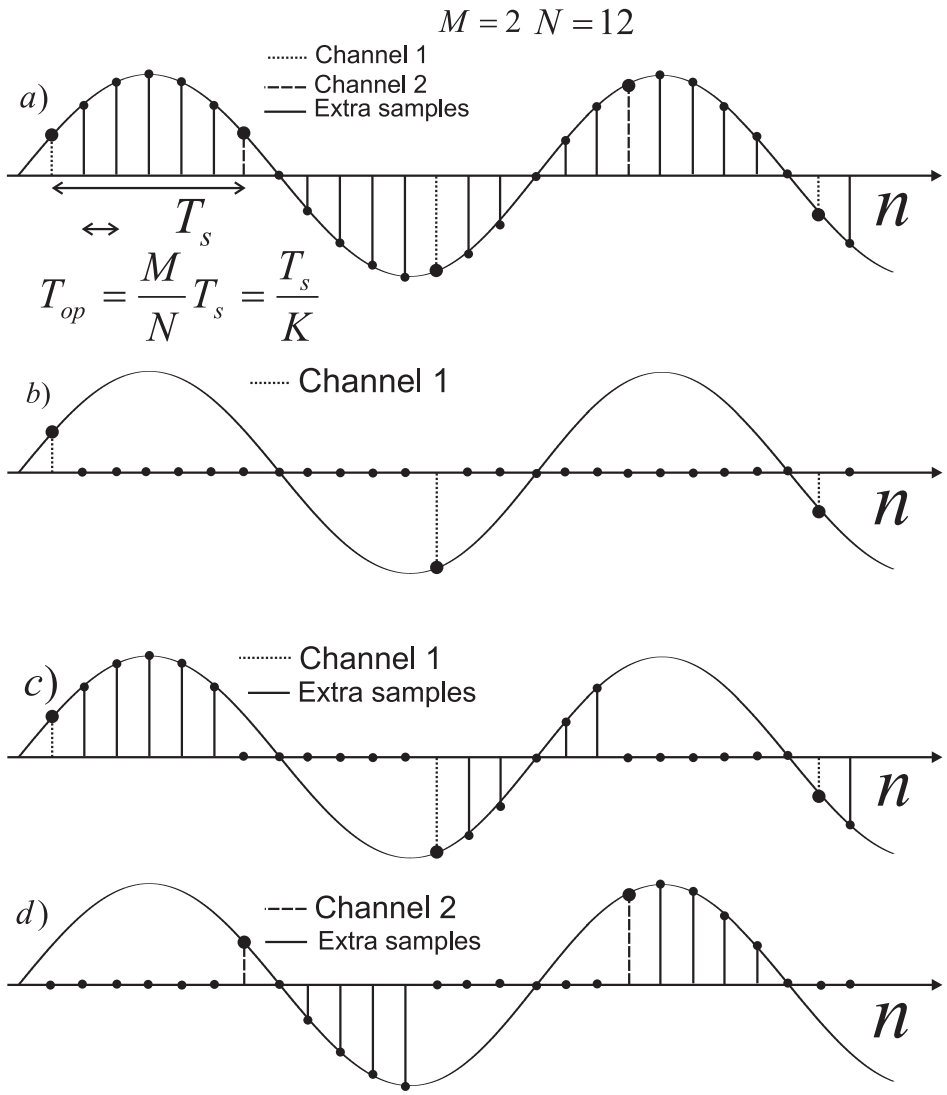


Figure 4.12: Example illustrating the new interpolation technique. a) input signal sampled at the operation frequency f_{op}, b) input signal at channel 1 with the interpolation by zeros, c),d) input signals at the channels 1 and 2 with the new interpolation technique with $N_s = K$ extra samples.

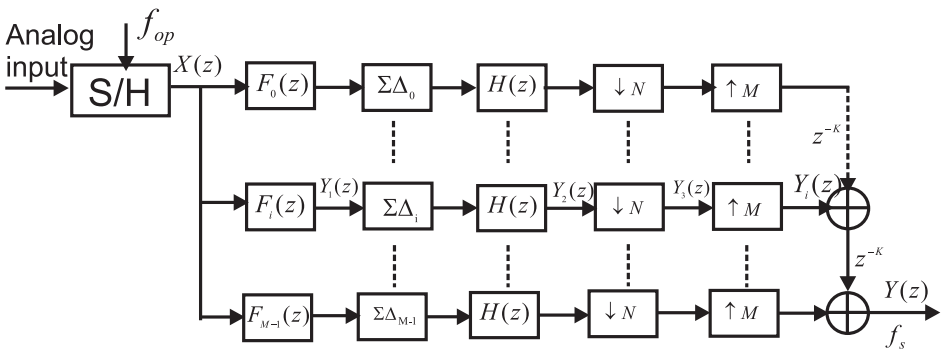


Figure 4.13: Mathematical model of the TI ΔΣ architecture with the new interpolation technique.

output $Y_1(z)$ can be expressed by:

$$\begin{aligned} X_2(z) &= X_1(z)|_{\downarrow N} = \frac{1}{N}\sum_{l=0}^{N-1} X_1(z^{\frac{1}{N}}W_N^l); \quad W_N = e^{-j\frac{2\pi}{N}} \\ &= z^{\frac{-(N-iN_s-j)}{N}}\frac{1}{N}\sum_{l=0}^{N-1} W_N^{-l(N-iN_s-j)}X(z^{\frac{1}{N}}W_N^l) \end{aligned} \tag{4.31}$$

$$\begin{aligned} Y_1(z) &= \sum_{j=0}^{N_s-1} z^{-j}X_3(z) = \sum_{j=0}^{N_s-1} z^{-j}X_2(z^N) \\ &= z^{-(N-iN_s)}\sum_{j=0}^{N_s-1}\frac{1}{N}\sum_{l=0}^{N-1} W_N^{-l(-iN_s-j)}X(zW_N^l) \end{aligned} \tag{4.32}$$

Relying on the linear model of the modulator shown in Fig. 4.6 and assuming that the signal transfer function of the ΔΣ modulator is a pure delay, the useful signal $Y_1(z)$ is filtered by the digital filter $H(z)$ before being decimated by N and interpolated by M. The following expressions describe mathematically these different operations:

$$Y_3(z) = Y_2(z)|_{\downarrow N} = \frac{1}{N}\sum_{p=0}^{N-1} Y_2(z^{\frac{1}{N}}W_N^p) \tag{4.33}$$

$$Y_i(z) = Y_3(z)|_{\uparrow M} = Y_3(z^M) = \frac{1}{N}\sum_{p=0}^{N-1} Y_2(z^{\frac{M}{N}}W_N^p) \tag{4.34}$$

$$Y(z) = \sum_{i=0}^{M-1} z^{-iN_s}Y_i(z) = z^{-M}\sum_{i=0}^{M-1} z^{-(N_s-1)i}\left[\frac{1}{N}\sum_{p=0}^{N-1}\left[W_N^{-p(N-iN_s)}\sum_{j=0}^{N_s-1}\frac{1}{N}\sum_{l=0}^{N-1} W_N^{-l(-iN_s-j)}X(z^{N_s}W_N^{l+p})\right]H(z^{N_s}W_N^p)\right] \tag{4.35}$$

Finally, the expression of the output $Y(z)$ is given by Eqn. 4.35. This equation is very complex. It is thus very difficult to analytically evaluate the impact of the proposed interpolation technique on the overall performance of the converter and the complexity of the digital filter. In order to complete our study, the choice of the Comb-filter on each channel

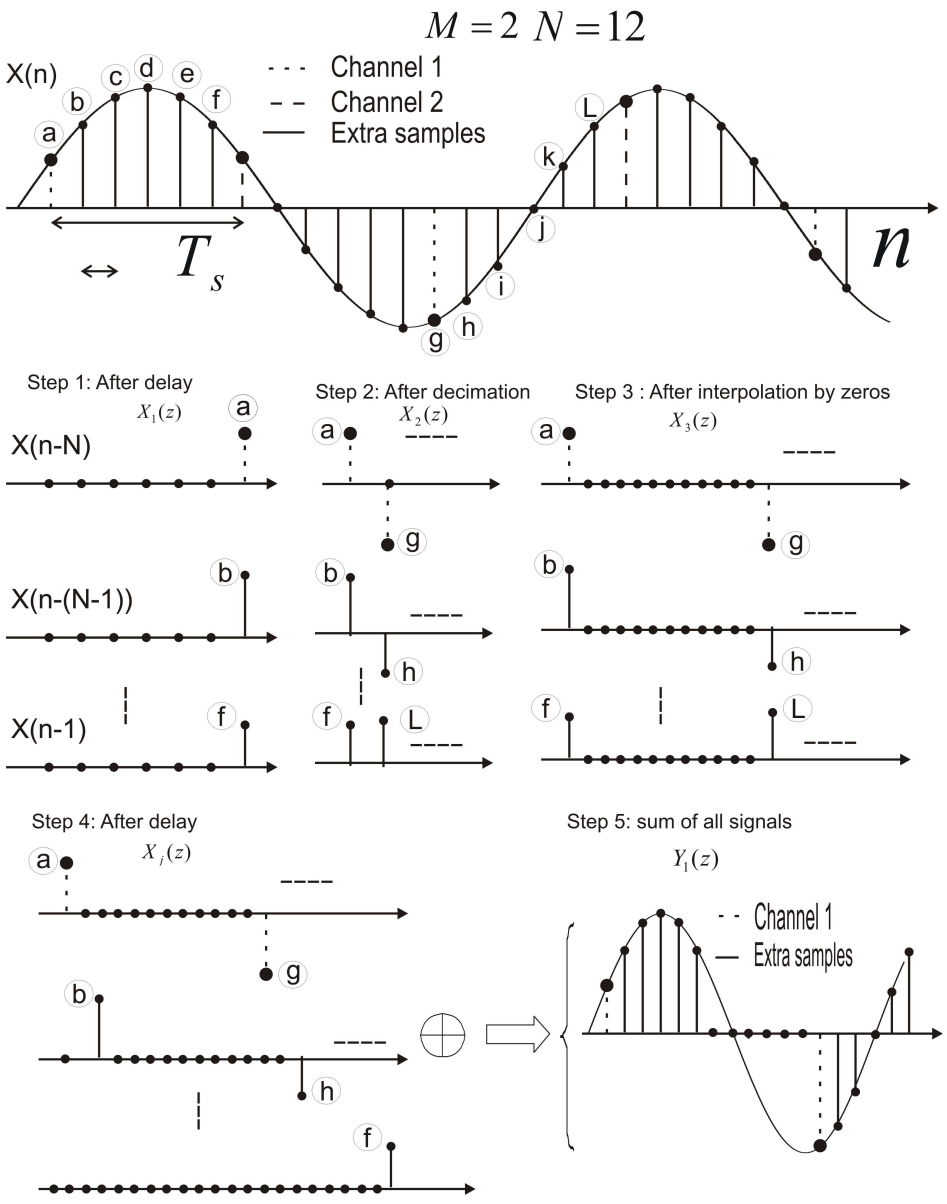


Figure 4.14: The different steps for the construction of the signal of the first channel.

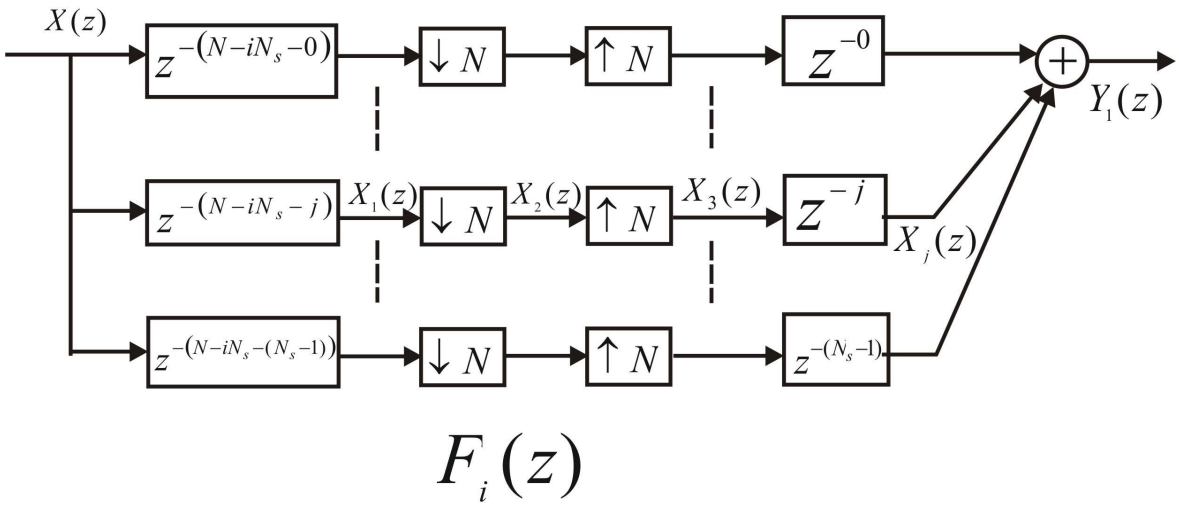


Figure 4.15: Transfer function $F_i(z)$

will be kept due to its implementation simplicity (section 4.2.1.3). Then, simulations will be performed to estimate the impact of the new interpolation on the performance of the whole system and the hardware complexity of the equalization filter $Eq(z)$ at the output.

4.2.2.2 Simulation results

The number of inserted samples N_s controls the dynamic range of the converter, the SNDR and the complexity of the equalization filter which must ensure good equalization of the ripples without introducing a large amplification of the quantization noise.

The main factor controling the performance and the hardware complexity is the ripple magnitude due to filtering effects introduced by the Comb-filters. In fact, the higher the ripple magnitude, the higher the order of the equalization filter and higher the amplification of the quantization noise. To estimate the ripple magnitude, a sine cardinal signal is applied at the input of the TI ΔΣ ADC due to its constant power spectral density throughout the useful band. A 4 channel TI ΔΣ ADC with an interpolation factor of 80 is considered to perform system simulations.

Fig. 4.16 shows the PSD of the signal $X(z)$ sampled at the frequency f_{op}. Fig. 4.17 shows the PSD of the signal $Y(z)$ for different values of N_s and Fig. 4.18 shows the ripple magnitude with respect to the number of inserted samples N_s for two different values of interpolation factor N. It can be noticed that :

- the ripple magnitude reaches its maximum value for N_s equal to $\frac{N}{2} - 1$ and $N - 1$,
- the maximum value for N_s increasing the power of the useful signal with no large ripple magnitude is equal to $K - 1$. This implies that the optimal case is first to perform the interpolation in each channel by adding extra samples resulting from oversampling until the next "Nyquist sample" dedicated to the adjacent channel, then, to continue the interpolation by adding zeros (Fig. 4.12 c)).

It must be noted also that the new interpolation technique increases the power of the useful signal in each channel and may saturate the integrators inside the ΔΣ modulator. Fig. 4.19

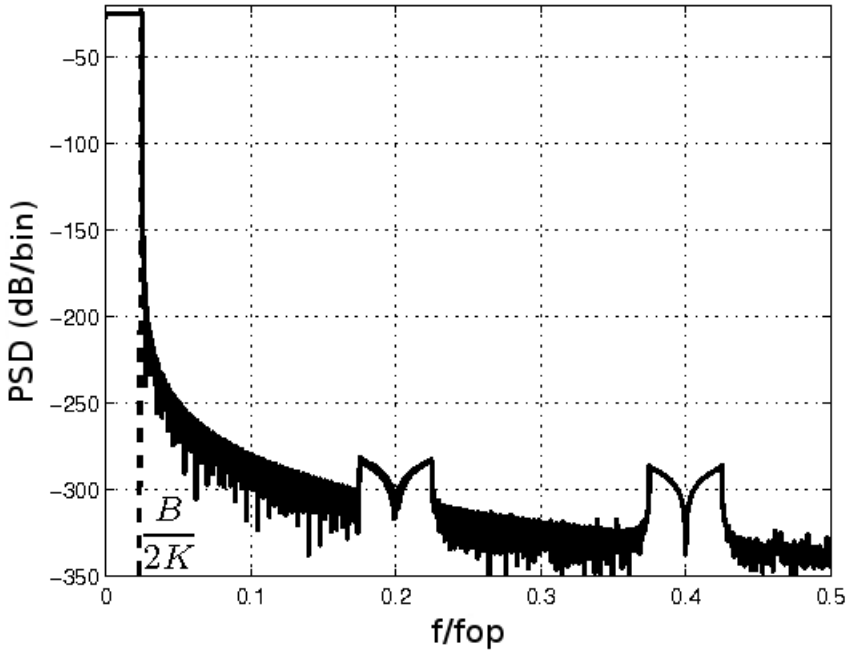


Figure 4.16: Power Spectral Density of the input signal sampled at f_{op}.

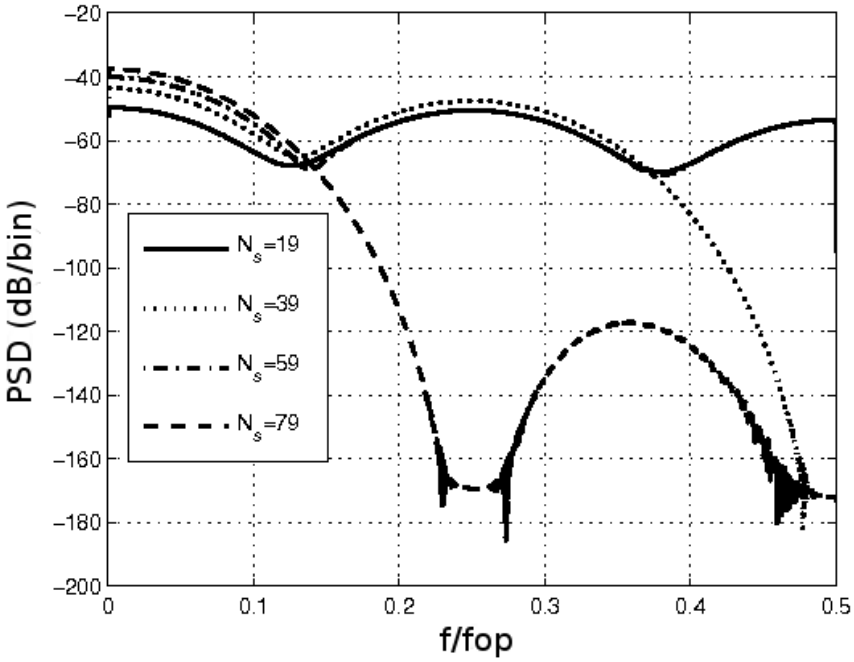


Figure 4.17: PSD at the output for different values of N_s with a sine cardinal signal at the input.

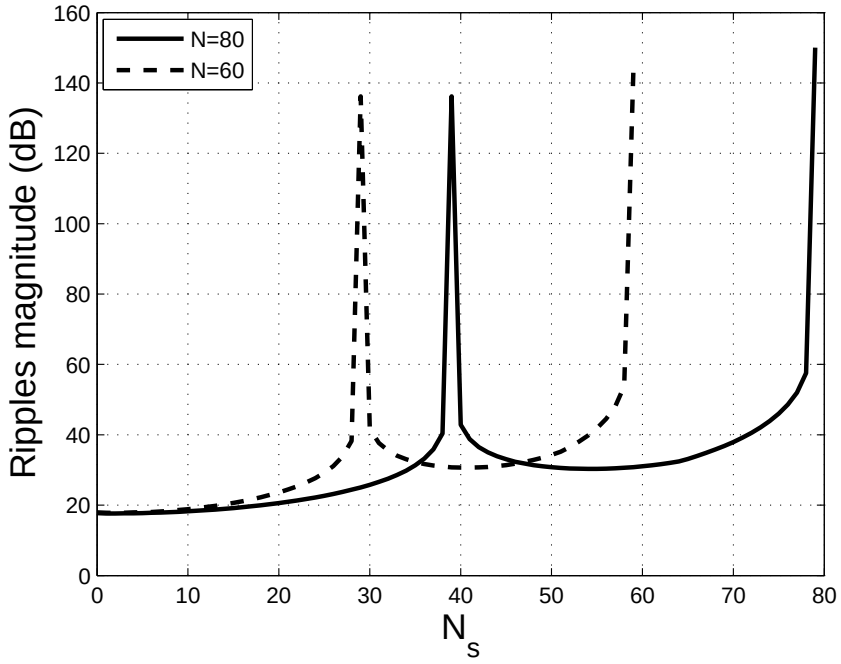


Figure 4.18: Ripple magnitude on the PSD at the output respect to N_s for the two interpolation factor $N = 80$ and $N = 60$.

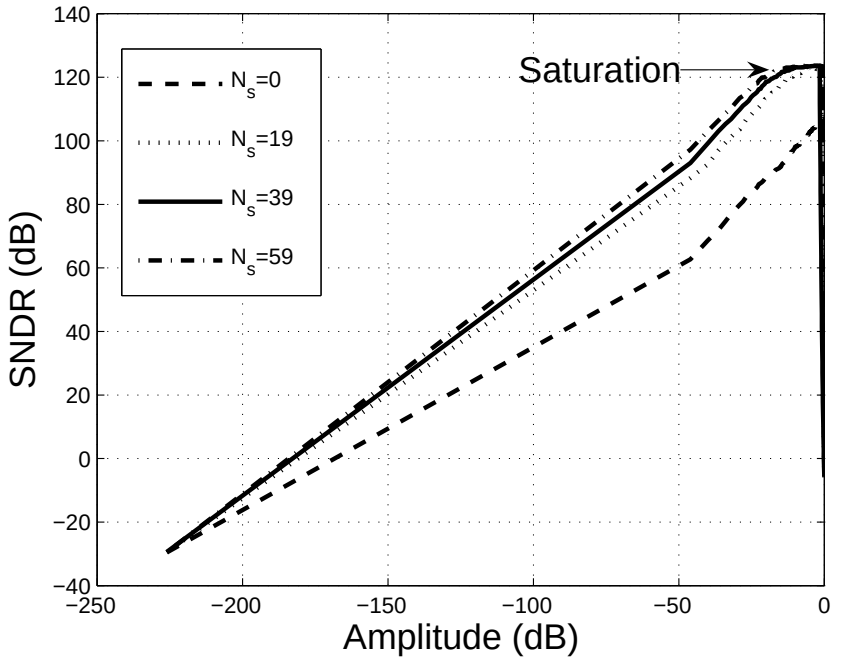


Figure 4.19: SNDR with respect to the input signal magnitude for different inserted samples.

shows the SNDR with respect to the amplitude of the input signal for different values of inserted samples N_s.

The value $N_s = 0$ corresponds to the case of interpolation technique by zeros. It can be easily noted that interpolating with extra samples improves the SNDR. This result is expectable beacuse increasing N_s increases the useful signal power and consequently the SNDR. However, inceasing N_s increases also integrators' swings and thus the maximum stable amplitude is reduced.
To avoid this problem, a decrease of the integrators' coefficients could ensure a linearly dynamic range and maintain the expected maximum SNDR. Fig. 4.20 shows the SNDR compared to the input signal magnitude for different values of N_s with two sets of integrator gains. The set with lower integrator gain allows a wide linear dynamic range at the cost of a slight decrease in the SNDR.

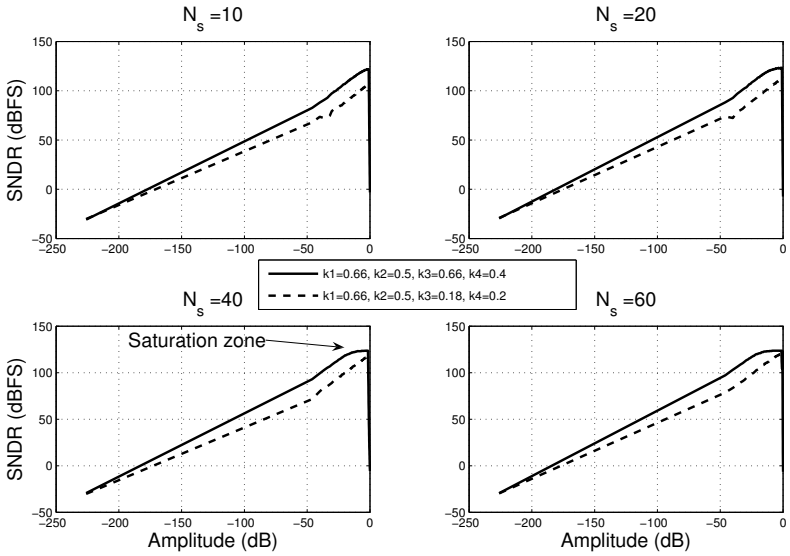


Figure 4.20: SNDR with respect to the input signal magnitude for different inserted samples with two sets of gain integrator.

4.2.2.3 Equalization filter complexity

After determining that the optimal number of inserted samples N_s is equal to $K - 1 = \frac{N}{M} - 1$, let us estimate the complexity of the equalization filter. Indeed, the equalization filter equalizes the filtering effect introduced by the Comb-filter whereas it amplifies the quantization noise at the output leading to a small loss of the SNDR. An inband ripple magnitude of 2 dB is tolerated. So, the optimal order of the equalization filter must ensure magnitude ripples lower than this value without large amplification of the quantization noise. Fig. 4.21 shows the SNDR and the magnitude ripples with respect to the equalization filter length. The SNDR was estimated using a sine signal at the input located at the frequency for which the attenuation introduced by the filtering effect reaches its maximum value. It can be noticed that a 30^{th} order equalization filter is sufficient to have magnitude ripples less than 2 dB and an SNDR of 95 dB.

To illustrate the equalization filter effect, Fig. 4.22 shows the power spectral densities at the output, before and after equalization, while considering a sine wave signal at the input at

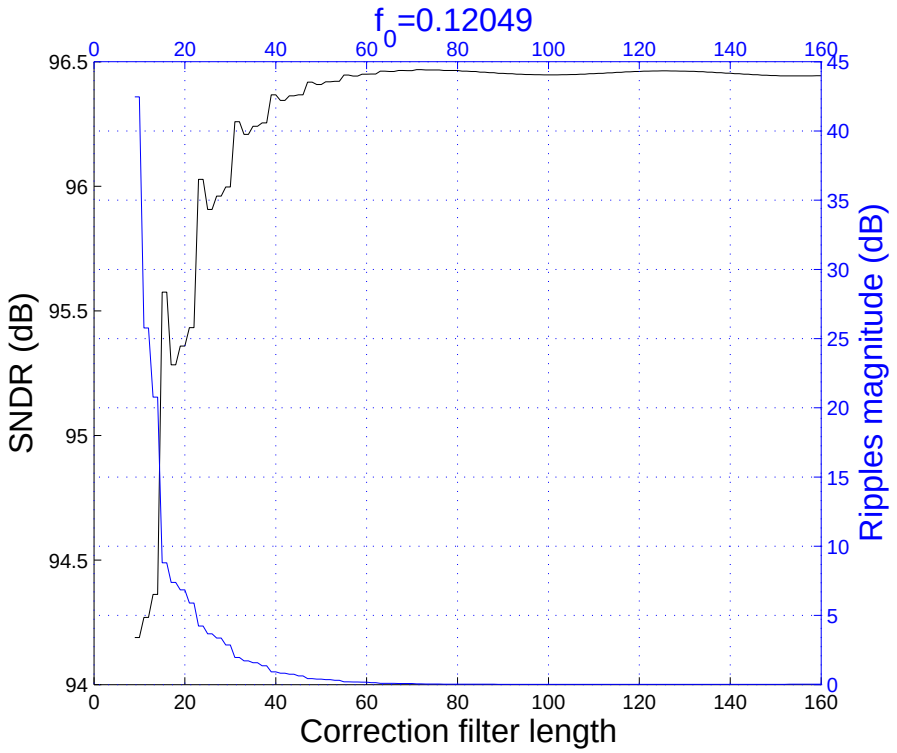


Figure 4.21: SNR and magnitude ripples after equalization compared to equalization filter length.

the normalized frequency f_0.
It can be noticed that :

- for a low normalized frequency ($f_0 = 0.02$) the SNDR before equalization is equal to 111 dB. There is no attenuation at low frequencies by the filtering effect and thus the expected SNDR is maintained. After the equalization filter, the SNDR is reduced to 96 dB because the equalization filter does not amplify the useful signal while amplifying the quantization noise.
- for the normalized frequency $f_0 = 0.12$, the SNDR before equalization is equal to 94 dB. This is because the attenuation introduced by the filtering effect reaches its maximum value at this frequency. The SNDR will be slightly improved to 95.5 dB after the equalization filter. In this case, the equalization filter amplifies the useful signal and the quantization noise at the same time that regaining the useful signal amplitude and introducing a slight improvement of the SNDR.
- after the equalization filter, the SNDR is almost constant (96 dB) regardless of the frequency of the input signal.

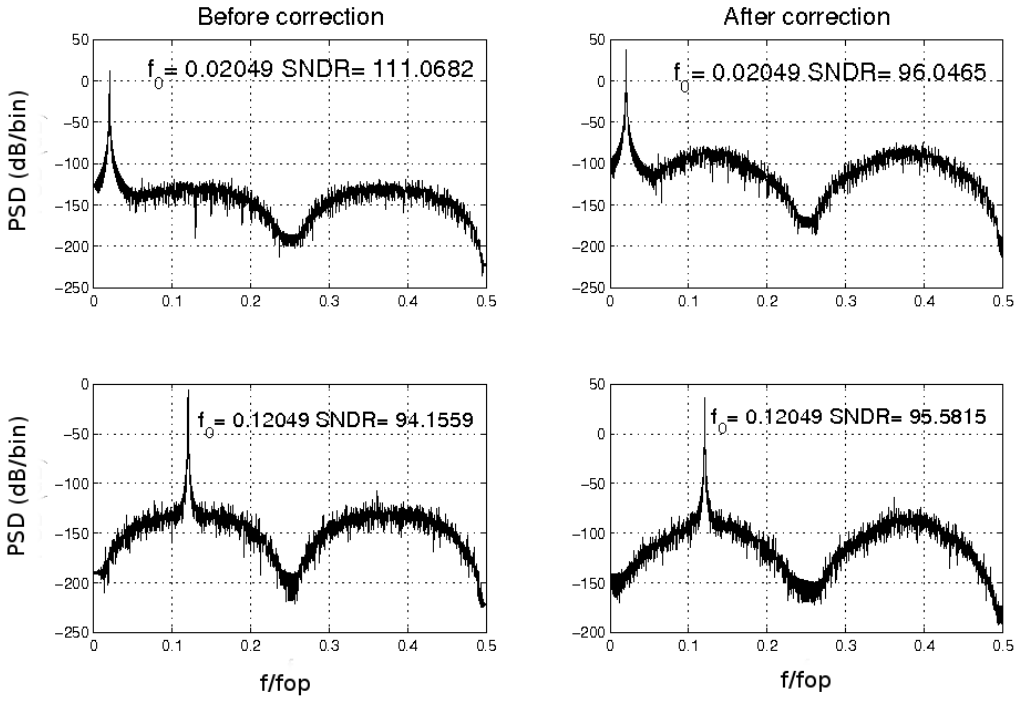


Figure 4.22: Power spectral density at the output before and after equalization with a sine signal at the input.

4.2.2.4 Choice of the operation frequency of the S/H

With the new interpolation technique, Eqns 4.25 and 4.29 become respectively :

$$P_{th} = \frac{4K_{bol}T}{C\frac{f_{S/H}}{f_s}} \tag{4.36}$$

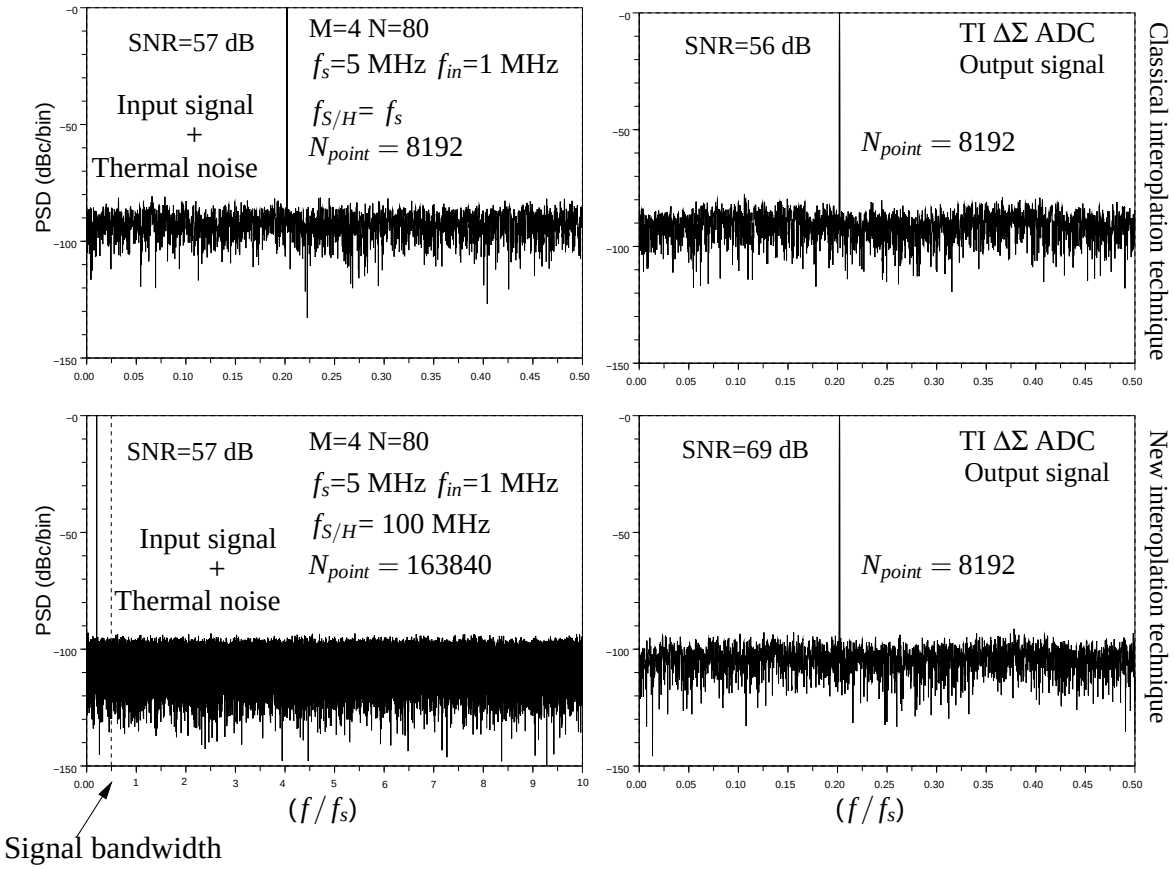


Figure 4.23: Classical interpolation technique vs new interpolation technique

$$P_s = \frac{A^2}{2.N}\frac{f_{S/H}}{f_s} \tag{4.37}$$

Where $f_{S/H}$ is the operation frequency of the S/H.

Since the S/H power signal (Eqn. 4.26) and the integrator thermal noise power (Eqn. 4.28) remain the same, the capacitor size for both of them can be divided by $\frac{f_{S/H}}{f_s}$ (which is equal to K if $f_{S/H} = f_{op}$) while maintaining the same signal to thermal noise ratio.

Fig. 4.23 shows a comparison between the classical interpolation technique and proposed technique. It was made in sort for both simulations that the thermal noise dominates the quantization noise. As it can be seen, when using the classical method, the SNR is the same at the ADC input and output. However, with the new interpolation technique, the SNR is increased by 12 dB $\approx 10Log(\frac{\overbrace{100\ \text{MHz}}^{f_{S/H}}}{\underbrace{5\ \text{MHz}}_{f_s}}) = 10Log(\frac{\overbrace{80}^{N}}{\underbrace{4}_{M}}) =$ 13.01 dB.

The new interpolation technique has been exposed for a rise of the sampling frequency from f_s to f_{op}. However, sampling at such a high frequency as f_{op} may amplify the constraints on S/H components such as the switches and the OTA. Therefore, other S/H sampling frequencies can be considered. Fig. 4.24 shows the proposed interpolation technique for a sampling frequency of $f_{op}/2$. In this case, since the sampling operation requires $2T_{op}$, the number of available extra samples between two "Nyquist samples" will be reduced compared to the case where the sampling frequency is f_{op}. The interpolation by N is performed by using

the available extra samples between two "Nyquist samples" and by inserting the appropriate number of zeros to achieve an increase of the data rate by N factor (see Fig. 4.24).

In this case, the signal power increase and consequently the sampling capacitor decrease will not be as high as when sampling at f_{op} but it could relax the constraints design of S/H. These constraints do not increase as it can be supposed with $f_{S/H}$ increase. In fact, each time $f_{S/H}$ is multiplied by a certain factor, the sampling capacitors can be divided by the same factor while maintaining the same signal to thermal noise ratio. Consequently, the OTA slew rate and gain bandwidth will be almost multiplied by the same factor and therefore their ratio to $f_{S/H}$ will remain unchanged. As a consequence, the distortions generated due to settling error will also remain unchanged [72]. While thermal, flicker and other noises preserve the same impact and even for some of them the impact is reduced when $f_{S/H}$ increases due to the fact that out of band noise is eliminated by the $\Delta\Sigma$ decimation filter[73]. Nevertheless, some problems due to OTA's parasitic capacitances and to switch non-idealities increases with $f_{S/H}$ increase and therefore the optimal $f_{S/H}$ may be different than f_{op}.

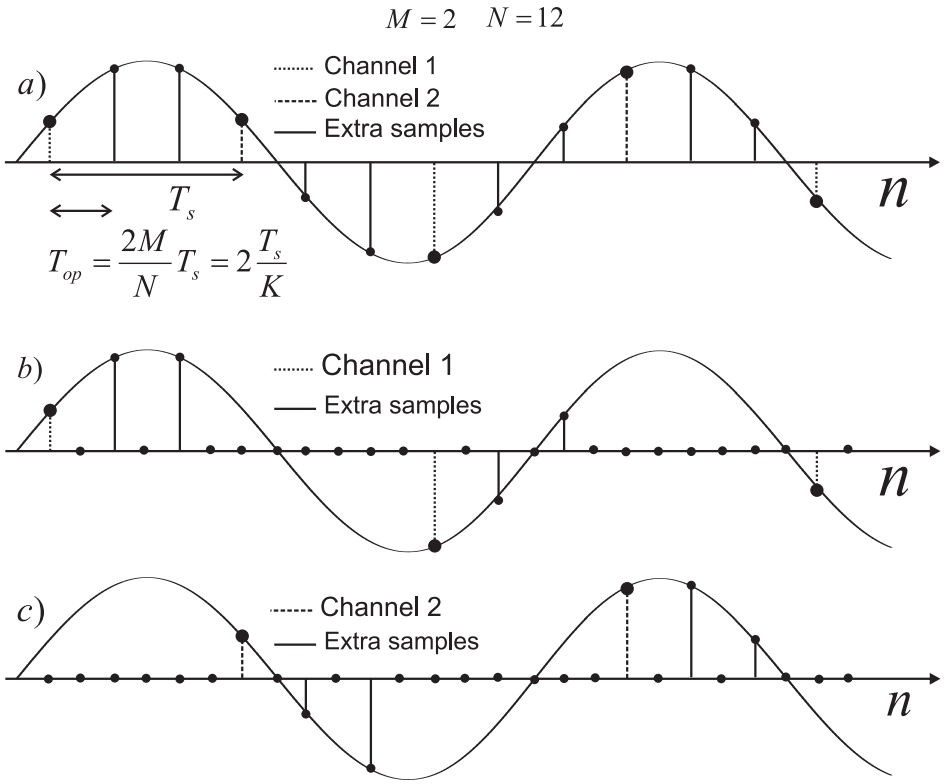


Figure 4.24: Example illustrating the new interpolation technique. a) input signal sampled at the operation frequency $f_{op}/2$, b),c) input signals at the channels 1 and 2 with $N_s = K/2$.

Another important advantage of this novel interpolation technique is reducing the complexity of the anti-alias filter (AAF). In order to show this complexity reduction, let us consider the digitization of a UMTS channel using a Zero-IF architecture. The spectrum of the useful signal and of the adjacent channels at the input of the A/D converter are shown in Fig. 4.25. If the classical technique is employed, the adjacent channels will alias inside the useful band and thus their amplitude after filtering should be lower than the quantum of the A/D converter. Therefore, we should have:

$$P_{block} < P_{signal} - ADC_{res}$$

Where P_{block} is the power in dB of the blockers after filtering , P_{signal} the power in dB of the useful signal and ADC_{res} is the targeted resolution in dB
In the considered scenario, to fulfill this condition, a 20-th order butterworth filter is required that in addition to its complexity adds a 4 dB inband attenuation that should be corrected in the digital baseband.
On the other hand, for the proposed interpolation technique, the adjacent channels just reduces the dynamic range of the A/D converter. Consequently, the required attenuation for the blockers is significantly lower. For example, to have the power of the blockers after filtering equal to 1% the power of the useful signal which just causes à 0.01 dB reduction of dynamic range, a 6-th order AAF is required.

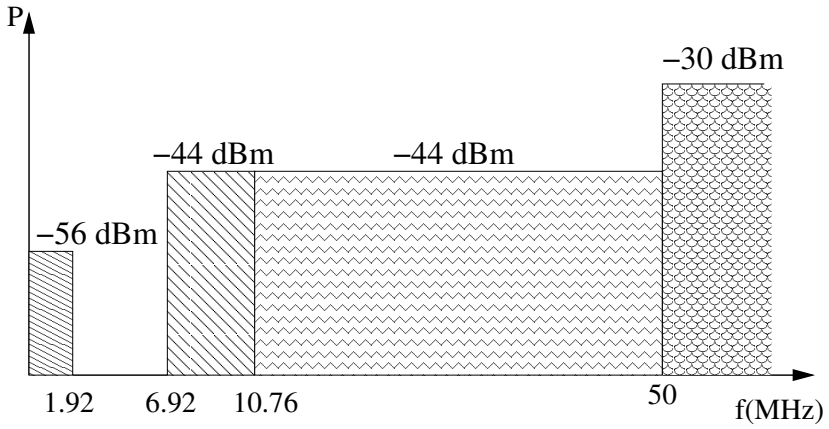


Figure 4.25: Worst case blocking signals for a UMTS scenario

Besides, $f_{S/H}$ has an impact also on the SNDR and stability. In fact, sampling at a higher frequency increases the signal power and consequently the SNDR but it reduces on the other hand the ADC stability as shown in Fig. 4.26. Therefore, the S/H frequency is chosen as a compromise of performance, capacitor size, AAF order and S/H complexity.

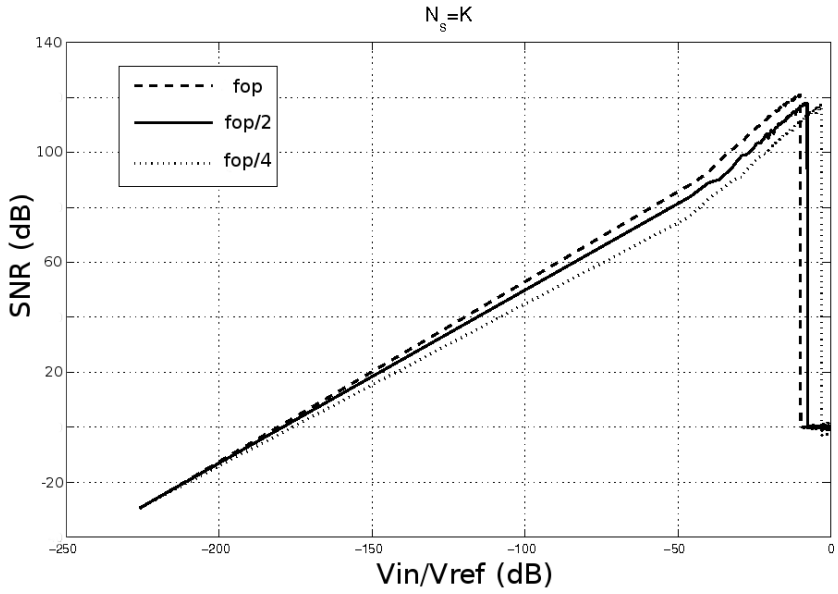


Figure 4.26: SNDR with respect to the input signal magnitude for different $f_{S/H}$

4.3 Calibration

The second major drawback of the TI $\Delta\Sigma$ architecture is its high sensitivity to channel mismatches. As shown in chapter 2, these imperfections cause the arising of parasitic tones that degrade significantly the SNDR.

4.3.1 Clock skew and bandwidth mismatch

As indicated in the previous section, the two-ranks S/H front-end technique was chosen to avoid the clock skew problem[74]. In parallel Nyquist ADCs, this solution is not optimized due to the fact that the shared S/H operates at a frequency M times higher than the channels and as a consequence limits the speed of the parallel ADC. However, in the proposed $\Delta\Sigma$ architecture, the S/H operates, in the worst case, at the same speed of channels and consequently the overall speed of the ADC is not limited by this block. This solution was preferred to other techniques such as global passive sampling[75] or clock calibration[76][77][78]. The operation of the global passive technique consists of adding an extra switch shared by all channels whose clock determines all of sampling instants. This will reduce significantly the clock skew problem. Nevertheless, it will not be removed completely due to the parasitic capacitances of the extra switch that cause coupling between channels. The drawbacks of the clock calibration approach are its lower efficiency compared to the two-ranks S/H and its long design time. Besides, the two-ranks S/H solution has another important advantage that it allows also to avoid bandwidth mismatches since all samples are processed by the same sampling capacitor and switches.

4.3.2 Offset and gain mismatch

Several solutions were proposed to deal with the offset and gain mismatches. The solution proposed in [68] uses an additional channel to perform a randomization operation. It spread out the spurious tones energy over the whole bandwidth thereby allowing to improve the

SFDR. The drawbacks of this technique are that the SNDR remains unchanged and that an additional channel is required which is not very optimized in terms of power consumption and die area. The solution proposed in [79] achieves the calibration by equalizing channel's offset and gain to the offset and gain of an additional channel assumed to be the reference element. This technique suffers also from the problem of requiring an additional channel. In the solution proposed in [80], a digital ΔΣ Modulator is added on each channel to correct its gain and offset mismatches which also causes an significant increase of the power consumption.

To overcome the drawbacks of these techniques, a novel calibration technique was developed in our research group[81]. The proposed solution does neither need additional modulator nor reference signal generator. It just requires an accumulator on each channel in addition to the existing digital resources in the TI ΔΣ architecture. Furthermore, it presents high accuracy for offset and gain estimation with very short convergence time.

The correction of the offset requires first the estimation of its value. This operation is achieved by connecting the channel input to the ground and then the Comb-filter on each channel, dedicated to the signal reconstruction is used to estimate the value of the offset. This value will be then subtracted from the output signal thereby allowing to have an offset almost equal to zero. Simulation results showed that 10 clock cycles are required to achieve an accuracy of 10^{-7} for the estimated value[81].

The proposed gain calibration algorithm must be employed after the offset correction. Its operation is based on equalizing the gain of all channels to the gain of one of the channels selected as the reference channel. Fig. 4.27 shows the implementation of the correction algorithm. As shown, a DC input signal is applied to all channels. This signal may be one of the existing signals of the ADC such as a quantizer comparison level. The output of the i^{th} modulator is then measured by the Comb-filter. Afterwards, the Sign Data Least Mean Square (SD-LMS) algorithm [82] calculates the weight value W_i to equalize the gain of the i^{th} channel to the gain of the first channel selected as the reference channel in our scenario. Simulation results showed that 15 clock cycles are required to achieve an accuracy of 5.10^{-7} for the estimated value [81].

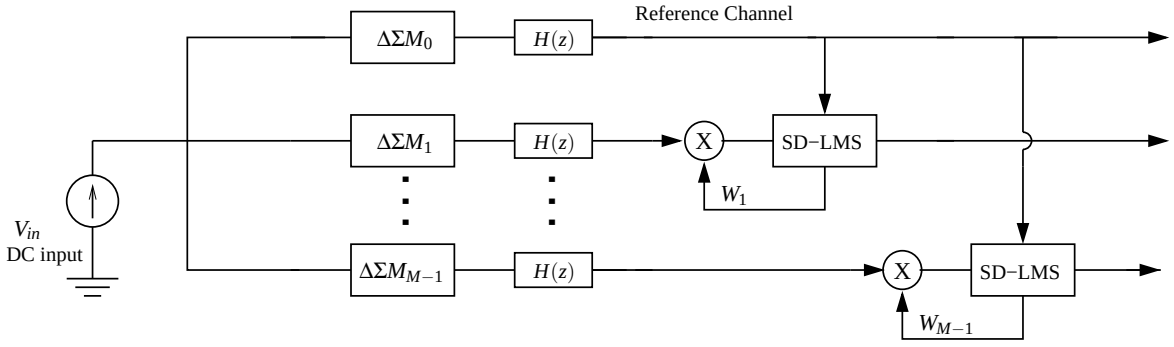


Figure 4.27: Block diagram of the gain calibration

To illustrate the influence of these errors and show the efficiency of the proposed correction method, a 4 channel TI ΔΣ ADC using a 4^{th} order ΔΣ modulator with an interpolation factor of 80 and a 6^{th} order Comb-filter is considered. The input is a sinusoidal signal with a normalized amplitude of 0.6 located at the normalized frequency 0.02. Realistic values for channels' offset and gain were chosen, they are given by the following vectors: O = [-20.2, 71.7, 76.5, 18.32] μV and g = [1.0113, 1.0146, 1.0029, 0.9884]. The offset calibration was applied first and then the gain calibration algorithm is applied taking into account the residual offset

mismatch remaining after the offset calibration. Fig. 4.28 shows the PSD at the output before and after calibration. It can be noticed that a SNDR improvement of 66 dB was achieved.

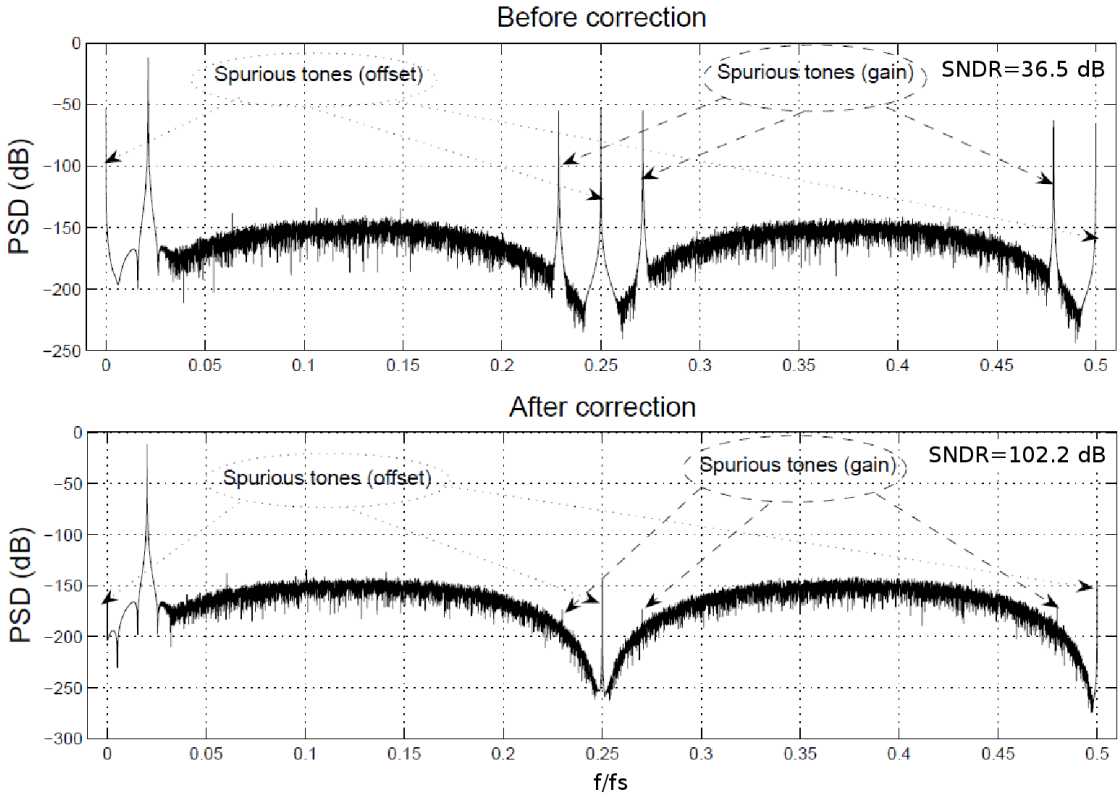


Figure 4.28: PSD before and after calibration

4.4 Conclusion

After comparing four architectures of paralell $\Delta\Sigma$ ADCs, it has been shown that the TI architecture offers the best compromise in terms of complexity, reconfigurability and design time. The two main drawbacks of this architecture are its sensitivity to thermal noise and to channel mismatch. The first problem was adressed by a novel interpolation technique that allows to reduce the size of the sampling capacitors and relaxes the constraints on the AAF. The drawbacks of this new technique are an increase of the complexity of the clock generation circuit and of the order of the equalization filter from the 10th to the 30th order. Nevertheless, these inconvenients are negligible compared to the acquired benefits.
A two-ranks S/H was used to deal with clock skew and bandwidth mismatch. Whereas the gain and offset mismatches were overcomed by employing novel correction algorithms that just requires an accumulator on each channel in addition to the existing digital resources.

Chapter 5

Prototype

Versanum standing for versatile wideband digitization is a project funded by the french national research agency (ANR) [83]. The aim of the project is to study the versatile wideband ADC concept. Three solutions are considered : hybrid filter banks ADC, parallel Delta Sigma ADC and parallel band-pass Delta Sigma ADC. Our work lies in the second section. The objective is to design an ADC for a direct conversion multimode receiver suited for GSM, EDGE, UMTS, DVB-T, WiFi and WiMax standards. The targeted specifications are shown in Table. 5.1. For the sake of design simplicity, the specifications of some standards were merged.

Table 5.1: Standards specifications

Modes	B	SNR
GSM/EDGE	135 KHz	80 dB
UMTS/DVBT	4 MHz	80 dB
WiFi/WiMax	12.5 MHz	52 dB

In this chapter, the design of Versanum prototype is presented. Some of characteristics of this ADC were discussed in the previous chapters. In fact, it was decided that the ADC will be implemented using the SC technique and the $\Delta\Sigma$ modulator is a LP. The retained architecture of the parallel ADC is a TI $\Delta\Sigma$ using the novel interpolation technique exposed in section 4.2. The clock skew and the gain mismatch problem will be dealt with using the two-rank S/H solution. While the offset and the bandwidth mismatch will be corrected using the algorithms presented in section 4.3. The other design aspects will be discussed in the chapter.

5.1 System Design

For the GSM/EDGE mode, a single channel with a 2^{nd} order modulator is sufficient. In fact, since the band in this mode is very narrow, a very large OSR can be achieved while maintaining a low operation frequency. Consequently, there is neither a need to use a multi-channel ADC, neither a modulator of a higher order.
Fig. 5.1 shows the architecture of the employed modulator. This architecture proposed in [84] reduces the constraints on the integrators compared to a distributed feedback architecture.

In fact, since the signal is fed forward to the quantizer input, the integrators process just the quantization error [84]. This allows to reduce the excursion and the linearity constraints on the OTAs, hence their power consumption. The drawback of this architecture is the adder at the quantizer input. In fact, as explained in (Section A.4), this adder can be implemented either passively or actively. A passive implementation is almost power consumption free but it causes an attenuation of the signal excursion at the quantizer input. This increases the impact of the non-idealities of the quantizer and may lead to a SNR loss. On the other hand, an active implementation does not affect the performance but it requires an OTA and as consequence the power consumption is increased. Nevertheless, the active solution was adopted because of two main reasons: 1) The targeted resolution in the GSM/EDGE mode is high and a passive adder may limit the performance; 2) For the other modes, a 4^{th} order cascaded modulator is employed. The first stage adder output is fed to the input of the second stage and therefore, if a passive adder is used, the signal in the second stage will be attenuated which causes an SNR loss.
A 1.5 bit quantizer is preferred to a 1 bit quantizer because it allows to increase the resolution by 3 dB and the DR by almost 3 dB as well. Besides, the STF peaking is lower for the 1.5 bit quantizer because the quantizer gain variation is lower. The added circuitry required to achieve the 1 bit to 1.5 bit transition is a comparator and some switches in the DAC. This complexity increase remains negligible compared to the acquired benefits.
The modulator coefficients are chosen as a compromise between modulator stability, suppression of quantization noise, unity STF and maximum hardware reusability [12]. Its output spectrum for a -3 dBFS input signal is shown in Fig. 5.2. The SQNR for an OSR of 96 is 87 dB.

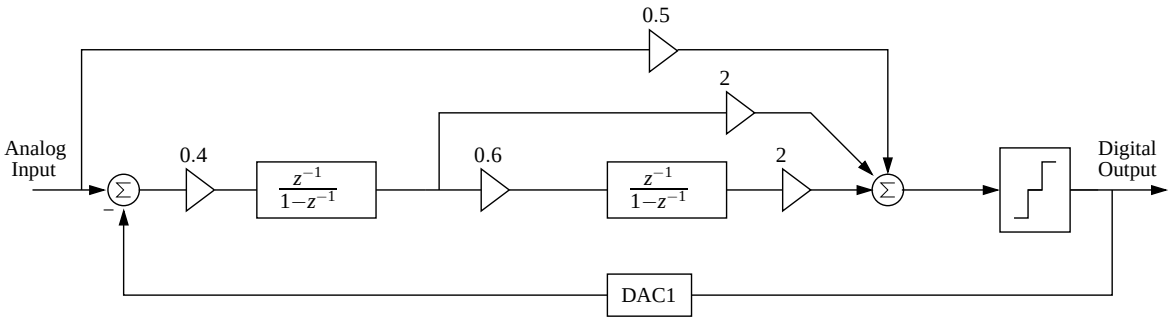


Figure 5.1: Silva structure.

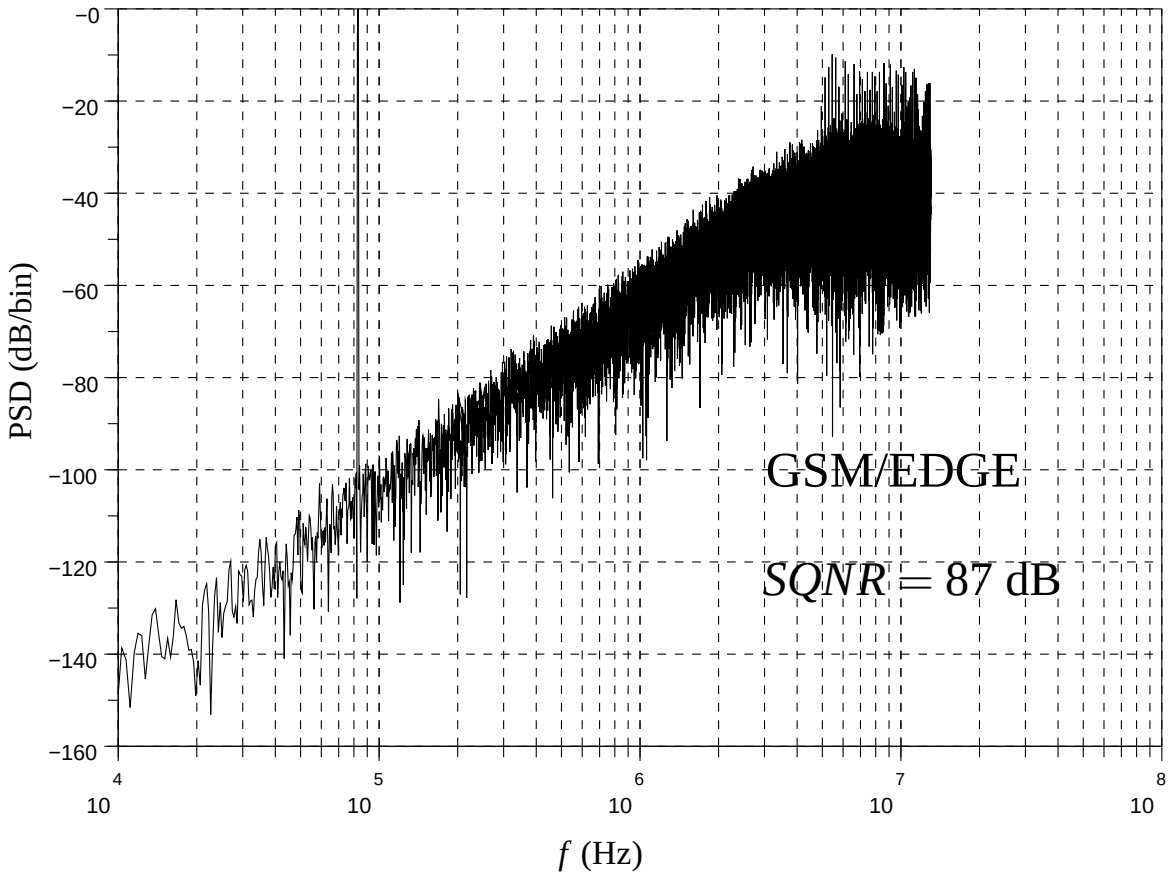


Figure 5.2: Output spectrum in the GSM/EDGE mode

In the UMTS/DVBT and WiFI/WiMax modes, the targeted conversion rate is much higher than in GSM/EDGE mode. Therefore, a higher order modulator is required because of the lower achievable OSR.
One of the main drawbacks of traditional MASH structures is their need to have an accurate matching between the analog STF of the first stage and the transfer function of the second stage pre-digital filter[85] [86]. In fact, due to non-idealities of the analog blocks and to process and environment variation, the analog STF can not be predicted before manufacturing and consequently calibration techniques must be employed to match the digital filtering to the analog STF or vice versa[85][86].
A new generation of MASH modulators known as SMASH (sturdy MASH) or GMSCL (generalized multi stage closed loop) overcome this problem[87][88] [89] [90]. Their operation is based on introducing a global feedback as it can be seen in Fig. 5.3. This architecture has also the advantage of relaxing the constraints on analog components compared to traditional MASH structures [89] [90].
A ($M = 2$, $N = 52$) solution is employed for the UMTS/DVBT mode and a ($M = 4$, $N = 32$) for the WiFI/WiMax mode. These sets of (M , N) allow to reach the required SQNR for the two modes and to use the same f_{op} for the two modes which simplify the design.
Fig. 5.4 shows the spectrums of the reconstructed signals at the output of the TI $\Delta\Sigma$ ADC for the UMTS/DVBT and WiFi/WiMax modes. The respective SQNRs are 89 dB and 63 dB. The system parameters are summarized in Table 5.2.

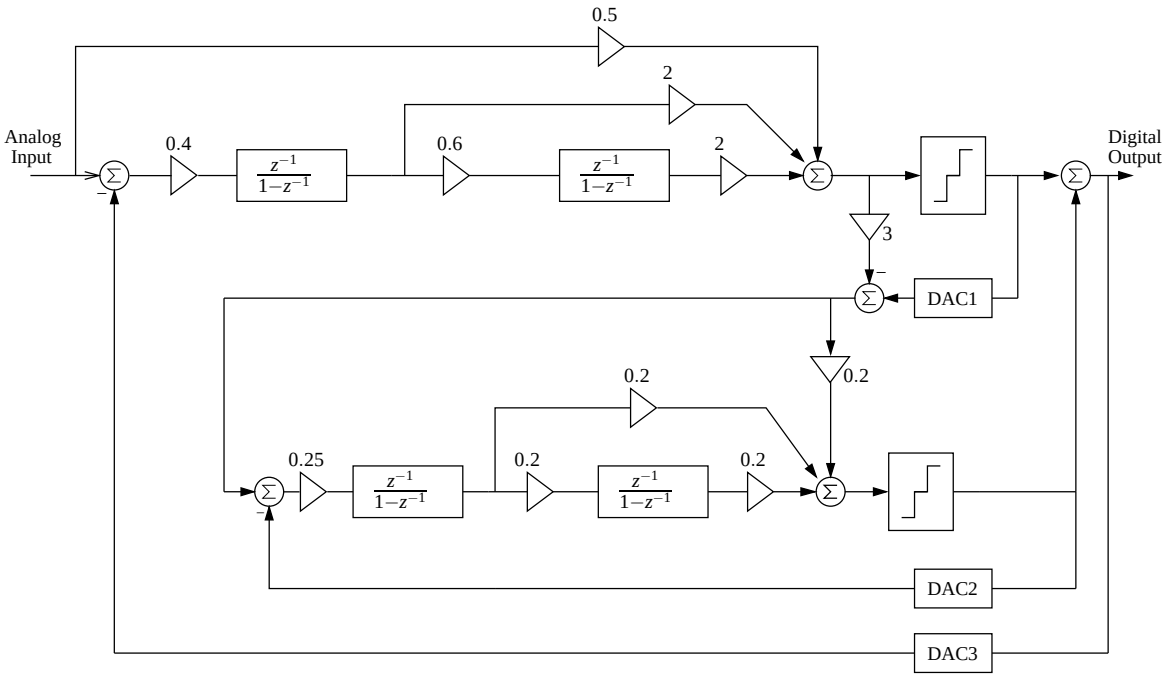


Figure 5.3: GMSCL $\Delta\Sigma$ structure.

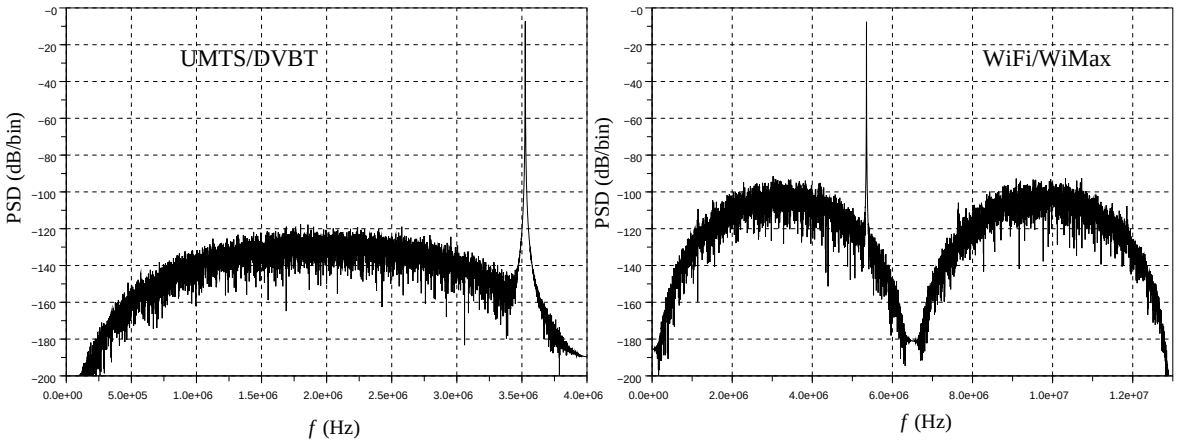


Figure 5.4: Output spectrum in the WiFi/WiMax mode

Table 5.2: System Parameters of the TIΔΣ ADC.

Standard	M	N	Modulator order
GSM/EDGE	1	96	2
UMTS/DVBT	2	52	4
WiFi/WiMax	4	32	4

5.2 Electrical Design

5.2.1 Analog design

Fig. 5.5 shows the schematic of the front-end S/H that distributes the samples among channels. As said before, the S/H was placed to avoid clock skew and bandwidth mismatch. Figs. 5.6 and 5.7 show, respectively, the schematic of the modulator in the 2^{nd} order configuration and 4^{th} order configuration. For the sake of simplicity, a single-ended representation is illustrated. A control bit that will be referred to as $ULAN$ allows to switch from on mode to the other. It controls from one side, the master bias circuit that provides the reference currents for the OTAs and the pre-amplifiers of the comparators. The reference currents are used to generate the biasing voltage for the OTAs. Thus, if the circuit is configured as a 2^{nd} order modulator, the reference currents of second stage's blocks are set to zero to avoid unnecessary power consumption and the reference currents of first stage's blocks are set to the values that optimize the operation for a f_{op} of 26 MHz that is required in GSM/EDGE mode($\underbrace{96}_{OSR} \times 2 \times \underbrace{135\text{ kHz}}_{\text{Band}} =$ 26 MHz).

The $ULAN$ bit controls also the OTAs of the first stage. In fact, these OTAs need to operate at 26 MHz in the GSM/EDGE mode and at 208 MHz for the UMTS/DVBT and WiFi/WiMax modes ($\underbrace{\overbrace{\frac{52}{2}}^{N}}_{M} 2 \times \underbrace{4\text{ MHz}}_{\text{Band}} = \underbrace{\overbrace{\frac{32}{4}}^{N}}_{M} 2 \times \underbrace{13\text{ MHz}}_{\text{Band}} = 208$ MHz). Therefore, given the big difference between the two frequencies, a simple change of the reference current does not allow an optimized operation in both cases and as a consequence a reconfiguration of the OTA itself is needed. This is achieved by allowing a $ULAN$ controlled change of sizes of some transistors

of the OTAs.

Fig. 5.8 a) shows the schematic of the OTA employed for the first and second integrators.

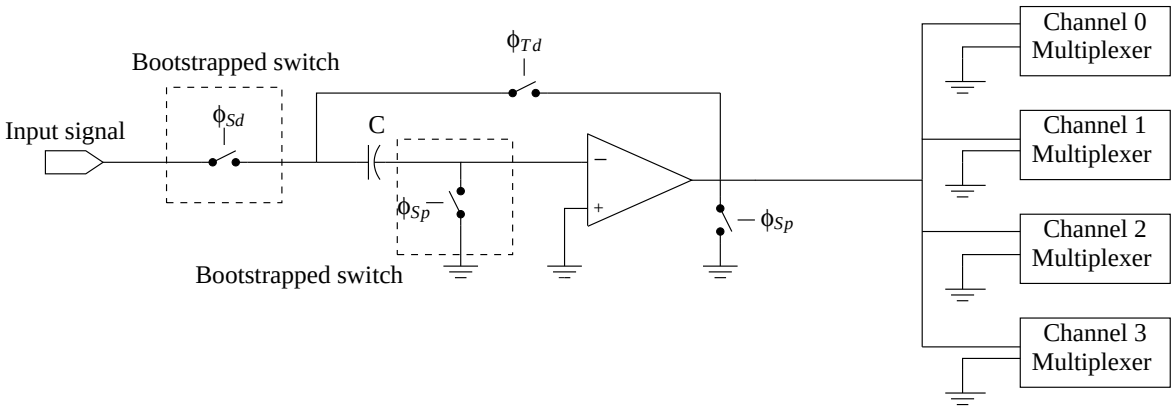


Figure 5.5: Circuit of the Front-end S/H

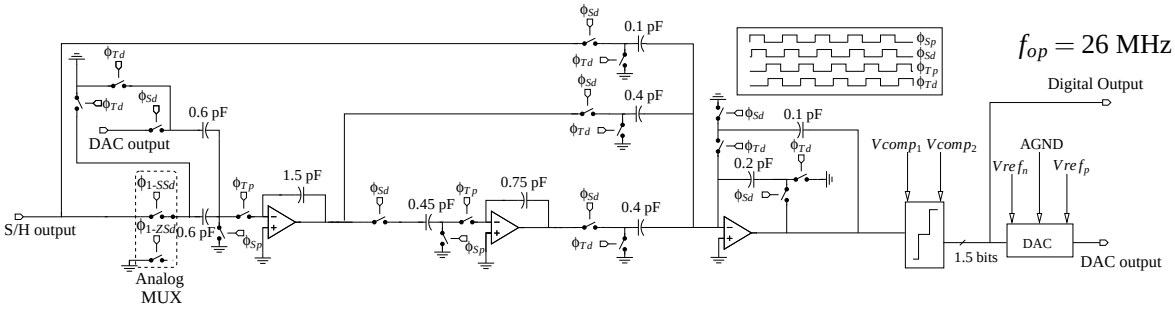


Figure 5.6: Circuit of the 2^{nd} order modulator

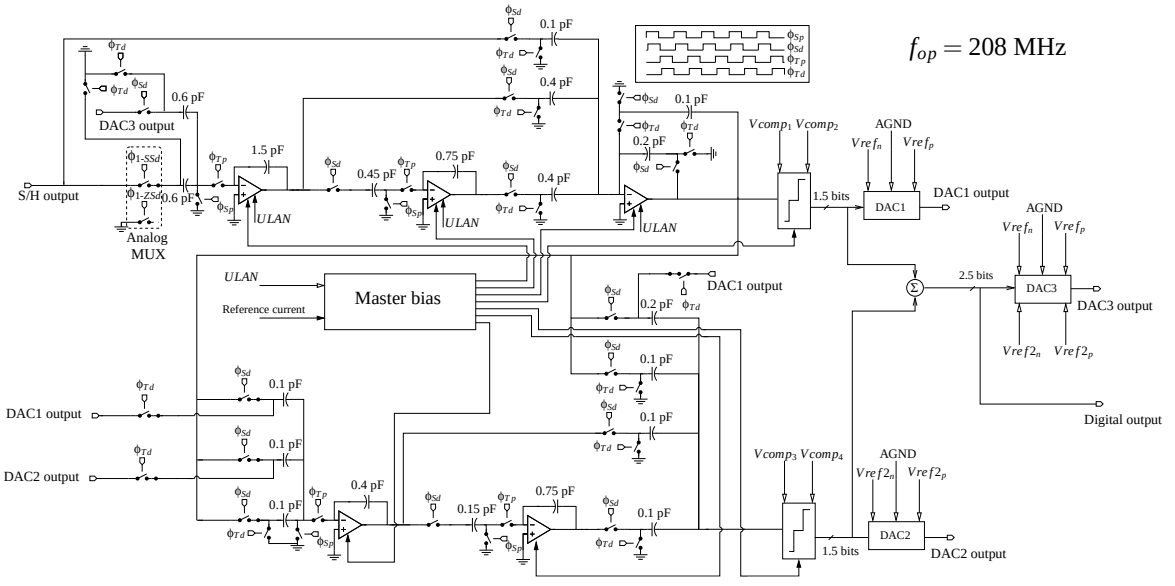


Figure 5.7: Circuit of the 4^{th} order modulator

All the components in dashed rectangles are reconfigurable. A two stages architecture with a Miller compensation was chosen for these OTAs to profit from its high dc-gain and output swing. The bulks of the input pair transistors are connected to their common source to avoid increasing their threshold voltage because of the bulk effect.

Fig. 5.8 b) shows the schematic of the OTA used for the third and fourth integrators. It has

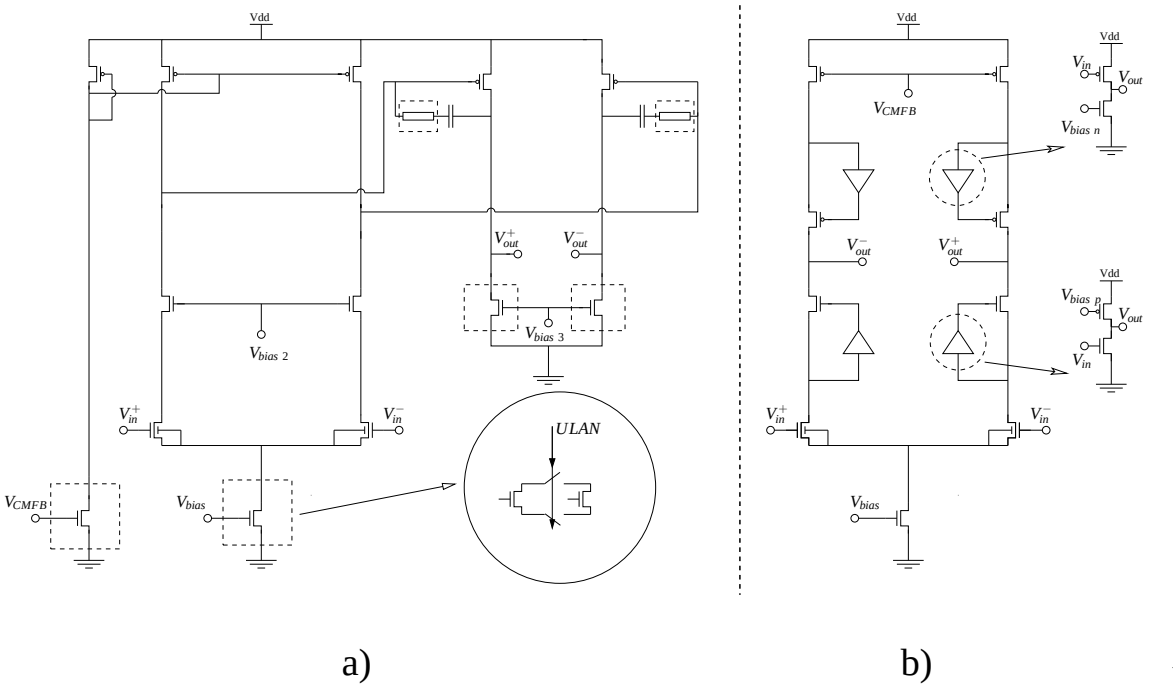


Figure 5.8: a) Reconfigurable two stages OTA used in the first and the second integrators b) Single stage OTA used in the third and the fourth OTA

a telescopic with boosted cascode architecture. A single stage architecture has the advantage of having lower power consumption compared with a two stages architecture but it is paid by lower performances. Nevertheless, it can be used in the third and fourth integrators seen their lower requirements in terms of dc-gain and GBW with respect to the OTAs of the first stage. To deal with the low output excursion of the OTA architecture, small values for the integrator gains were used.

The 1.5 bit quantizer of each stage is implemented as a flash ADC. Its comparison levels are generated off-chip. The dynamic latches are preceded by a pre-amplifiers to increase their robustness against quantizer non-idealities and specially metastability. In fact, the adder takes $T_{op}/2$ to achieve the addition operation and thus the comparator has to take its decision during the short non-overlap times between clocks ϕ_{Sd} and ϕ_{Tp}.

The diagram of the clocks is shown in Fig. 5.7. Two delayed versions of the sampling and the tracking clocks were generated to allow a time difference between the opening of the sampling switch and the input switch. This technique known as bottom plate sampling reduces strongly the signal dependent charge injection of the switches (Section A.2.3.1).

Besides, to avoid significant SNDR loss due to the non-linearity of the switch, the input switches of the S/H and of the first integrator were bootstrapped. The employed circuit is shown in Fig. A.10.

Note that all the used transistors are low Vt transistors.

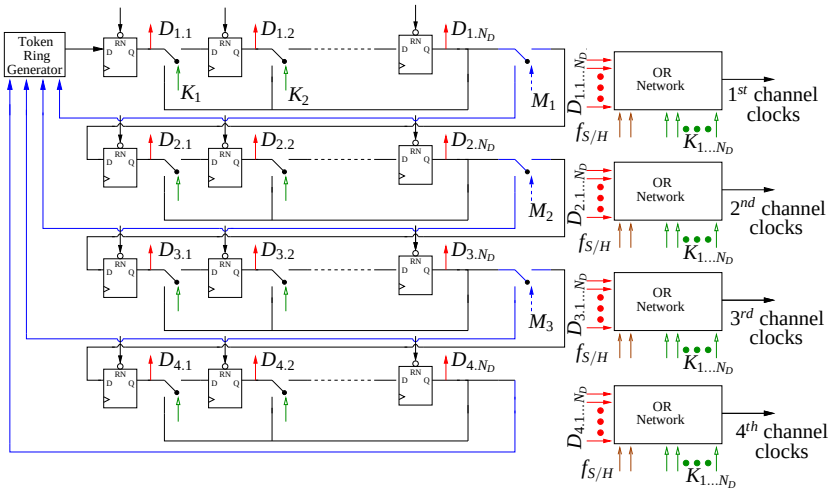


Figure 5.9: Interpolation network architecture.

The UMTS/DVBT mode has the highest constraints in terms of thermal noise and thus fixes the value of the sampling capacitor. When the using the novel interpolation technique, a 600 fF capacitor is required to achieve a thermal SNR of 83 dB at 363 K (90^o C) compared to a 15.6 pF capacitor required when using the classical interpolation technique.

5.2.2 Interpolation network implementation

To validate the proposed interpolation technique, a reconfigurable clock generation circuit that will be refer to as the interpolation network has been designed. It generates the analog multiplexer clock signals for a given N, M and S/H sampling frequency. Four different S/H sampling frequencies can be achieved: f_{op}, $f_{op}/2$, $f_{op}/4$ and $f_{op}/8$. The implemented interpolation network operation is based on the common tokenring. In fact, each channel has N_D D-flipflops. These flipflops are placed in series and connected to each other via tri-state cell. The tri-state cell control signals $K_{1...N_D}$ set the number of flipflops that are crossed by the token equal to K (K is the number of added signal samples per channel which is equal to N/M). Moreover, the channel flipflop chains are also placed in series and are connected together via another tri-state cell. Its control M_i enables or disables the next channel. For operation explanation, an example scenario of $M = 2$, $K = 16$ and consequently $N = 32$ will be considered :

- Once the system is reset, the tokenring generator shown in Fig. 5.9 injects a token at the input of the 1^{st} flipflop of the 1^{st} channel. Its consists of a Vdd signal during one clock period. At this point, all flipflop outputs are low

- One T_{op} later, $D_{1.1}$ will be equal to "1" and the rest of the outputs will remain low. The token will then reach the 1^{st} tri-state cell of the 1^{st} channel. Its control signal is at a high level because K is larger than 1. Consequently, the token will be passed to the 2^{nd} flipflop of the 1^{st} channel.

- At the next clock front, $D_{1.1}$ will return to "0", $D_{1.2}$ will become high and the other flipflop outputs will remain low.

- Similarly, the token will go through flipflops and tri-state cells to reach the 16^{th} tri-state cell of the 1^{st} channel. As $K = 16$, the tri-state control will be low and the token will be directed to the flipflop that connects the 1^{st} channel chain to the 2^{nd} channel chain.

- The control of this tri-state cell is high because M was set to be equal to 2. The token will be directed thereby to the input of the 1^{st} flipflop of the 2^{nd} channel.

- 16 T_{op} later, the token will get to the tri-state cell that connects the 2^{nd} channel chain to the 3^{rd} channel chain. However at this time, its control signal will be low. The token will then be directed to the tokenring generator that will introduce a new token at the 1^{st} channel input.

In the meantime, the flip-flop outputs are recovered in OR networks to generate Multiplexers clock signals ϕ_{i-SSd} and ϕ_{i-ZSd} (Fig. 5.7). At ϕ_{i-SSd} clock front, a signal sample is processed and at ϕ_{i-ZSd} clock front, a sample of value 'zero' is obtained. As said before, when sampling at f_{op}, the 1^{st} channel performs its interpolation by a factor N by adding the first K signal samples followed by $N - K$ zeros. Meanwhile when sampling at $f_{op}/2$, $K/2$ samples are acquired during $K.T_{op}$. Therefore, the even samples are replaced by zeros. Similarly, the modulo 2 to 4 signal samples when sampling at $f_{op}/4$ and the modulo 2 to 8 signal samples when sampling at $f_{op}/8$, are replaced by zeros.

To create these clock signals, the modulo 8 flip-flop outputs of each channel are firstly ORed together :

$$OR_{i.j} = \sum_{k=0}^{3} D_{i.(j+8k)}$$

For example, the OR output of ($D_{1.1}$, $D_{1.9}$, $D_{1.17}$ and $D_{1.25}$) will be referred to as $OR_{1.1}$, ($D_{1.2}$, $D_{1.10}$, $D_{1.18}$ and $D_{1.26}$) as $OR_{1.2}$ and so on. The 4 clock signals are generated as follows:

- For a sampling frequency of $f_{op}/8$, the i^{th} channel ϕ_{i-SSd} is given by :

  $$f_{op}/8\ \phi_{i-SSd} = OR_{i.1} \bullet \phi_{Sd}$$

  In fact, the token reaches $D_{1.9}$ 8 T_{op} after reaching $D_{1.1}$ creating thereby a clock signal having a front every 8 T_{op}. This will allow us to get the signal samples every 8 T_{op} as desired

- $$f_{op}/2\ \phi_{i-SSd} = (OR_{i.1} + OR_{i.5}) \bullet \phi_{Sd}$$

- $$f_{op}/4\ \phi_{i-SSd} = (OR_{i.1} + OR_{i.3} + OR_{i.5} + OR_{i.7}) \bullet \phi_{Sd}$$

- $$f_{op}\ \phi_{i-SSd} = \sum_{k=1}^{8} (OR_{i.k}) \bullet \phi_{Sd}$$

The $\bullet$ and the $+$ stand for an AND and OR operations respectively

During sampling phases, the integrator sampling capacitor must either store signal samples or zeros therefore ϕ_{i-ZSd} is the conjugate of ϕ_{i-SSd} when ϕ_{Sd} is high. It is generated as shown in Fig. 5.10.

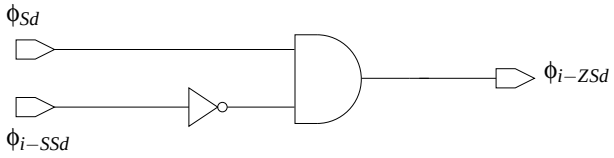


Figure 5.10: ϕ_{i-ZSd} generation circuit.

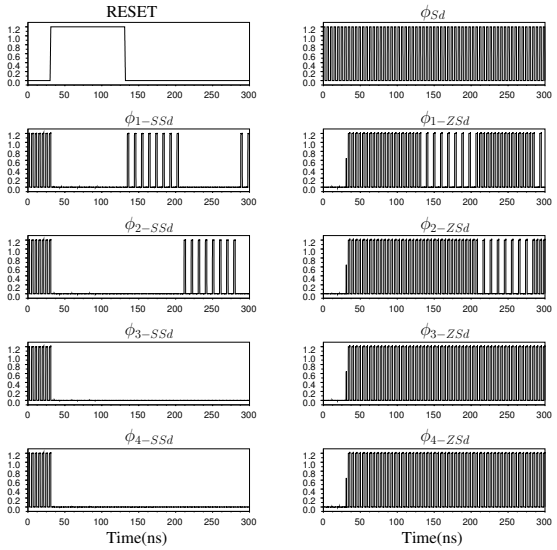


Figure 5.11: Clock signals for a $M = 2K = 16$ $f_{op}/2$ scenario

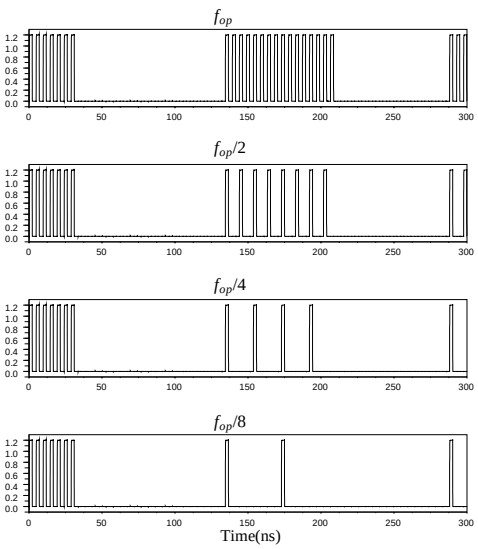


Figure 5.12: ϕ_{1-SSd} for a $M = 2K = 16$ scenario for the 4 sampling rates.

Fig. 5.11 shows the four channel clock signals in a $f_{op}/2$ case and Fig. 5.12 shows the 1^{st} channel sampling clock for the 4 different rates for the considered scenario. The parameters of the implemented four channels TI $\Delta\Sigma$ ADC are summarized in Table. 5.3. The interpolation network die area is $0.01mm^2$ and its consumption is 0.32 mW for a $f_{op} = 208$ MHz.
Electrical simulations for different corners that combine a -25^{o}C to 90^{o}C temperature variation, a $\pm$10% variation of supply voltages and a SS, TT and FF processes were carried out for a single channel mode. Simulations were achieved for the second order modulator clocked at 26 MHz and for the fourth order modulator clocked at 208 MHz. The expected performances were reached for all considered corners.
In TI mode, tracing a 8000 points spectrum of the constructed signal requires a simulation of 8000 $\times$ N cycles of the complete circuit which requires a very long simulation time. For example, such simulation using Spectre simulator would have required three months for the WiFi/WiMax mode using a 3.6 GHz Intel Xeon CPU. Consequently, we were not able to simulate the performance of the complete circuit in the TI mode. Therefore, in order to ensure its functionality, some tests were carried using ideal $\Delta\Sigma$ modulators instead of real $\Delta\Sigma$ modulators. The results of these tests were compliant with system simulations thereby confirming the functionality in the TI mode.

Table 5.3: Parameters of the implemented four channels TI $\Delta\Sigma$ ADC.

Standard	f_s (MHz)	M (dB)	N	Modulator order	f_{op} (MHz)	P (mW)
GSM/EDGE	0.27	1	96	2	26	1.74
UMTS/DVBT	8	2	52	4	208	55.2
WiFi/WiMax	25	4	32	4	208	110.4

5.3 Layout

Figures 5.13 and 5.14 show, respectively, the layout of the complete circuit with the I/O ring and a zoom over one channel. Note that just the analog part was implemented on-chip. The decimation operation and the signal reconstruction are achieved off-chip. A stand alone channel was added to increase the flexibility of the test. The circuit was fabricated in a 65nm 1P7M CMOS technology. In order to have capacitors with high density and high linearity, a metal insulator metal (MIM) option was used to implement them (Subsection B.1.3). To reduce the noise coupling between the analog and the digital parts, the supply voltages of each were separated. Besides, all digital blocks were placed inside triple wells to reduce the noise coupling through the substrate (subsection B.2.2.3). Since the analog supply signals are clean and the digital elements are not very sensitive for these operation frequencies, the wells polarisation signals and supply voltages were shorted in each part to reduce the complexity of the layout.

The reference and clock signals were routed with thick metals that have low resistivity in order to reduce the signal deformation. In the UMTS/DVBT and WiFi/WiMax modes, a large current crosses the analog supply rails of each channel. Therefore, to reduce the voltage drop, very large rails in thick metals were used to route the supply wires. To avoid their splitting due to the cutting operation, the rails were chopped (Subsection B.3.3). Besides, since the S/H and the first integrator are more critical than the other stages, the supply PAD were placed the nearest possible to them.

All critical components were matched carefully using techniques such as: symmetry, dummy element addition and element splitting. In the S/H and the first integrator, the common centroid technique was used in addition for the critical transistors of the OTAs to reduce the input referred offset and the magnitude of the even order harmonics(Subsection B.2.2.2). A metal exclude mask was applied to all analog blocks to avoid adding dummy metals over or under them because it may be a cause for mismatch arising.

The I/O ring is composed of 80 pads. It was divided in three parts: 1) for the analog inputs (input signal, analog supply signals and reference signals); 2) for the digital inputs (clock signal, control signals and digital supply signals); 3) for the digital outputs (ADC's output bitstream and synchronization output clock signal). The digital level is 1.8 V.

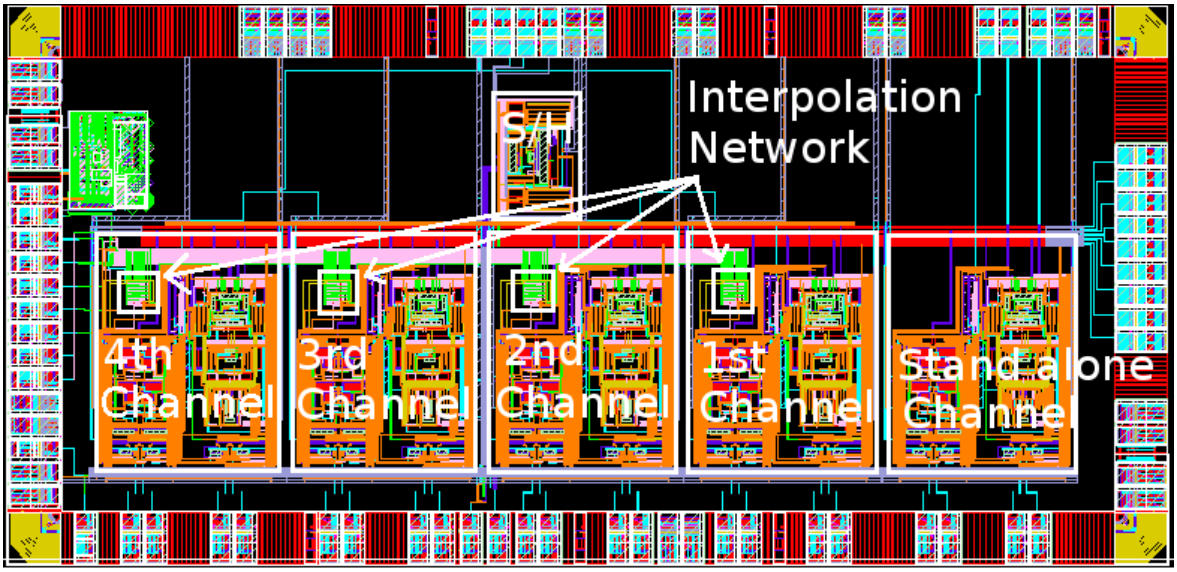


Figure 5.13: Circuit Layout

5.4 Test

5.4.1 Test setup

5.4.1.1 Chip

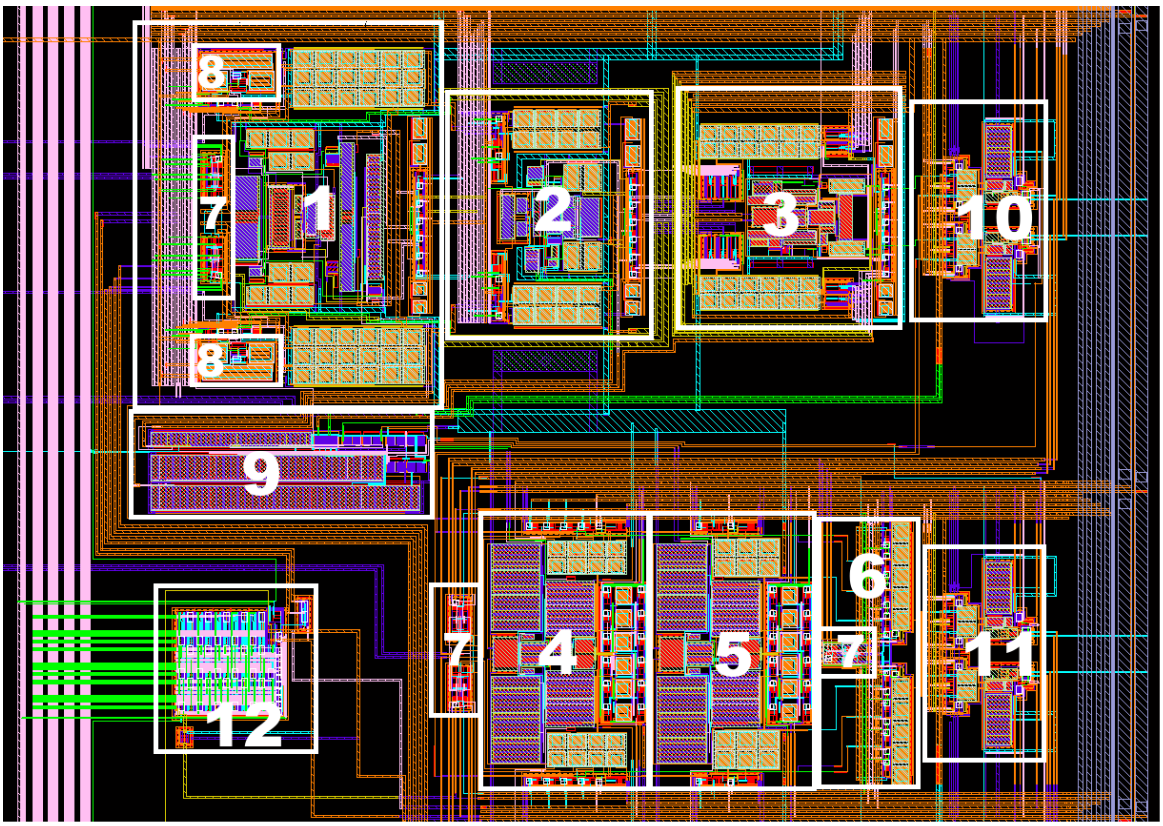
Fig. 5.15 shows a micrograph of the fabricated circuit. The overall circuit die area is 3 mm^2 (1.2 mm × 2.5 mm). A 100-pin CQPF (Ceramic Quad Flat Package) was used for packaging.

5.4.1.2 Test board

A four floor test board (Fig. 5.16) was used to test the circuit. One floor was used for the ground, another for the supply voltage and the two remaining for routing. The analog and the digital supplies for the core and the I/O ring were generated using four different regulators to avoid transferring noise for the digital to the analog parts. The common mode voltage, quantizers' comparison levels and DACs' reference voltages were generated using resistive ladders supplied by the analog core Vdd. In order to increase the flexibility of the test, each of the resistive ladders contained a potentiometer to allow an easy reconfiguration of the generated reference value. All DC voltages were decoupled carefully at the circuit input using surface mounted devices 0805 capacitors. The reference currents for the biasing were generated also using a reconfigurable resistive ladders. All the control digital signals were fixed using the set of switches shown in part 9 of Fig. 5.16

5.4.1.3 Test bench

The employed test bench is shown in Fig. 5.17. All devices were interfaced with a central PC included in the logic analyzer using GPIB-USB communications. The read/write codes were developed in C language and interfaced with Matlab to allow an easier signal processing.
The pulse generator is an Agilent 81130A. Its rms jitter measured using a spectrum analyser, is 120.2 ps for ±10 MHz noise integration at 26 MHz and 170.8 ps at 208 MHz for ±100 MHz



1- First integrator 2- Second integrator 3-First stage's Adder
4- Third integrator 5-Fourth integrator 6- Second stage's Adder 7-DACs
8-Bootstrapped switches 9-Biasing circuit 10-First stage's Quantizer
11-Second stage's Quantizer 12- Interpolation network

Figure 5.14: The layout of one channel of the circuit

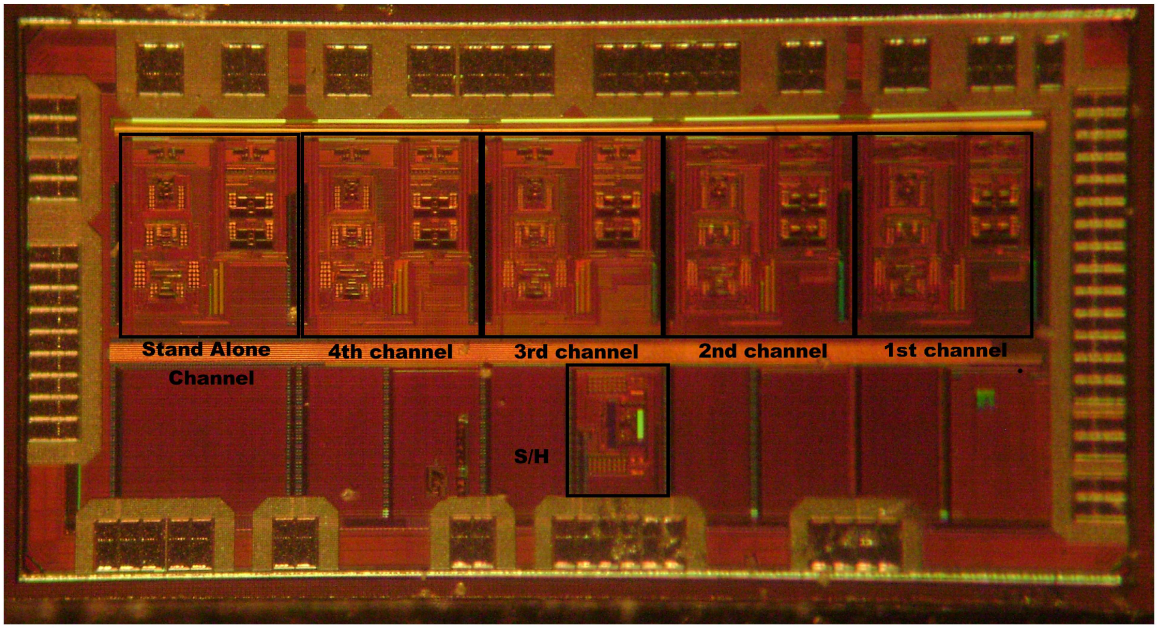
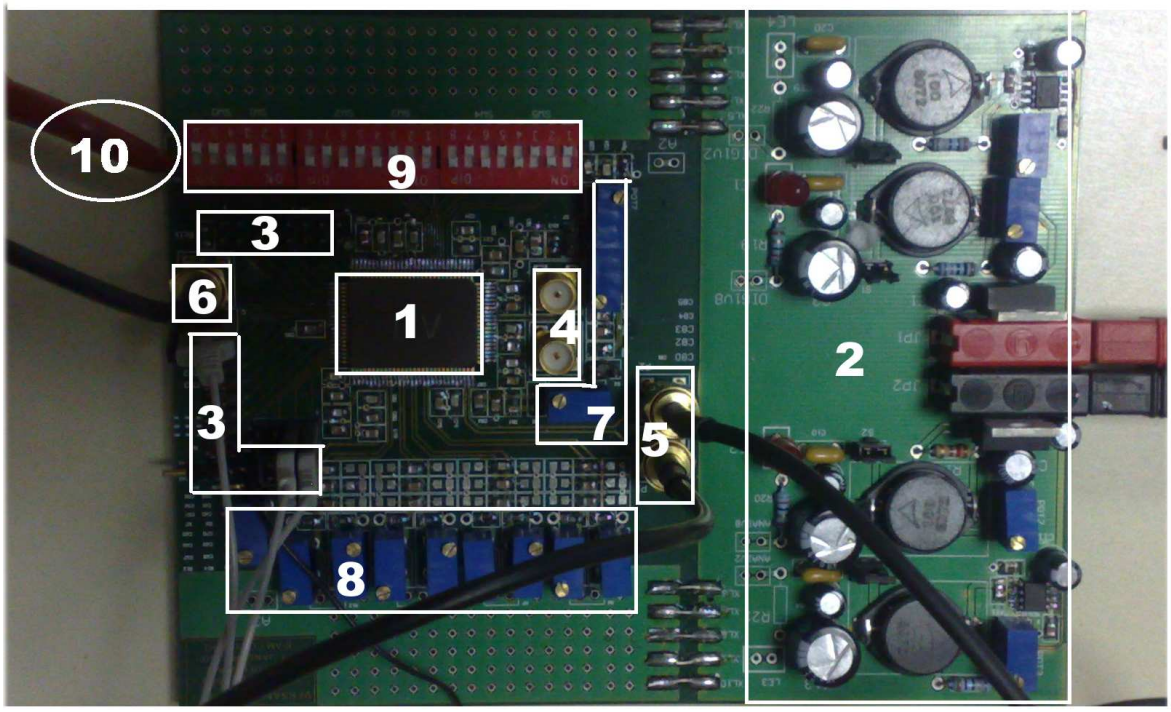


Figure 5.15: Chip micrograph



1- Chip 2- Supply unit 3- Outputs 4- TI ADC inputs
5- Stand alone channel inputs 6- Clock 7- Current references
8-Voltage references 9-control switches 10-Reset

Figure 5.16: Test board

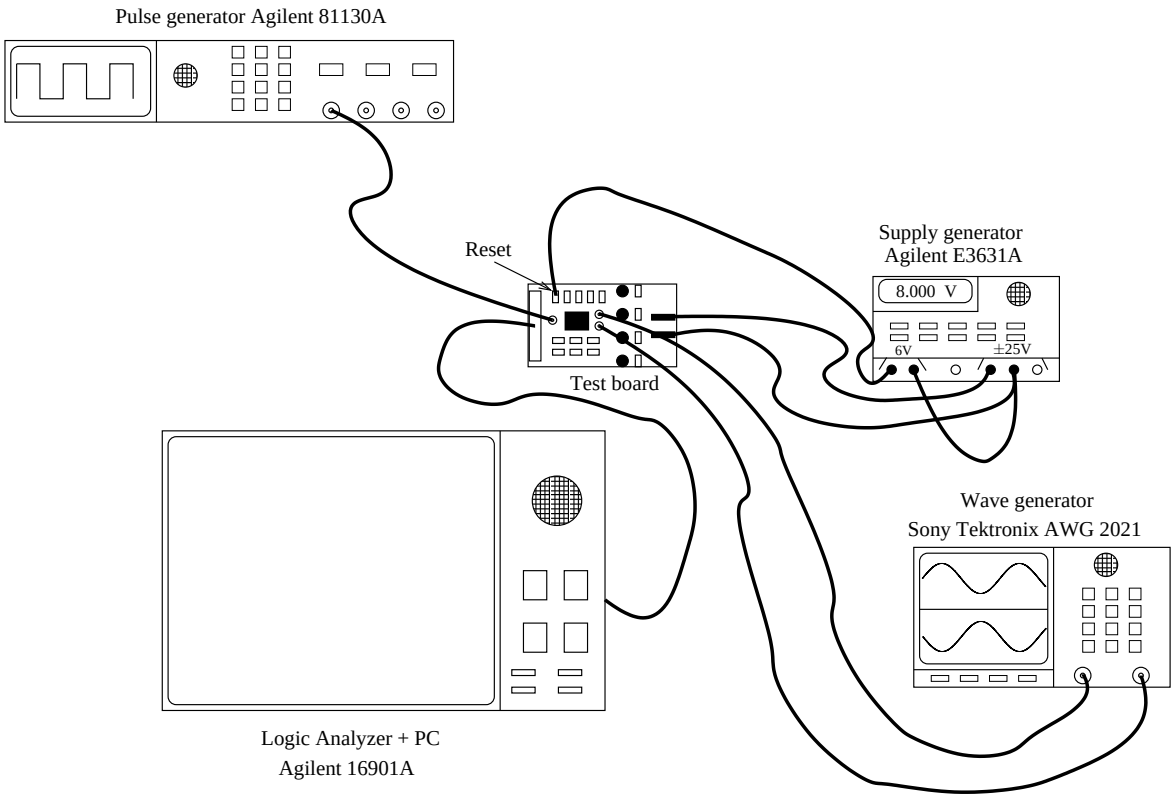


Figure 5.17: Test bench

noise integration. The supply generator is an Agilent E3631A. One of its outputs supplies the regulators and the other is used for the Chip reset. This allows us to achieve automatic resets between data acquisitions. The wave generator is a Sony Tektronix AWG 2021. Its measured spectrum for the EDGE band is shown in Fig. 5.18. As it can be seen, several parasitic tones due to the supply circuit of the generator appear in the spectrum. Besides, the noise floor level is at -130 dB/Hz which is 2 dB higher than the targeted ADC noise floor. The parasitic tones problem is not very critical for the test because since the positions of these tones are known, their PSD values can be replaced during signal processing by the value of the noise floor. However, the noise problem prevent an exact estimation of the resolution of the ADC. We were able to achieve some few tests using a Rohde & Schwarz SMU 200 A whose DAC has 16 bits resolution. Even though, we estimate that the ADC resolution is limited in some modes by the SMU noise floor and the use of a low pass filter as in [35][91] may increase slightly the measured SNR.

An important point to note is that the parasitic tones of the Sony generator appeared at the output of the ADC even when it was not connected to the circuit. This is due to the fact that the generator behaves as a transmitter and the test board as a receiver and thus the tones were transmitted as electromagnetic waves. The optimum solution in this case is the use of a Faraday cage. However, since we did not have a cage of the same size of the test board, all noisy generators were placed at a reasonable distance of the testboard.

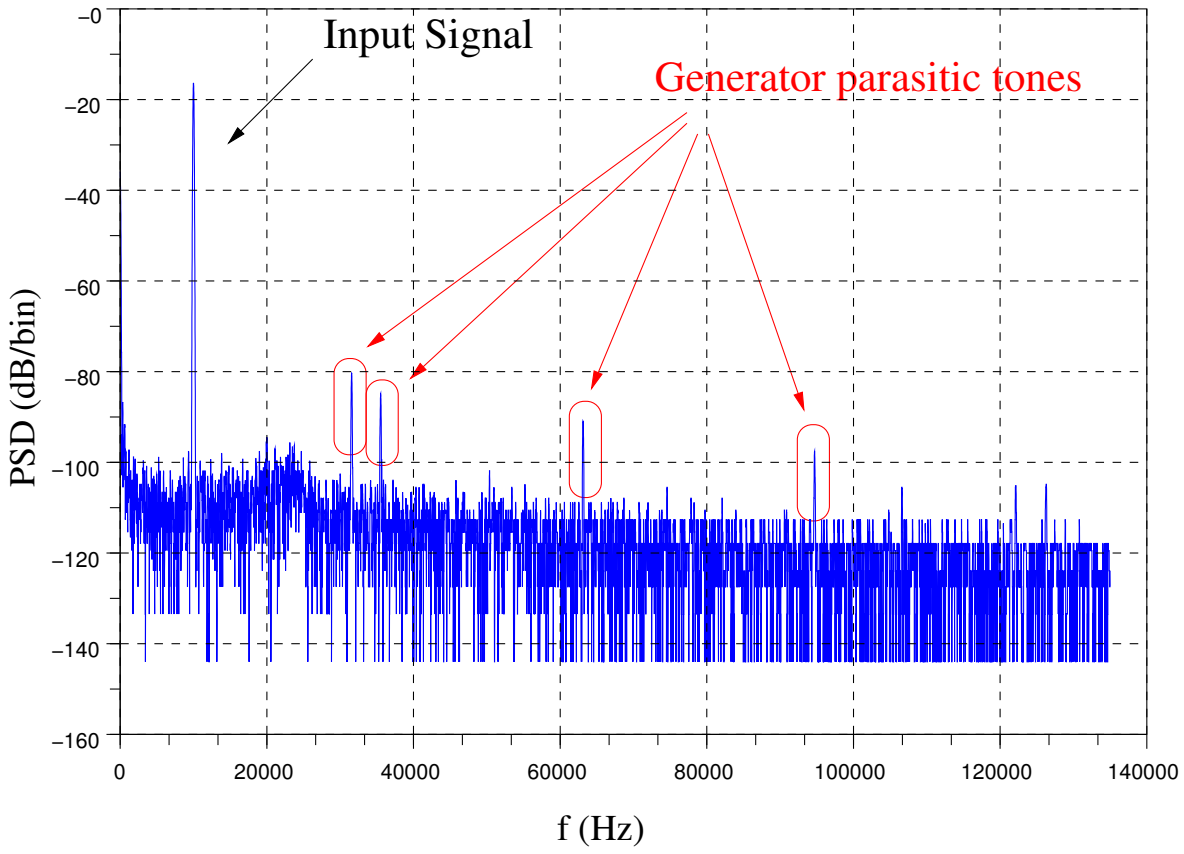


Figure 5.18: Wave generator spectrum in the EDGE band

5.4.2 Results

5.4.2.1 GSM/EDGE mode

Fig. 5.19 shows the measured output spectrum in the GSM/EDGE mode for a 10 KHz -4.5 dBFS input signal. This measure as all measures in this mode, is carried out using the stand alone channel. 2^{19} points were used to compute the FFT using a Blackman windowing for all the measures.

Fig. 5.20 shows the STF of the modulator for two different input amplitudes. The in-band

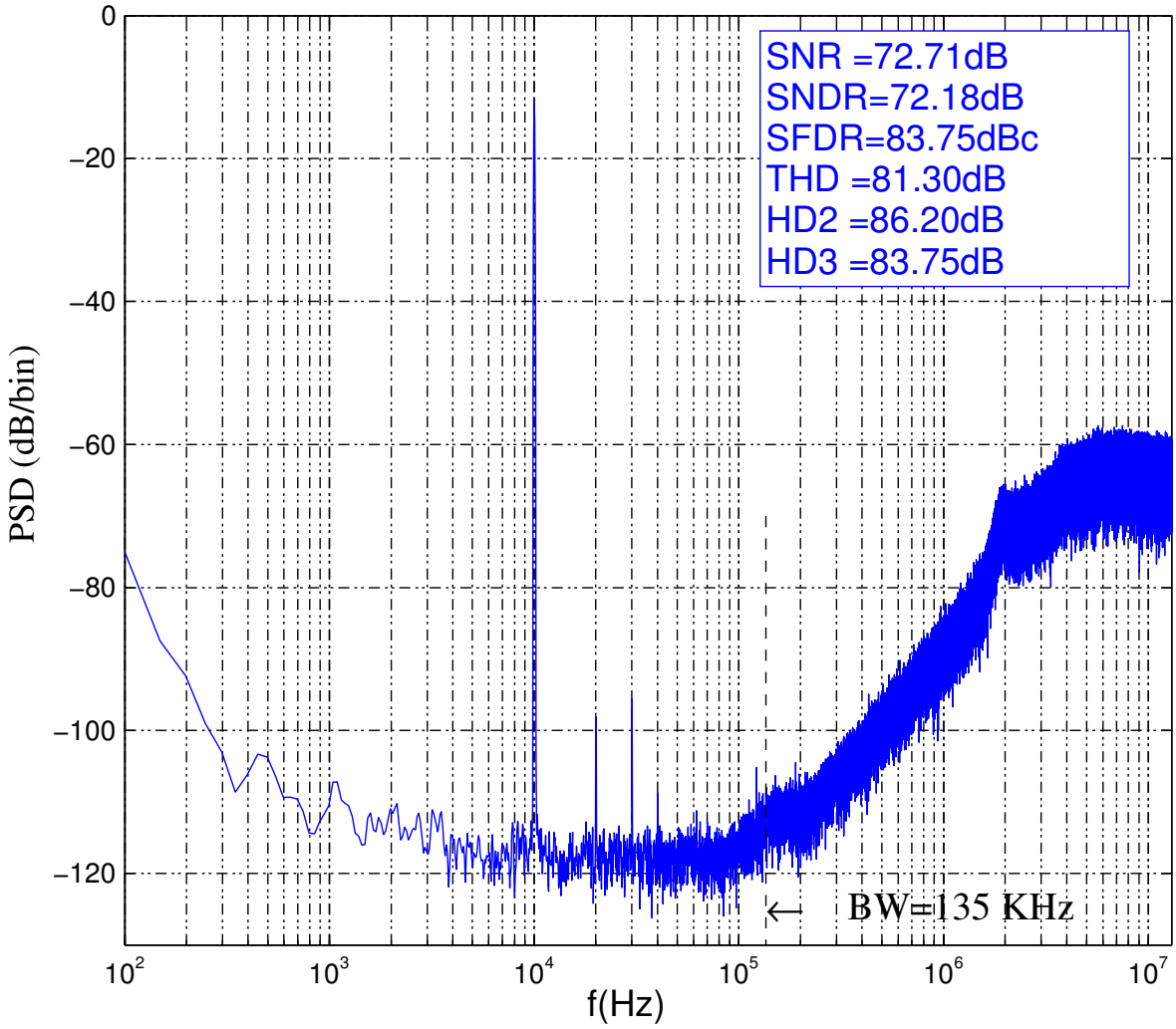


Figure 5.19: Output spectrum in the GSM/EDGE mode

ripple is lower than 0.01 dB. At 2MHz, a 4 dB peaking is observed. It is caused by the limited number of levels in the quantizer which cause a gain variation. This peaking must be taken into consideration during the design of the AAF to avoid saturating the modulator due to amplification of interferes that might exist at this frequency.

Fig. 5.21 shows the measured SNR and SNDR for a 10 KHz input sine and a f_{op} of 26 MHz. The peak SNR and SNDR are respectively, 80 dB and 78.5 dB. The DR of the ADC is 82 dB.

Some other tests were carried out to characterize all the aspects of the ADC in this mode. The results are summarized in Table 5.4.2.1. All this measures were achieved using the Rohde

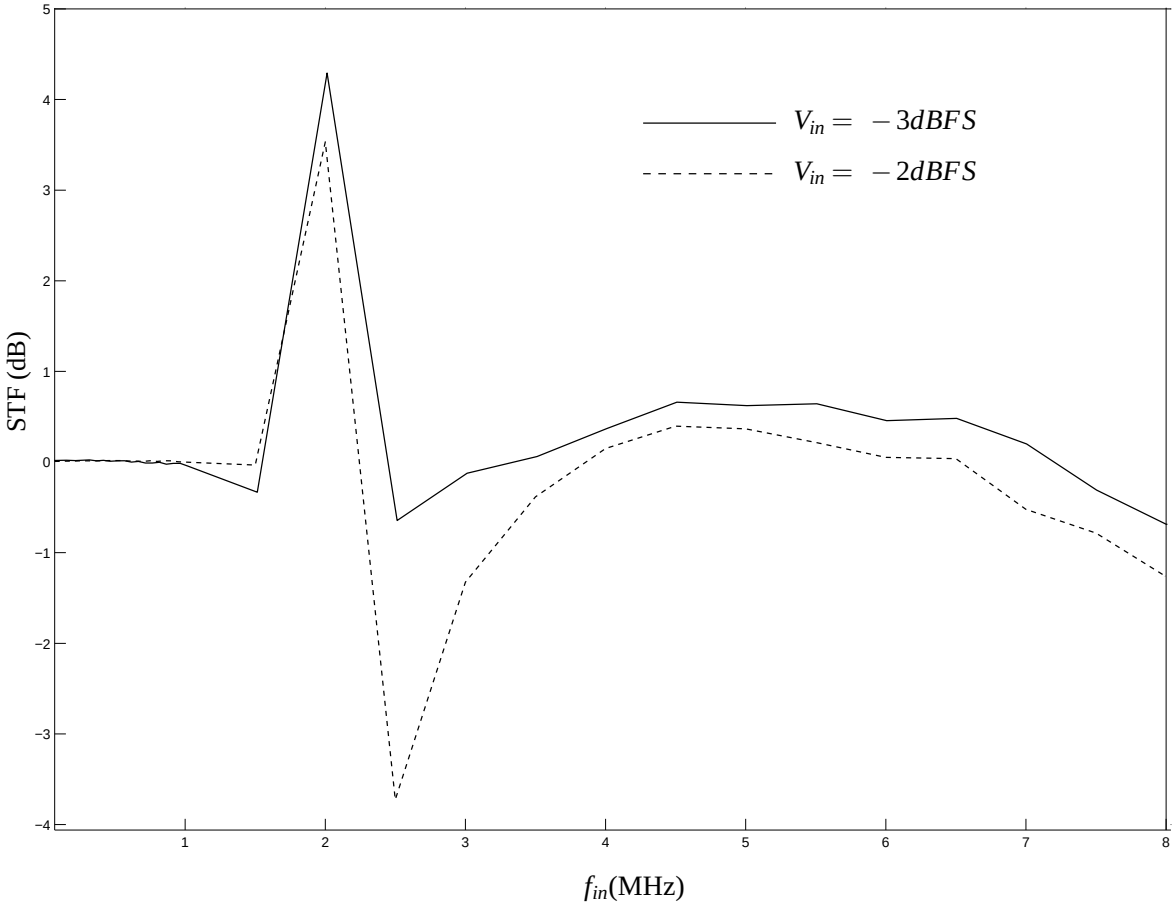


Figure 5.20: STF of the 2^{nd} order modulator

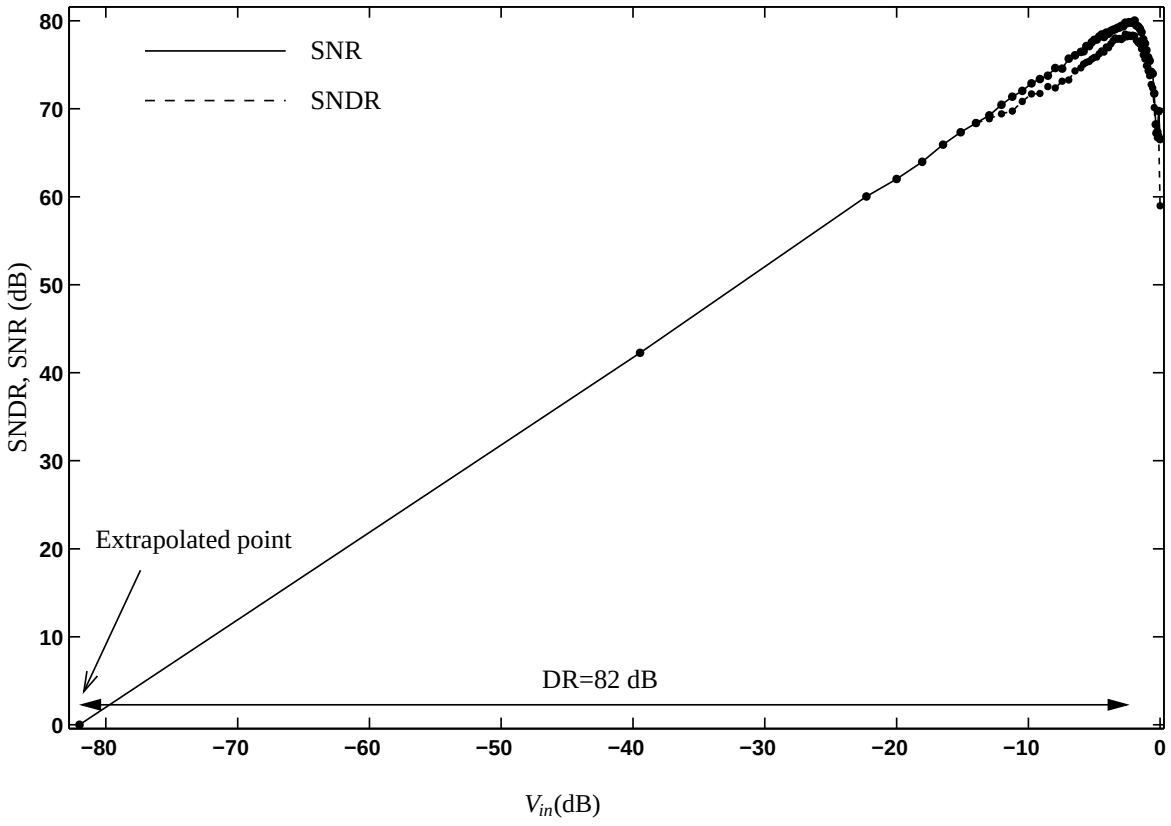


Figure 5.21: SNR and SNDR vs V_{in}

& Schwarz generator. The primary measures in this mode and all the measures in the two other modes were achieved using the Sony generator.

B	f_{op}	Clock jitter	Input offset	In Band tone	STF Ripple f<B	STF Ripple f>B	DR	Peak SNR	Peak SNDR
135 KHz	26 MHz	120 ps_{rms}	<1 mV	<-89 dBFS[1]	<0.01 dB	4 dB	82 dB	80 dB	78.5 dB

Peak THD	Peak SFDR	IM2	IM3	Input range	Power	FoM	Supply	Process	Core area
-85 dB	88 dBc	90 dBc	86 dBc	1.6 $V_{pp\ diff}$	1.74 mW (2)	0.94 pJ/conv	1.2 V	65 nm	0.081 mm^2

Table 5.4: Performances in the GSM/EDGE mode (1) Measured for shorted inputs (2) Reference voltages' generation is not included

5.4.2.2 UMTS/DVBT and WiFi/WiMax modes

For the UMTS/DVBT and WiFi/WiMax modes, the specifications were not reached because of two main problems:

1-DAC's mismatches

In the two considered modes, the 4^{th} order modulator is used. The global feedback DAC (DAC 3 in Fig. 5.3) is a multi-bit and therefore its sensitivity to mismatch must be dealt with to avoid degrading the resolution of the modulator. This can be achieved by employing calibration techniques [92] or/and dynamic element matching techniques[93] [94]. Some other approaches can be also used to handle this problem [95] [96]. However due to the limited design time, we decide to deal with this problem by tuning off-chip the reference voltages of the DAC. Unfortunately, no techniques were figured out to set these values accurately and as it can be seen in Fig. 5.22, very high harmonics were observed at the output of the 4^{th} order modulator. This spectrum was measured using the stand alone channel.

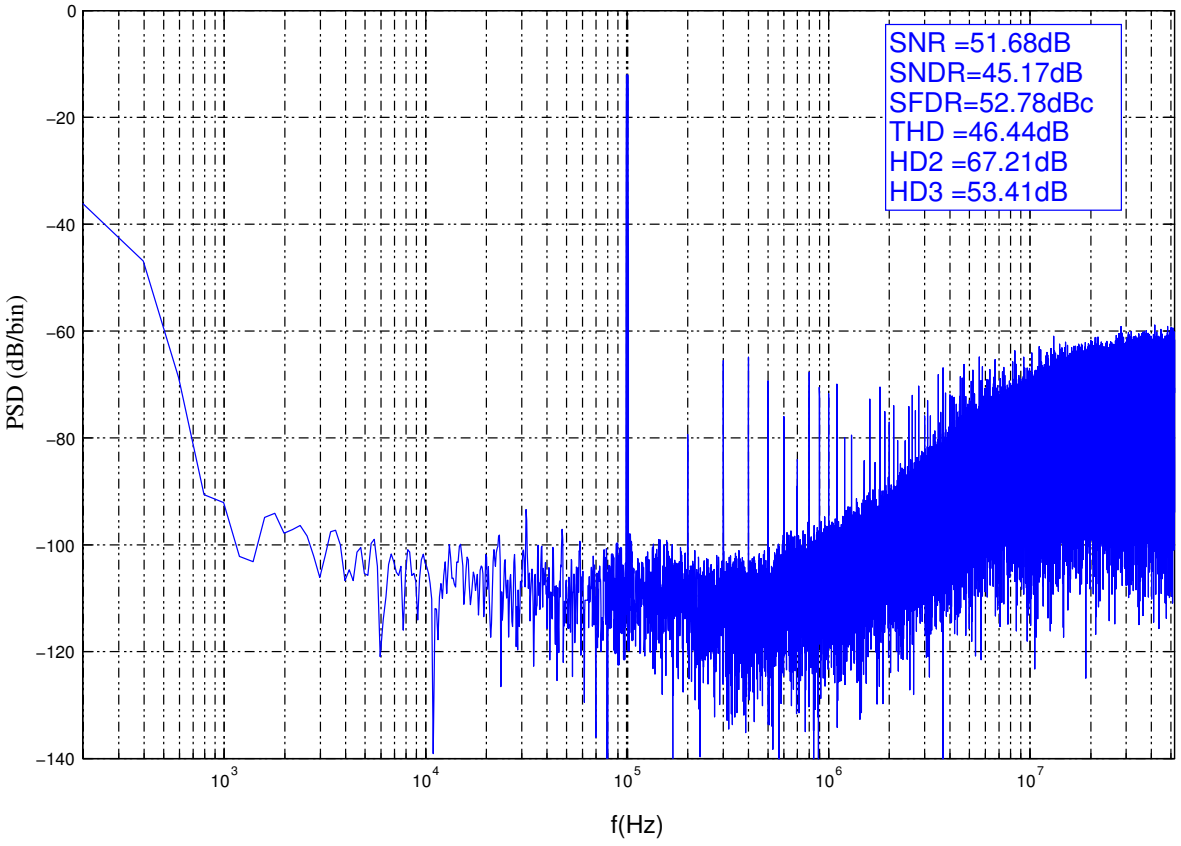


Figure 5.22: Output spectrum of the GMSCL modulator using the stand alone channel

2-SH's problem

The second problem was observed in the S/H. To illustrate it, we configured the TI $\Delta\Sigma$ ADC in a single channel scenario. If the S/H is operational, the output signal in this configuration must be identical to the signal obtained when using the stand alone channel. Unfortunately, the obtained spectrum, shown in Fig. 5.23 a), suffers from an increased noise floor and a very attenuation of the input signal. Interestingly, when the bias current of the S/H is decreased

from 125 μA to 50 μA, the input signal power is almost unchanged at the output and the noise floor is improved significantly.

Some investigations were conducted to understand the causes of the problem. The answer

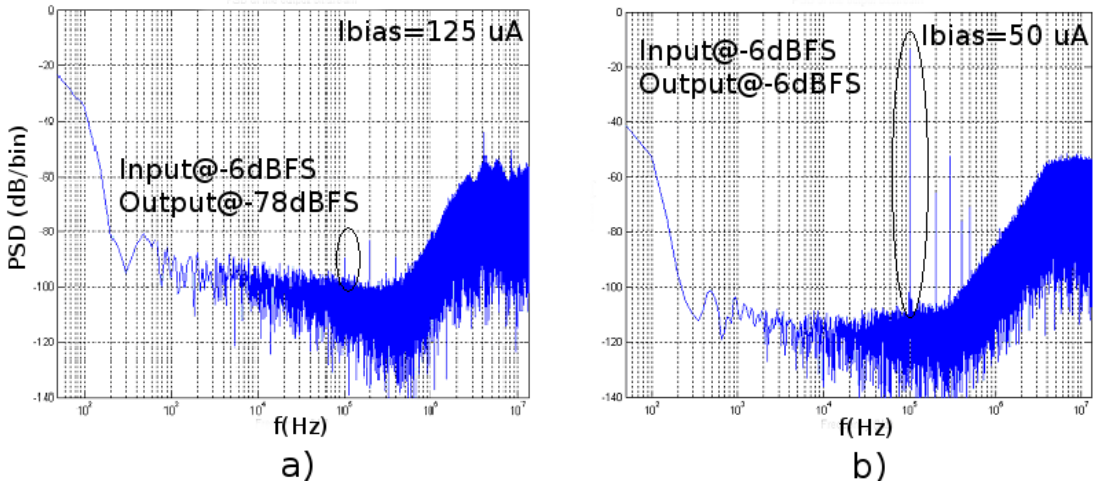


Figure 5.23: Output spectrum of a single channel of the TI $\Delta\Sigma$ ADC a) with Ibias = 125 μA b) with Ibias = 50 μA

came from the parasitic extraction of the S/H layout. This operation was not achieved during the circuit design because the tool was not available at that time. The extraction allowed to detect a biasing problem of the output stage of the S/H OTA due to a highly resistive wire. It caused a large voltage drop at the source of the PMOS transistor of the second stage of S/H's OTA as it can be seen in Fig. 5.24.

To examine the impact of this biasing problem, three simulations of the S/H were carried out: a) using the schematic before extraction with Ibias S/H = 125 μA (nominal current); b) using the extracted circuit with Ibias S/H = 125 μA; c) using the extracted circuit with Ibias S/H = 50 μA. The input is a 0.3 Vp 100 KHz sinusoidal signal. The results are shown in Fig. 5.25. A zoom around the input signal maximum is illustrated in Fig. 5.26. As it can be seen in Fig. 5.26 b), the S/H with the extracted schematic does not track the input signal it is in the nominal biasing conditions. However, when Ibias S/H is decreased, the S/H behaviour is significantly closer to the desired behaviour but it is not exactly as in Fig. 5.26 a). This causes the arising of harmonic tones in the spectrum of the simulated circuit. The values of these tones are very close of those of Fig. 5.23 b). In fact, the simulated HD2 is -48.65 dBc compared to a measured HD2 of -52.35 dBc and the simulated HD3 is -39.5 dBc compared to a measured HD3 of -39.5 dBc.

Thus, the problem can be summarized as follows: when the S/H is biased in the nominal conditions, the voltage drop at the output stage is very large. As a consequence, the PMOS of the output stage is not in the saturation region as designed. This causes a complete dysfunctionality of the OTA, hence the S/H. However, when the biasing current is decreased, the voltage drop is also decreased and thus the PMOS transistor is in saturation region. Nevertheless, since the saturation current is lower than desired, the performances of the OTA in terms of GBW and SR are lower thereby causing the arising of harmonic distortions.

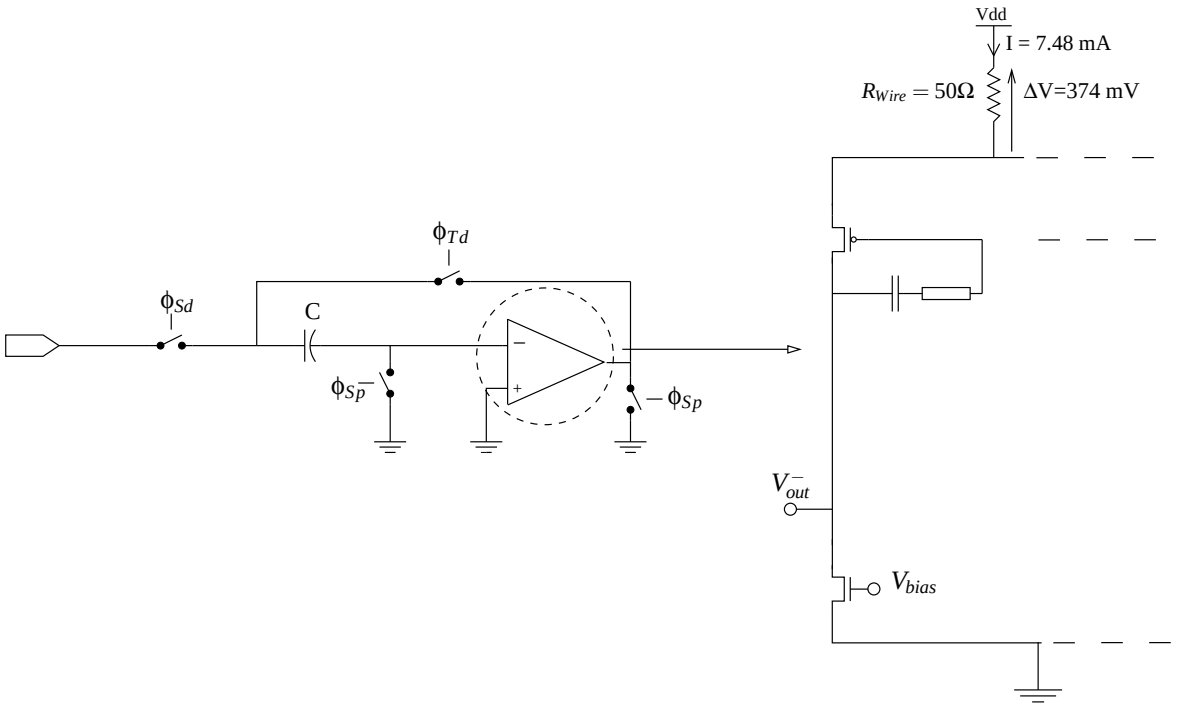


Figure 5.24: Biasing problem of the S/H

Functionality tests

The two exposed problems prevent us from characterizing the performances of the TI ΔΣ ADC. Nevertheless, some tests were carried out to validate its functionality.
Fig. 5.27 shows the output spectrums before decimation of the four channels for a ($M = 4$, $N = 52$) scenario. The input is a 10 KHz sinusoidal signal and the ADC is clocked at 26 MHz. According to Eqn. 4.1, N versions of the signal must appear around all the multiples $\frac{f_{op}}{N}$ due to the interpolation operation. The positions of the aliased tones in Fig. 5.27 are in accordance with Eqn. 4.1. Some other tests were carried out for different Ns and f_{in}s and all of them went along with Eqn. 4.1 thereby proving that the interpolation property of the ADC is functional.

Fig. 5.28 shows the output spectrums before decimation of the four channels for a ($M = 2$, $N = 32$) scenario. Similarly to the previous measure, the input is a 10 KHz sinusoidal signal and f_{op} is 26 MHz. It can be seen that the control on the number of channels is functional as well. Fig. 5.29 shows the reconstructed signal at the output of the TI ΔΣ ADC.

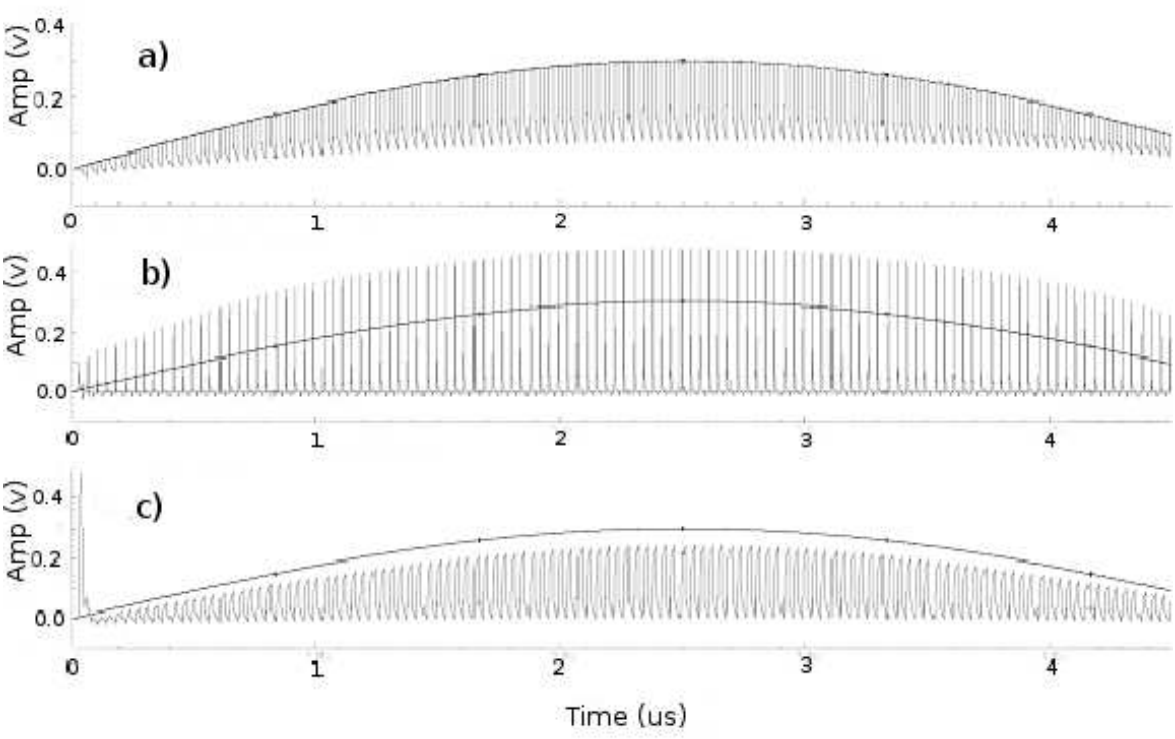


Figure 5.25: S/H output in time domain a) using the schematic before extraction with Ibias S/H = 125 μA (nominal current); b) using the extracted circuit with Ibias S/H = 125 μA; c) using the extracted circuit with Ibias S/H = 50 μA.

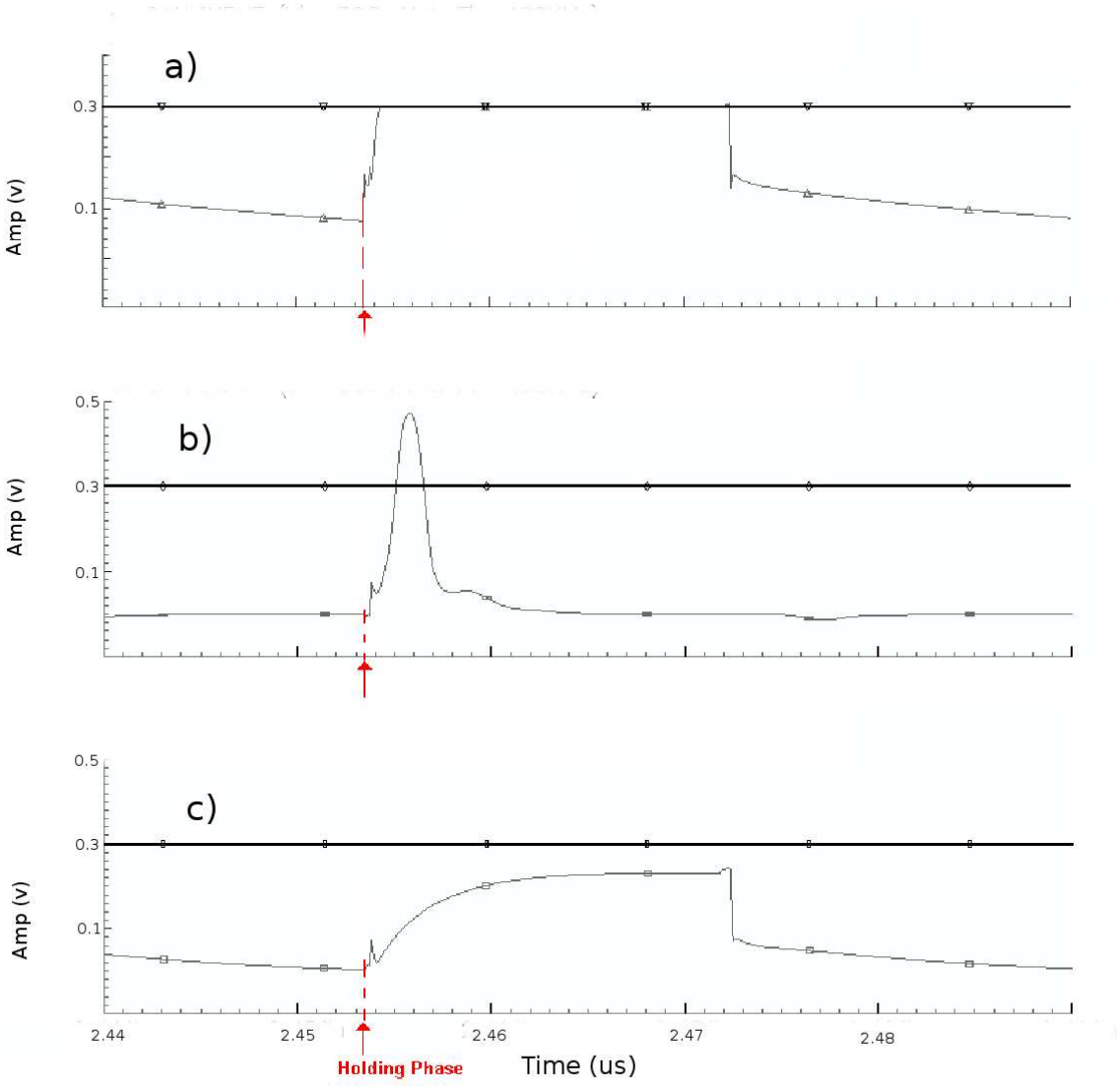


Figure 5.26: Zoom around the input signal maximum of Fig. 5.25

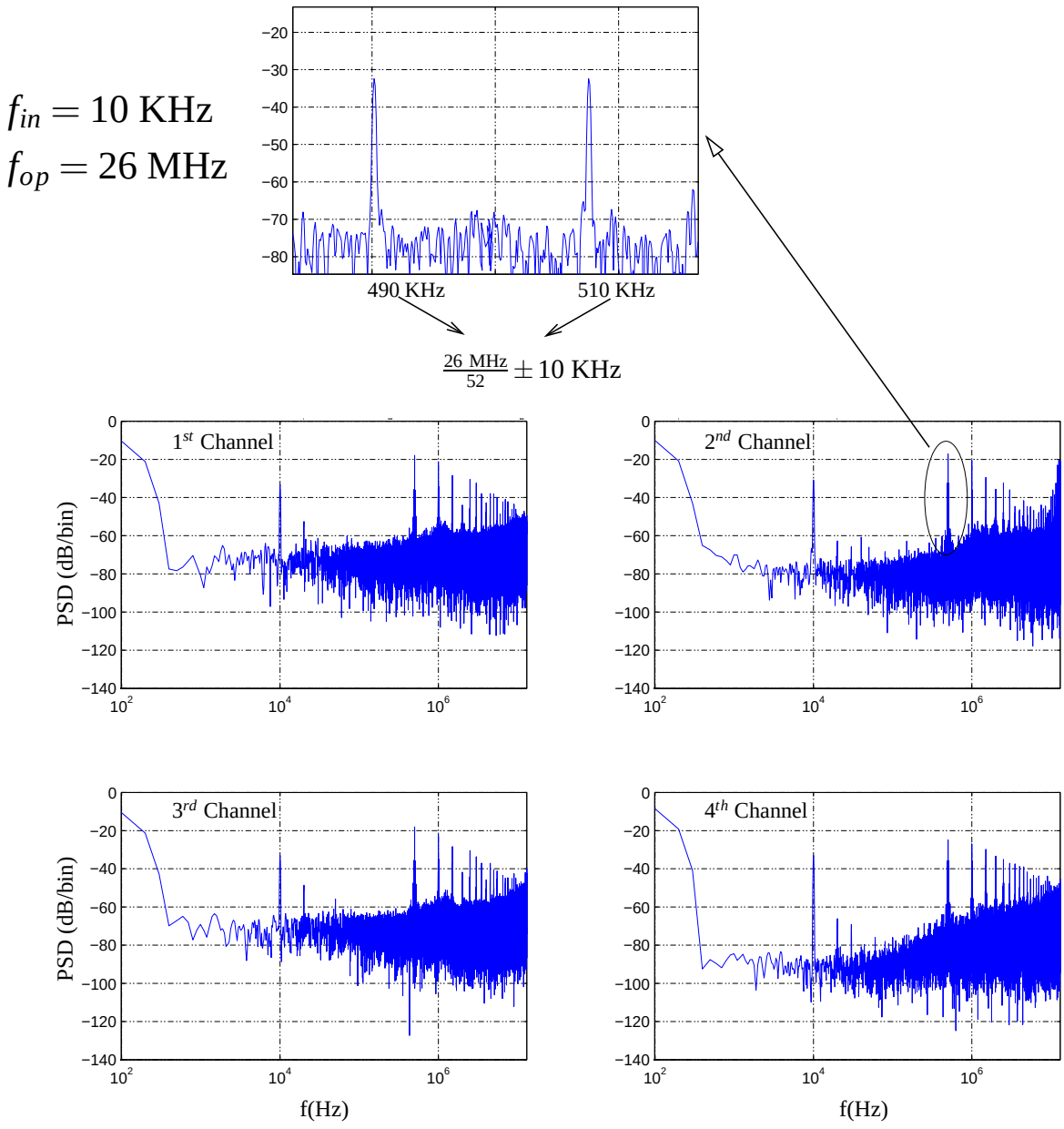


Figure 5.27: Channels' outputs for a ($M = 4$, $N = 52$) scenario

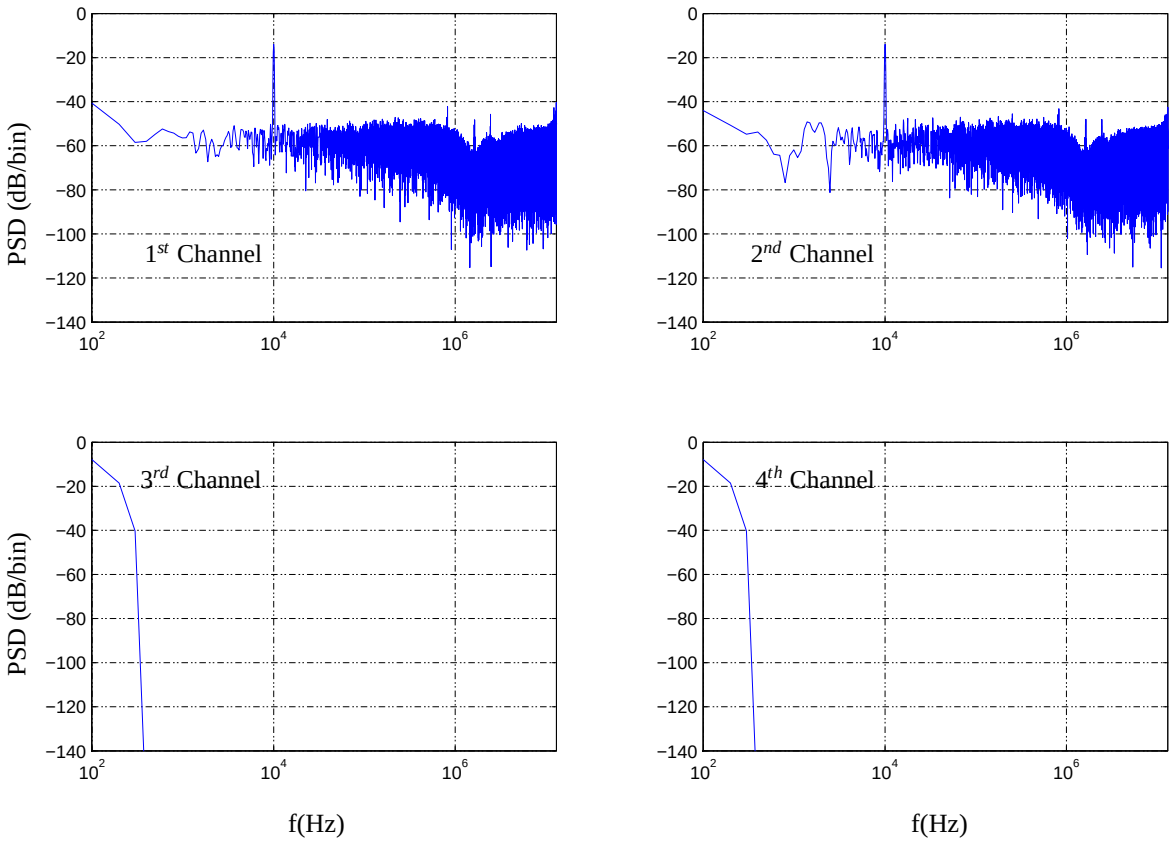


Figure 5.28: Channels' outputs for a ($M = 2$, $N = 32$) scenario

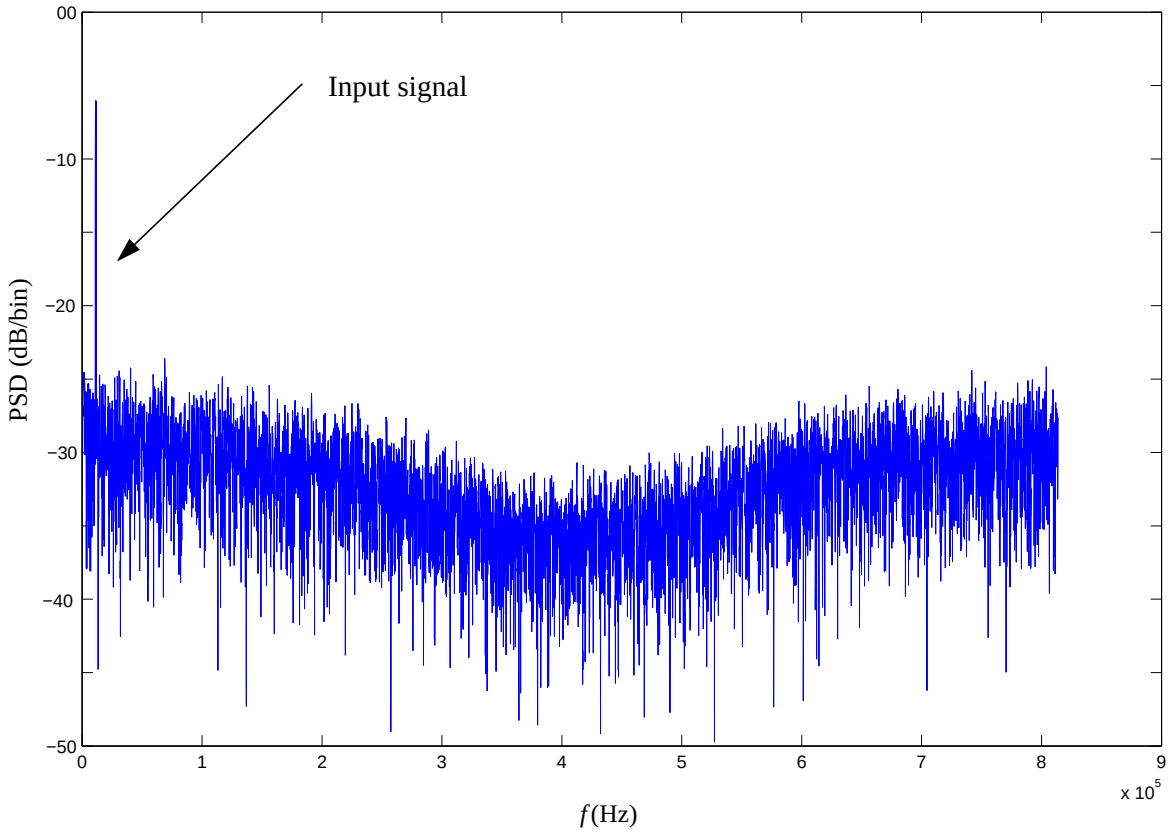


Figure 5.29: Reconstructed signal for a ($M = 2$, $N = 32$) scenario

5.5 Conclusion

The design, the layout and the test of a four channels TI $\Delta\Sigma$ ADC suited for the radio standards have been presented. The specifications were reached in the GSM/EDGE mode. In the UMTS/DVBT and WiFi/WiMax modes, the performances were not secured because of a biasing problem in the S/H and a mismatch problem in the feedback DAC.
The ADC has four reconfigurable parameters: f_{op}, L, N and M, which allow it to perform bandwidth-resolution-power consumption exchanges. The tests on the reconfigurability of the ADC were successful.
The corrupted signals in the TI mode prevent the evaluation of the calibration technique exposed in Chapter 4. The verification of the reconfigurability on $f_{S/H}$ was not possible due to the same reason as well.

Ref	B	f_{op}	Input	SNDR	DR	P	FoM	Supply	Process
[97]	100 KHz	50 MHz	1.6 Vpp	77 dB	85 dB	3.43 mW	2.86 pJ/conv	1.2 V	90 nm
[98]	100 KHz	26 MHz	1.4 Vpp	85 dB	88 dB	2.9 mW	0.99 pJ/conv	1.2/3.3 V	130 nm
[99]	100 KHz	48 MHz	1.6 Vpp	84 dB	85 dB	3.3 mW	1.27 pJ/conv	1.2 V	65 nm
[100]	100 KHz	39 MHz	0.8 Vpp	81 dB	82 dB	2.4 mW	1.31 pJ/conv	1.2 V	130 nm
This work	135 KHz	26 MHz	1.6 Vpp	78.5 dB	82 dB	1.74 mW	0.94 pJ/conv	1.2 V	65 nm

Table 5.5: Performance comparison for the GSM/EDGE mode

Ref	B	f_{op}	M	Input	SNDR	DR	P	FoM	Supply	Process
[97]	2 MHz	320 MHz	1	1.6 Vpp	65 dB	66 dB	6.83 mW	1.2 pJ/conv	1.2 V	90 nm
[98]	1.92 MHz	61.44 MHz	1	1.4 Vpp	77 dB	79 dB	7.4 mW	0.3 pJ/conv	1.2/3.3 V	130 nm
[101]	3.125 MHz	50 MHz	1	1.4 Vpp	73.9 dB	-	22 mW	2.57 pJ/conv	1.8 V	180 nm
[102]	4 MHz	100 MHz	1	1 Vpp	66.8 dB	69.6 dB	11.76 mW	0.82 pJ/conv	1.2/3 V	90 nm
[103]	4.2 MHz	100 MHz	2	1.44 Vpp	81 dB	83 dB	28 mW	0.48 pJ/conv	1.5 V	180 nm
This work	4 MHz	208 MHz	2	1.6 Vpp	80 dB (1)	-	55 mW (2)	0.84 pJ/conv	1.2 V	65 nm

Table 5.6: Performance comparison for the UMTS/DVBT mode (1) Targeted SNDR (2) Measured power consumption

Ref	B	f_{op}	M	Input	SNDR	DR	P	FoM	Supply	Process
[98]	10 MHz	240 MHz	1	0.7 Vpp	63 dB	67 dB	20.5 mW	0.9 pJ/conv	1.2/3.3 V	130 nm
[104]	20.48 MHz	330 MHz	1	1.3 Vpp	63 dB	-	78 mW	1.5 pJ/conv	1.4 V	90 nm
[105]	12.5 MHz	200 MHz	1	1.6 Vpp	82 dB	84 dB	200 mW	3.9 pJ/conv	1.8 V	180 nm
This work	12.5 MHz	208 MHz	4	1.6 Vpp	52 dB (1)	-	110 mW (2)	8 pJ/conv	1.2 V	65 nm

Table 5.7: Performance comparison for the WiFi/WiMax mode (1) Targeted SNDR (2) Measured power consumption

Tables 5.5, 5.6 and 5.7 compare this work in the three modes to state of the art ADCs. For the UMTS/DVBT and WiFi/WiMax modes, the SNDR value in the two tables is the targeted resolution and the power consumption is the measured one. This gives an idea on the performance of the ADC if the specifications would have been reached in these two modes.
It can be noted that the achieved FoM in the GSM/EDGE mode and the targeted FoM in the UMTS/DVBT mode are in the same order of magnitude of the other FoMs. In the WiFi/WiMax modes, the FoM is significantly higher in this work compared to the other ADCs. A reconfiguration of OTAs to relax the constraints on them, hence to decrease their power consumption would have been possible since the targeted resolution in this mode is lower than in UMTS/DVBT mode. This would have improved the FoM but increased the design time.

In [98], it has been shown that the digitization of the targeted standards is possible using a single channel while maintaining a low power consumption. This means that larger bandwidths should have been targeted for the prototype in order to profit from the potential of the TI architecture.

Chapter 6

Conclusions and perspectives

6.1 Conclusions

This work focused on the design of a reconfigurable parallel ΔΣ ADC.

Chapter 2 discussed parallelism. It showed that when the sampling frequency exceeds a threshold value f_{lr}, the use of parallelism optimizes the FoM compared to a one channel solution. The value of f_{lr} depends on many parameters such as: the process, the targeted resolution, the complexity of the channel mismatch correction ...

Chapter 3 analysed ΔΣ modulators. A DT implementation was preferred to a CT or hybrid implementation because it is more robust against clock jitter and loop delay and especially is more prone to reconfigurability. On the other hand, a LP modulator was preferred to a HP modulator because of the high sensitivity to clock jitter and signal sampling errors of latter.

Chapter 4 reviewed parallel ΔΣ ADCs. The TI ΔΣ architecture was retained over the block filtering, the FBD and the ΠΔΣ architectures because it offered the best compromise in terms of complexity, reconfigurability and design time. A novel interpolation technique was proposed to address the sensitivity of the TI architecture to thermal noise. This interpolation technique uses extra samples resulting from the oversampling of the input signal instead of zeros and distributes them in a manner that does not cause aliasing due to the decimation operation that follows the ΔΣ modulator.

Chapter 5 presented the design in a 1.2 V 65 nm CMOS process of a four channels TI ΔΣ ADC using the novel interpolation technique. A LP DT feedforward architecture was employed when the modulator was configured as a 2^{nd} order and a LP DT GMSCL architecture when configured as a 4^{th} order. The ADC has four reconfigurable parameters: f_{op}, L, N and M, which allow it to perform bandwidth-resolution-power consumption exchanges. The tests on the reconfigurability of the ADC were successful.
In the GSM/EDGE mode, the prototype achieved 82 dB of dynamic range, a peak SNR of 80 dB and a peak SNDR of 78.5 dB. The power consumption is 1.74 mW and the operation frequency is 26 MHz. In the UMTS/DVBT and WiFi/WiMax modes, the performances were not secured because of a biasing problem in the S/H and a mismatch problem in the feedback DAC. Nevertheless, the functionality of the TI ΔΣ ADC was tested successfully.

6.2 Perspectives

A first perspective of this work is to propose a methodology to determine accurately the threshold frequency f_{lr} for oversampling converters. This methodology could be based on the approach presented in chapter 2 or on another approach. The difficulty for $\Delta\Sigma$ ADCs lies in the diversity of possibilities of implementing a modulator suited for a given scenario. In fact, several freedom degrees such as the modulator architecture and order, the oversampling ratio, the number of bits of the quantizer are the parameters to design a modulator. All of these parameters intervene in establishing the relation between power consumption and conversion bandwidth and thus should be taken into consideration to determine an optimized value of f_{lr}.

A second research perspective is to examine new possibilities for the reconfiguration. Here are some ideas:

In chapter 3, it was shown that a HP filter could be reconfigured in a LP integrator by switching off the chopping mechanism. Hence, a LP/HP reconfiguration of the modulator could be achieved just by turning Off or On the chopping mechanisms and by choosing the correct signs for the feedback and feedforward coefficients. This requires a few number of digital gates. This feature can be very interesting in the case of a reconfigurable low-IF/zero IF receiver.

Another reconfiguration possibility could be achieved at the OTA level. In fact, in our design, the reference current and the size of some transistors of the OTA were reconfigured to allow an efficient operation for different operation frequencies. Another idea of reconfiguration at this level is to perform a voltage swing to power consumption exchange. For example, in our ADC, the thermal noise constraints are lower for the WiFi/WiMax mode than for the UMTS/DVBT mode. As a consequence, the reference voltage and the input voltage amplitude could be reduced without affecting the resolution of the ADC. This will reduce the output voltage swing and slew rate requirements on the OTAs and consequently, a reconfiguration to avoid unnecessary power consumption could be considered.

Appendix A

CMOS Design

A.1 OTA design flow

With the scaling down of technology, the design of analog blocks and especially operational transconductance amplifiers (OTAs) has become more and more difficult. For this purpose, there is a need for a methodology to design OTAs that possess high robustness face to undesired effects such as process variation, operation environments' variation or ageing. In this section, the employed designed flow for OTAs is described. For sake of simplicity, this methodology is presented for the differential pair with active load simple architecture shown in Fig. A.2.a) but could be extended for any other architecture.

A.1.1 Technology parameters extraction

The first step in the design of an analog block is to determine the technology parameters. These parameters can be extracted using simple electrical simulations. In fact, a $I_{ds} = f(V_{gs})$ DC simulation allows to extract first μC_{ox} and V_{th0}. Once V_{th0} determined, the subthreshold mode's parameters ξ and I_0 can be figured out using the same simulation. As for λ, it can be determined by means of a $I_{ds} = f(V_{ds})$ simulation. Regarding γ, a noise analysis should be carried out to evaluate its value. Table. A.1.1 shows the extracted values for the employed 1.2 V 65 nm CMOS technology.

V_{thp0}	V_{thn0}	$\mu_n C_{ox}$	$\mu_p C_{ox}$	λ	ξ	I_0	γ
0.312 V	0.29 V	272 μA/V^2	80 μA/V^2	0.3/L	1.48	0.28 nA	0.69

Table A.1: Extracted parameters

Capacitance	expression
C_{gs}	$\frac{2}{3}WLC_{ox} + WL_{overlap}C_{ox}$
C_{gd}	$WL_{overlap}C_{ox}$
C_{sb}	$(Area\ _{source\ diode} + WL)\frac{C_{j0}}{\sqrt{1+V_{SB}/\Phi_0}}$
C_{db}	$(Area\ _{drain\ diode})\frac{C_{j0}}{\sqrt{1+V_{DB}/\Phi_0}}$

Table A.2: MOS transistor parasitic capacitances' equations in saturation region

A.1.2 OTA operation analysis

The second step of the proposed design flow consists of computing the different equations that describe the OTA operation using MOS transistors' first order equations.

A.1.2.1 Differential AC mode

Fig. A.2.b) shows the equivalent half circuit of the differential pair OTA in differential mode which is obtained by grounding all common nodes[56] [106].

A.1.2.2 Transfer function

Using the small signal equivalent circuit shown in Fig. A.3, the transfer function can be found
$C_{in} = C_{gs1} \qquad C_{out} = C_L + C_{db1} + C_{gd3} + C_{db3}$

$V_{out}(p) = V_{in}(p) - \frac{I_2}{C_{gd1}p}$

$V_{out}(p) = V_{in}(p) - \frac{gm_1 V_{in}(p) + gm_3 V_{gs3} + V_{out}(p)/Z_{eq}(p)}{C_{gd1}p}$

$Z_{eq}(p) = r_{o1}//r_{o3}//C_{out} = \frac{r_{o1}r_{o3}}{r_{o3}+r_{o1}+r_{o1}r_{o3}C_{out}p}$

$V_{out}(p) = \frac{(Z_{eq}(p)C_{gd1}p - gm_1 Z_{eq}(p))V_{in}(p) - gm_3 Z_{eq}(p)V_{gs3}}{Z_{eq}(p)C_{gd1}p+1}$

$A(p) = \frac{\delta V_{out}(p)}{\delta V_{in}(p)} = \frac{(Z_{eq}(p)C_{gd1}p - gm_1 Z_{eq}(p))}{Z_{eq}(p)C_{gd1}p+1}$

$A(p) = \frac{r_{o1}r_{o3}}{r_{o3}+r_{o1}} \frac{C_{gd1}p - gm_1}{\frac{r_{o1}r_{o3}}{r_{o3}+r_{o1}}(C_{gd1}+C_{out})p+1}$

The OTA DC gain is the gain for the frequency zero.
$A_{DC} = A(0) = -gm_1 Z_{eq}(0) = -gm1\frac{r_{o1}r_{o3}}{r_{o3}+r_{o1}}$

One Zero $\omega_z = \frac{g_{m1}}{C_{gd1}}$; One Pole $\omega_p = \frac{r_{o1}+r_{o3}}{r_{o1}r_{o3}(C_{gd1}+C_{out})}$

$GBW = A(0)\omega_p = \frac{gm_1}{C_{gd1}+C_{out}}$

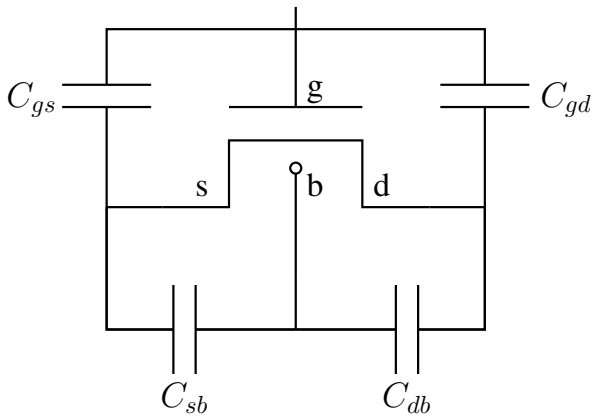


Figure A.1: MOS transistor parasitic capacitances

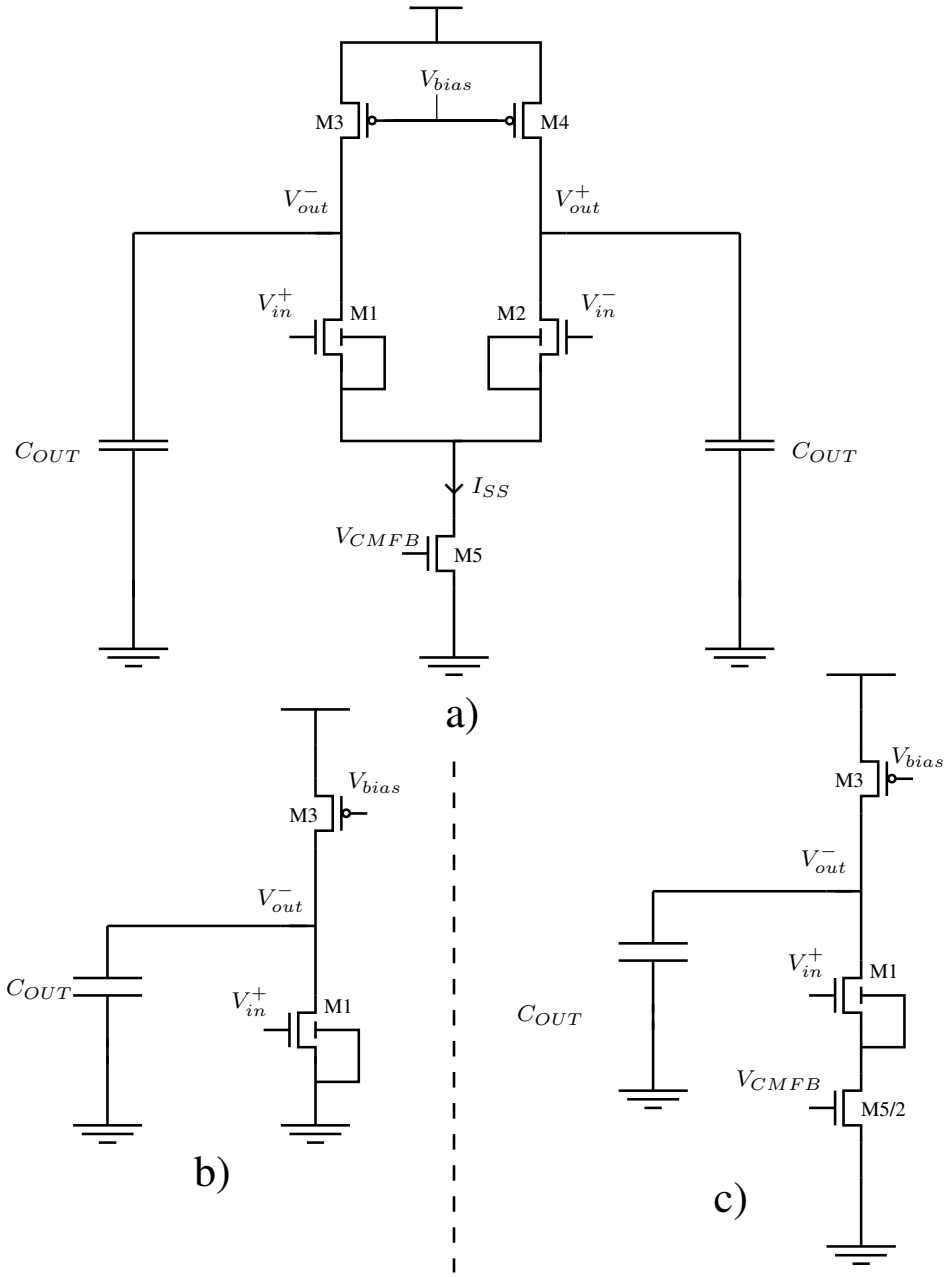


Figure A.2: a)Differential pair b)Equivalent half-circuit in differential mode c)Equivalent half-circuit in common mode

Input referred noise

To calculate the expression of the input referred noise, the contribution of each noise source must be first determined separately.

$$V^2_{1-2}(f) = \frac{I^2_{ds\ 1-2}(f)}{gm_1^2} \qquad V^2_{3-4}(f) = \frac{I^2_{ds\ 3-4}(f)}{gm_1^2}$$

$$V^2_{1-2}(f) = \underbrace{\frac{4K_{Bol}T\gamma}{gm_1}}_{A} + \underbrace{\frac{KF_n}{2\mu_n C_{ox} W_1 L_1 f}}_{B}$$

A is the contribution of the thermal noise and B the contribution of the flicker noise[107].

$$V^2_{3-4}(f) = (\frac{4K_{Bol}T\gamma}{gm_3} + \frac{KF_P}{2\mu_P C_{ox} W_3 L_3 f})(\frac{gm_3}{gm_1})^2$$

Assuming that $V_{1-2}(f)$ and $V_{3-4}(f)$ are not correlated, the overall input referred noise is given by:

$$V^2_{OTA}(f) = V^2_{1-2}(f) + V^2_{3-4}(f)$$

$$V^2_{OTA}(f) = \frac{4K_{Bol}T\gamma}{gm_1} + \frac{KF_n}{2\mu_n C_{ox} W_1 L_1 f} \ + \ (\frac{4K_{Bol}T\gamma}{gm_3} + \frac{KF_P}{2\mu_P C_{ox} W_3 L_3 f})(\frac{gm_3}{gm_1})^2$$

Input referred offset

In the previous study, OTA's half circuits were assumed to be perfectly symmetric. However, in reality, supposedly identical transistors do not share the exact same properties due to multiple effects that occur during manufacturing. These mismatches produce offset and even order harmonics. To establish the expression of the input referred offset, two DC sources will

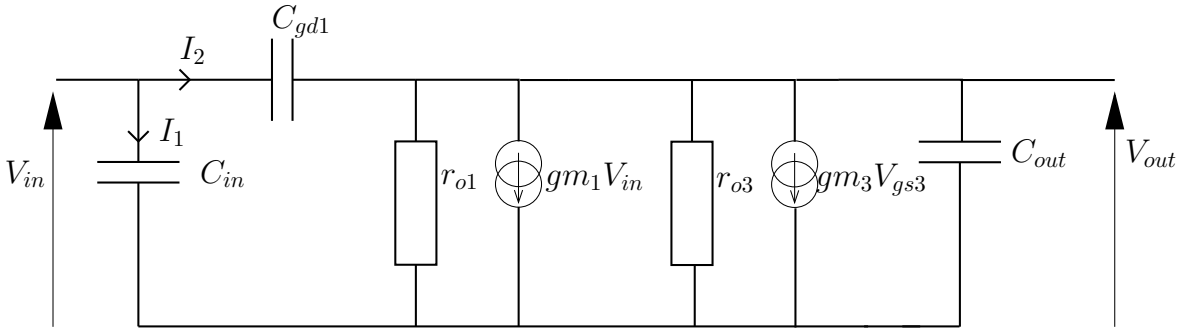


Figure A.3: Small signal equivalent circuit in differential mode

be added to impose that $I_1 = I_2$ and $I_3 = I_4$.
$I_3 = \frac{1}{2}\mu_p C_{ox}\frac{W_3}{L_3}(V_{gs3} - \mid V_{th3} \mid)^2$

$I_4 = \mu_p C_{ox}\frac{W_4}{L_4}(V_{gs4} - \mid V_{th4} \mid)^2$

$I_3 = I_4 \Rightarrow \frac{W_3}{L_3}(V_{gs3} - \mid V_{th3} \mid)^2 = \frac{W_4}{L_4}(V_{gs4} - \mid V_{th4} \mid)^2$

Let us pose $\Delta\frac{W}{L} = \frac{W_3}{L_3} - \frac{W_4}{L_4}$ and $\Delta V_{thp} = V_{th3} - V_{th4}$ and by using the approximation $\sqrt{1+\epsilon} \simeq 1 + \frac{\epsilon}{2}$, the expression of V_{offp} is obtained:

$V_{off\ p} = V_{gs4} - V_{gs3} = \frac{\Delta\frac{W}{L}_p}{2\frac{W}{L}_p}(V_{gs\ 3-4} - \mid V_{thp} \mid) + \Delta V_{thp}$

Similarly, the expression of V_{offn} can be found.

$V_{off\ n} = V_{gs2} - V_{gs1} = \frac{\Delta\frac{W}{L}_n}{2\frac{W}{L}_n}(V_{gs\ 1-2} - V_{thn}) + \Delta V_{thn}$

The overall input referred offset is the sum of the input pair offset and the load offset input referred $V_{off\ in} = V_{off\ n} + \frac{g_{m3}}{g_{m1}}V_{off\ p}$

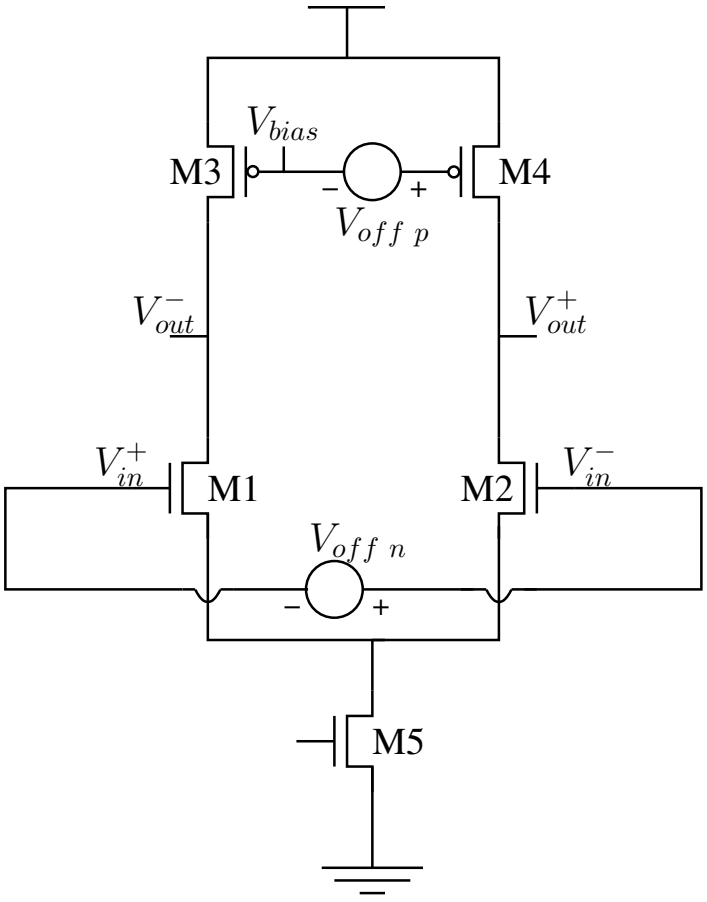


Figure A.4: Differential pair with inserted offset

A.1.2.3 Common mode

For common mode analysis, the equivalent half circuit shown in Fig. A.2.c) is obtained by dividing by two the width of all common transistors[56].

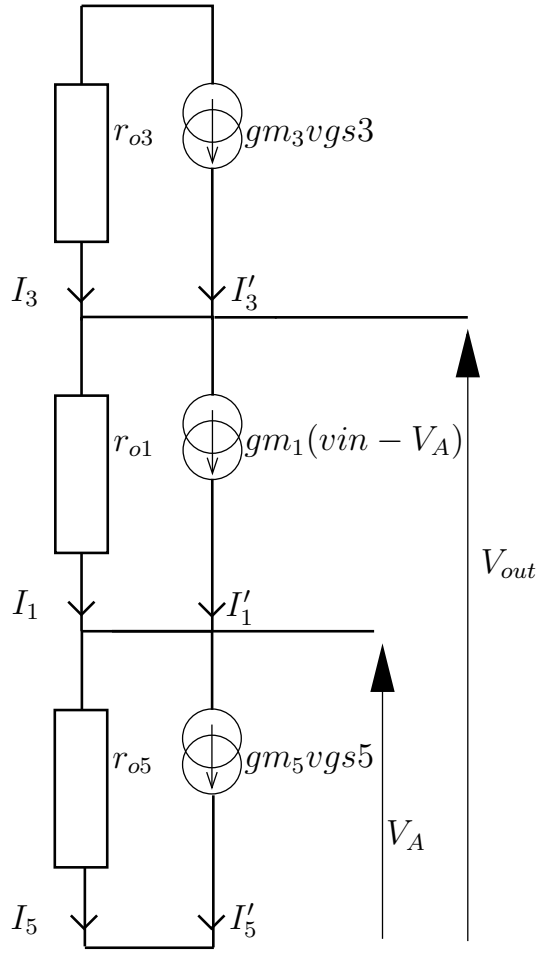


Figure A.5: Small signal equivalent circuit in common mode

$I_3 = I'_1 + I_1 - I'_3 \quad I_1 = I'_5 + I_5 - I'_1$

$V_A = r'_{o5} I_5 = r_{o5}(I_1 + I'_1 - I'_5)$

$V_A = r_{o5}(\frac{V_{out} - V_A}{r_{o1}} + gm_1(V_{in} - V_A) - gm5' V_{gs5})$

$V_A = \frac{r_{o5} V_{out} + gm_1 r'_{o5} r_{o1} V_{in} - gm'_5 r'_{o5} r_{o1} V_{gs5}}{r_{o1} + r'_{o5} + r_{o1} r'_{o5} gm_1}$

$V_{out} = V_A + r_{o1} I_1 = V_A + r_{o1}(I'_3 + I_3 - I'_1)$

$V_{out} = V_A + r_{o1}(\frac{Vdd - V_{out}}{r_{o3}} + gm_3 V_{gs3} - gm_1(V_{in} - V_A))$

$V_{out} = f_1 V_{in} + f_2 V_{gs3} + f_3 V_{gs5} + f_4 Vdd$

$f_1 = -\frac{r_{o1}r_{o3}gm_1}{r_{o1}+r_{o3}+r'_{o5}+r_{o1}r'_{o5}gm_1}$

$f_2 = \frac{r_{o3}gm_3(r_{o1}+r'_{o5}+r_{o1}r'_{o5}gm_1)}{r_{o1}+r_{o3}+r'_{o5}+r_{o1}r'_{o5}gm_1}$

$f_3 = -\frac{r'_{o5}r_{o3}gm'_5(1+r_{o1}gm_1)}{r_{o1}+r_{o3}+r'_{o5}+r_{o1}r'_{o5}gm_1}$

$f_4 = \frac{r_{o1}+r'_{o5}+r_{o1}r'_{o5}gm_1}{r_{o1}+r_{o3}+r'_{o5}+r_{o1}r'_{o5}gm_1}$

The common gain CM Gain$= \frac{\delta V_{out}}{\delta V_{in}} = f_1$

Parameter	expression
DC Gain	$gm_1 \frac{ro_1 ro_3}{ro_1 + ro_3}$
SR	$\frac{ISS}{C_{out}}$
GBW	$\frac{gm_1}{C_{out}}$
Slew Rate(SR)	$\frac{ISS}{C_L}$
ZERO	$\frac{g_{m1}}{C_{gd1}}$
V_{in}^2	$\frac{4K_{Bol}T\gamma}{gm_1} + \frac{KF_n}{2\mu_n C_{ox} W_1 L_1 f} + (\frac{4K_{Bol}T\gamma}{gm_3} + \frac{KF_P}{2\mu_P C_{ox} W_3 L_3 f})(\frac{gm_3}{gm_1})^2$
IR offset	$\frac{\Delta\frac{W}{L}_n}{2\frac{W}{L}_n}(V_{gs\ n} - V_{thn}) + \Delta V_{thn} + \frac{g_{m3}}{g_{m1}}(\frac{\Delta\frac{W}{L}_p}{2\frac{W}{L}_p}(V_{gs\ p} - \mid V_{thp} \mid) + \Delta V_{thp})$
HD3[56]	$\frac{A^2}{32(V_{gs\ 1} - Vth\ 1)^2}$
CM gain	$-\frac{r_{o1}r_{o3}gm_1}{r_{o1}+r_{o3}+2r_{o5}+2r_{o1}r_{o5}gm_1}$
Output swing	Vdd-3$V_{overdrive}$

Table A.3: OTA equations

A.1.3 Design Methodology

The third step of the methodology is the design. First, the OTA specifications must be fixed. For sake of simplicity, an example scenario (table. A.4) is considered. Targeting the specifications of table.A.4 would probably permit to design an OTA which reach the required specifications in the typical operation environment. However, a good designer should keep in mind that some environment variations such as temperature, supply voltage and process variations can degrade the OTA performance. Therefore, to ensure that the OTA meets the needs for all considered corners, the targeted specifications must be oversized with respect to the required ones Table.A.5 shows the targeted specifications. The oversizing ratio of each parameter is fixed by the common sense of the designer and his knowledge of the used technology. This operation may be repeated several times if electrical simulations show that the considered margins were too large or not enough for some cases. Two parameters can be deduced easily from the table:

GBW	SR	A_{dc}	C_L	Output swing
700 MHz	700 V/μs	20 dB	0.5 pF	0.45 V

Table A.4: OTA required specifications

GBW	SR	A_{dc}	C_L	Output swing
1 GHz	1000 V/μs	25 dB	0.5 pF	0.6 V

Table A.5: OTA targeted specifications

$GBW = \frac{gm_1}{C_L} \Rightarrow gm_1 = GBW.C_L$

$SR = \frac{ISS}{C_L} \Rightarrow ISS = SR.C_L$

$(\frac{W}{L})_1 = \frac{gm_1^2}{ISS\mu_n C_{ox}} = \frac{GBW^2 C_L}{\mu_n C_{ox} SR}$

For M_3 and M_5, the overdrive voltages should be chosen. Since Vdd is equal to 1.2 V and the targeted swing is equal to 0.6 V, 0.6 V are available to saturate M_1, M_3 and M_5. Therefore, 0.25 V will be reserved for M_1 and 0.35 V will be used to saturate M_3 and M_5:0.2 V for M_5 and 0.15 V M_3.

$gm_3 = \frac{ISS}{V_{overdrive3}}$

$(\frac{W}{L})_3 = \frac{gm_3^2}{ISS\mu_p C_{ox}} = \frac{SR.C_L}{\mu_p C_{ox} V_{overdrive3}^2}$

$gm_5 = \frac{2ISS}{V_{overdrive5}}$ $(\frac{W}{L})_5 = \frac{gm_5^2}{2ISS\mu_n C_{ox}} = \frac{2SR.C_L}{\mu_p C_{ox} V_{overdrive5}^2}$

Concerning transistors' length, the couple (L_1 L_3) fixes A_{dc} . Therefore, a value for L_1 will be choosen based on common sense and then the L_3 recquired to achieve the desired DC gain will be determined. $r_{o1} = \frac{2L_1}{K_{\lambda 1} ISS}$ $r_{o3} = \frac{2L_3}{K_{\lambda 3} ISS}$

$L_3 = \frac{L_1.A_{dc}.K_{\lambda 3}.SR}{2L_1.GBW - A_{dc}.K_{\lambda 1}.SR}$

The obtained transistors' dimensions are shown in table A.6.

W_{1-2}	L_{1-2}	W_{3-4}	L_{3-4}	W_5	L_5
90	1	80	1.1	119	1.25

Table A.6: Transistors dimensions

A.1.4 Electrical Simulations

A.1.4.1 Corner Simulations

Electrical simulations of the designed circuit were carried out to validate the design. To ensure the circuit robustness, the simulations were performed for 14 different corners that combine a ± 10% supply voltage variation, a -25^{o}C to 90^{o}C temperature variation and SS, TT and FF processes. The results are shown in table. A.1.4.1. As it can be seen, the specifications of table.A.4 were reached for all corners. The most constraining corner in terms of GBW, SR and A_{dc} was for 90 ^{o}C, 1.08 V and SS process. This is predictable due to the fact that for a higher temperature and a slower process, transistors mobility decreases. As for supply voltage, reducing it leads to a decrease of transistors' overdrive voltage and consequently their current. It can be noted also that some variations that cause a performance amelioration may lead if combined to a corner for which the performance are not reached. In fact, for the -25

^{o}C, 1.32 V and FF process corner, the three variations causes usually a performance increase but combined they cause the worst case in terms of phase margin.

Vdd (V)	Process	T (^{o}C)	GBW (GHz)	SR (V/ns)	A_{dc} (dB)	Phase margin (^{o})	Out swing (V)
1.2	TT	27	1.023	1.06	26.1	65	0.55
1.32	TT	27	1.7	2.3	26.38	62.8	0.6
1.32	FF	-25	2	2.4	26.96	61.65	0.63
1.32	TT	90	1.44	2.2	25.58	64.16	0.58
1.32	SS	27	1.51	1.92	26.67	63.37	0.63
1.08	TT	27	0.9	0.88	25.3	65	0.5
1.2	SS	27	0.849	0.86	25.46	66	0.52
1.2	FF	27	1.23	1.23	25.8	64	0.5
1.2	TT	-25	1.17	1.02	26.63	63.6	0.58
1.2	TT	90	0.902	1.14	25.52	66	0.51
1.08	TT	27	0.9	0.88	25.3	65	0.5
1.08	FF	27	0.954	0.93	25.1	65	0.4
1.08	SS	-25	0.972	0.84	26	64	0.56
1.08	SS	90	0.717	0.87	24.64	68	0.45

Table A.7: Simulations results for the considered corners

A.1.4.2 Ageing Simulations

Another aspect that should be investigated is the robustness of the circuit versus ageing to ensure that the designed OTA preserves its performance for its life time[108]. The ageing phenomenas that were taken into consideration are:
Hot Carrier Injection (HCI) - this phenomenon charges gain sufficient energy to overcome a potential barrier and then migrate to a different area of the device. Such phenomenon occurs at the end of the drain junction of a transistor in saturation, creating many interface traps, which increase the substrate leakage current and cause drain current to decrease. The HCI takes effect when the V_{gs} is greater than or equal to zero and the V_{GS} is very high[109].
Negative Bias Temperature Instability (NBTI) - this phenomenon generates positive charges and interface traps. The NBTI is typically seen as a threshold voltage shift after stress. The threshold voltage degradation can be recovered if the stress is stopped[109].
To simulate the impact of these two phenomenas on circuit operation, the used tool is the Mentor Eldo simulator with the automatically extracted BSIM transistor ageing model characterized with the ageable parameters provided by the process design kit. The results of Table. A.1.4.2 for 10 years ageing show that the designed OTA is robust versus ageing.

	Vdd (V)	Process	T (^{o}C)	GBW (GHz)	SR (V/ns)	A_{dc} (dB)	PM (^{o})	Out swing (V)
Fresh	1.2	TT	27	1.023	1.06	26.1	65	0.55
Aged	1.2	TT	27	0.996	1.04	26.1	65.5	0.5

Table A.8: OTA specifications with 10 years ageing

	Vdd (V)	Process	T (^{o}C)	GBW (GHz)	SR (V/ns)	A_{dc} (dB)	PM (^{o})	Out swing (V)
Before	1.2	TT	27	1.023	1.06	26.1	65	0.55
After	1.2	TT	27	0.978	1.04	25.9	61	0.5

Table A.9: OTA specifications before and after parasitic extraction

A.1.5 OTA Layout

The last step of the proposed design methodology is the layout drawing. This operation is critical because parasitic capacitances and resistances are created between the different OTA nodes during it. Besides, process variation and other parasitic effects make in sort that symmetrical components such as the input pair do not share the same electrical properties as they are supposed to. These mismatches between symmetrical elements leads to an increase of the offset and the even order distortions[110].
Several layout habits and techniques could be used to reduce the impact of these imperfections. First, the rails' width should be chosen adequately in order to have negligible voltage drop. Therefore, the resistance value must be fixed depending on the current passing through. For example, the width of a rail that loads a gate can be much thinner than the supply one. For parasitic capacitors, their values must be decreased as much as possible for AC signals. This could be done by increasing the spacing between rails. While for DC signals, parasitic capacitors are welcomed. They allow to filter high frequency noise. It is for this reason that Vdd rail and gnd rail were placed in a manner that increases their capacitance as shown in Fig. A.6 . Moreover, the layout must be symmetrical as much as possible to ensure that symmetrical components share the same couplings. Besides, to reduce the impact of process variation, the common centroid technique could be used for the input pair and for the load pair. It consists on interdigitating the fingers of the two transistors to make them share the same center[56]. Placing dummy fingers at both sides of the pair improves also the matching because it helps in creating the same operation environment for all useful fingers[110]. Note that the input pair was placed in a triple-well because its bulk is not connected to the ground. Layout considerations will be depicted in details in Appendix B

In order to evaluate the impact of the added parasitic components on the OTA performance, a parasitic extraction of the layout shown in Fig. A.6 is performed. Electrical simulations of the extracted circuit give the results shown in table. A.9.

A.2 Switch

The switch is a key element in switched capacitor circuits. It must operate as very high resistor when OFF to reduce the charge leak and as a very small resistance when ON to minimize the settling time. Unfortunately, this type of operation can not be exactly achieved with CMOS technology. Moreover, the lower scability of threshold voltage with respect to supply voltage with the technology advance, is leading, among others, to a larger gap between the ideal and real operation of the switch. This section presents the main errors caused by the non-ideal switch behaviour and solutions to overcome them. Electrical simulations are carried out in a 1.2 V 65 nm CMOS technology to confirm or to complete the results obtained in the means of analytical calculations.

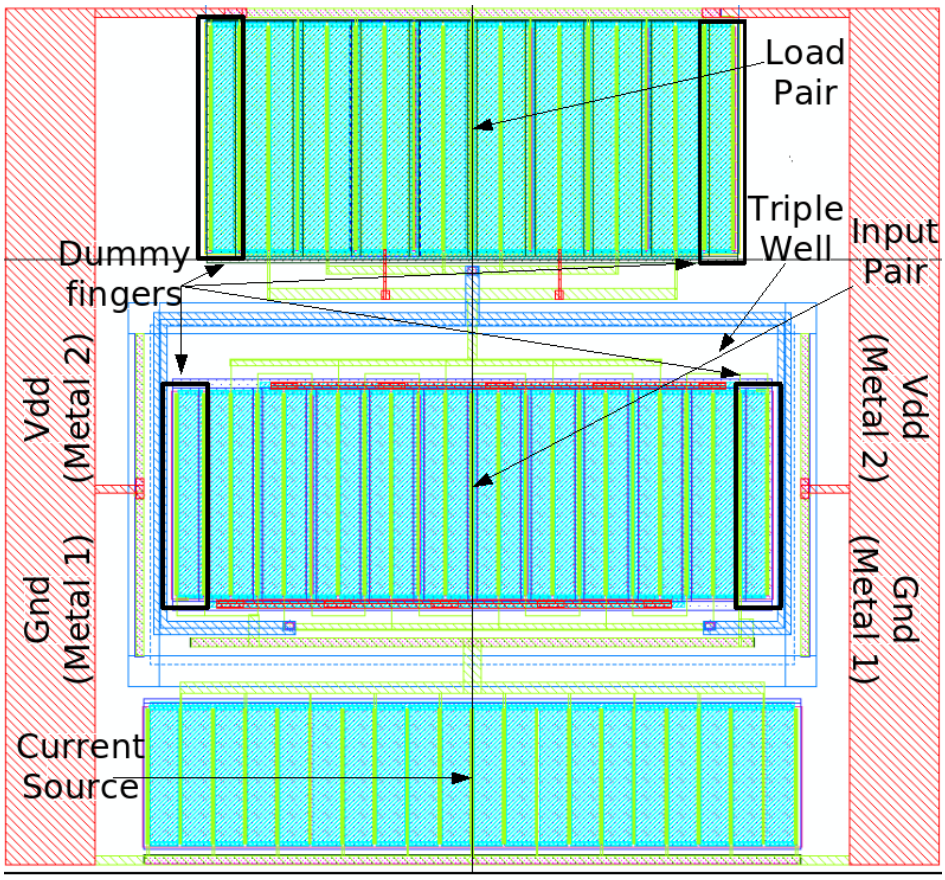


Figure A.6: Layout of a the designed OTA

A.2.1 Switch finite On-conductance

A.2.1.1 Low pass filtering

To examine the need for a small On-resistance, let us consider the Sample and Hold (S/H) shown in Fig. A.7. During phase S, the sampling circuit is equivalent to the circuit of

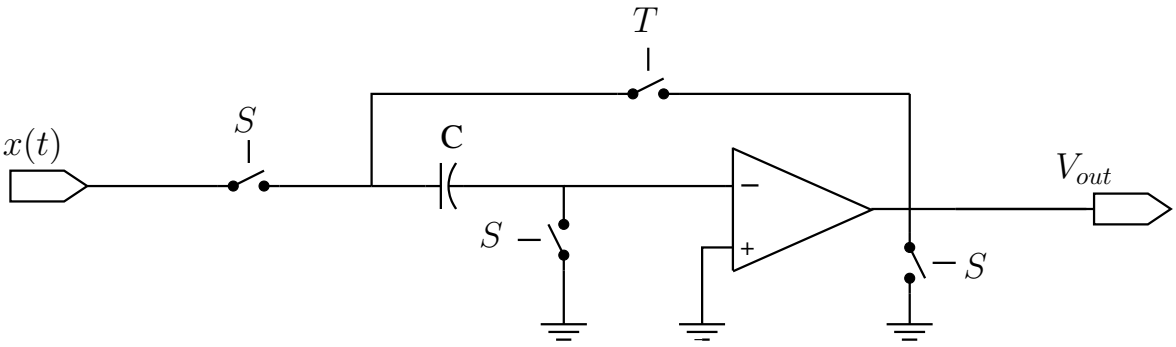


Figure A.7: S/H circuit

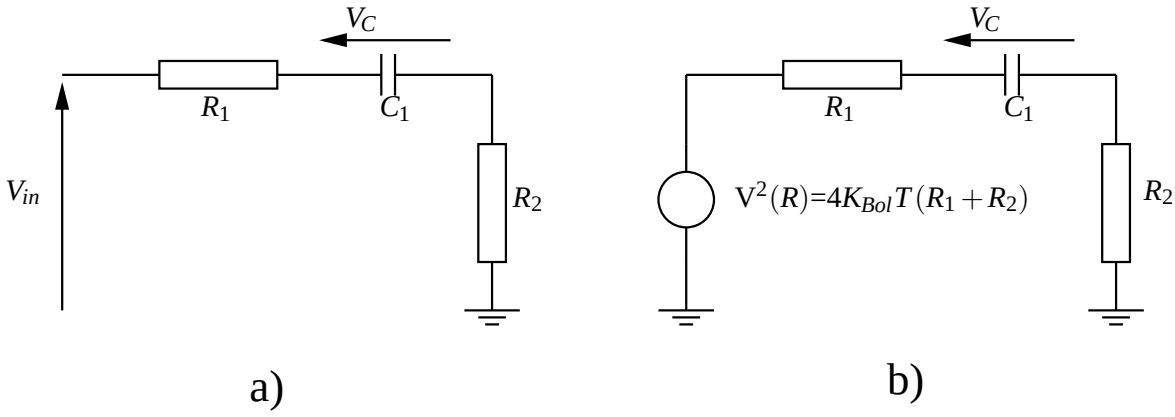


Figure A.8: a)Equivalent circuit in sampling mode b)Resistor thermal noise model

Fig. A.8.a). Its transfer function is given by :

$$H(j\omega) = \frac{V_c(j\omega)}{V_{in}(j\omega)} = \frac{1}{(R_{eq})Cj2\pi f + 1} \tag{A.1}$$

Where $R_{eq} = R_1 + R_2$
It is clear that the sampling circuit behaves as a low - pass filter whose cut-off frequency $f_c = \frac{1}{2\pi.(R_{eq}).C}$. This low pass filter causes an attenuation of the input signal specially for high frequencies. Two approaches can be considered to deal with this problem. The first consists of compensating the low pass filtering by applying the inverse high pass filtering in this digital baseband. The drawbacks of this approach are increasing the overall noise power and increasing the complexity due to the additional filter. The second approach is to increase the cut-off frequency of the sampling circuit in a manner to make the in-band attenuation negligible with respect to the considered resolution. Therefore, f_c must be fulfill the following condition [17]:

$$f_c > 2^{\frac{SNR-7.78}{12.04}} B \tag{A.2}$$

Where B is the signal bandwidth and SNR the targeted signal to noise ratio.
Increasing f_c can be achieved by decreasing C or R_{eq}. The minimal value of C is fixed by thermal noise considerations. In fact, C is chosen in order to guarantee that the ratio of the signal power P_s to switches' thermal noise power stocked in the capacitor P_{th} is equal to the thermal noise budget that constitutes an important part of the overall noise. To calculate P_{th}, the resistor thermal noise model shown in Fig. A.8.b) can be used [56].

$$|V_C|^2 \;=\; 4K_{Bol}TR_{eq}\frac{1}{4\pi^2R_{eq}^2C^2f^2+1} \tag{A.3}$$

Where K_{bol} is the Boltzmann constant and T is the temperature in Kelvin
The thermal noise power stocked in C is then given by:

$$P_C \;=\int_0^{\infty} 4K_{Bol}TR_{eq}\frac{1}{4\pi^2R_{eq}^2C^2f^2+1}df \tag{A.4}$$

$$P_C = \frac{2K_{Bol}T}{\pi C}\;\; atan(2\pi R_{eq}Cf)|_0^{\infty} = \frac{K_{Bol}T}{C} \tag{A.5}$$

P_C corresponds to switch thermal noise stocked during phase S. By similar calculations, it can be proved that during phase T, an equal noise power is added to the capacitor due to the track switch. In differential circuit, the overall thermal noise power is twice the noise of a single-ended circuit and P_{th} is then given by:

$$P_{th} = \frac{4K_{Bol}T}{C} \tag{A.6}$$

Using Eqn. A.6, the minimal value for C can now be determined:

$$10Log(\frac{P_s}{P_{th}}) = 10Log(\frac{A^2/2}{4K_{Bol}T/C}) = SNR_{th} \tag{A.7}$$

with A the differential input signal amplitude and SNR_{th} the targeted signal to thermal noise ratio

$$C = \frac{8K_{Bol}T.10^{SNR_{th}/10}}{A^2} \tag{A.8}$$

Based on the computed value of C, the value of R_{eq} must be adapted to guarantee the needed f_c. This is done by choosing the appropriate architecture and dimensions of the switch as it will be shown in section A.2.2.

A.2.1.2 Track-mode distortion

The frequency analysis of the equivalent circuit during the sampling phase (Fig. A.8.a)) showed that it behaves as a low pass filter. Let us now perform a time analysis of the circuit by establishing the expression of the capacitor voltage $v_c(t)$ for a sine input wave.

$$R_{eq}.i(t) \;+\; \frac{\int i(t).dt}{C} \;=\; Asin(\omega t \;+\; \phi)$$

$$v_c(t) \;=\; \frac{\int i(t).dt}{C} \Longrightarrow i(t) \;=\; C\frac{dv_c(t)}{dt}$$

$$R_{eq}.C\frac{dv_c(t)}{dt} \;+\; v_c(t) = Asin(\omega t \;+\; \phi)$$

The general solution of this differential equation is given by
$v_c(t) = \lambda e^{-(\frac{t}{R_{eq}.C})}$

To obtain the particular solution of the equation, the constant variation technique is used.

$$R_{eq}.C(\lambda'(t)e^{-(\frac{t}{R_{eq}.C})} + \lambda(t)e^{-(\frac{t}{R_{eq}.C})}\frac{-1}{R_{eq}.C}) +$$
$$\lambda(t)e^{-(\frac{t}{R_{eq}.C})} = Asin(\omega t + \phi)$$

$$R_{eq}.C\lambda'(t)e^{-(\frac{t}{R_{eq}.C})} = Asin(\omega t + \phi)$$

$$sin(\omega t + \phi) = \frac{e^{(+j\omega t+\phi)} - e^{(-j\omega t-\phi)}}{2j}$$

$$\Longrightarrow \lambda'(t) = \frac{A}{2R_{eq}.C.j}(e^{(j\omega t+\phi+\frac{t}{R_{eq}.C})} - e^{(-j\omega t-\phi+\frac{t}{R_{eq}.C})})$$

$$\Longrightarrow \lambda(t) = \frac{A}{2j - 2R_{eq}.C.\omega}e^{(j\omega t+\phi+\frac{t}{R_{eq}.C})} -$$
$$\frac{A}{2j + 2R_{eq}.C.\omega}e^{(-j\omega t-\phi+\frac{t}{R_{eq}.C})}$$

$$v_c(t) = \lambda(t)e^{-(\frac{t}{R_{eq}.C})}$$

$$v_c(t) = \frac{A}{2j - 2R_{eq}.C.\omega}e^{(+j\omega t+\phi)} - \frac{A}{2j + 2R_{eq}.C.\omega}e^{(-j\omega t-\phi)}$$

$$v_c(t) = A\frac{sin(\omega t+\phi) - R_{eq}.C.\omega.cos(\omega t+\phi)}{1 + R_{eq}^2.C^2.\omega^2}$$

The complete solution is obtained by summing the general solution and the particular one.

$$v_c(t) = \lambda e^{-(\frac{t}{R_{eq}.C})} + A\frac{sin(\omega t+\phi) - R_{eq}.C.\omega.cos(\omega t+\phi)}{1 + R_{eq}^2.C^2.\omega^2}$$

At the end of the sampling phase, $v_c(t)$ is then given by:

$$v_c(\frac{T_s}{2}) = \underbrace{\lambda e^{-(\frac{1}{2.R_{eq}.C.f_s})}}_{Transitory Response} + \underbrace{\frac{Asin(\omega\frac{T_s}{2}+\phi-atan(R_{eq}.C.\omega))}{\sqrt{1 + R_{eq}^2.C^2.\omega^2}}}_{Steady\ response} \tag{A.9}$$

Using the steady response, the group delay of the filter can be determined:

$$t_g(\omega) = \frac{\delta\ atan(R_{eq}.C.\omega.)}{\delta\omega} = \frac{R_{eq}.C}{1 + (R_{eq}.C.\omega.)^2} \tag{A.10}$$

Let us reconsider the two approaches considered in the previous sub-section. If the second approach that consists of reducing the in-band attenuation by increasing f_c (Eqn. A.2) is employed, the group delay can be approximated to $R_{eq}.C$ and thus is frequency independent. If the first approach is employed, the digital correction filter should achieve in addition to the gain correction, a phase correction in order to make the output's group delay constant.

A.2.2 On-resistance signal dependency

In CMOS technology, the simplest way to implement a switch is to use either a NMOS transistor, a PMOS transistor or both in parallel to form a CMOS switch. The value of the respective conductances are given by:

$$G_{Nmos} = \mu_n.C_{ox}\frac{W_n}{L}(V_{gsn} - V_{thn})$$

$$G_{Nmos} = \mu_n.C_{ox}\frac{W_n}{L}(Vdd - V_{in} - V_{thn})$$

$$G_{Pmos} = \mu_p.C_{ox}\frac{W_p}{L}(V_{gsp} - \mid V_{thp} \mid)$$

$$G_{Pmos} = \mu_p.C_{ox}\frac{W_p}{L}(V_{in} - \mid V_{thp} \mid)$$

$$G_{Cmos} = G_{Nmos} + G_{Pmos}$$

$$G_{Cmos} = \mu_n.C_{ox}\frac{W_n}{L}(Vdd - V_{in} - V_{thn}) + \mu_p.C_{ox}\frac{W_p}{L}(V_{in} + \mid V_{thp} \mid)$$

$$G_{Cmos} = \mu_n.C_{ox}\frac{W_n}{L}(Vdd - V_{thn}) - \mu_p.C_{ox}\frac{W_p}{L} \mid V_{thp} \mid + \underbrace{V_{in}(-\mu_n.C_{ox}\frac{W_n}{L} + \mu_p.C_{ox}\frac{W_p}{L})}_{A}$$

In order to make G_{Cmos} signal independent, A must be nullified. To achieve this, the following condition must be fulfilled:

$$\mu_n W_n = \mu_p W_p \tag{A.11}$$

This yields:

$$G_{Cmos} = 2\mu_n C_{ox}\frac{W_n}{L}(Vdd - V_{thn} - \mid V_{thp} \mid) \tag{A.12}$$

Fig. A.9 shows the values of the resistances of a NMOS switch, a PMOS switch and a CMOS switch with respect to V_{in} obtained with electrical simulations. The 3 switches are implemented in a 1.2 V 65 nm CMOS process and have the minimum length and the same width ($W_P = W_N = W_{p-C} + W_{n-C}$). For the CMOS switch, $\frac{W_{p-C}}{W_{n-C}}$ was fixed equal to $\frac{\mu_n}{\mu_p}$ which has a value of 3.4 in the considered technology. As it can be seen, the NMOS switch and the PMOS switch resistances are very V_{in} dependent and have a limited voltage swing of operation. The CMOS switch resistance has a lower V_{in} dependency but its value still suffers from some variation although that the condition of Eqn. A.11 is respected. This dependency is caused mainly by the bulk effect that if taken into consideration yields in:

$$G_{Cmos} = \mu_n.C_{ox}\frac{W_n}{L}(Vdd - (\mid V_{thp0} + \gamma_p(\sqrt{Vdd - V_{in} + 2 \mid \phi_F \mid} - \sqrt{2 \mid \phi_F \mid}) \mid) - V_{thn0} - \gamma_n(\sqrt{V_{in} + 2 \mid \phi_F \mid} - \sqrt{2 \mid \phi_F \mid})$$

Where ϕ_F is the surface potential and γ the body effect coefficient

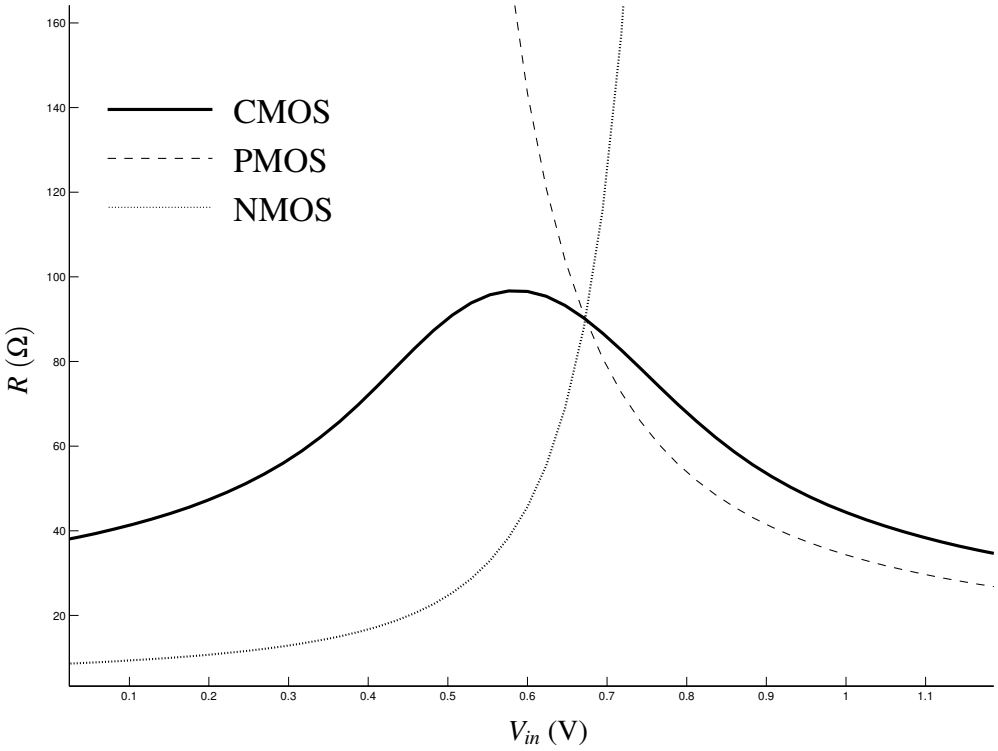


Figure A.9: Resistance of NMOS, PMOS and CMOS switches Vs input

A.2.2.1 Bootstrapped switches

The bootstrapping technique is one of the most efficient solutions to make switch's On-resistance voltage independent. Its operation consists of imposing to the gate voltage to track the input voltage with a constant offset, V_{boost} . This makes the switch V_{gs} almost input independent and consequently its resistance.

Fig. A.10 and A.11 show two circuits that can be used to implement the charge pump that allows to have a constant offset between V_s and V_g. Other architectures of charge pumps were proposed in [111] [112] [113]. The circuit of Fig. A.10 was proposed in [114]. It is one of the most employed bootstrapped switch. It operates as follows: during CLK_n, C_3 is charged through T_3 and T_4 and in the meantime the $T_{bootstrap}$ gate voltage is grounded across T_6 and T_7. When CLK goes up, T_9 and T_5 become closed. Thus, C_3 bottom plate will be connected to the input voltage through T_9 and its top plate to $T_{bootstrap}$ gate through T_5. Consequently, $T_{bootstrap}$ gate voltage will be equal to Vdd + V_{in} and its V_{gs} to Vdd.
The circuit of Fig. A.11 was proposed in [115]. Its uses a CMOS switch instead of using a NMOS one. We modified the circuit to allow its operation with low supply voltage technology. Its operation is quite similar to the former circuit. During CLK_n, C_N and C_P are charged. In this case, the value charged is equal to $\pm\frac{\text{Vdd}}{2}$. During CLK, the two capacitors are placed between V_{in} and the PMOS and the NMOS gates creating thereby a constant voltage.

Fig. A.12 shows a comparison between the bootstrapped NMOS switch of Fig. A.10, the bootstrapped CMOS switch of Fig. A.11 and a regular CMOS switch. Note that for CMOS switches, $\frac{W_{p-C}}{W_{n-C}}$ was fixed equal to $\frac{\mu_n}{\mu_p}$. First, it can be seen that, as predicted, bootstrapped switches have lower relative variation of their resistance compared to a regular CMOS switch. Some variation can still be observed due to the bulk effect. It is lower for the CMOS switch

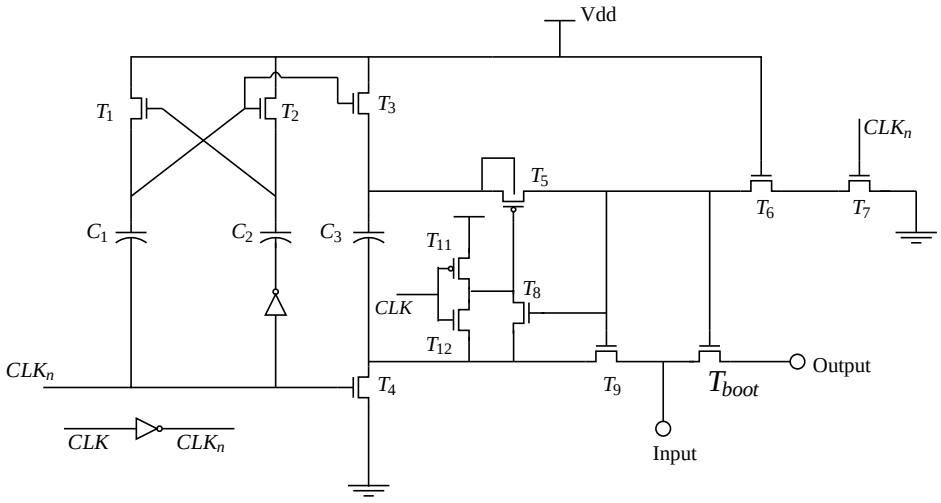


Figure A.10: Charge pump for a NMOS switch

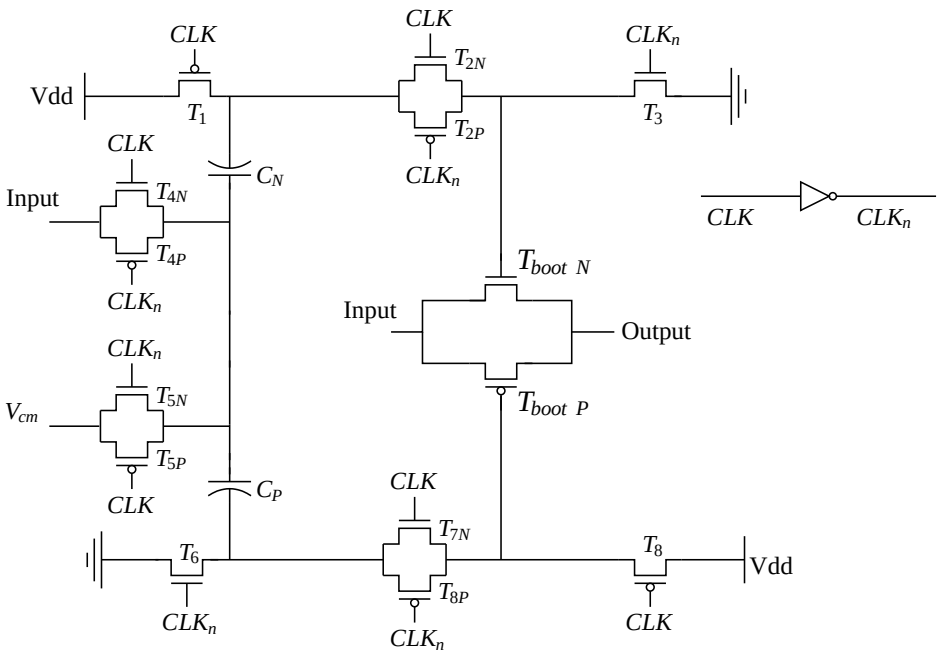


Figure A.11: Charge pump for a CMOS switch

because the variation of the threshold voltage are opposite for NMOS and PMOS transistors. On the other hand, for a same width, the bootstrapped NMOS switch has a significant lower resistance compared to the bootstrapped CMOS switch. This is due to the higher V_{boost} employed for this switch i.e. Vdd compared to $\frac{\text{Vdd}}{2}$.

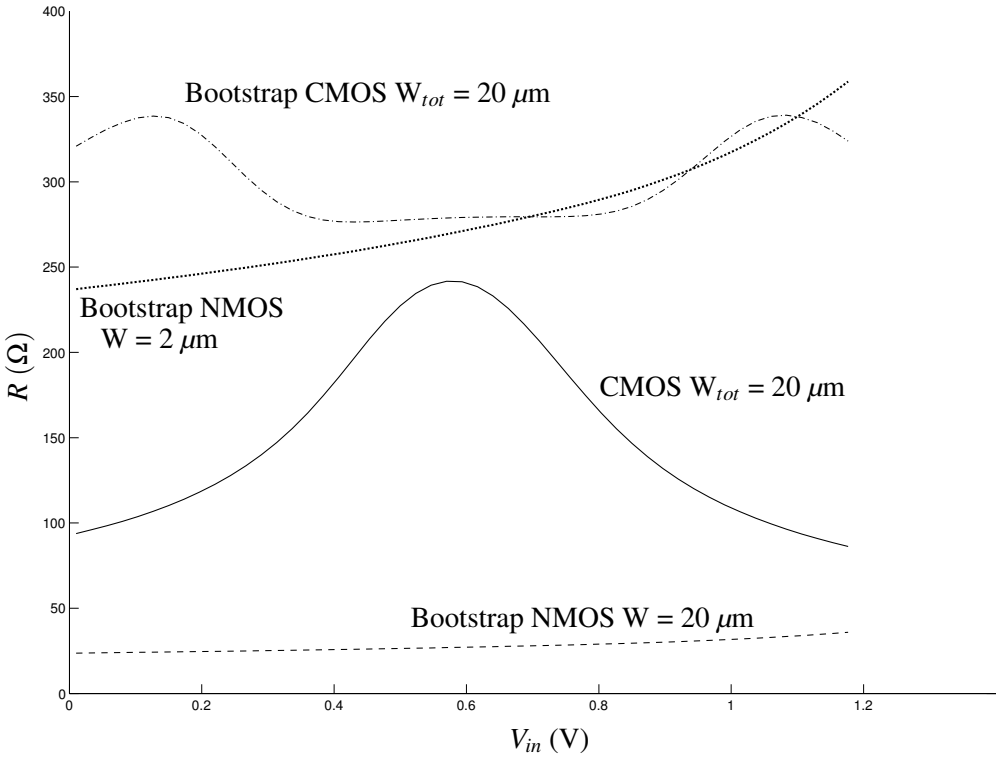


Figure A.12: Resistance of a bootstrapped NMOS, a bootstrapped CMOS and a regular CMOS Vs input

The main drawback of bootstrapped switch is their high complexity. Therefore, they are used only in critical points of the circuit. For example, in the pipeline ADCs proposed in [116] [117] and in the $\Delta\Sigma$ ADCs proposed in [98] [118], they were employed in the first stage only. Another point that must be considered also when using this type of switches is their reliability. In fact, in some cases, switch V_{gs} surpasses the breakdown voltage of the transistor which reduces strongly its life time. To overcome this problem, thick oxyde transistors can be employed for the bootstrapped switch as in [98]. Another way to ensure reliability is by addressing this problem during the design of the charge pump. In fact, for the circuit of Fig. A.10, T_6 and T_8 were added to ensure that V_{gs} does not exceed Vdd for the bootstrapped transistor and for T_5. We employed this switch in our design using regular transistors and no reliability problems were noted.

A.2.3 Charge injection and clock feedthrough

To achieve a good explanation of the charge injection and clock feedthrough phenomenas, let us reconsider the circuit of the S/H shown in Fig. A.7. At the end of the sampling phase (if assumed ideal), the charge stored in C is equal to $C.V_{in}(t_0)$, where t_0 is the sampling instant. This charge must be preserved unchanged during the hold phase to obtain the desired output. Unfortunately, the value of this charge is affected by many parasitic phenomena. Some occur

Capacitance	Triode region	Off region
C_{gs}	$WL_{overlap}C_{ox} + 0.5WLC_{ox}$	$WL_{overlap}C_{ox}$
C_{gd}	$WL_{overlap}C_{ox} + 0.5WLC_{ox}$	$WL_{overlap}C_{ox}$
C_{sb}	$(Area\ _{source\ diode})\frac{C_{j0}}{\sqrt{1+V_{SB}/\Phi_0}}$	
C_{db}	$(Area\ _{drain\ diode})\frac{C_{j0}}{\sqrt{1+V_{DB}/\Phi_0}}$	

Table A.10: MOS transistor parasitic capacitances' equations in linear and off region

during the on-off transitions of the switch such as the charge injection and clock feedthrough. Other occur during the off phase such as the signal feedthrough that will be discussed in next section.
The charge injection is caused by the distribution of the charges stored in the channel capacitance that stops to exit during the off phase. This charge is distributed between the transistor terminals. A first part of the whole charge is absorbed by the substrate. The amount of this charge increases when the slope of the clock is very slow or when the transistor has very large length [119]. The rest of the charge is divided between the source and the drain. The ratio of each depends also on the slope of the clock and on the impedance seen by each terminal. If the rise-fall time of the clock is small, the charge is distributed equally between the source and the drain. While, when the clock slope becomes slower, the channel charge is divided depending on the impedance seen by the source and the drain.

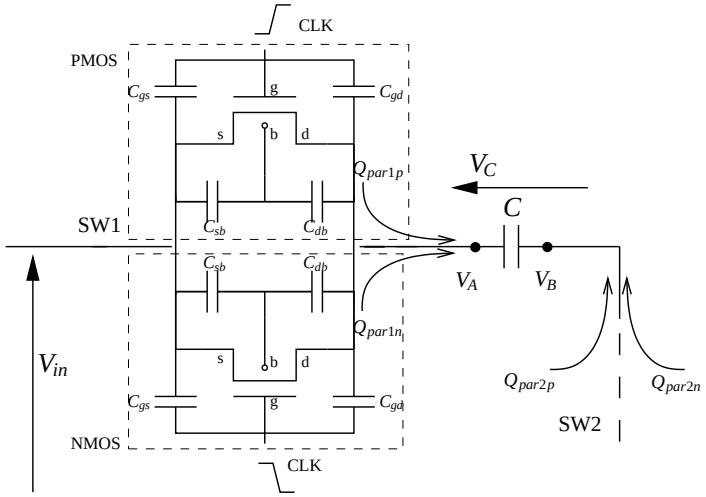


Figure A.13: Impact of parasitic capacitors on sampling

During the sampling phase, SW1 and SW2 are connected to the capacitor (Fig. A.13). The charges injected in C are:
$Q_{par1} = Q_{par1\ n} + Q_{par1\ p} = \alpha_1(W_{1N}L_{overlap}C_{ox} + 0.5W_{1N}LC_{ox}).(Vdd - V_A - V_{th1n}) + \alpha_1(W_{1P}L_{overlap}C_{ox} + 0.5W_{1P}LC_{ox}).(-V_A + \mid V_{th1p} \mid)$

$Q_{par2} = \beta_2(W_{2N}L_{overlap}C_{ox} + 0.5W_{2N}LC_{ox}).(Vdd - V_B - V_{th2n}) + \beta_2(W_{2P}L_{overlap}C_{ox} + 0.5W_{2P}LC_{ox}).(-V_B + \mid V_{th1p} \mid)$

where α and β are the portions of the overall charge injected in the drain and source re-

spectively
These parasitic charges cause a respective variation of V_c equal to:

$$\delta V_{c1} = \frac{Q_{par1}}{C+C_{gd-off-n}+C_{gd-off-p}} \simeq \frac{Q_{par1}}{C+(W_{1n}+W_{1p})L_{overlap}C_{ox}}$$

$$\delta V_{c2} = \frac{Q_{par2}}{C+C_{gs-off-n}+C_{gs-off-p}} \simeq \frac{Q_{par2}}{C+(W_{2n}+W_{2p})L_{overlap}C_{ox}}$$

The impact of δV_{c1} on the signal is much more critical than δV_{c2}. In fact, V_A is approximatively equal to V_{in} and V_B to zero and the lower the time constant of the sampling circuit, the righter this approximation (Eqn. A.9).
Using larger values of C allows to reduce the error caused by the charge injection as it can be seen in the expression of δV_{c1}. This result is confirmed in Fig. A.14 that shows the variation of the SNDR and the SFDR at the output of a S/H as a function of the value of the sampling capacitor. The simulation parameters are : f_s= 33 MHz, f_{in}=1 MHz and V_{in} = 0.1 Vpp.
However, enlarging C has some drawbacks because it increases the constraints on the operational transconductance amplifier (OTA) in terms of slew rate and gain bandwidth product and it reduces the cut-off frequency of the sampling filter. Another approach that can be used to decrease the impact of charge injection is to reduce transistors' dimensions which leads to a decrease of the channel capacitances and thus the injected charge. Unfortunately, this approach causes an increase of the switch resistance.

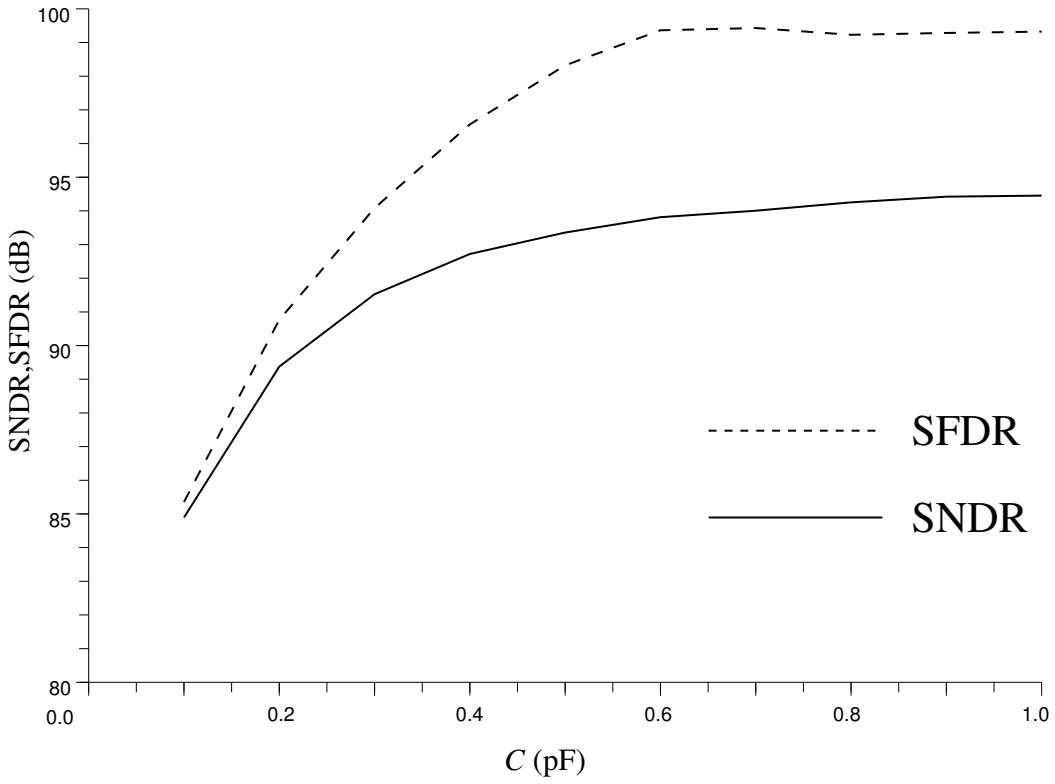


Figure A.14: SNDR and SFDR vs C

The second phenomena that occurs during the on-off transition of the switch is the clock feedthrough. It is caused by the coupling of the clock transitions through the overlap capacitances. It leads to a variation of V_c equal to:

$$\delta V_{c\ clk} = V_{clk}\frac{C_{gd-off-n}}{C+C_{gd-off-n}} - V_{clk}\frac{C_{gd-off-p}}{C+C_{gd-off-p}}$$

The effect of clock feedthrough is, thus, the arising of an offset and even order harmonics in the output signal spectrum. Consequently, in differential circuits, its impact is strongly attenuated.
Another way to reduce the clock feedthrough error is to use switches having $W_p = W_n$. This leads to a $C_{gd\ off\ n} \simeq C_{gd\ off\ p}$ and consequently to a $\delta V_{c\ clk} \simeq 0$. Having a $W_p = W_n$ reduces also the charge injection impact because it minimizes the error's power and centers it around $\frac{Vdd}{2}$.

A.2.3.1 Bottom plate sampling

The bottom plate sampling (BPS) technique is one of the most efficient techniques to reduce input dependent charge injection [120]. It consists on opening the sampling switch SW2 slightly before the input switch SW1 as it can be seen in Fig. A.15 and .A.16. In fact, when S_p goes down, a parasitic charge Q_{par2} is injected in the sampling capacitor C. This charge is significantly less V_{in} dependent than Q_{par1} and consequently its impact is not critical. Later, when S_d goes down, the switch SW1 opens. Nevertheless, its parasitic charge Q_{par1} can not alter the value of the charge stored in C because its bottom plate is floating during this lapse time due to the opening of SW2. Fig. A.17 shows a comparison between the output spectrum

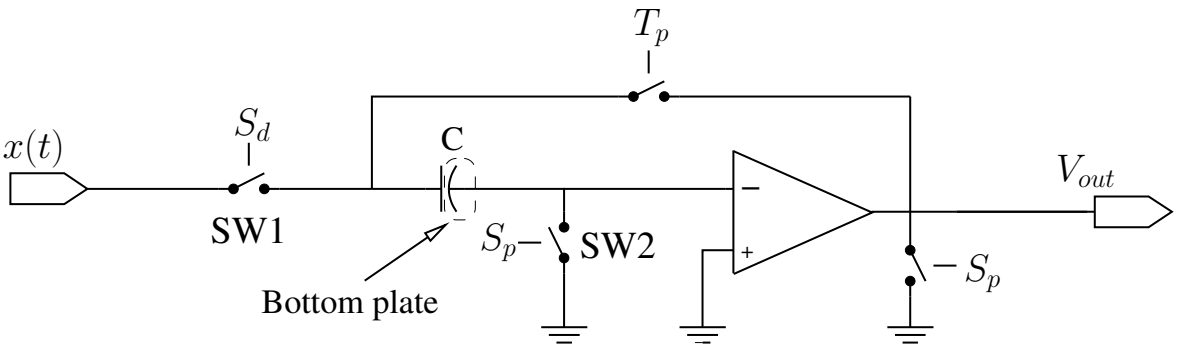


Figure A.15: S/H circuit with BPS

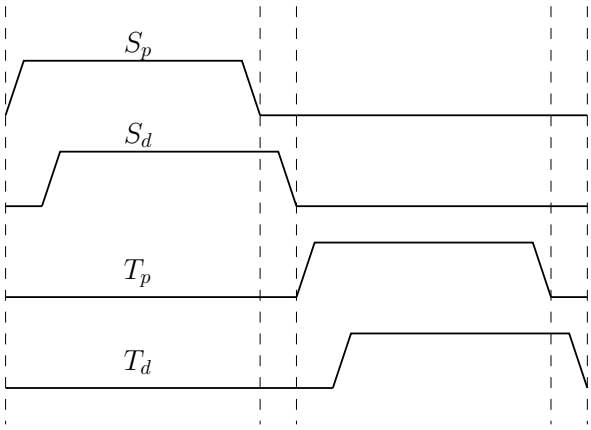


Figure A.16: Timing when using the BPS technique

of a two S/Hs among which one is using the BPS technique and the other is using the regular sampling technique. All components are implemented as ideal models except the switches that were implemented as CMOS switches with $W_p = W_n = 50\ \mu m$ and $L_p = L_n = 60\ nm$. The input signal has an amplitude of 0.6 Vpp and a frequency of 1 MHz. The system was sampled at $f_s = 33\ MHz$, $C = 1\ pF$ and the delay between S_p and S_d is equal to 400ps. A 20 dB improvement of the SFDR can be noted when the BPS is used.
The delay between S_p and S_d is a compromise: it must be large enough to be sure that SW2 is entirely opened and to take into consideration the random variation that exists between the falling edges of the two clocks. On the other hand, the delay must not be too large in order to preserve enough time for the OTA to perform the tracking operation.

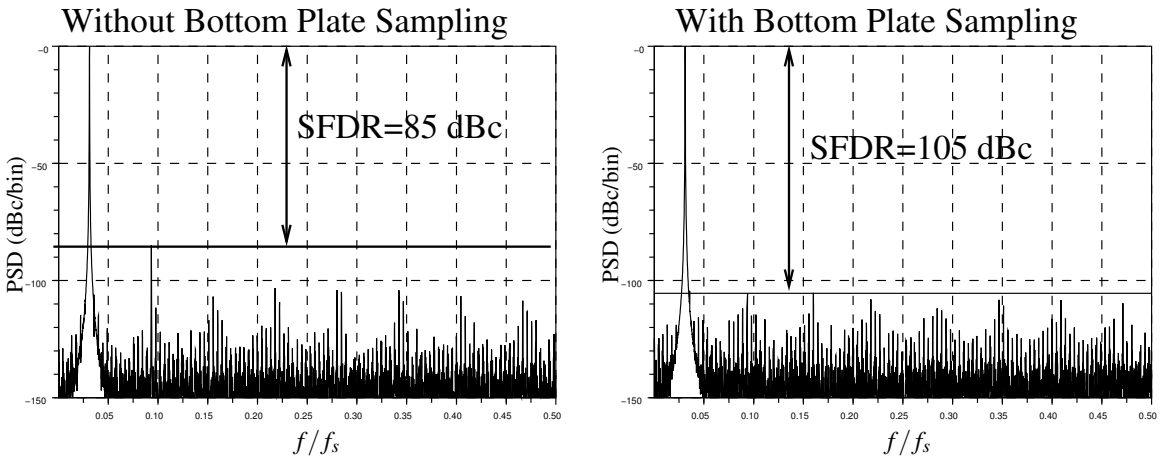


Figure A.17: Comparison of S/Hs' output spectrums with and without bottom plate sampling

A.2.4 Signal feedthrough

In the off-phase, no current should pass through the switch. However, some current still passes through causing what is known as signal feedthrough. This leak current changes the charge stocked on connected capacitors reducing thereby the circuit performances.
Fig. A.18 shows the most common implementation of a CMOS switch with its clocking circuit. The NMOS transistor's gate is driven by the buffer (Inv_{n1} ; Inv_{n2}) and not by the main clock in order to reduce the load on this latter, to reduce the rise/fall time and to synchronise the sampling instant with the PMOS transistor.
When CLK is low, the switch can be modelled by the circuit of Fig. A.19. It is formed by a resistor R_{off} and two high pass filters per transistor in parallel. The resistor R_{off} is not critical. Its value is very high as shown in Fig. A.20 and consequently the leak current through it can be considered as null. This means that the signal feedthrough is critical mainly for input switches because the circuit internal switches process blocked signal.

In addition to R_{off}, two high pass filters per transistor are formed by the overlap capacitances with the sum of the gate resistance and the Vdd rail resistance from one side and by the junction capacitances with the resistance between the substrate and its supply from the other side. This high pass behavior is confirmed by Fig. A.21 that shows the leak current vs input signal frequency for different type of switches and for different widths. As it can be seen, the leak current increases with the input signal frequency. Moreover, Fig. A.21 shows that the leak current increases also with the width of the transistors. In fact, the values of parasitic

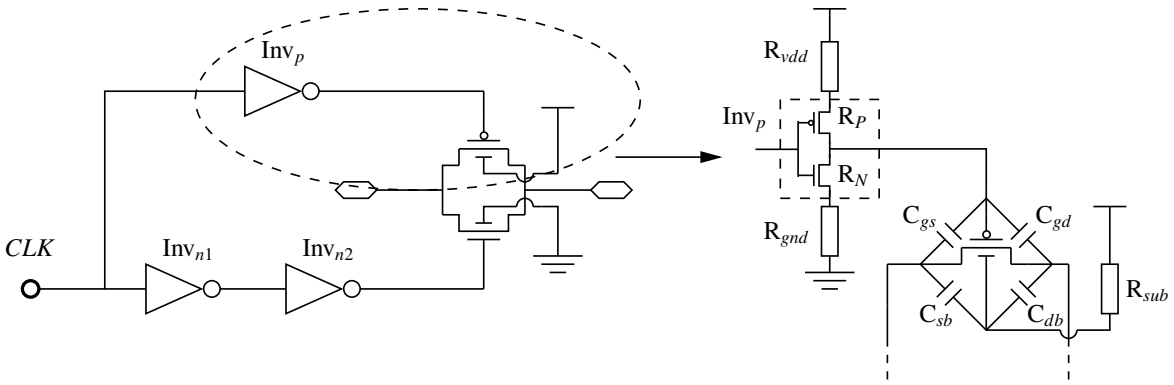


Figure A.18: Switch equivalent model during the Off-phase

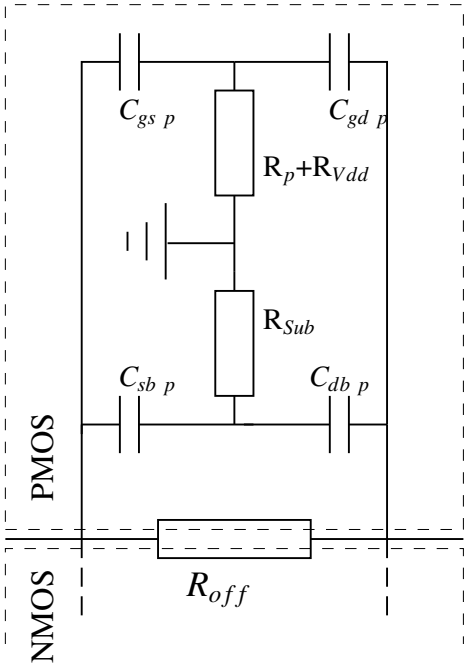


Figure A.19: Switch equivalent model during the Off-phase

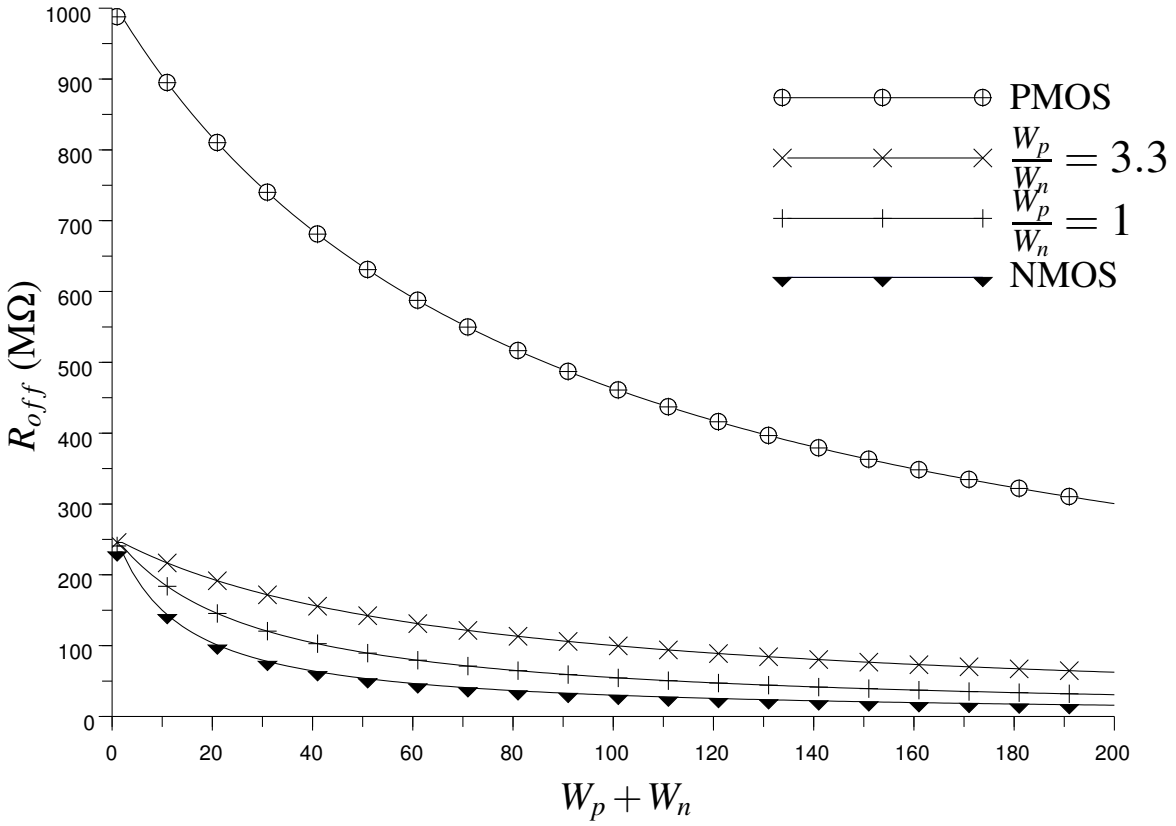


Figure A.20: R_{off} vs transistor width

capacitances become larger with the transistor width increase as presented in Table. A.10. This decreases the cut-off frequency and consequently increases the leak current. Another important point is the values of the resistances. In order to decrease the leak current their values must be minimized. This can be done by increasing the size of the digital gates that drive the input switches and by reducing the resistances of the rails that connect these gates and the bulks of switch transistors to the supply voltages during layout.

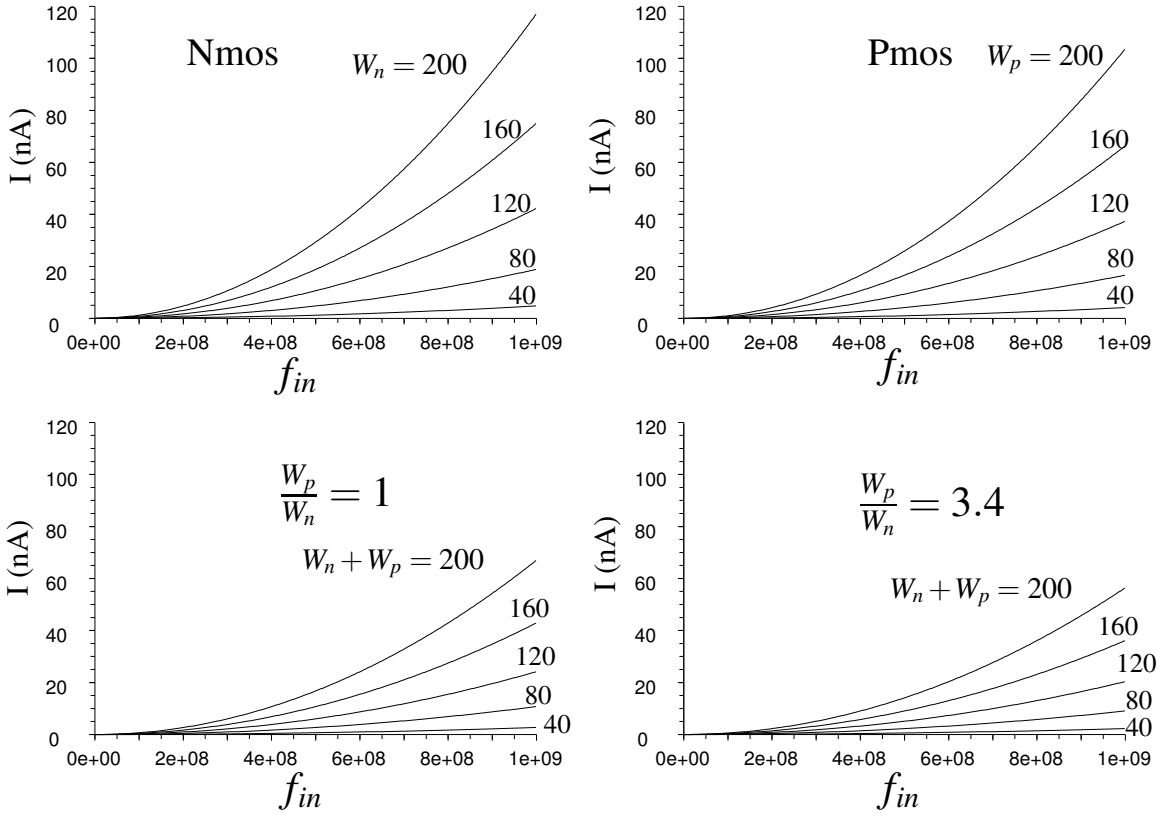


Figure A.21: Leak current vs f_{in}

One method to perform the calibration of signal feedthrough is to add an extra switch whose width is half of the sampling one as shown in Fig. A.22 [121]. The extra switch will be connected to the negative input for the positive sampling switch and vice versa. In a first order approximation, the leak current of this dummy switch is the opposite of the leak current of the sampling switch and thus cancels it. Fig. A.23 shows the leak current of 2 switches before and after calibration. The employed switch is a CMOS switch with $W_p = W_n = 50\ \mu m$ and $L_p = L_n = 60\ nm$. A 23 dB reduction of the leak current has been achieved thanks to the proposed calibration technique.

A.2.5 Eliminating the bulk-effect

As it was seen before, the body effect makes the On-resistance and the charge injection signal dependent. Cancelling this effect reduces strongly the switch non-linearities. This can be achieved by connecting the switch bulk to the switch source which makes V_{th} equal to V_{th0}. Fig. A.24 shows a comparison between the output spectrums of two S/Hs. The first S/H has its input switch bulk connected to its source and the second is using the regular sampling

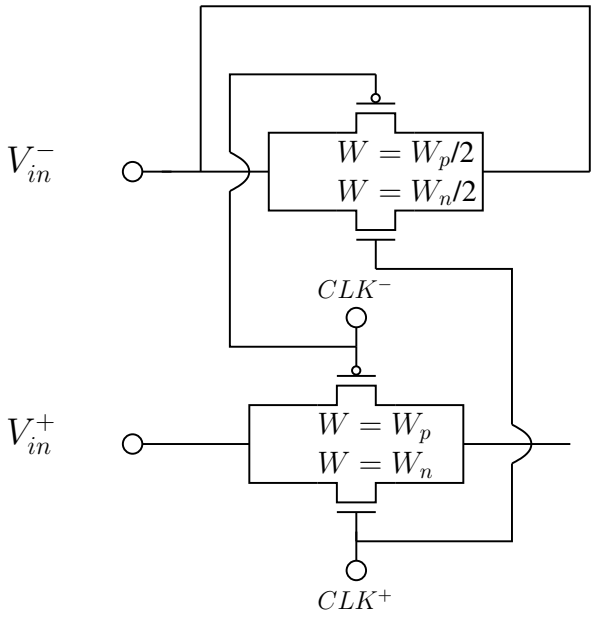


Figure A.22: Signal feedthrough calibration

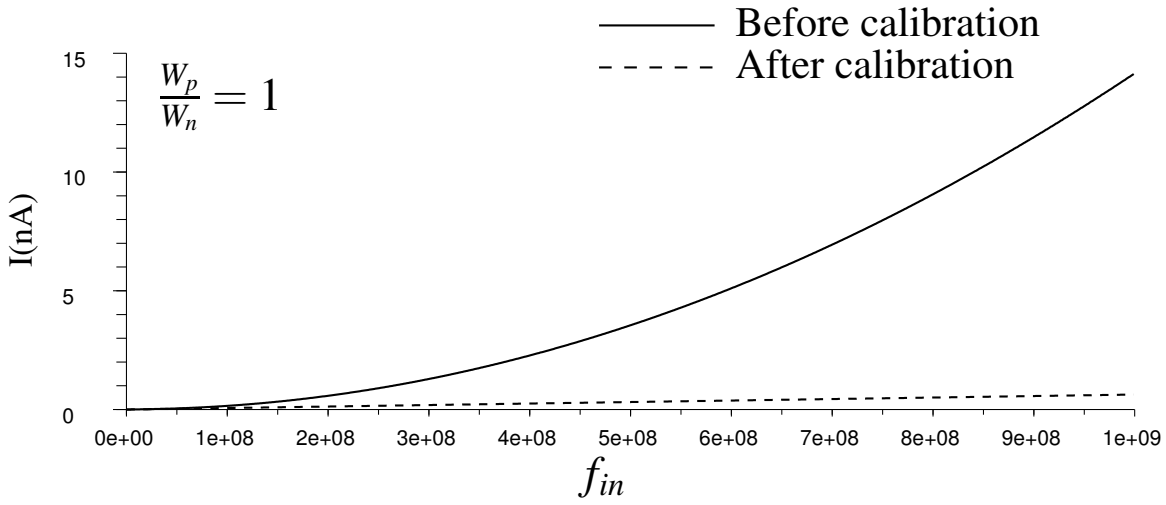


Figure A.23: Leak current Vs f_{in} before and after calibration

technique. All components are implemented as ideal models except the switches that were implemented as CMOS switches with $W_p = W_n = 50\ \mu m$ and $L_p = L_n = 60\ nm$. Both S/Hs are using the BPS technique. The input signal has an amplitude of 1 Vpp and a frequency of 3.5 MHz. The system was sampled at $f_s = 10\ MHz$. A 7 dB improvement was achieved thanks to proposed technique as shown in Fig. A.24..

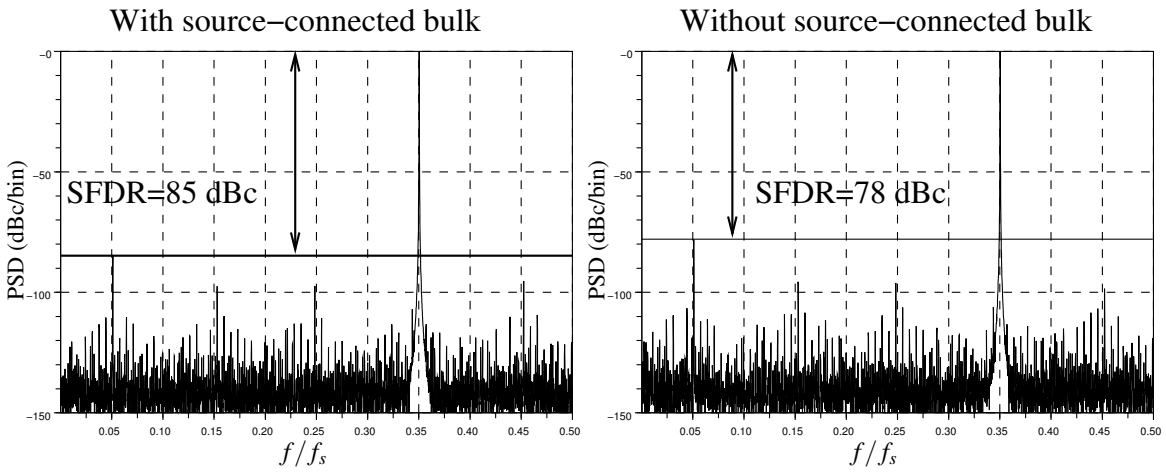


Figure A.24: Comparison of S/Hs‘ output spectrums with and without souce connecting bulk

Nevertheless, some aspects should be taken into consideration when this technique is used. First, the transistor effective source is not always the same node. In fact, it is depending if V_{ds} is positive or negative that the placement of the effective source and the effective drain will be determined. As a consequence, for some input values, the switch bulk will be connected to the drain and not to the source which is one cause of the remaining distortions. On the other hand, in a typical process with a p-type substrate, connecting the PMOS bulk to the input can be easily achieved because PMOS transistors are implemented in separate n-wells. Meanwhile, the NMOS transistor must be implemented in a triple well to isolate it from the die substrate. The use of a triple well increases the switch area and its layout complexity. Moreover, two additional diodes are created as shown in Fig. A.25. Since they are blocked, they behave as capacitances. C2 is not critical since it is between Vdd and the ground. While, C1 is between the switch source and Vdd which may disturb the circuit operation. An important point that must be considered also is the diode D_{db}. In fact, since the bulk is connected to V_{in} and not to the ground, V_{bd} can become positive and may reach values higher than D_{db} threshold voltage which can be fatal to the system due to the large current that may pass through the bulk. Therefore, the decision to use this technique for a given switch depends on the architecture of the block, on the placement of switch in the block and on the signal swing to be sure that V_{bd} does not exceed the threshold voltage of D_{db}.

A.2.6 Jitter

The falling edges of the clock fix the sampling instants. Two successive falling edges must be separated by exactly one sampling period. Unfortunately, the clock edges suffer from a random variation known as jitter. It can be modeled as a Gaussian distribution whose mean is equal to zero and its standard deviation to σ_t. The impact of the clock jitter on the sampled

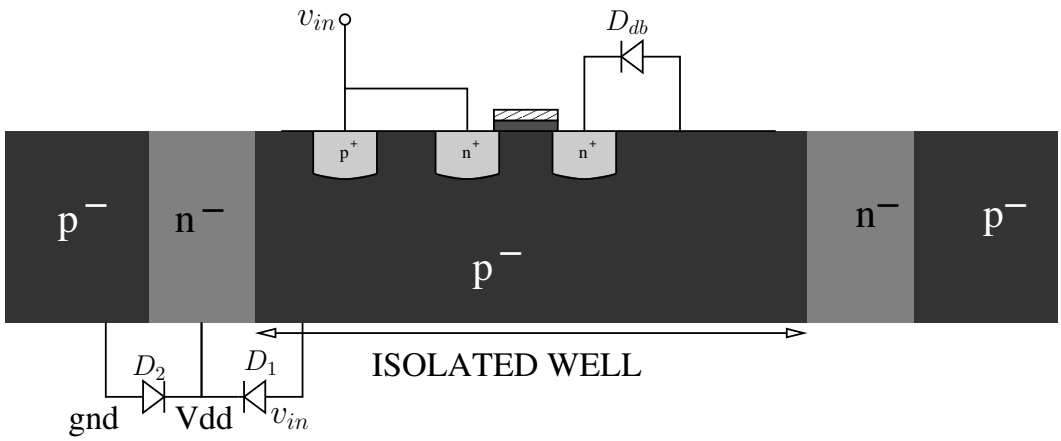


Figure A.25: Triple well

signal can be seen as an additive white noise. The jitter error can be expressed as follows:

$$A_{err} \simeq Asin(2\pi f_{in}t) - Asin(2\pi f_{in}(t+\sigma_t)) \tag{A.13}$$

Since the maximum rate of change of a sine wave occurs at zero, an upper bound of the jitter error can be found by assuming that all errors due to jitter are committed when the sine wave is around zero. Then, using a first order Taylor polynomial, we obtain:

$$A_{err} \simeq Asin(2\pi f_{in}\sigma_t) \tag{A.14}$$

$$If\ \sigma_t << 1/f_{in} \Longrightarrow sin(2\pi f_{in}\sigma_t) \simeq 2\pi f_{in}\sigma_t$$

$$A_{err} \simeq 2A\pi f_{in}\sigma_t \tag{A.15}$$

To verify the accuracy of Eqn.A.15, electrical simulations of the S/H circuit of Fig. A.7 were performed. All the components were implemented as ideal models except the clock that suffers from jitter. Fig. A.26.a) shows the SNR at the S/H output with respect to jitter for several input frequencies. Fig. A.26.b) shows the SNR at the S/H output with respect of jitter for several sampling frequencies. Three observations can be made: the SNR decreases when the jitter increases, the decrease rate gets higher when the input frequency increases and the sampling frequency has no impact on the SNR. These observations go along with Eqn.A.15. However, regarding the sampling frequency, it is true that, for a given jitter, changing the sampling frequency does not affect the jitter error power but it is important to note that the jitter, for most oscillators, increases when the sampling frequency increases which makes the jitter error f_s dependent also. The value of the jitter is affected as well by the quality of the Input/Output buffer and the number of digital gates through which the clock signal passes before reaching the sampling switch.

A.2.7 Design considerations and robustness

A.2.7.1 Design considerations

In section A.2.2, it has been shown that in order to decrease switch's resistance, $\frac{W}{L}$ has to be maximized. On the other hand, as shown in section A.2.3 and A.2.4, the product $W.L$ must be minimized to reduce the impact of charge injection and signal feedthrough. From this, it can de deduced that the most appropriate length for the switch is the minimal length but

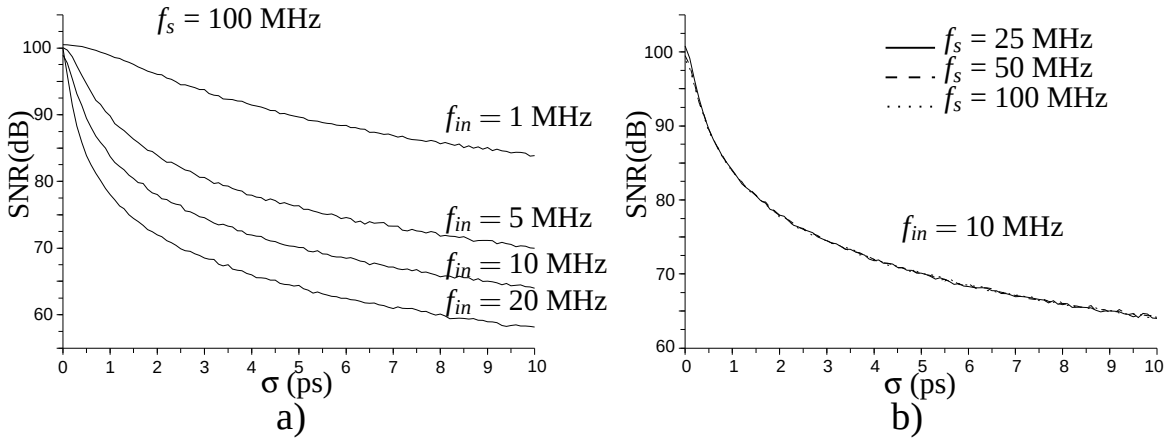


Figure A.26: a)SNR Vs jitter for different input frequencies b)SNR Vs jitter for different sampling frequencies

unfortunately, no conclusion can be made for the switch width. Another parameter that must be fixed is the ratio $\frac{W_p}{W_n}$. In fact, in section A.2.2, it was proved that for $\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$, the most linear resistance is obtained. Meanwhile, based on section A.2.3, a $\frac{W_p}{W_n} = 1$ minimizes the charge injection and clock feedthrough. Therefore, since the optimal couple (W_p , W_n) can not be found analytically, electrical simulations for various widths and ratios were carried out. Fig. A.27 shows the $SNDR$ with respect to $W_p + W_n$ for five values of $\frac{W_p}{W_n}$. For Fig. A.27.a), the input signal has an amplitude of 0.4 Vpp and a frequency of 35 MHz and the system is sampled at 100 MHz. Meanwhile, for Fig. A.27.b), the input signal is at a lower frequency equal to 100 kHz and the system is sampled at 1 MHz. It can be seen that for both scenarios, the most appropriate $\frac{W_p}{W_n}$ ratio is equal to one. This ratio offers the lowest charge injection among the five considered ratios. Besides, it has also the lowest resistance due to the fact that a larger portion of $W_p + W_n$ is used in the NMOS transistor which has a lower resistance than the PMOS transistor.

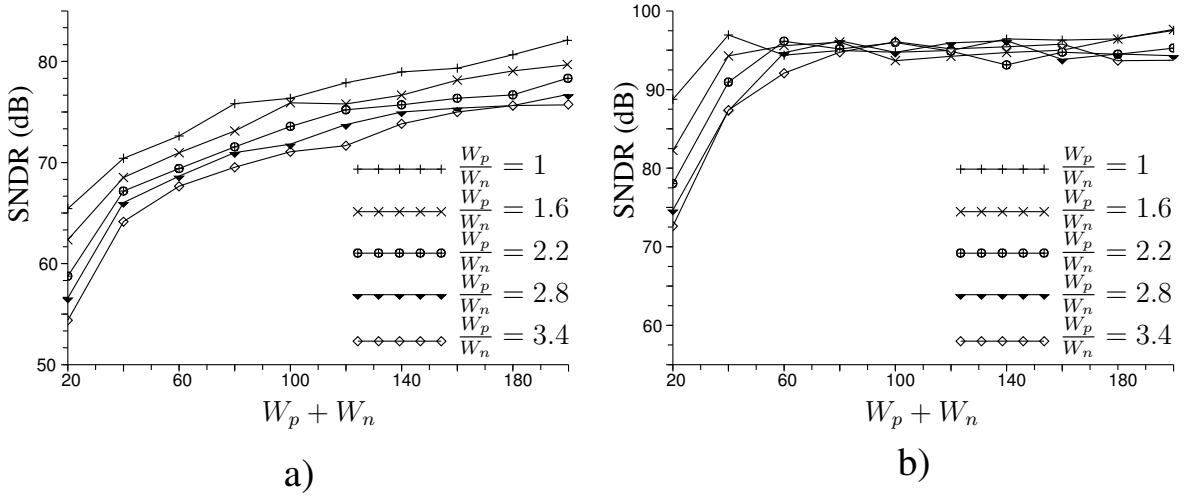


Figure A.27: SNDR Vs width for various $\frac{W_p}{W_n}$

As discussed in Section A.2.1, the input signal amplitude must be maximized to reduce as

much as possible the size of the sampling capacitor. Higher input amplitude intensifies the impact of signal dependent On-resistance which leads to an increase of the distortions as it can be seen in Fig. A.28. Nevertheless, since the signal power increases also, the SNDR remains almost constant. In fact, the maximum input voltage is fixed, usually, depending on the operational transconductance amplifier constraints and not depending on switches' ones.

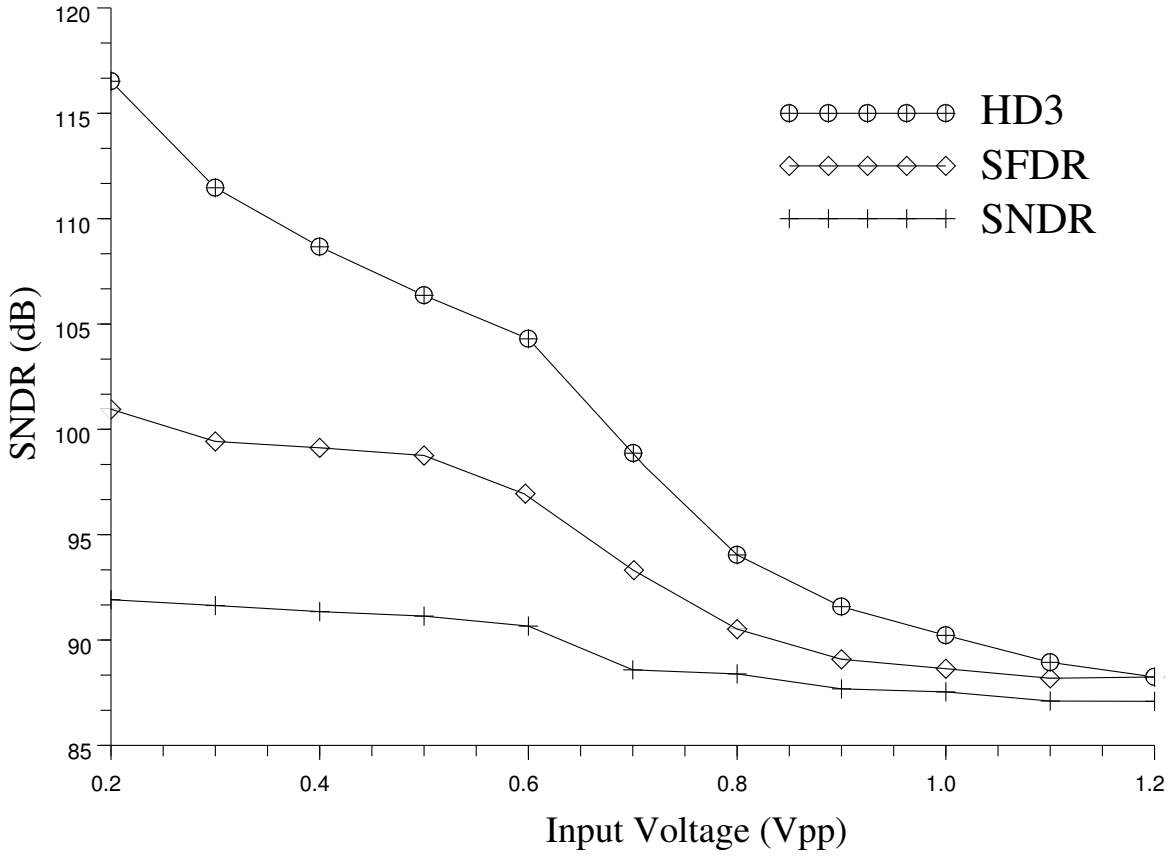


Figure A.28: HD3, SFDR and SNDR Vs input signal amplitude

Fig. A.29.a) shows the SNDR with respect to input signal frequency at the output of a S/H sampled at 100 MHz using the BPS technique. It can be noted that the higher the f_{in}, the lower the SNDR. This is due to an increase of the leak current of signal feedthrough. Besides, since the BPS technique is employed, the charge injected in the capacitor is the one generated in the bottom switch (SW2 in Fig. A.15). The value of this charge depends mainly on V_B (Fig. A.13) whose dependency with V_{in} increases when f_{in} increases. Consequently, the SNDR degradation observed at high f_{in} is caused also by a higher impact of charge injection.
Fig. A.29.a) shows the SNDR with respect to the sampling frequency for an input signal at 5 MHz. It can be noted that the SNDR remains almost constant and decreases significantly once f_s becomes higher than a certain value. This behavior can be explained by Eqn. A.9. For low sampling frequencies, the transitory response can be considered to be negligible with respect to the steady response. Once f_s begins to be of the same order of $R_{eq}.C$, the transitory term is not anymore small with respect to the steady term and causes thereby a SNDR loss.

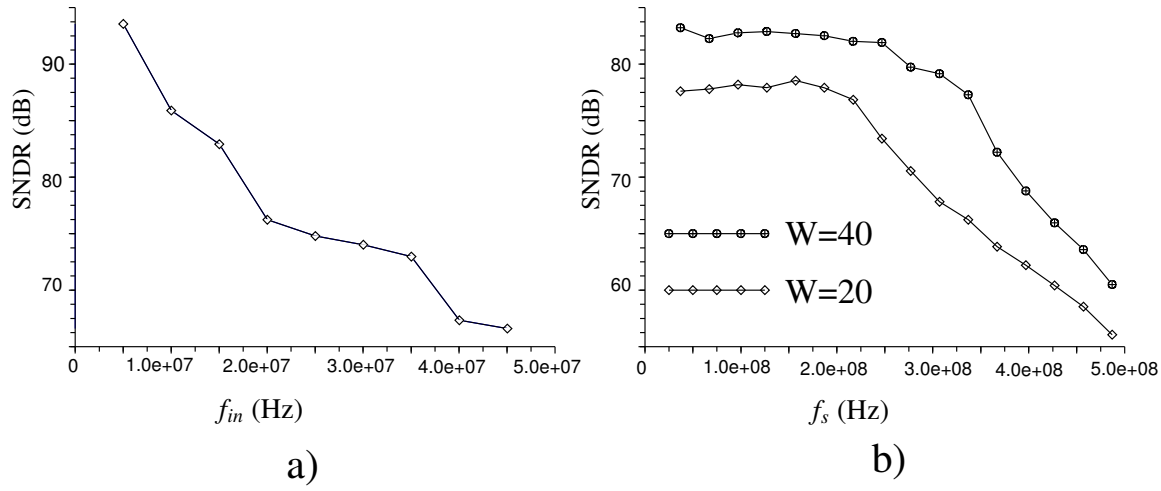


Figure A.29: a)SNDR Vs f_{in} b)SNDR Vs f_s

A.2.7.2 Robustness

An important aspect that should also be investigated is the switch behaviour for the different corners. Three parameters are considered: Supply voltage, temperatue and process variation.

Fig. A.30 shows the SNDR with respect to the supply voltage for a S/H using bootstrapped switch for the input switch and another using regular CMOS switches. Both S/H are sampled at 10 MHz and uses the BPS technique. The input signal has an amplitude of 0.8 Vpp and a frequency of 2 MHz. It can be seen for the S/H that uses only CMOS switches, that for supply voltages lower than the typical one, an important SNDR loss can be noted. Using bootstrapped switch for the input switch overcomes this problem as it can be observed in Fig. A.30. In fact, when Vdd decreases, the bootstrapped switch On resistance increases but remain signal independent. While, for the CMOS switch, decreasing Vdd leads to an input voltage swing for which the NMOS transitor of the CMOS switch is in the subthreshold region instead of being in the linear region. The lower the supply voltage the wider this swing. This dysfunctionnality along with the increase of the resistance cause this SNDR decrease.

Fig. A.31 shows the SNDR measured at a S/H output with respect to the temperature for three types of processes. The electrical simulation conditions are identical to those of Fig. A.30 with $W_p = W_n = 50\mu m$ and Vdd=1.2 V. As it can be seen, the SNDR is enhanced by the temperature increase. This result is explained by Fig. A.32.a) that shows that the switch resistance decreases with temperature increase. In fact, temperature variation affects mainly two parameters that determine the switch resistance(Section A.2.2): the mobility μ and the threshold voltage V_{th}. Both of them decrease with temperature increase but cause opposite variations of the value of the resistance. Fig. A.32.a) shows that V_{th} variation dominates μ variation.

Regarding the impact of process, it can be noticed that for faster process, the SNDR is boosted. This result can be explained by the fact that for faster process, mobility gets higher and V_{th} gets lower which leads to a lower resistance value as shown in Fig. A.32.b).

A.2.8 conclusion

We reviewed in this section the operation of CMOS switches. It has been shown that switch induced errors can be divided into three categories: On phase errors, Off-phase errors and

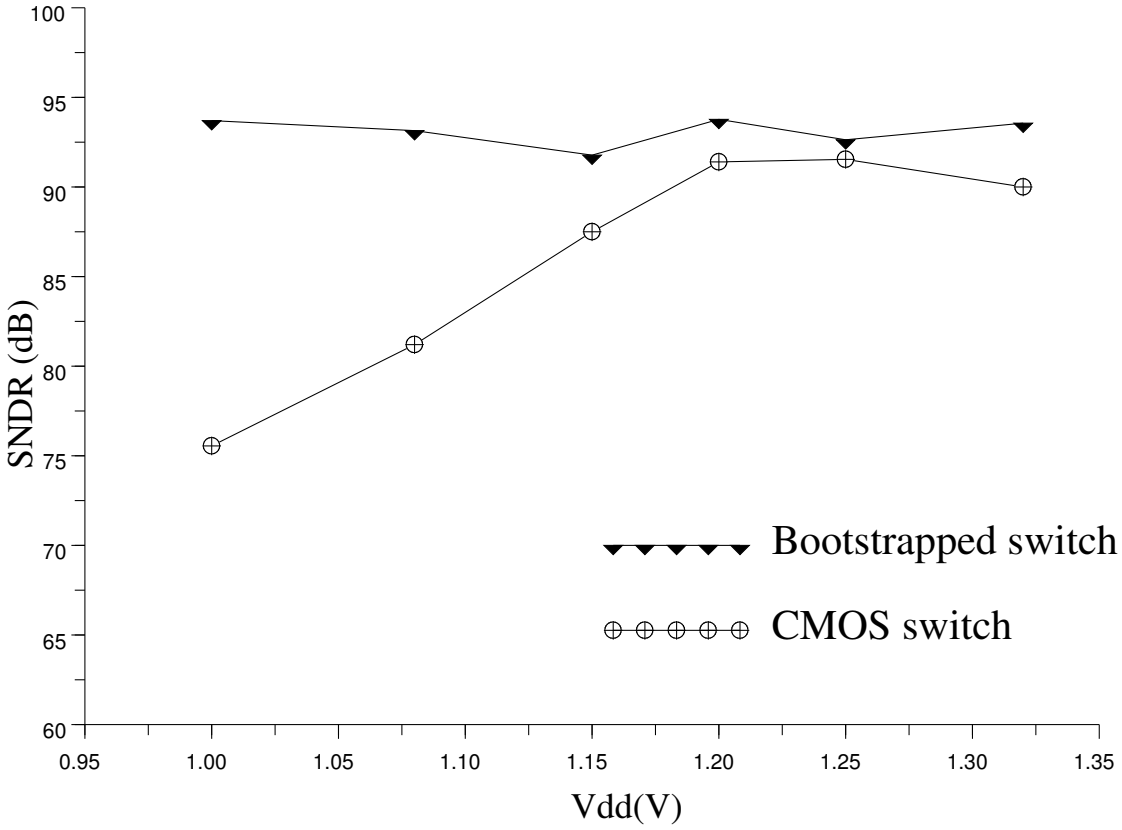


Figure A.30: SNDR Vs Vdd

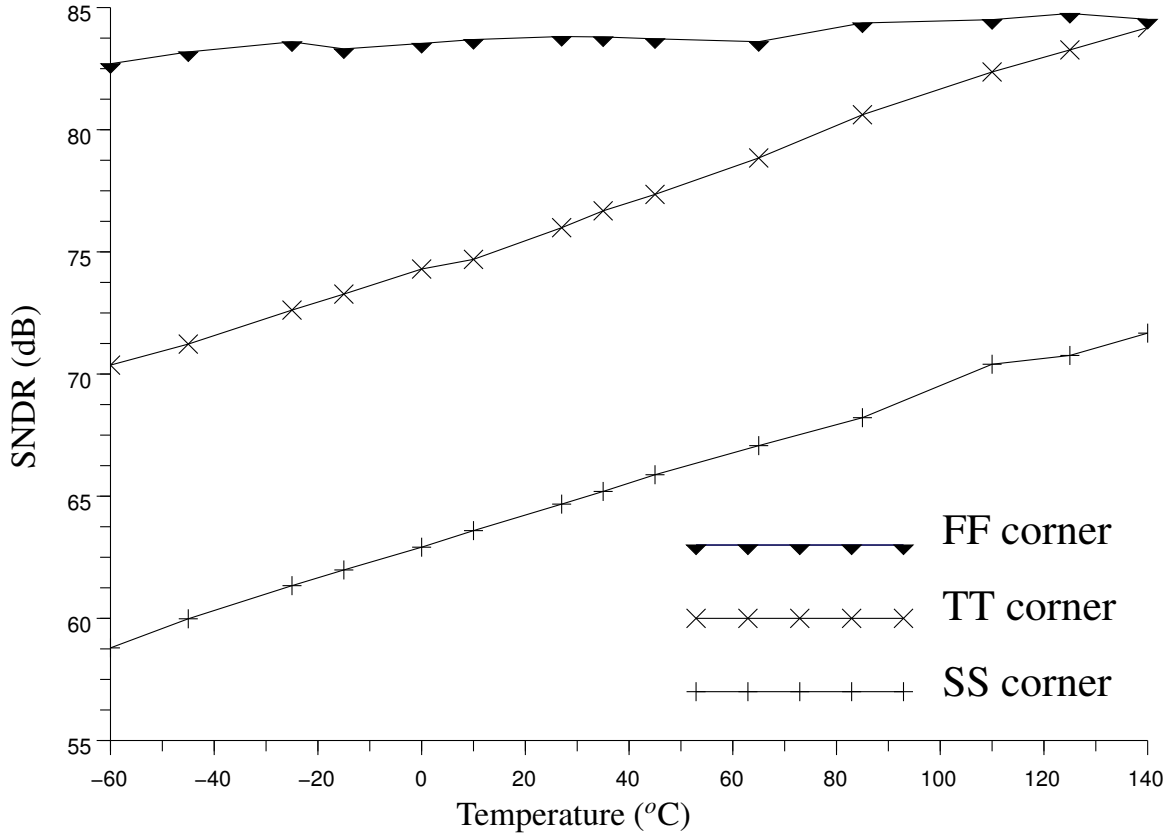


Figure A.31: SNDR Vs temperature for different process corners

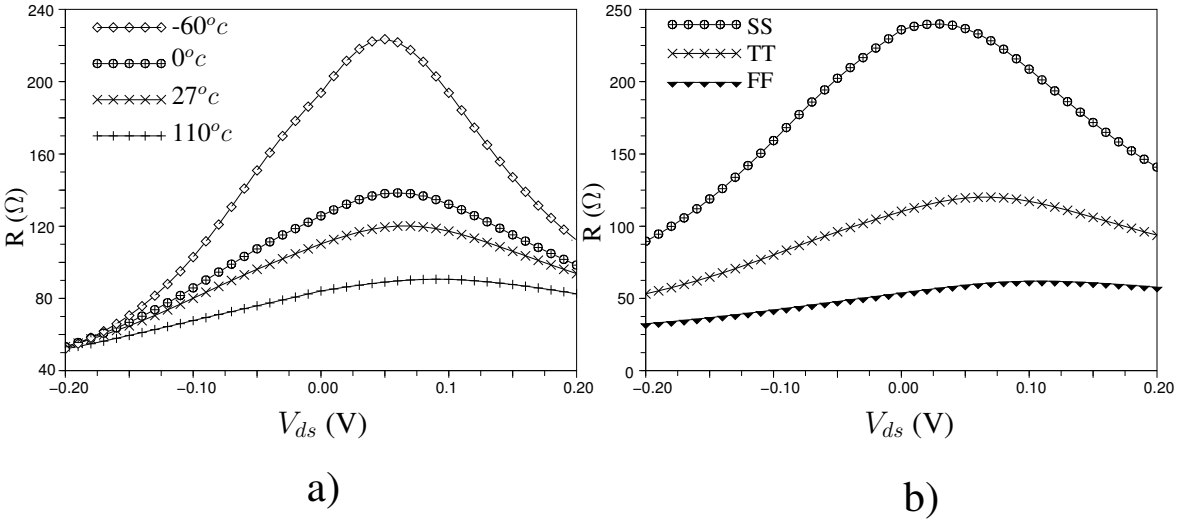


Figure A.32: a)Resistance Vs V_{in} for different values of temperature b)Resistance Vs V_{in} for different process corners

transition phase errors.
In the On-phase, the two main errors are the switch finite On-resistance and its signal dependency. The first causes a large in-band attenuation if the time constant of the sampling circuit is not negligible with respect to the sampling period. Therefore, this error is a concern just in high speed blocks. It is often corrected by employing a digital equalization. The On-resistance signal dependency is a very critical error specially when the required input swing is high. This is often needed when targeting large resolutions in order to increase signal power with respect to the thermal noise. This error causes the arising of distortions in the signal band. Using bootstrapped switches reduces strongly its impact but it is paid by an increase of the die area and the complexity. Therefore, bootstrapped switch use is limited to critical points of the circuits.
In the Off-phase, we showed that the switch behaves as a high pass filter. The error due to the leak current known as the signal feedthrough is thus concern for high speed blocks or sub-sampling blocks. Its impact can be reduced by the use of larger sampling capacitors and by employing correction technique such as the dummy switch addition.
The clock feedthrough and the charge injection errors occur during the On-Off and Off-On transition phases. Their impact is significantly more penalizing in the On-Off transition. The charge injection can be reduced significantly by employing the bottom plate sampling technique and by a good sizing of the sampling capacitors and switches. As for the clock feedthrough, using differential circuits minimizes strongly its effect.

A.3 Quantizer

Since they operate generaly at very high speed and need to achieve the analog to digital conversion in one clock cycle, $\Delta\Sigma$ quantizers are implemented using the flash architecture. A n bits flash ADC is composed by $2^n - 1$ comparators that compare the input signal to $2^n - 1$ reference voltages. These values are usually uniformly distributed between 0 and V_{ref}. Commonly, they are generated on chip, using a resistor ladder but an off chip generation could be considered to increase the flexibility if n is very low. Each comparator is composed by a pre-amplifier, a dynamic latch and a RS latch. The pre-amplifier which use is optional, amplifies the difference between V_{in} and the $V_{comp\ i}$. Then the dynamic latch takes a decision that will be preserved during the clock cycle by the RS latch. The $2^n - 1$ comparators' output is a thermometer code that is converted to a binary code by the encoder.

A.3.1 Dynamic latch

Fig. A.34 shows one way to implement a dynamic latch using CMOS technology [122]. It operates as follows. In the OFF-phase, M7 and M8 connect V_{out}^+ and V_{out}^- to Vdd. In the ON-phase, the circuit can be seen as two inverters in a positive feedback IV1(M9 , M3) and IV2(M10 , M4). In the beginning of the phase, both of their outputs were reset to Vdd in the OFF-phase. At the clock front, V_{out}^+ and V_{out}^- begin to decrease through the NMOS transistors. However, the decrease of the first causes the increase of the second and *viceversa*. Therefore, the node that has a faster decrease in the beginning of the ON-phase thus a lower time constant τ will go down and the other one will remain high. The difference between the two branches of the latch is the R_{ON}s of the input transistors M1 and M2 which depend on the dynamic latch input. Consequently, if

$$V_{in}^+ > V_{in}^- \Rightarrow R_{ON}1 < R_{ON}2 \Rightarrow \tau_{V_{out}^-} < \tau_{V_{out}^+} \Rightarrow V_{out}^- \rightarrow 0$$

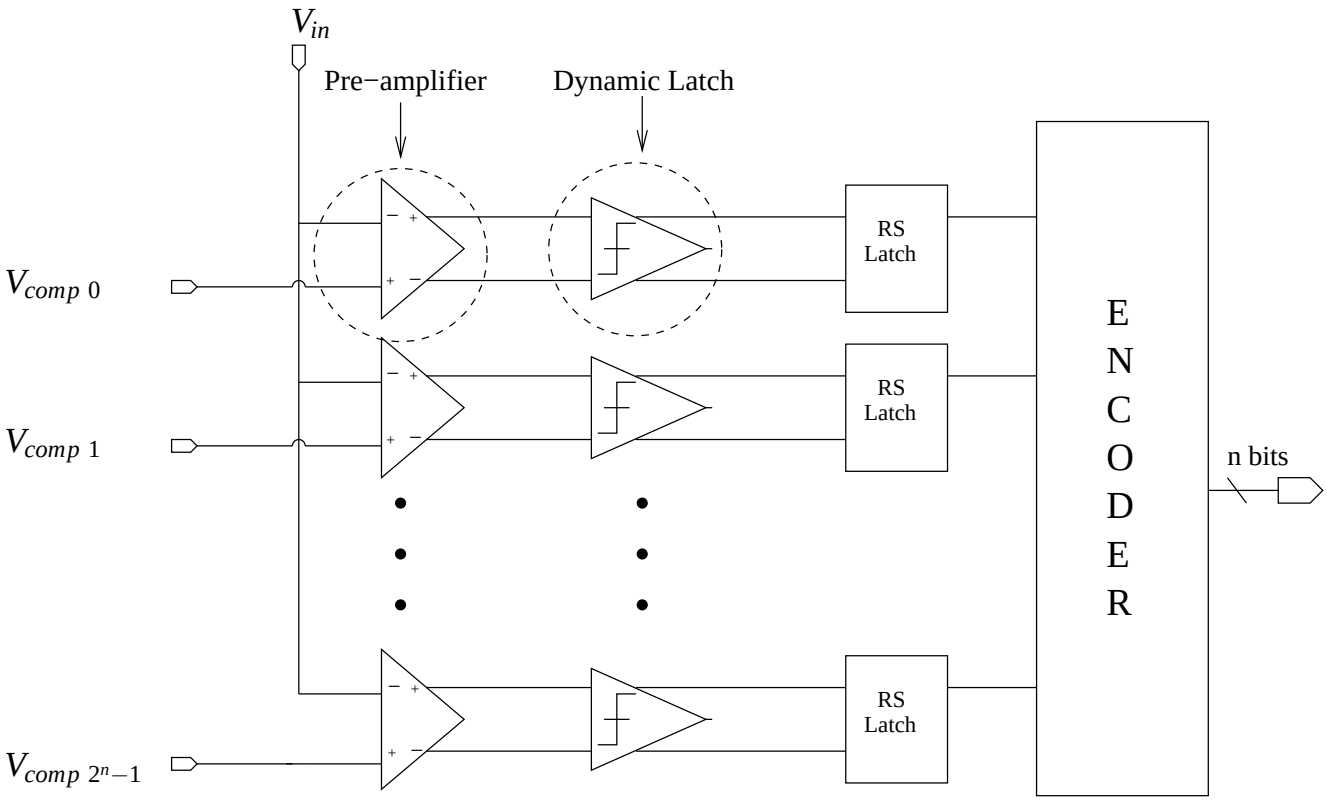


Figure A.33: Flash quantizer

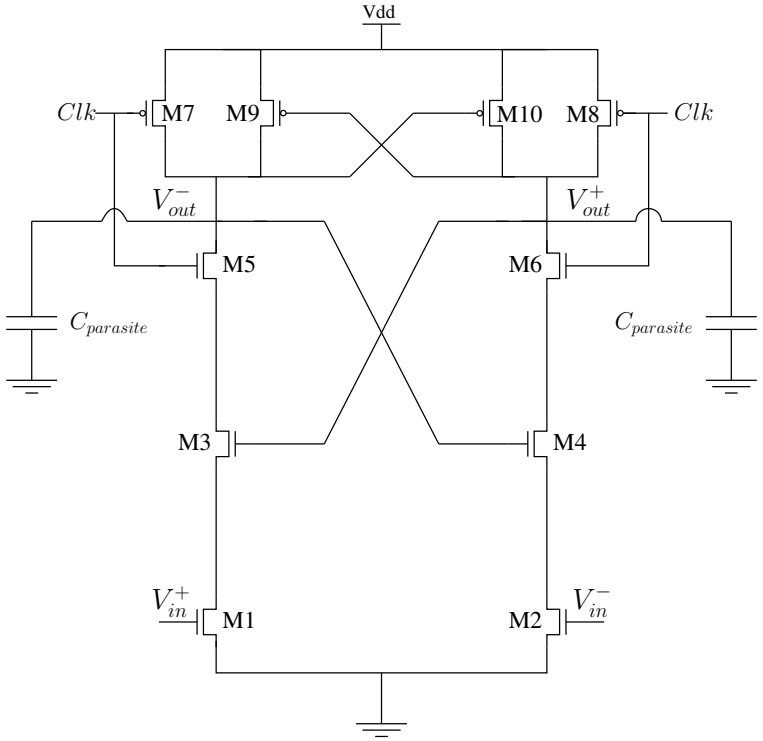


Figure A.34: Dynamic latch circuit

And it is the oppposite if $V_{in}^- > V_{in}^+$.

A.3.1.1 Offset

Offset can be seen as an added voltage to the latch input signal. It is caused mainly by mismatches of dynamic latch transistors and mismatches of switches that are connected to the comparator input[59].

A.3.1.2 Metastability

Metastability occurs when the signal at the input of the latch is very low. In fact, latch settling time depends on $|R_{ON}1 - R_{ON}2|$ and consequenlty on V_{in}. Then, if the latch time exceeds the length of the latch phase, the output of the comparator will be an undetermined value[42]. The use of preamplifing stage reduces strongly its effect.

A.3.1.3 Hysterisys

This exposed description of the dynamic latch operation is based on the assumption that V_{out}^+ and V_{out}^- are exactly equal to Vdd in the beginning of the ON-phase. This assumption is not perfectly correct[123]. In fact, let us suppose that V_{out}^+ was high and consequently V_{out}^- was low in the previous ON-phase. When the next OFF-phase begins, the parasitic capacitance $C_{parasite}$ between V_{out}^- and the ground is charged through transistor M7. At the end of the the phase, V_{out}^- value is not exactly Vdd due to the settling error that was committed during $C_{parasite}$ charge. The value of this error depends on the value of $C_{parasite}$, $R_{ON}7$ and the sampling period. It results in

$$V_{out}^- < V_{out}^+ \Rightarrow R_{ON}4 - R_{ON}3 = \Delta R > 0$$

Then, if in the next ON-phase, $V_{in}^- - V_{in}^+ = \Delta V > 0$, V_{out}^- should remain high and V_{out}^+ should go low. However, if ΔV is not big enougth to compensate the ΔR created due to V_{out}^- settling error, the outputs of the latch will remain unchanged althougth that they should have changed. This error is known as hysterisys.

A.4 Adder

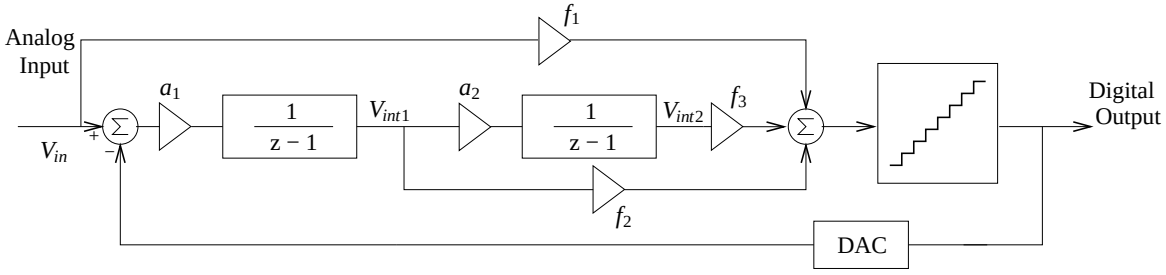


Figure A.35: $\Delta\Sigma$ modulators

In feed forward $\Delta\Sigma$ architectures such as the architecture shown in Fig. A.35, a summing operation is realized just before the quantizer. Unlike other summing operations, it can not profit from integrators' OTA and capacitors and therefore requires a dedicated adder.

This adder can be either implemented using an active circuit or using exclusively passive components. Fig. A.36 shows an implementation of an active adder. By the means of a

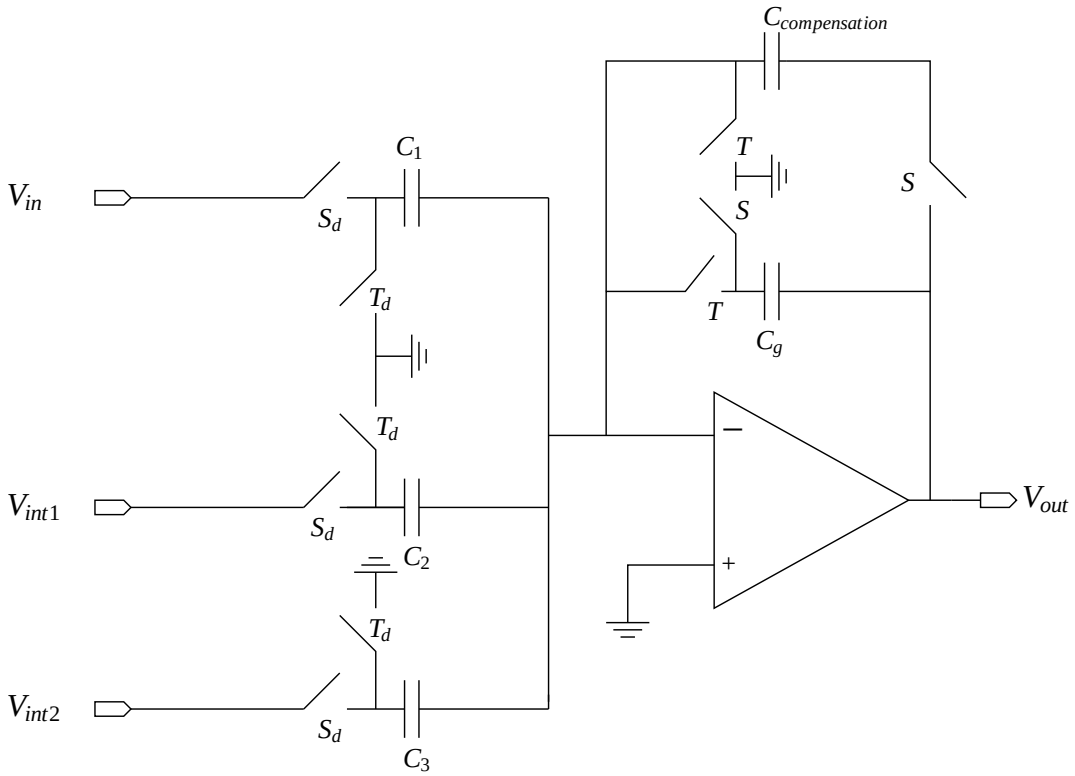


Figure A.36: Active adder

charge transfer calculation, the expression of the adder output can be determined.

$$V_{out} = \frac{\sum_{i=1}^{M} C_i V_i}{C_g} \tag{A.16}$$

If capacitors' values were chosen as follows: $C_1 = f_1 C_g$; $C_2 = f_2 C_g$; $C_3 = f_3 C_g$, V_{out} becomes:

$$V_{out} = f_1.V_{in} + f_2.V_{int1} + f_3.V_{int2} \tag{A.17}$$

Fig. A.37 shows the circuit of a passive adder. The output expression is given, in this case, by:

$$V_{out} = \frac{\sum_{i=1}^{M} C_i V_i}{\sum_{i=1}^{M} C_i} \tag{A.18}$$

If capacitors' values were chosen as follows: $f_1 C_1 = f_2 C_2 = f_3 C_3$, V_{out} becomes:

$$V_{out} = \frac{f_1.V_{in} + f_2.V_{int1} + f_3.V_{int2}}{\underbrace{f_1 + f_2 + f_3}_{\kappa}} \tag{A.19}$$

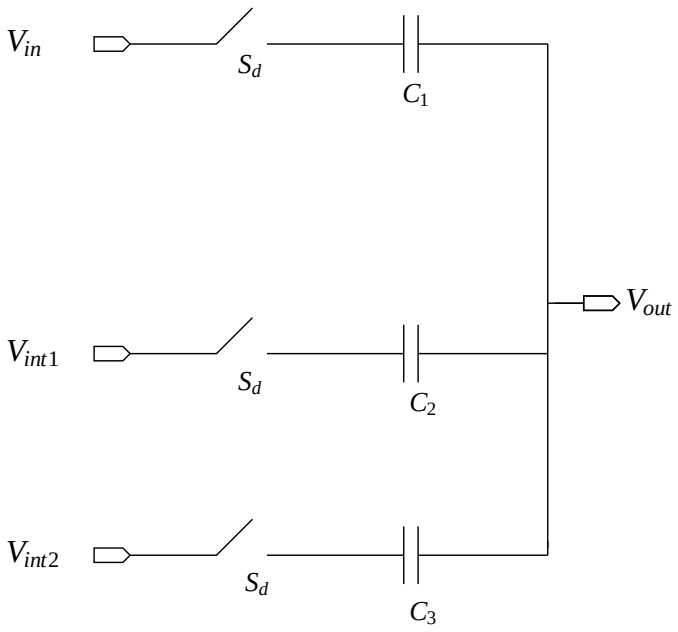


Figure A.37: Passive adder

The expression of V_{out} is not as desired. Nevertheless, the attenuation error can be corrected by dividing the comparison levels of the quantizer by κ.

The choice of the adder architecture depends on many parameters. In fact, the passive implementation has almost no power consumption and needs a smaller die area than the active implementation. However, it suffers from two main drawbacks. First, the attenuation factor κ reduces the signal excursion at the quantizer input which increases the constraints on the quantizer in terms of offset, hysteresis and specially metastability. This can be reduced during quantizer design specially by enlarging pre-amplifiers' gain but it will cost additional power consumption and die area. Moreover, the parasitic capacitance at node V_{out} that is mainly formed by quantizer input capacitor, has an important impact on the operation of the passive adder because it contributes, proportionally to its value, in fixing the potential at node V_{out}. Therefore, the values of feed forward capacitors must be quite higher than the parasitic capacitance which will be paid also in a die area increase and a larger load on integrators.

Appendix B

Layout considerations and techniques

To reduce as much as possible its induced performance degradation, analog layout must be carried out while taking into account a large numbre of considerations. Some of these considerations such as speed and area are considered also in the layout of the digital blocks. However, others as matching and coupling are proper to layout of analog blocks. This section discusses analog layout considerations and presents some techniques that allow to improve matching and secure manufacturability.

B.1 General

B.1.1 Wires

Wires are used to connect circuit components such as transistors, resistors and capacitors to each other. They usually consist of a metal rail. Several layers of metal exist in the process as shown in Fig. B.1, thereby allowing the implementation of any circuit even if it has complex architecture. Each rail has a minimal width and should be separated to other rails in the same layer by a minimal distance. These rules are fixed by the process precision. Moreover, a rail can be connected to another one at a higher or lower level using inter-layer connector known as "viax".

Two important parameters must be taken into consideration when a wire is drawn: resistance and parasitic capacitances.

B.1.1.1 Resistance

A rail resistance is given by [106]:

$$R = R_{\square}\frac{l}{W} \tag{B.1}$$

where $R_{\square}$ is the sheet resistance, l and W the rail length and width respectively

When several rails are used to form a wire, the overall resistance is the sum of the rails resistance and the inter-layer connections resistance. These connections are formed by a number of viax in parallel and therefore their resistance is equal to the resistance of one via divided by the number of used viax.

The wire resistance value is fixed to satisfy one of two requirements: voltage drops and rise-fall times. The voltage drop caused by a wire is given by:

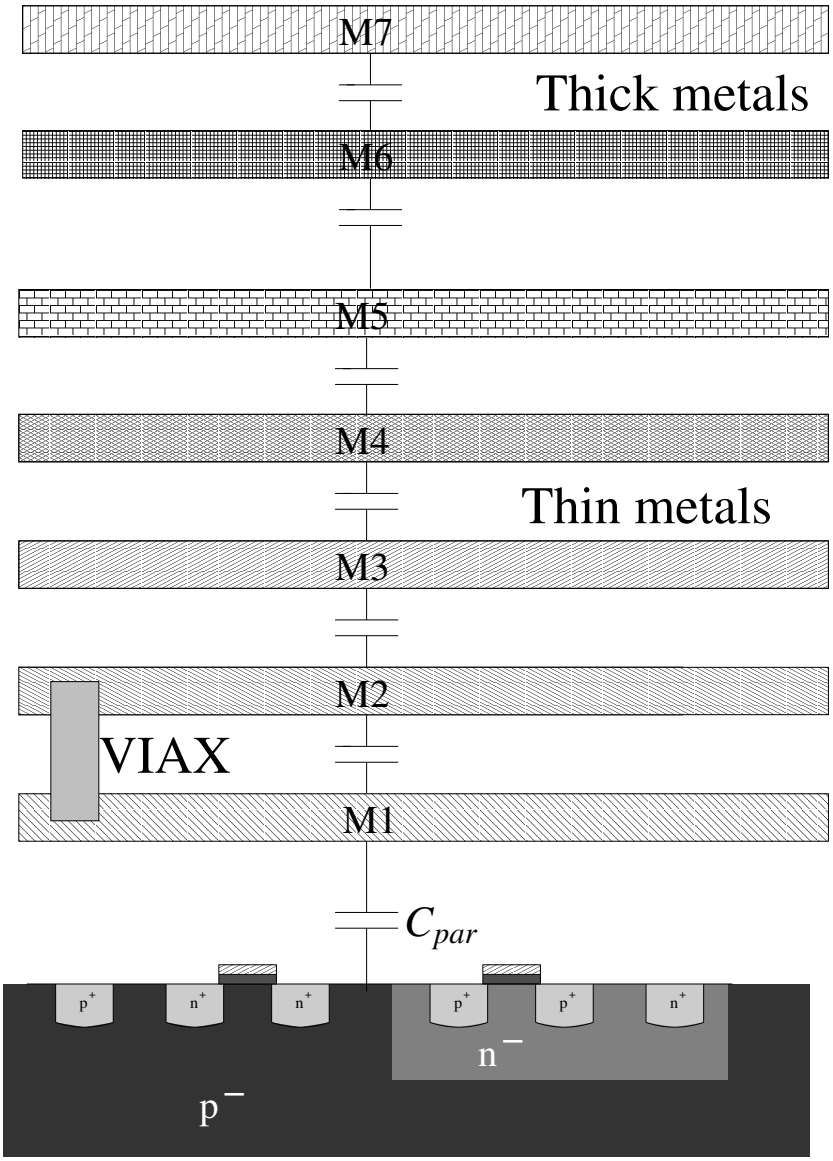


Figure B.1: Chip layers

$$\Delta V = R.I, \tag{B.2}$$

where R is the wire resistance and I the current passing through

The maximum tolerable voltage drop is fixed usually by common sense. However, for wires crossed by important current such as power supply ones, electrical simulations are performed to find the maximum tolerable voltage drop for which the circuit performances still satisfy the targeted specifications. On the other hand, a low wire resistance can be required to reduce a rise-fall time. For example, the sampling switches must have a fast transition control clock to sample the input value correctly [121]. The transition time constant is equal to:

$$\tau = R.C_{par}, \tag{B.3}$$

where R is the wire resistance and C_{par} the sum of all parasitic capacitances.

B.1.1.2 Parasitic capacitances

As shown in Fig. B.2, two adjacent rails form together a capacitor. If the two rails are on different layers and cross, the created capacitor is called a crossing capacitor. Meanwhile, if two rails run parallely on the same layer or on different layers, the capacitance is called a fringing capacitor. In both cases the parasitic capacitance value is given by:

$$C = \varepsilon_0 \varepsilon_r \frac{S}{e} \tag{B.4}$$

where ε_0 is the void permitivity, ε_r the relative permitivity of the insulating material, S the surface and e the thickness

The existence of this parasitic capacitance creates a coupling between the signals of the two rails. If the two rails transport DC signals, the effect of coupling is positive because it allows to filter high frequency noise. Therefore, the parasitic capacitance between such rails should be maximized. In practice, supply and reference rails are placed in the same position in successive metal layers or in parallel in the same metal layer with a very low spacing between them. For all other rails, coupling should be minimized specially if one of the signals is an analog one. To achieve this, the parasitic capacitance should be minimized by increasing the spacing between rails for fringe capacitor and by taking several metal layer gap for crossing capacitance.

B.1.2 Transistors

A MOS transistor is composed by 2 heavily doped regions that form the source and the drain and a polysilicon layer separated for the substrate by a oxide layer that forms the gate. The minimal length achievable for the gate is the parameter that characterizes a process. In 1965, Moore predicted that the number of transistors in a given die area of silicium should double each two years. That is why the transistors minimal length is divided by approximatively by $\sqrt{2}$ from one process to the following.
A NMOS transistor is realized in a p-well, its source and drain are doped N+. While a PMOS is implemented in a n-well and its source and drain are doped P+. Generally, the substrate is one big p-well and local n-wells are realized for PMOS transistors. Several types of NMOS and PMOS transistors are generally available. Two main parameters distinguish them: the

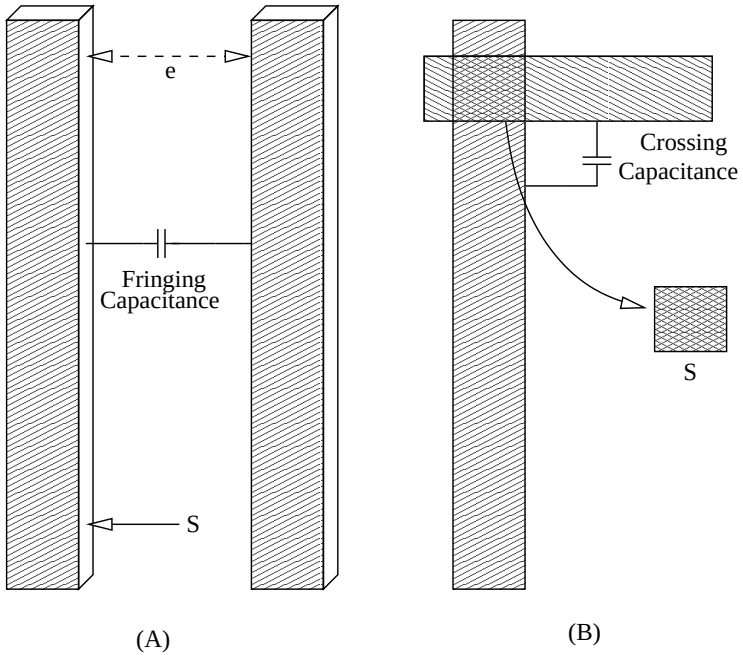


Figure B.2: Fringe and crossing parasitic capacitors

threshold voltage which is controlled by the active regions doping and the breakdown voltage which is fixed by the gate thickness. In the digital flow, only the standard type of transistor is available.

In analog circuits, transistors' width could reach very large values compared to the ones used in digital circuits. Therefore, large transistors are usually divided into smaller ones called finger. This technique allows firstly to improve the transistors geometry, secondly it permits to reduce the source and drain parasitic capacitances to substrate as shown in Fig. B.3 [107] [110]. Moreover, the gate resistance is reduced when using the mutli-fingering technique. Its main drawback is the layout complexity increase because all gates, sources and drains must be connected by additional wires.

B.1.3 Capacitors

To implement a capacitor, two conductive plates separated by an insulating material are required. Three options are available to achieve this in CMOS technology: either using the intra-layer insulating material, the inter-layer one or both.

A number of parameters are critical in capacitor design:

- Linearity is the criteria that determines if the capacitor preserve a constant value regardless of potential difference on its terminals
- Density is defined as the ratio of the capacitor value to its surface
- Parasitic capacitances: The capacitor two plates form together the desired capacitance but unfortunately they form parasitic capacitances with other element and specially the substrate.
- Precision: The precision can be seen as the deviation of the capacitor value due to process variation in comparison to the theoretical value.

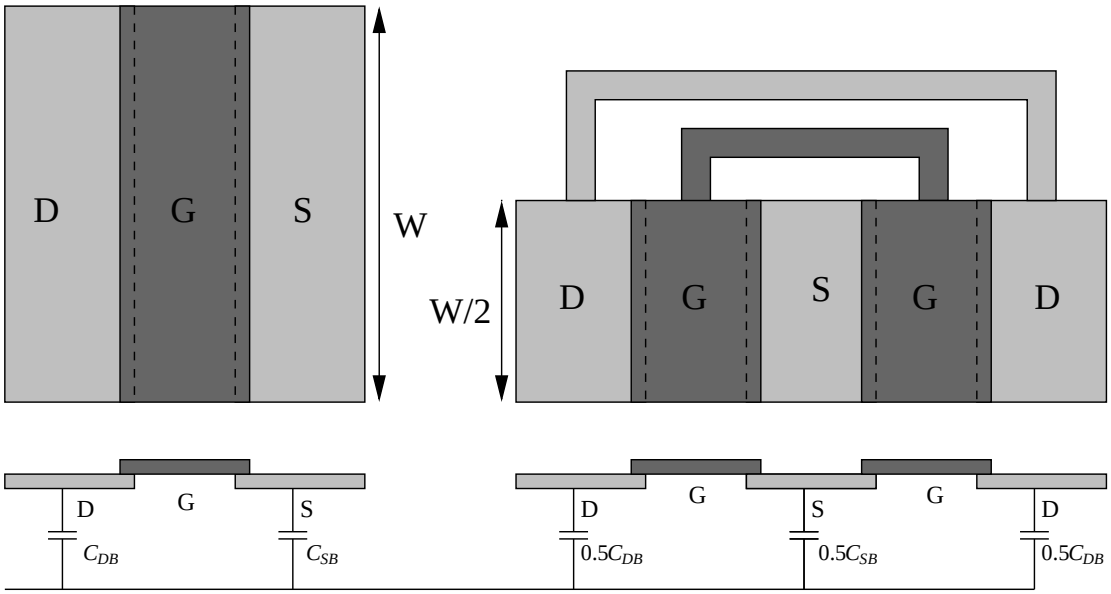


Figure B.3: Comparison between a one finger and a two finger MOS transistor

Various types of capacitor were proposed. Each has its advantages and drawbacks

- Crossing capacitor: Fig. B.4 shows one way to implement a crossing capacitor. The overall capacitance is the sum of all crossing capacitors. It can be formed on two or more metal layers. The crossing capacitor density depends on the number of the layers used to form the capacitor. Its parasitic capacitance to the substrate depends on the distance between the lower layer used to the substrate. As a consequence, the number of layer used is a compromise of the cited criterias. The linearity of these capacitors is very good

- Fringe capacitor: The fringe capacitor uses the other type of capacitance that may exist between two rails. As shown in Fig. B.5, each rail form with the four surrounding rails four fringe capacitor.(For simplicity, the connections between bottom plate rails and top plate rails were not shown.)
  The linearity of fringing capacitor is similar to crossing capacitor one.

- Poly-oxide Capacitor: A poly-oxide Capacitor is a NMOS or a PMOS transistor of which source and drain are connected. This type of capacitor has a high density but it is strongly non-linear. Fig. B.6 shows the capacitor value of poly-oxide capacitor as a function of its terminals voltage obtained in a electrical simulation using a 65 nm process. As it can be seen, the big variation of its value makes this sort of capacitor inadequate for application where the accuracy on capacitor value is important such as pipeline stages or $\Delta\Sigma$ integrators. The value variation of Poly-oxide Capacitor is due to the fact that it is composed mainly by the channel capacitance of the MOS transistor. The charge stocked by this capacitor is given by [56]:

$$Q = WLC_{ox}(V_{gs} - V_{th}) \tag{B.5}$$

  where W and L are the transistor width and length respectively, C_{ox} the oxide capacitance, V_{gs} the gate-source voltage and V_{th} the threshold voltage

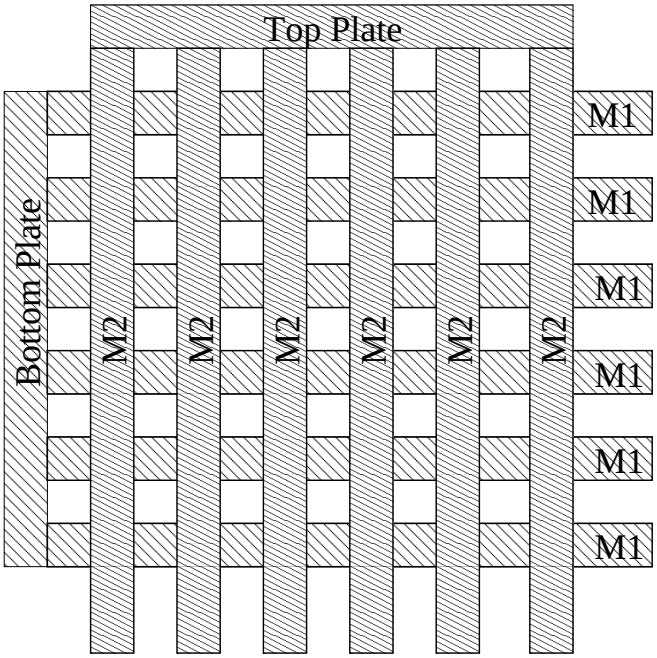


Figure B.4: Crossing capacitor

Consequently the capacitance value is given by:

$$C = \frac{Q}{V_{gs}} = WLC_{ox}\frac{V_{gs} - V_{th}}{V_{gs}} \tag{B.6}$$

- MIM capacitor: MIM capacitor implementation requires additional processing steps compared to the standard digital flow. Two dedicated metal layers are used to realize the two plates. As they are not used to achieve wires, the distance between these two plates is reduced. A high-k material is used for insulation. MIM capacitors are highly linear and have a good density. Moreover, the parasitic capacitance to the substrate is very low because they are realized above all thin metals. However, the application of the MIM mask makes the chip 1 to 2% more expensive which may limit their use specially if the chip analog area is a lot smaller than the digital one.

B.2 Matching

Design studies and most electrical simulations consider that devices have the same electrical properties before and after fabrication. Unluckily, this assumption is not perfectly correct. In fact, due to process variation, coupling and other phenomenas, devices suffer from modification of their electrical properties [106] [110]. Mismatches cause the arising of offset and even order distortions[56]. To overcome this problem, critical components that share the same operation should be matched. For example, in the OTA shown in Fig. B.9, mismatches of the input pair (T_1-T_2) and current sources (T_3-T_{10}-T_{11} and T_4-T_5) are more critical than the mismatches on other transistors. Therefore these components should be matched carefully to secure the OTA performance.

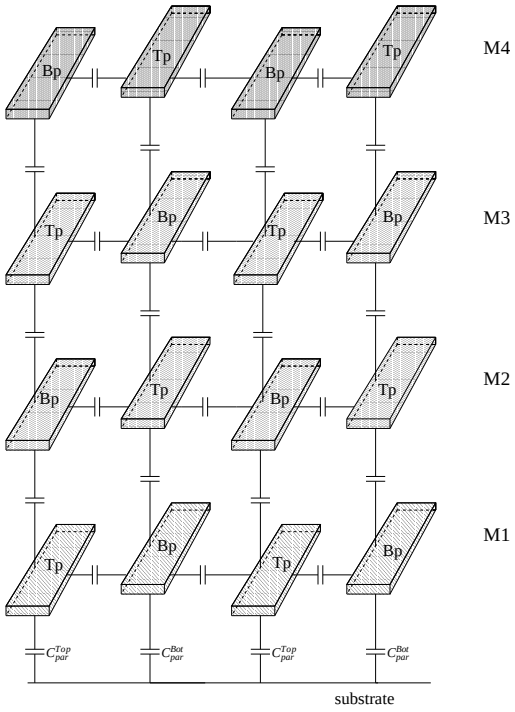


Figure B.5: Fringe capacitor

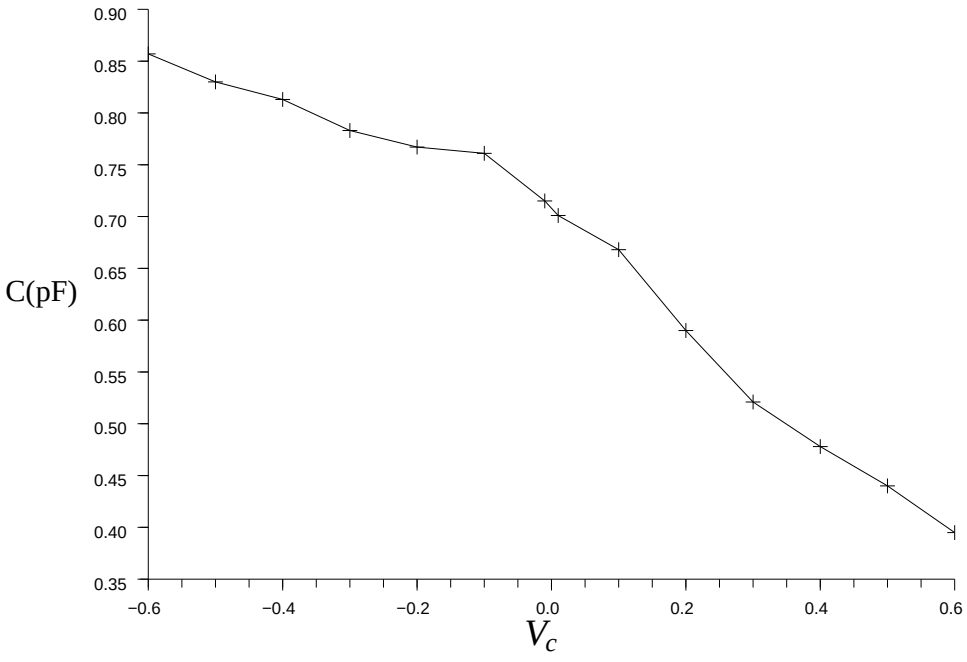


Figure B.6: Capacitance vs voltage for a MOS capacitor

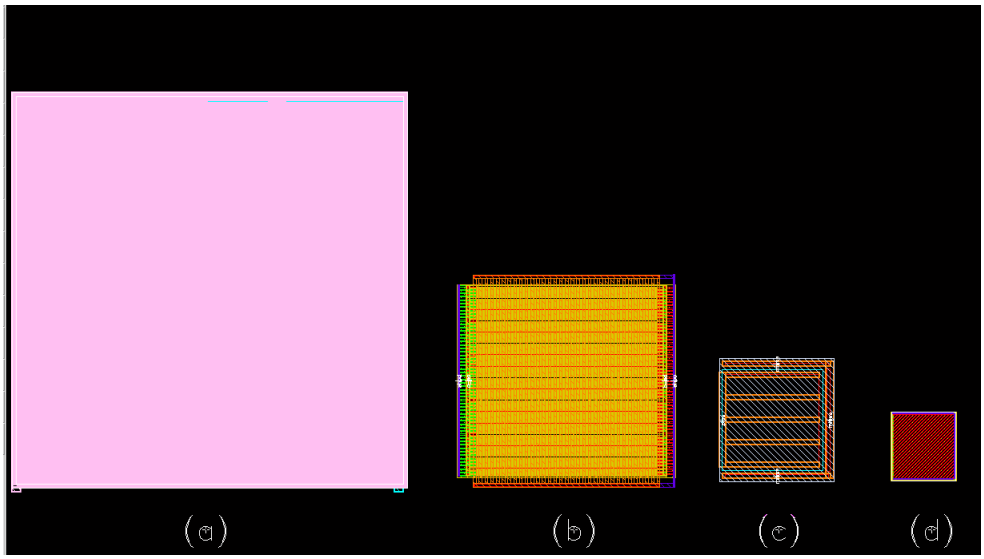


Figure B.7: 1 pF capacitor with 4 different techniques a-crossing, b-Fringe, c-MIM and d-MOS

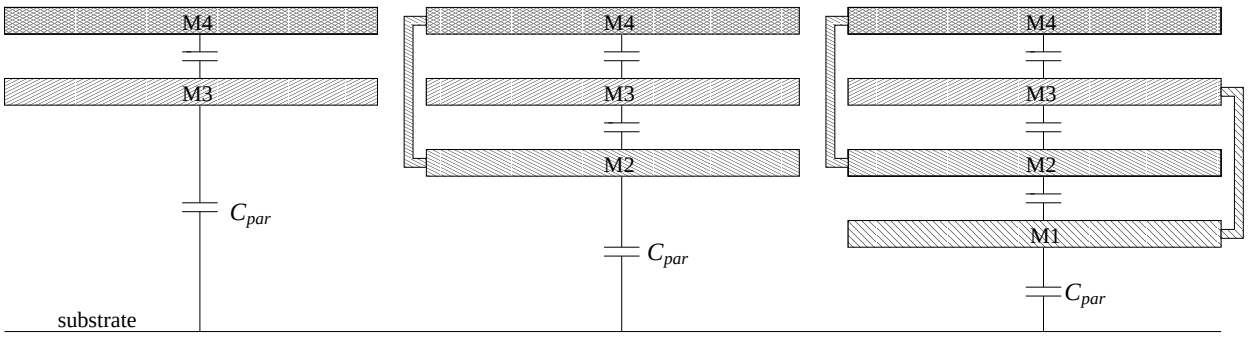


Figure B.8: Parasitic capacitance

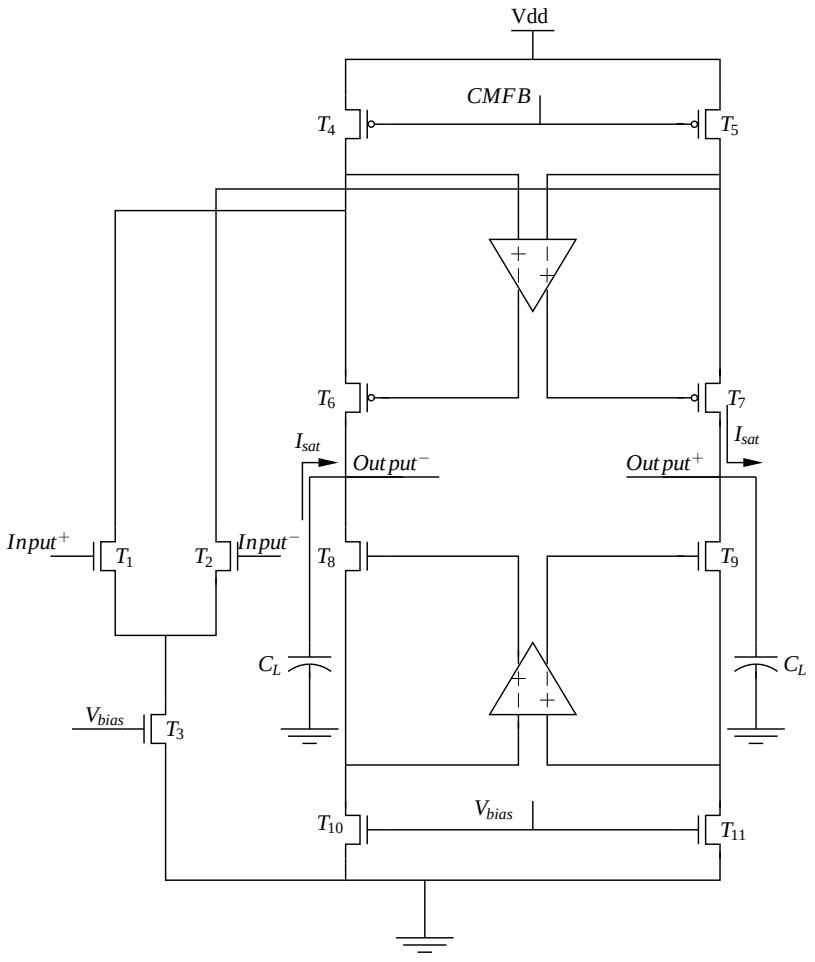


Figure B.9: Gain boosted folded cascode OTA

B.2.1 Mismatch Sources

B.2.1.1 Size variation

During fabrication, components effective sizes differ from the sizes on the layout mask. This difference is due to fabrication problems such as mask misalignments, printing imperfections and etching problems[56].

B.2.1.2 Coupling

Coupling is one of the majors mismatch sources. To understand its effect, let us take the example of Fig. B.10. T1 and T2 are two transistors that should be matched and should have the exact same operation. However, a noisy digital transistor is placed next to T1. The glitches generated by this transistor will be coupled through the substrate and will affect the signal processed by T1 and T2, but since T1 closer than T2 to the noisy transistor, the coupling will be more important for T1 creating thereby a mismatch between the two transistors. To avoid this, the simplest way is to increase the spacing between noisy transistors and sensitive analog transistors. Another scenario for which coupling can be a mismatch source is shown

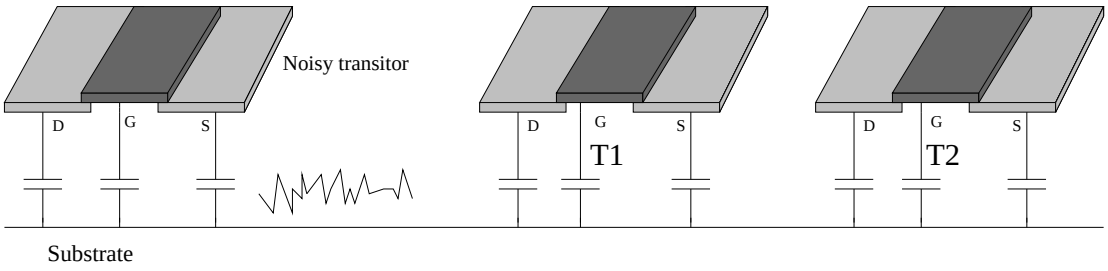


Figure B.10: Substrate coupling

in Fig. B.11. In fact, in this case, the signal that crosses above T1 will be coupled with T1 signals and not T2 signals which generates a mismatch between T1 and T2. For this reason, it is important to avoid passing wires above or under analog transistors, resistors or capacitors specially those that should be matched.

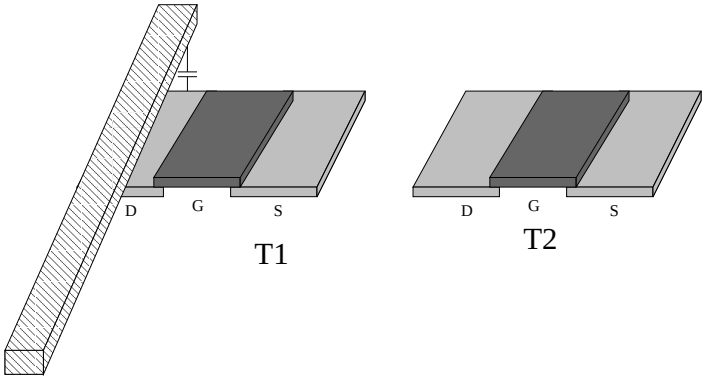


Figure B.11: Coupling

B.2.1.3 Gate shadowing

Gate shadowing is caused by the fact that the implantation of source and drain is tilted [56]. It creates an asymmetry between source and drain. Therefore, gate shadowing should be taken into consideration when designing transistors that should be matched because it may create an asymmetry between them.

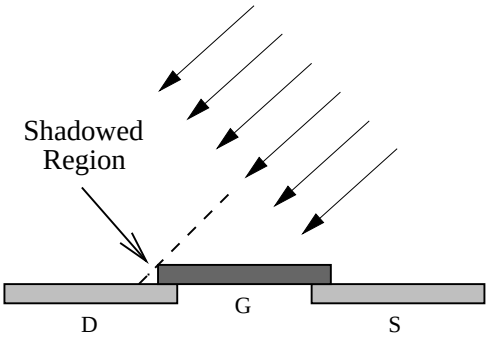


Figure B.12: Shadowing

B.2.1.4 Thermal gradient

Temperature gradient occurs if some of the circuit components such as resistors generate too much heat and since the electrical properties of most elements are temperature dependent, those that should be matched must be placed symmetrically to the heating component to ensure that they operate at the same temperature.

B.2.2 Matching techniques

B.2.2.1 General considerations

Some common practices are necessary to achieve a well-matched layout. Symmetry is one key practice in differential circuits. It minimizes offsets and even-order non-linearities. For example, if the wires connecting symmetric transitors in a OTA have different resistances, an offset at the output of the OTA appears. Therefore, it is preferable to layout one side of any differential block and to mirror it to have the other side.

It is also important to place components that should be matched at the minimum spacing possible. In fact, the process in two distant points of the circuit is random and consequently these components will suffer from uncorrelated variations. This may create a big mismatch between them.

Another good common practice to improve matching is to decompose big components into smaller ones. For example, if 2 capacitors of 1 pF are to be implemented, it is better for the matching to achieve this using 10 smaller capacitors of 200 fF instead of using two capacitors of 1 pF. The choice of the unity element depends on several parameters. In fact, choosing a very small value for the unity element allows to improve matching but it has on the other hand some drawbacks. Firstly, precision on very small elements is not as good as for bigger one. Secondly, using many elements increases layout complexity and in the cases where spacing between components is required it cause an increase of the die area needed also. Therefore, the value of the unity element is choosen as compromise of these parameters. It must be also a common divider for all elements that should be matched to allow the implementation of

the components using a integer number of unity elements. It is also important that all of unity elements share the same electrical propreties. Therefore, it is important that they have the same environment during fabrication. Suppose that eigth unity capacitors are placed in a row. Each one of them see at its left and at its right another similar capacitor except the two peripherical ones. To overcome this problem, two additional capacitors, called dummies, can be placed from one side and the other to ensure that all of the eigth capacitors have the same environment.

B.2.2.2 Common centroid

Common centroid is a thechnique that is used to improve matching . It can applied for capacitors, resistors and transistors. The main idea of this technique is to make in sort that all the components that should be matched share the same center of symmetry[107] [106] [56].

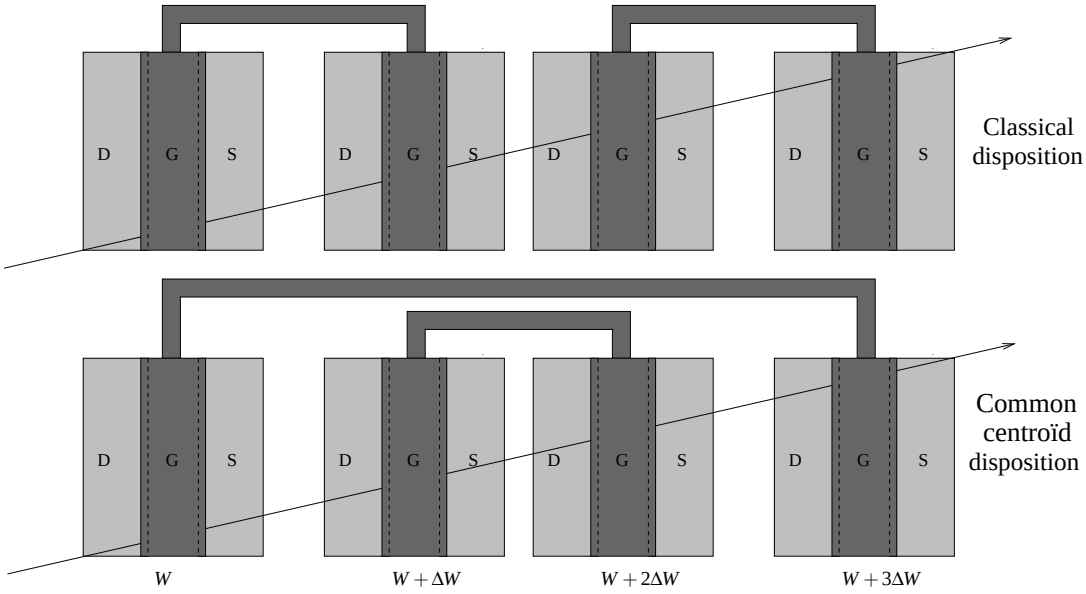


Figure B.13: Effect of a one-direction gradient

Fig. B.13 shows two ways of implementing two identical transistors using four smaller ones. As it can be seen, using the commond centoid method allows to reduce the effect of size variation. In fact, the size variation effect can be modelised as a two dimension gradient. In this case, its vertical composant is identical for all of the four transistors. Meanwhile, the horizontal one is different from one transistor to another but when placed in commond centoid disposition, this effect is compensated. Besides, the common centoid has another advantage. In fact, since the matched elements are intercalated, the effect of environment variation due to coupling, supply or temperature variation is reduced in comparison to a classical disposition. However, common centroid has a small drawback is that it makes the layout more complex. Fig. B.15 shows the layout of the current mirror of Fig. B.14 using the commond centroid technique.

B.2.2.3 Triple-well

The triple well is a technique that allows to create a p-Well that has another potential that the main substrate. It is achieved as shown in Fig. B.16 by implementing a ring of a deep

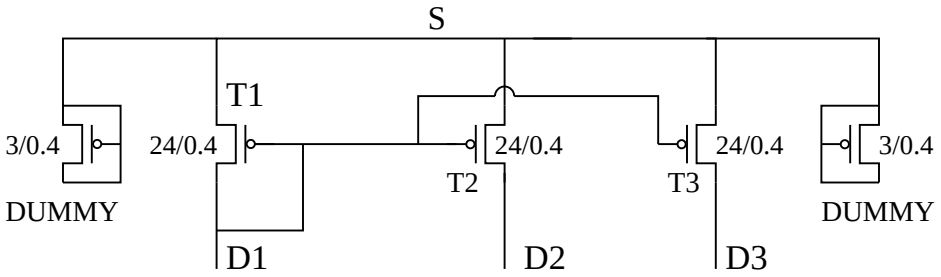


Figure B.14: Circuit of the current source

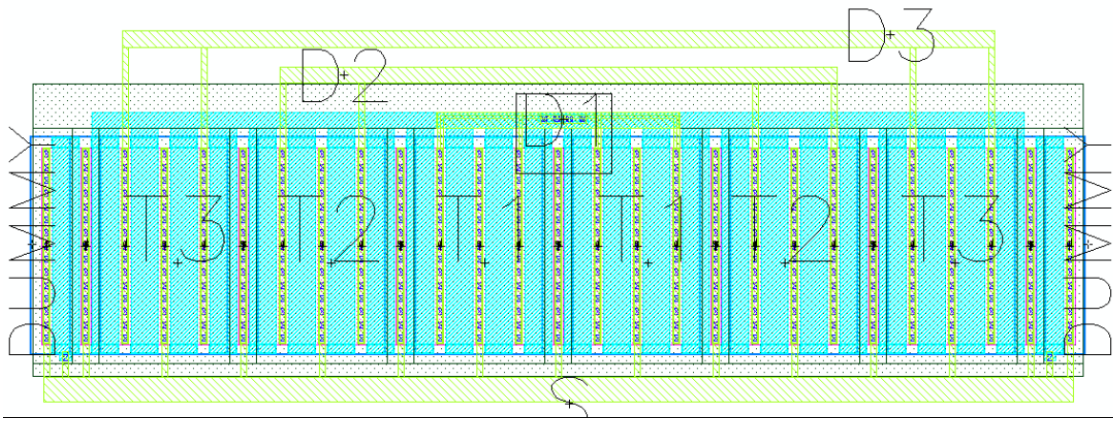


Figure B.15: Layout of the current source with the common centroid

n-Well around the area where it is desired to have the triple well. The difference between a triple well and a regular one is that the former is achieved on all the depth of the substrate allowing thereby the isolation of the triple well for the rest of the substrate. This technique has two main purposes. The first one is for design. In fact, in many cases, better performance could be achieved by connected the transistor bulk to a potential different than the ground. For example, it is common to connect OTA input pairs' bulks to their common source. This provide them a constant and smaller threshold voltage. Triple wells are used also for isolation. In general, it is used to isolate the analog part from the digital one in mixed circuit. In fact, digital transistors are very noisy and generate glitches that are absorbed by the substrate. If the analog and the digital parts of the chip share the same well, the analog signals will be affected by the glitches of the digital circuit and this may result in performance loss in the analog part. To avoid this the digital or the analog part could be placed in one or several triple wells.

B.2.2.4 Guard ring

Another way to achieve protection of a sensitive circuit from substrate noise is guard ring [110]. It consists simply of a continuous ring of substrate ties that surrounds the considered circuit as shown in Fig. B.17. Substrate noise will be then absorbed by the guard ring. It is common to use guard rings for capacitor networks specialy those which have high parasitic capacitances to the substrate.

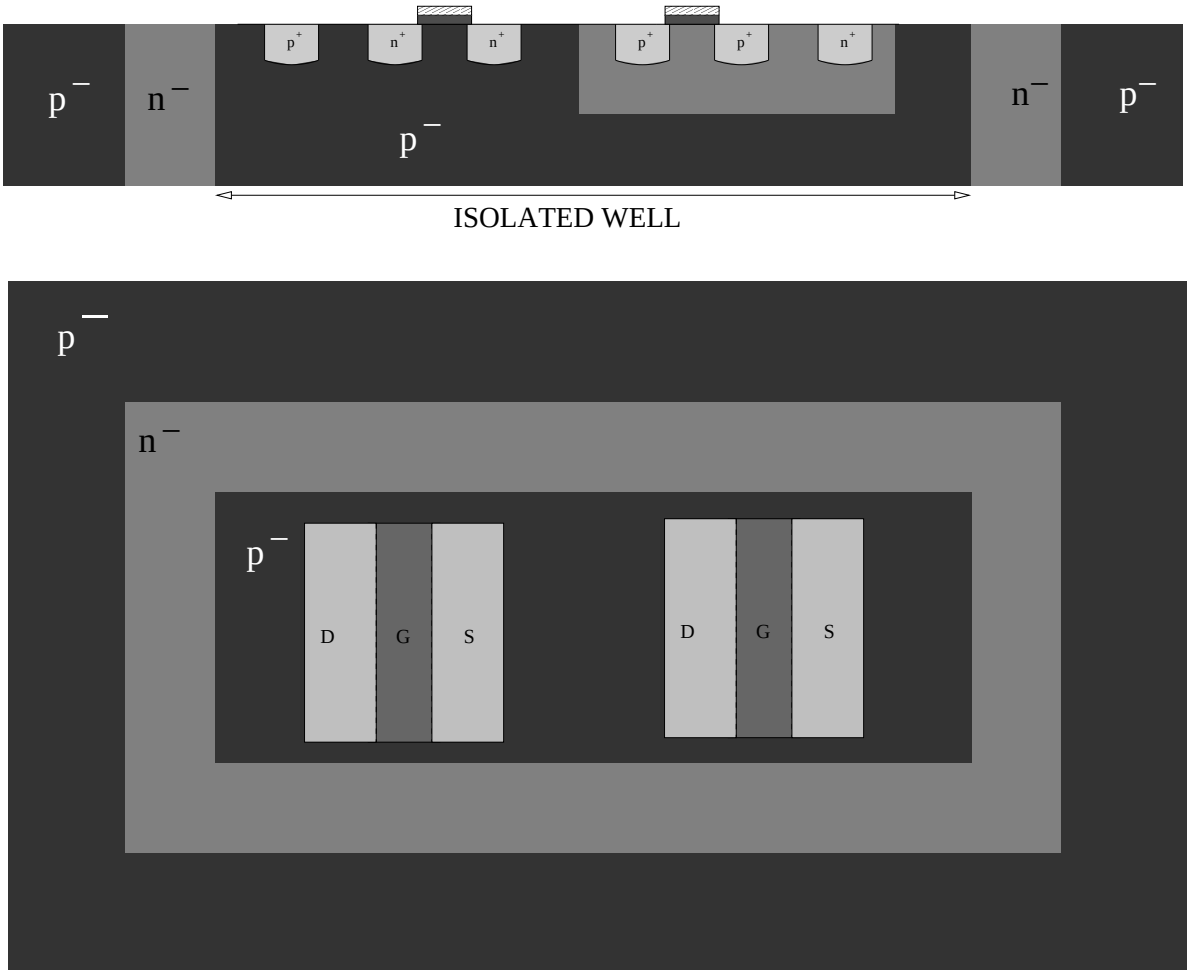


Figure B.16: Triple well

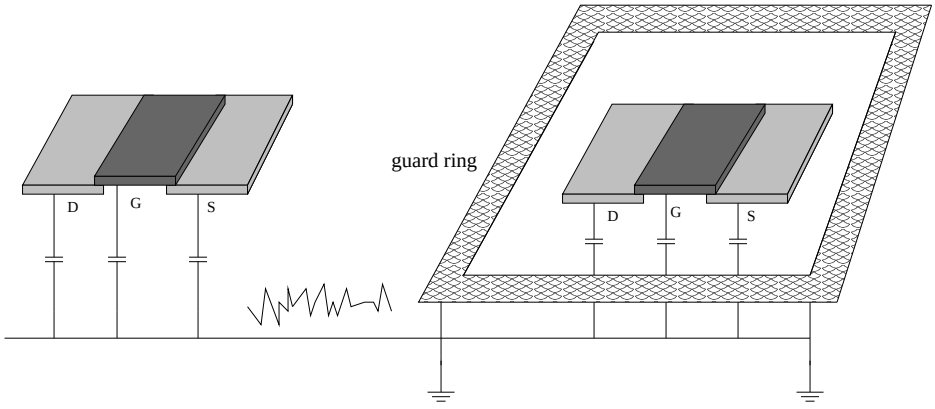


Figure B.17: Guard ring

B.2.2.5 Shields

It was mentioned before that the simplest way to reduce coupling between two elements is to reduce the parasitic capacitance by increasing the spacing separating them. In some cases, enough spacing can not be achieved. Therefore, a wire connected to a DC voltage such as ground could be placed between the two elements. This wire known as coupling shield allows to protect the sensitive wire for the noisy one [110]. The drawback of this technique is the increase of signal loading. In fact, since the shield is closer than the noisy wire to the sensitive wire, the value of parasitic capacitance becomes larger and consequently the loading also.

Figure B.18: Shield

B.3 Manufacturty rules

B.3.1 Latch up

Latch-up occurs when the chip substrate is crossed by large currents. This effect can cause irreparable damages to the circuit [106] [56].
To understand this phenomena, let us consider a NMOS and a PMOS transistor placed side by side as shown in Fig. B.19. A parasitic npn bipolar transistor and pnp one are formed between the doped region of the two MOS transistors. Moreover, since the n-well and the p-well are lightly doped, 2 parasitic resistances R_1 and R_2 exist between the bipolar bases and the n-well and p-well contacts. If for a reason or another, a current is injected at node A, the voltage at this node will increase and since it is connected to the base of Q_2, the current crossing Q_2 and consequently R_1 will increase. This will cause the voltage at node B to decrease causing thereby the increase of the current crossing Q_1 and R_2 which forces voltage at node A to increase further. If the loop gain is greater than one, the current crossing this part of the chip will become excessively high and lead up to its destroy. To minimize latch-up occurrence probability, several techniques can be used. Reducing space between different contacts allows to decrease the value of R_1 and R_2 and the loop gain as a consequence[106]. Larger spacings between NMOS and PMOS transistors permit also to reduce the loop gain. This extra spacing should be performed for large transistors that may generate large glitches which cause latch-up.
Another case for which the latch-up could happen is for transistors that are directly connected to the wirebond. In fact, the static charges on the wirebond could launch the latch-up. To overcome this problem, the simplest way is to connect the transistor source or drain to its bulk. The extra charges are then absorbed by the source and the latch-up risk will be minimized. If the design does not permit such connection, the manufacturer offers a procedure to prevent this problem.

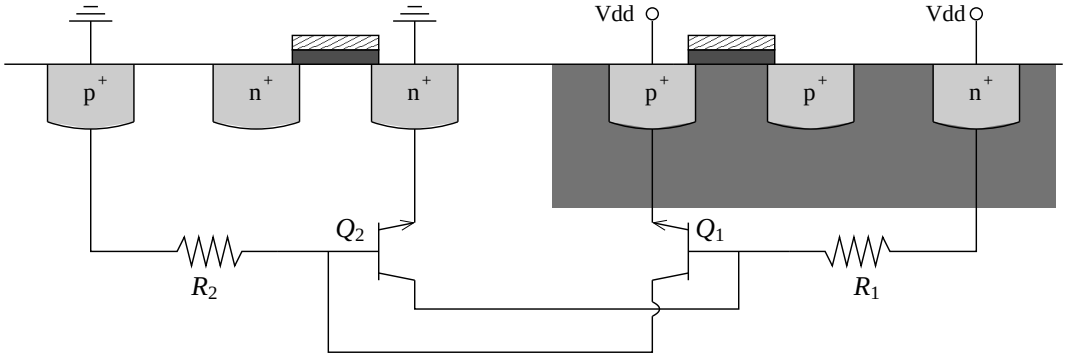


Figure B.19: Latch-up

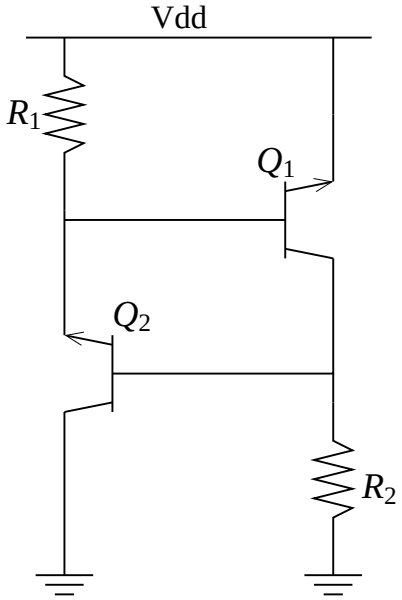


Figure B.20: Latch-up equivalent circuit

B.3.2 Antenna

When a large area of metal is connected to a transistor gate as in Fig. B.21-a, it acts as an antenna attracting some ions. If the metal rail etching began from the gate side, the attracted ions will produce an increase of the rail voltage and if its area is large enough, its voltage can exceed the transistor breakdown voltage. A technique to reduce the impact of this effect is to connect diodes to the transistor gates which are driven by large area rails [56]. Then, if the ions collected during the metal etching cause a voltage increase, the diode will turn on and absorb the charges ensuring thereby that the gate voltage remains lower than the breakdown voltage. Another way to achieve gate protection is to introduce some discontinuity in the gate rail as shown in Fig. B.21-c [56]. However, it is important that the charges collected by the other part of the rail have been absorbed before the implant of "M1-M2" via.

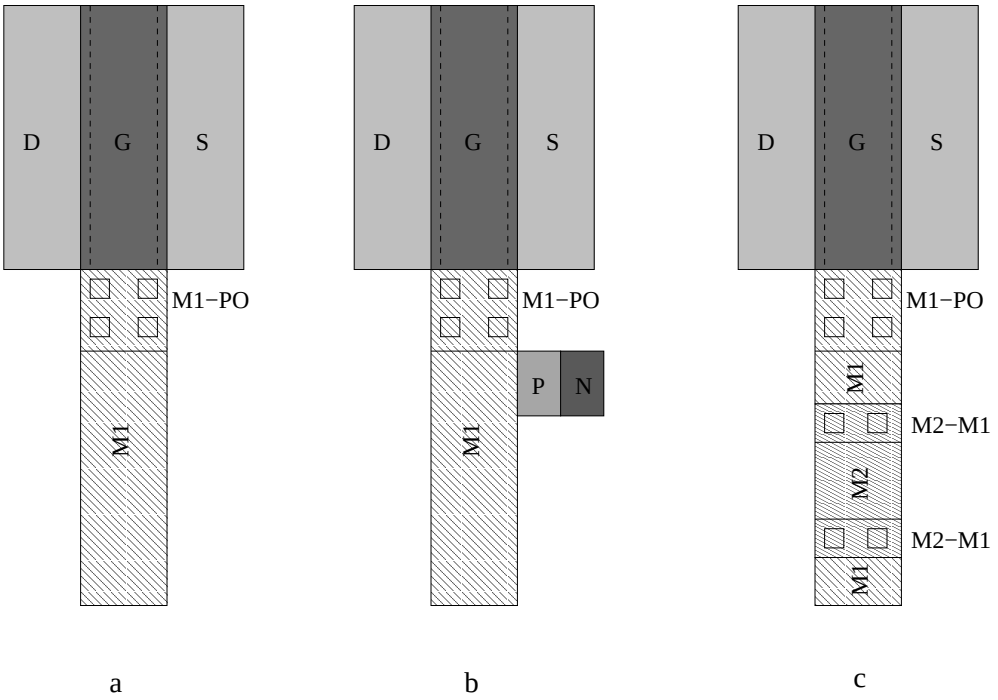


Figure B.21: Antenna

On the other hand, if the metal rail connected to the transistor gate is not too large, the effect will be just the arising of some imperfections in the gate. However if the considered transistor is a part of a current mirror or input pair, these imperfections could be an important source of mismatch. Therefore, even if the rails connected to their gate are not large, transistors that should be matched must be protected by one the two techniques exposed before.

B.3.3 Mechanical Stress

Once fabricated, the silicium wafer contains tens even hundreds of circuits. These circuits must be separated to allow their use. The cutting operation is very accurate and precise. Eventhought it can be a problem source. In fact, during the cutting operation, some mechanical stress is applicated to the chip. This stress is very strong near the I/O ring. Therefore no element should be placed in this region to avoid its split. Moreover very large metal rails

are also very sensitive to mechanical stress. To provide them higher resistance to the stress, they should chopped as shown in Fig. B.22.

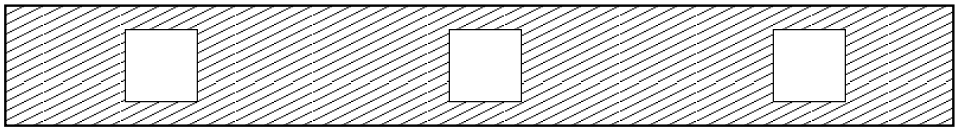


Figure B.22: Chop technique

If the previous conditions were respected, the split probability due to mechanical stress will be very low. Nevertheless, the stress stills cause some imperfections on circuit components that may lead to the arising of mismatches. Therefore, critical blocks should be placed in the center of the chip to reduce as much as possible the impact of the mechanical stress.

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