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Compensation de l'erreur de bande passante dans les convertisseurs analogique numérique à entrelacement temporel

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Résumé en Français

I Introduction

Le nombre important de standards pour la communication sans fil déjà présent sur le marché (GSM, EDGE, TDS-CDMA, WCDMA), ainsi que tous les futurs standards en développement (HSPA, LTE) poussent les ingénieurs système à développer des émetteurs récepteurs extrêmement flexibles pouvant s'accommoder de plusieurs standards différents. Ceci est particulièrement vrai dans les stations de base où le coût d'un redéploiement de station de base est important. C'est le but ultime des "software programmable system" où le traitement analogique est minimisé, ce qui signifie que le traitement spécifique des standards est réalisé en programmant la partie numérique.

D'autres part, la demande grandissante des utilisateurs à accéder à des applications multi-média via leurs téléphones portables, ordinateurs portables ou tablettes poussent les opérateurs à proposer des réseaux cellulaires avec une plus en plus grande capacité de débit. Il est indispensable pour les opérateurs d'offrir des réseaux alliant un débit plus important et un contrôle drastique de la consommation énergétique. Un des défis pour les fournisseurs d'infrastructures de réseaux cellulaires sans-fils est donc de fournir des équipements offrant plus de débit, moins de consommation énergétique et une compatibilité entre les différents standards. Un des points d'attention pour la puissance dissipée étant la chaîne de transmission.

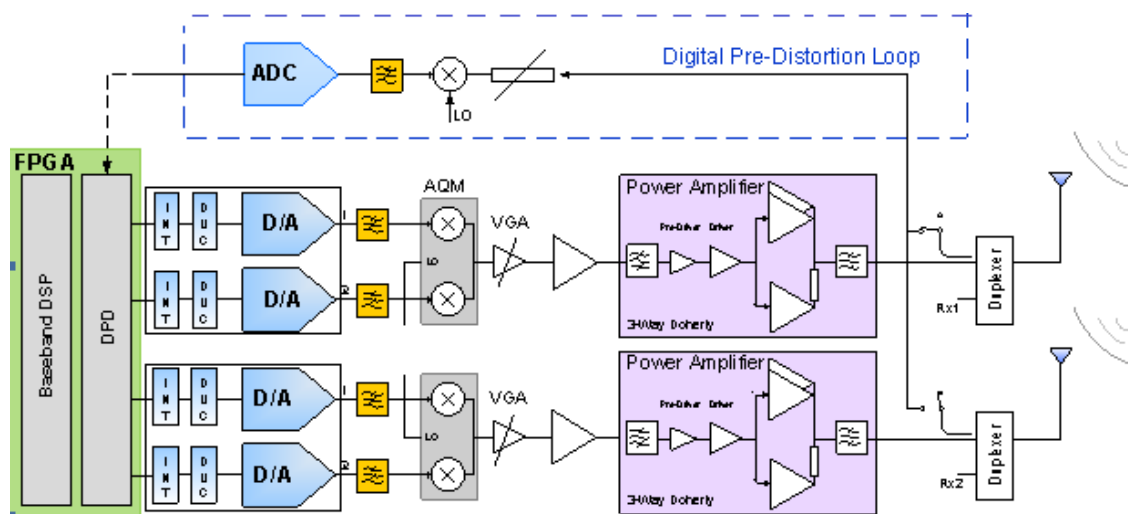


FIGURE 1 – Schéma bloc d'une chaîne de transmission

La Figure 1 représente l'architecture d'une chaîne de transmission la plus couramment utilisée dans les stations de base. Le convertisseur Analogique Numérique faisant l'interface entre le monde, il est très important qu'il soit le plus fidèle à l'information transmise. En effet, transmettre plus d'information nécessite une bande d'utilisation plus large. Pour le convertisseur analogique-numérique (CAN/ADC), cette augmentation de la bande passante implique l'intégration de plus de bruit thermique des étages précédents dans la chaîne radio, ce qui diminue la dynamique d'entrée du convertisseur. Pour palier à ce problème et diminuer le plancher de bruit d'une chaîne de réception, deux solutions :

- augmenter la fréquence d'échantillonnage du CAN,
- diminuer le bruit total du convertisseur, en travaillant à la fois sur le bruit thermique et le bruit de quantification (en augmentant sa résolution).

Pour le CAN, et à linéarité constante, il est aussi difficile de réaliser l'une ou l'autre de ces solutions. Le but des travaux de thèse décrits dans ce document est d'étudier et de concevoir un CAN haute vitesse (500MSPs), haute résolution (16 bits) pour des applications station de base, et plus particulièrement dans la chaîne de réception. Ce CAN devra avoir d'excellentes performances statiques et dynamiques, une très large bande passante, tout en ayant une consommation en puissance, ce qui permettra une meilleure intégration. Le tableau ci-dessous résume alors les paramètres clés pour le convertisseur à réaliser pour les deux modes de transmission émission (Tx) et réception (Rx) ; à savoir : la vitesse (fréquence d'horloge), la résolution (spécifiée par le SNR), la puissance dissipée du convertisseur et le SFDR.

Application	Speed (MSPs)	Resolution (bits)	SNR (dBFS)	SFDR (dBc)	Conso (mW)
Station de base(Rx)	500	14/16	73 _{10MHz} 73 _{380MHz}	94 _{10MHz} 90 _{380MHz}	< 650
Station de base(Tx)	500	12/14	67 _{10MHz} 65 _{380MHz}	88 _{10MHz} 85 _{380MHz}	

TABLE 1 – Spécification du convertisseur hautes performances à réaliser.

II Choix de l'architecture et description du problème

II.1 Etat de l'art

Afin de choisir une architecture adéquate à l'application visée et être compatible avec le niveau d'exigence des spécifications (combinant linéarité, rapport signal-sur bruit, bande passante élevée et faible puissance), un état de l'art a été effectué sur les CANs existants. Celui-ci a permis une comparaison des différentes architectures les plus utilisées dans le marché depuis les années 2000, à savoir le Flash, Folding, le Pipeline, le SAR et le Sigma Delta (Figure. 2). Il apparaît alors que le pipeline est l'architecture qui se distingue le plus par sa haute vitesse pour des résolutions élevées. Par ailleurs, la figure montre qu'il existe un compromis vitesse/résolution pour cette architecture et que pour des résolutions de 16 bit, on ne dépasse pas la vitesse de 20MSPs.

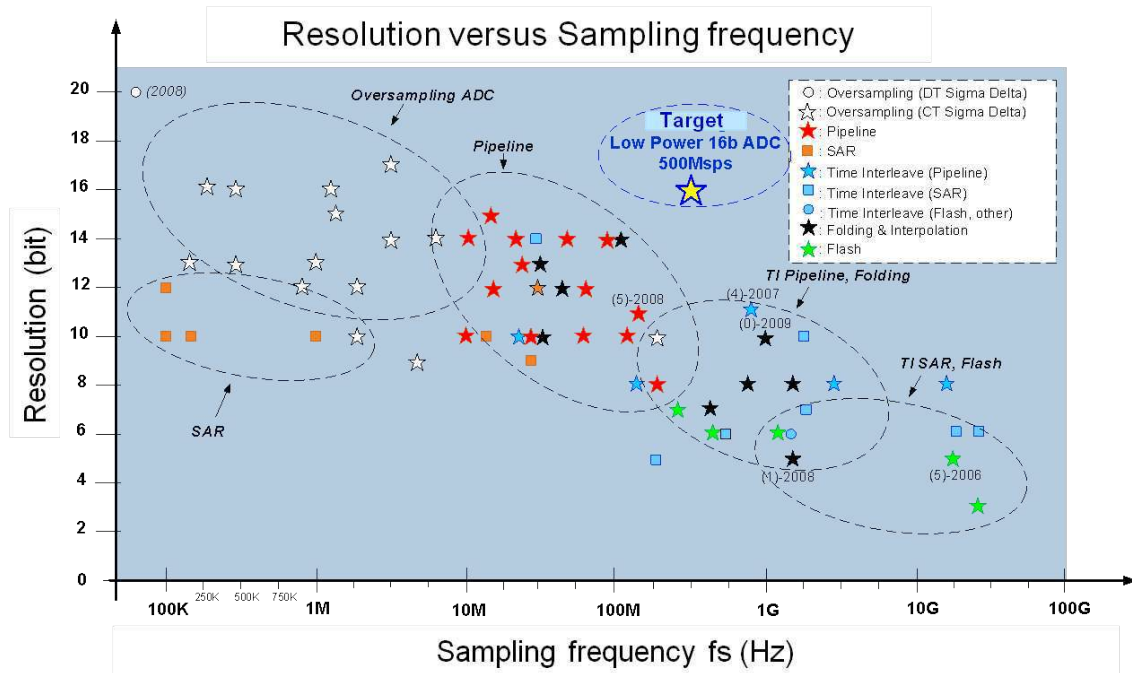


FIGURE 2 – Resolution vs. Vitesse des ADCs dans la littérature (IEEE Journal of Solid-State Circuits, ISSCC International Solid-State Circuits Conference, IEEE transaction on Circuits and System, ESSCIRC, European Solid-State Device Research)

Le principe de fonctionnement de cette architecture est décrit dans la Figure. 3 où le signal d'entrée $x(t)$ est converti successivement par chacun des convertisseurs et est ensuite reconstruit à l'aide d'un multiplexeur. Ceci permet alors de multiplier la vitesse d'une voie par le nombre de canaux pour avoir une fréquence d'échantillonnage plus élevée (f_s). De ce fait, et puisque la vitesse souhaitée de 500 Mps pour un convertisseur pipeline à 16 bits de résolution est à atteindre, le choix de l'architecture à entrelacement temporel (TIADC) peut s'avérer judicieux.

De plus, et afin d'atteindre les performances en consommation souhaitées, le CAN à entrelacement temporel est le meilleur choix architectural pour des fréquences d'opération élevées. En effet pour un noeud technologique donné, la Figure. 4 montre que la puissance consommée par un convertisseur monocanal varie exponentiellement avec la fréquence d'échantillonnage. L'architecture à entrelacement temporel profite alors de la caractéristique linéaire de la puissance consommée de chacune des voies en fonction de la vitesse et par conséquent la puissance dissipée est le produit de la consommation d'une seule voie par le nombre de canaux.

De ce fait, l'architecture à entrelacement temporel combine de bonnes performances en vitesse et en puissance dissipée, ce qui semble être le meilleur choix pour adresser notre problème.

II.2 Convertisseur analogique numérique à entrelacement temporel

L'entrelacement temporel, bien qu'ayant les avantages comme la vitesse ou la consommation dissipée, présente toutefois des imperfections dues aux mésappariements entre les

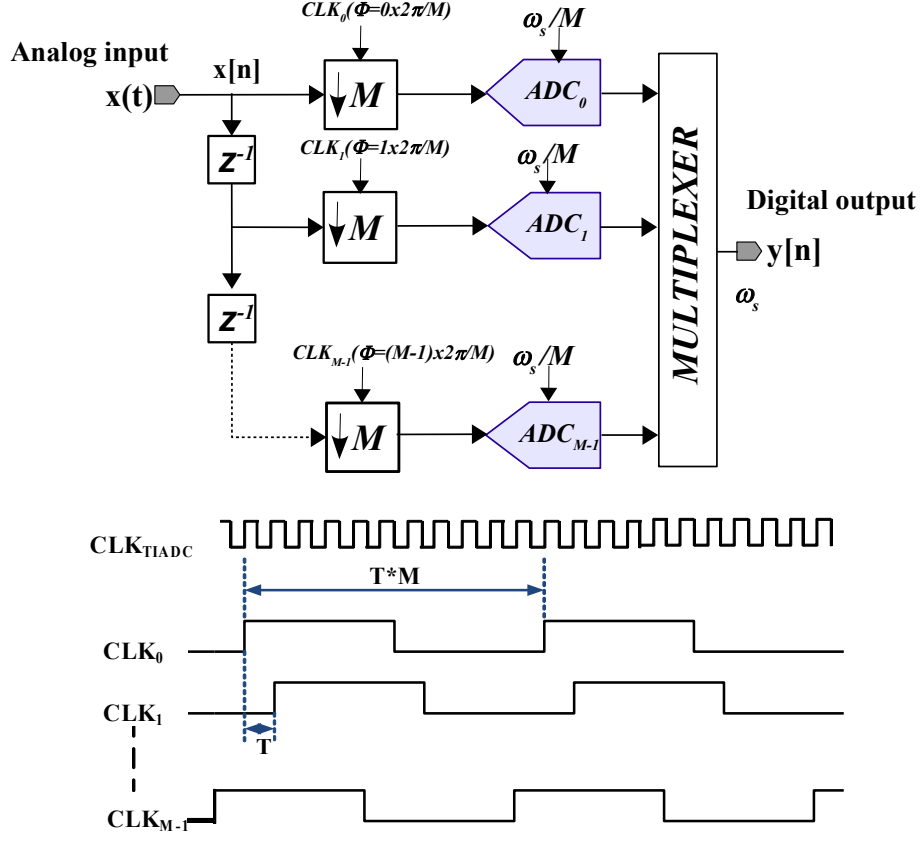


FIGURE 3 – Convertisseur à entrelacement temporel.

voies liés aux changements de l'environnement. Les quatre erreurs les plus connues sont : le décalage en tension (offset), le gain, l'erreur de l'instant d'échantillonnage (skew) et l'erreur de bandes passantes entre les filtres d'entrée des différents convertisseurs.

Soit alors M convertisseurs CANs entrelacé, chacun fonctionnant à une vitesse ω_s/M (Figure 2.4), la sortie de chaque voie i constituant le convertisseur à entrelacement temporel notée y_i et est exprimée par :

$$y_i[k] = g_i x((kM + i)T - t_i) * h_{\tau_i}(t) + o_i. \quad (1)$$

où o_i représente l'erreur d'offset du canal i , g_i l'erreur de gain, t_i l'erreur de l'instant d'échantillonnage et H_{τ_i} , le filtre d'entrée de chaque voie. La réponse en fréquence de la sortie globale incluant toutes les erreurs est donnée par :

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} \left[\frac{1}{M} \sum_{i=0}^{M-1} g_i H_i(j(\omega - k\frac{\omega_s}{M})) e^{-j(\omega - k\frac{\omega_s}{M})t_i} e^{-jk\frac{2\pi}{M}} \right] X(j(\omega - k\frac{\omega_s}{M})) + \frac{1}{T} \sum_{k=-\infty}^{+\infty} \frac{1}{M} \sum_{i=0}^{M-1} o_i e^{-jk\frac{2\pi}{M}} \delta(\omega - k\frac{\omega_s}{M}). \quad (2)$$

L'impact de ces erreurs sur le spectre de sortie est représenté sur la Figure. 6, où nous voyons apparaître des raies de distorsion pour 2 et 4 canaux. Il faut noter que le nombre

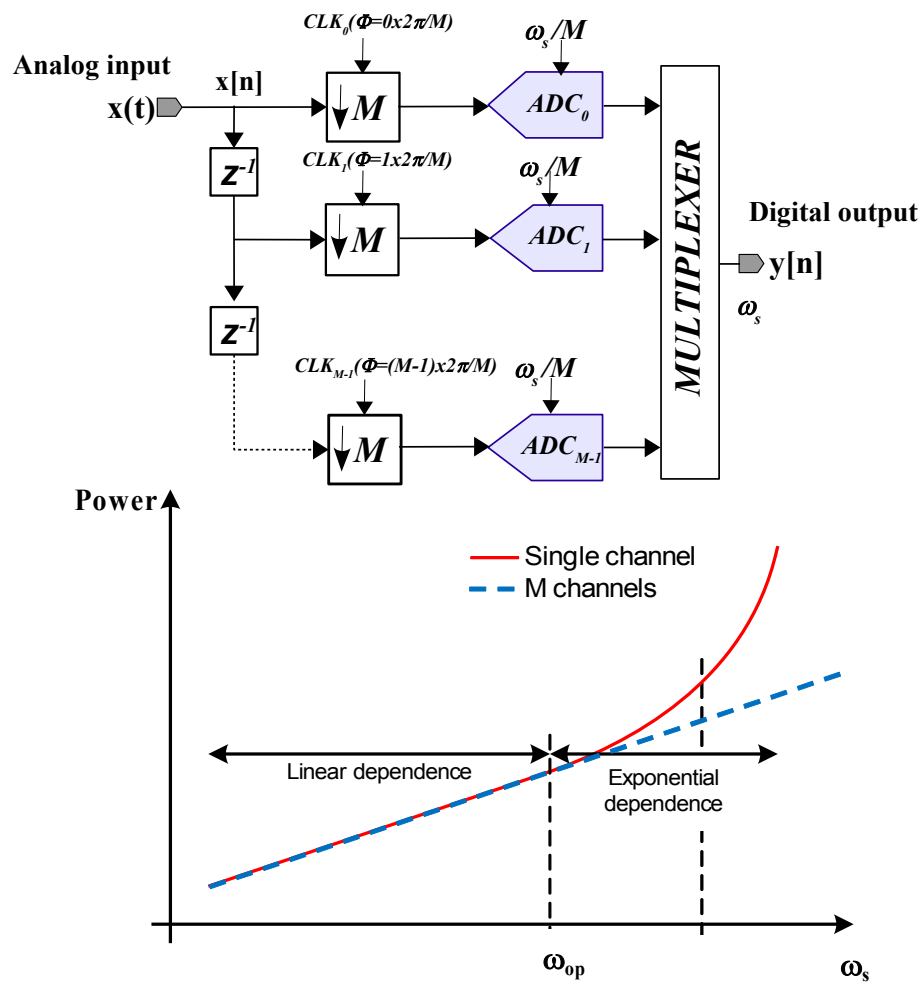


FIGURE 4 – Convertisseur à entrelacement et consommation pour un noeud technologique donné.

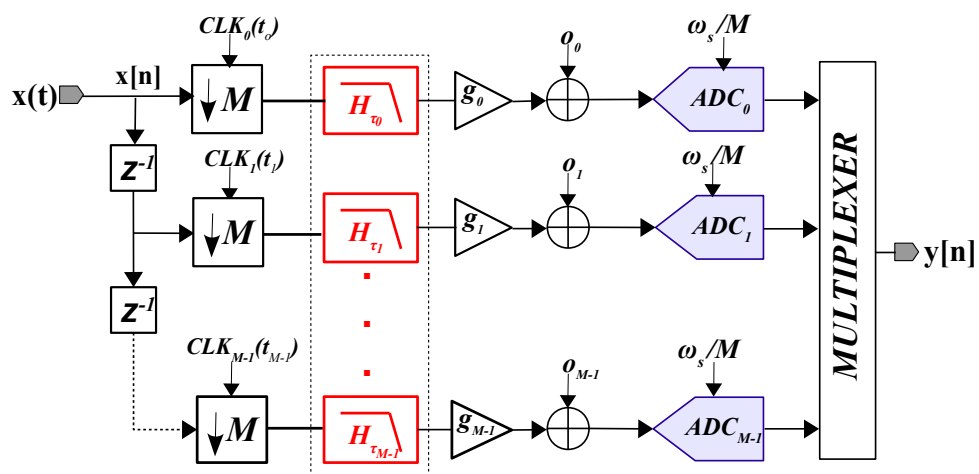


FIGURE 5 – CAN à entrelacement temporel à M canaux.

de raies de distorsion dépend du nombre de voies. Il est aussi montré sur cette figure que l'offset est une erreur qui est indépendante du signal d'entrée et apparaît tous les ω/M ce qui rend sa compensation assez triviale [34,35].

En ce qui concerne les erreurs de gain, skew et l'erreur de bande passante, elles génèrent des raies de distorsion aux fréquences $\pm\omega_{in} + k\frac{\omega_s}{M}$.

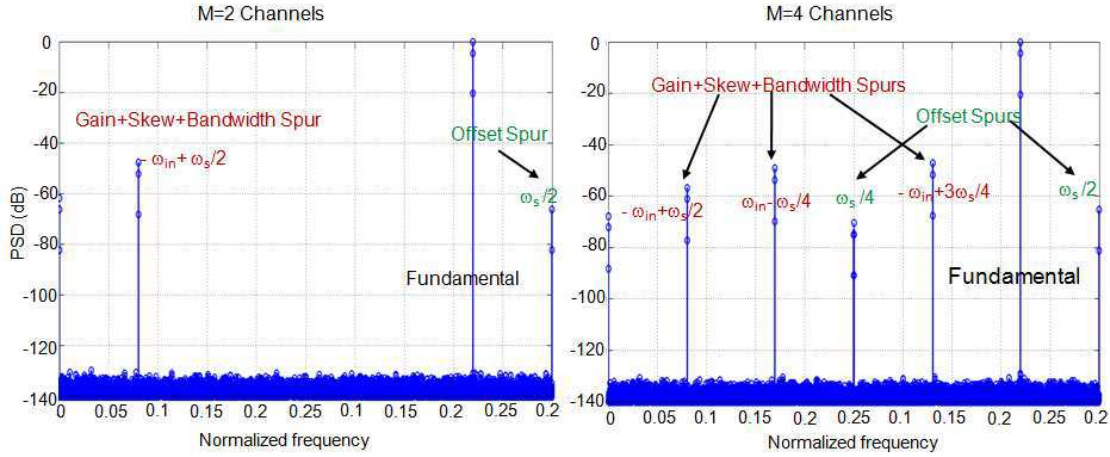


FIGURE 6 – Impact des erreurs à la sortie d'un CAN à entrelacement temporel.

De ce fait, la linéarité du convertisseur, représentée par le SFDR, est dégradée par la raie de distorsion la plus élevée. Il devient alors nécessaire de compenser les erreurs d'appariements afin que le convertisseur atteigne les performances visées. Des abaques ont alors été tracés afin de définir les résolutions nécessaires pour les différentes erreurs afin d'atteindre les performances en SFDR visées.

La figure 2.6 montre que l'erreur de gain ne doit pas dépasser les 0.006% entre deux canaux d'un convertisseur à entrelacement temporel, tandis que le skew doit être inférieur à 25 fs afin d'avoir un SFDR >90 dB pour des fréquences élevée (380 MHz) (Figure. 8).

Dans la littérature, plusieurs travaux visent à compenser ces deux erreurs (gain et skew) et permettent alors d'atteindre de bonnes performances [7,8,9,35,36,37,45,47]. Cependant, l'erreur de bande passante apparaissant avec les applications très larges bandes peut altérer ces corrections des erreurs de gain et de skew. En effet, l'erreur de bande passante est causée par les appariements entre les filtres d'entrée des canaux constituant le convertisseur à entrelacement temporel. Elle présente des contributions en gain et en phase qui dépendent de la fréquence d'entrée ce qui rend la calibration aveugle plus difficile à réaliser. Très peu de travaux traitent cette erreur et à ce jour, à notre connaissance aucune méthode d'extraction de cette erreur n'a été proposée dans la littérature. Nous nous sommes alors intéressés à cette erreur et des solutions analogiques et numériques ont été proposées durant la thèse pour compenser l'erreur de bande passante.

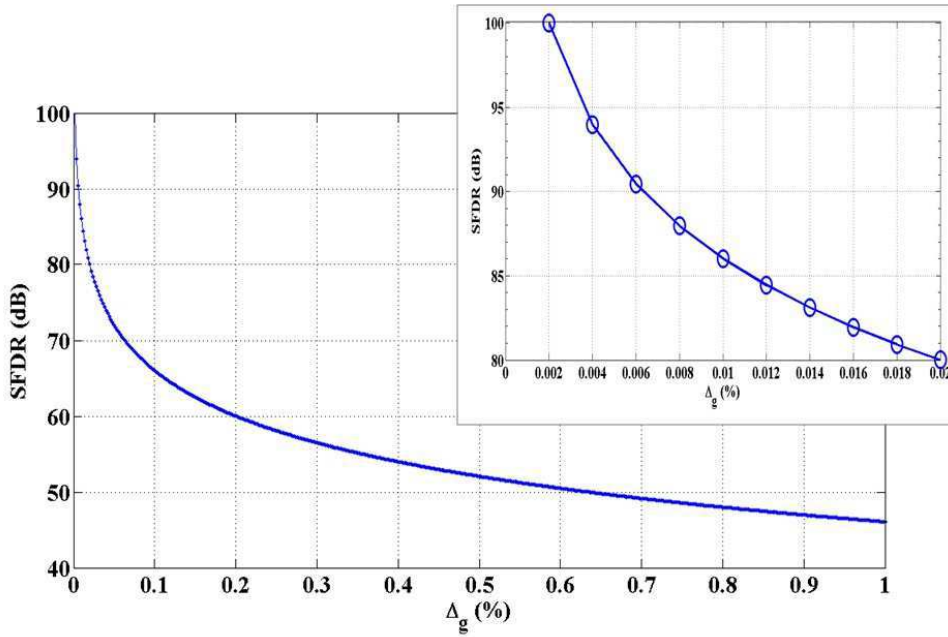


FIGURE 7 – SFDR versus erreur de gain statique.

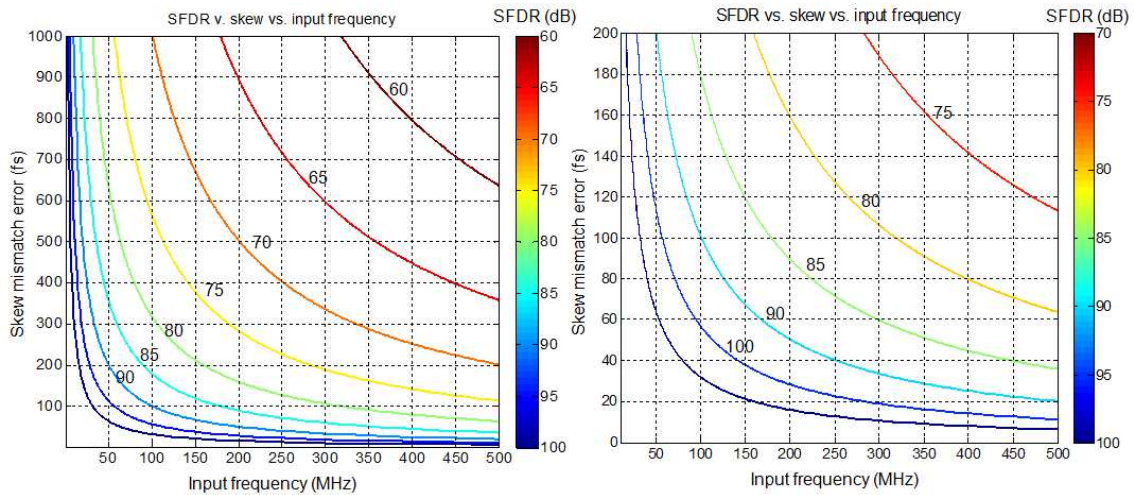


FIGURE 8 – SFDR versus erreur de skew.

III Erreur de bande passante dans un TIADC

III.1 Analyse de l'erreur de bande passante

Pendant la phase d'échantillonnage, chaque réseau d'entrée à capacités commutés se comporte comme de filtre passe. Pour un convertisseur à entrelacement temporel à deux voies, nous représentons pas H_0 et H_1 , les filtres d'entrée ayant des fréquences de coupures différentes (Figure 9).

L'hypothèse de notre étude est de considérer un filtreur passe bas de premier ordre et la

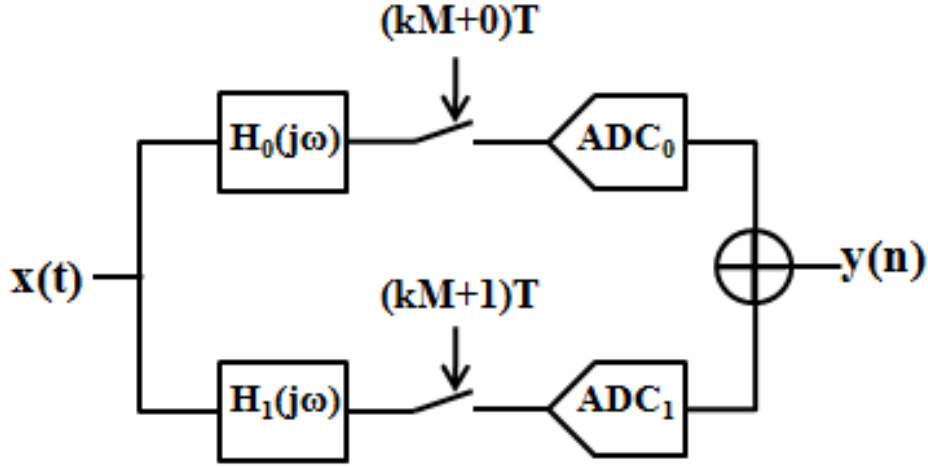


FIGURE 9 – CAN à entrelacement temporel à deux canaux.

sortie de chaque CAN i s'exprime par :

$$y_i[k] = (g(\tau_i))x((kM + i)T + f(\tau_i)). \quad (3)$$

Où τ_i représente la constante de temps et

$$\begin{cases} g(\tau_i) &= \frac{1}{\sqrt{1+(\omega\tau_i)^2}}, \\ f(\tau_i) &= -\arctan(\omega\tau_i). \end{cases} \quad (4)$$

Le gain et la phase dus au filtrage d'entrée.

L'impact de cette erreur sur les performances en SFDR en fonction de la fréquence est présenté sur la Figure. 10 et permet de spécifier la résolution souhaitée pour atteindre les performances souhaitée. En effet, pour l'application station de base visée, l'erreur de bande entre deux canaux ne doit pas dépasser 0.02% pour des fréquences d'entrée jusqu'à 384MHz (ici la fréquence de coupure de moyenne est de 1.1 GHz). Cependant, des simulations Monte Carlo montrent que l'erreur d'appariement entre les filtres d'entrée dans un circuit peut dépasser 2% ce qui dégrade fortement les performances.

III.2 Contributions et Techniques de calibration de l'erreur de bande passante

Une fois la spécification en termes d'erreur de bande établie, deux modes de calibration ont été considérés afin proposer des solutions de calibration de l'erreur de bande passante :

- Considérer les erreurs séparées : cela supposerait alors que les erreurs sont indépendantes et donc peuvent être traitées séparément. Or, l'erreur de bande apparaît dans le gain et la phase du signal de sortie et ces composantes dépendent de la fréquence d'entrée de façon non linéaire. D'autre part, ces contributions en gain et en phase dues à la bande s'ajoutent respectivement au gain statique et au skew. Par conséquent, l'application des techniques de calibration aveugles de gain et de skew proposées dans la littérature deviennent obsolètes et sont gênées par la présence de l'erreur de bande passante. En effet, les simulations ont montré qu'en considérant des erreurs séparées,

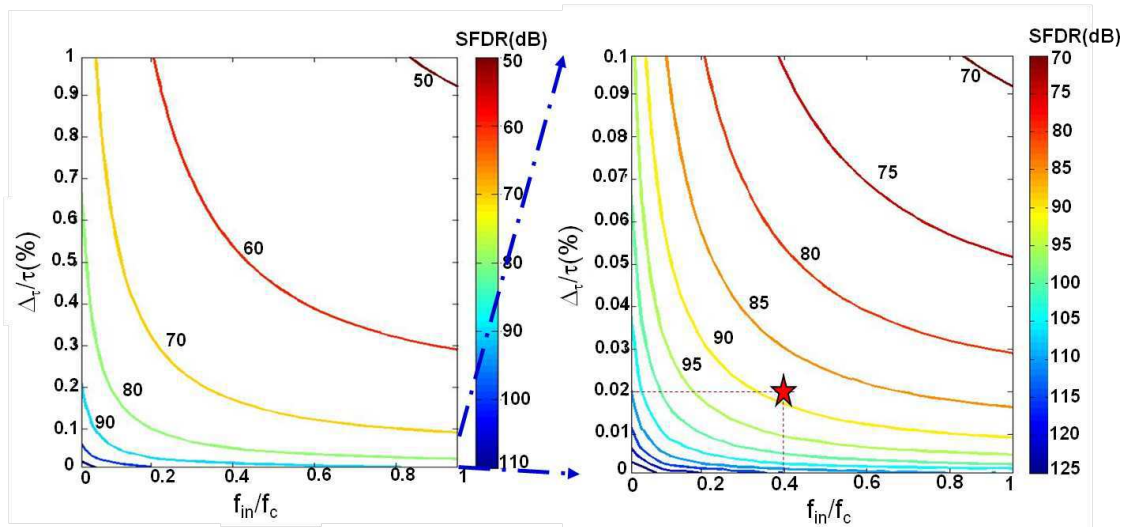


FIGURE 10 – SFDR versus erreur de bande passante.

le SFDR de 85 dB est atteint pour chacune des résolutions de 0.001% d'erreur de gain, 25 fs d'erreur de skew et 0.02% d'erreur de bande passante. Cependant l'application successive des corrections de gain, skew puis la bandes passante en présence de toutes les erreurs et pour les mêmes résolutions nous donne un SFDR de 70 dB. En conséquence, il est important que les techniques appliquées pour les corrections de gain et de skew intègrent l'erreur de bande et pour se faire, une estimation de l'erreur de bande d'une façon dissociée des autres erreurs est impérative afin que les solutions de correction de skew et de gain soient applicables.

- Le deuxième cas prévoit une estimation de l'erreur globale incluant le gain, le skew ainsi que l'erreur de bande passante limitant ainsi le mode de correction à une correction numérique [18]. Pour les résolutions déjà évoquées (0.006% pour le gain, 25 fs pour le skew et 0.02% pour l'erreur de bande passante), la taille de filtres de correction devient très importante ramenant la consommation du bloc de correction à plus de 200 mW, ce qui représente un grand pourcentage comparé à la consommation visée (620 mW). Il est alors préférable de considérer une correction analogique permettant d'avoir une puissance globale dissipée plus faible. Cependant, la méthode d'estimation de l'erreur globale n'est pas adaptée à une correction analogique où les erreurs sont traitées séparément.

Suite aux limitations que présentent les solutions existantes pour la calibration de l'erreur de bande, nous avons proposé des solutions pour améliorer le SFDR ainsi que la consommation visée, tout en garantissant une vitesse d'opération globale de 500 Msp.

1. *Randomisation des réseaux d'échantillonnage*

Cette solution analogique consiste à ajouter un ou plusieurs réseaux d'échantillonnage afin de randomiser l'effet cyclique de l'erreur de bande dans l'architecture à entrelacement temporel. Le modèle proposé est décrit dans la Figure. 11. Ceci permet d'étaler les raies parasites sur toute la bande et donc d'améliorer le SFDR, cependant la puissance de bruit globale reste constante comme le montre la Figure. ???. Cette solution se distingue de l'existant où des canaux entiers sont ajoutés pour effectuer la randomisation et donc consommerait plus de puissance et de surface [TS01]. Cependant, la solution que nous proposons est plus adaptée aux erreurs suffisamment petites afin

que le bruit ajouté ne dégrade pas suffisamment le SNR.

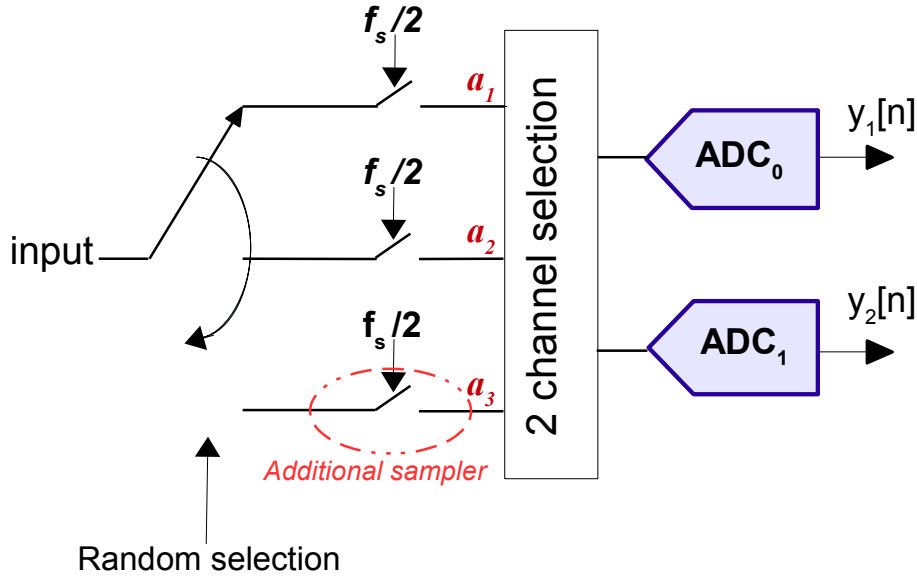


FIGURE 11 – Modèle de randomisation des réseaux d'échantillonnage proposé.

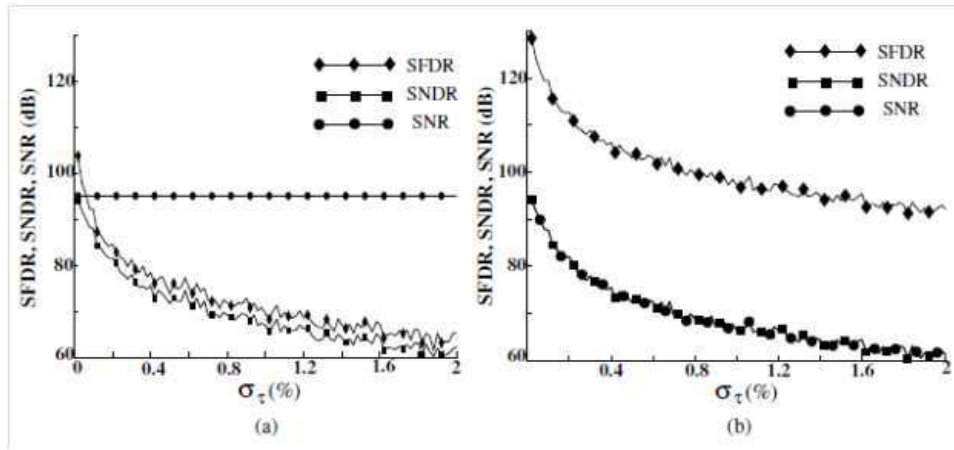


FIGURE 12 – Amélioration du SFDR après randomisation des réseaux d'échantillonnage d'entrée.

2. Compensation de l'erreur de bande passante : estimation et correction

Une seconde démarche consiste à extraire l'erreur de bande d'une façon numérique et la corriger ; soit en analogique. Il n'existe à ce jour aucune solution qui permet d'estimer l'erreur de bande d'une manière aveugle. En effet, seulement deux solutions traitent cette problématique d'estimation. La première, semi aveugle, utilise un signal additionnel pour extraire l'erreur [18]. La seconde, propose une estimation globale ; c'est-à-dire de toutes les erreurs [69]. Cependant, cette dernière ne permet pas une correction analogique des erreurs ; ce qui est préféré à la correction numérique qui présente une puissance consommée plus élevée.

– a. Principe de fonctionnement

La solution d'extraction proposée dans cette thèse de l'erreur de bande passante

est basée sur l'estimation de l'erreur de gain entre les deux voies constituant le convertisseur TIADC. Dans un premier temps, nous avons considéré des toutes les autres erreurs (offset, gain et skew) préalablement compensée et nous verrons par la suite l'impact de ces erreurs sur la solution proposée. L'architecture est décrite dans la Figure. 13 où la différence des deux puissances y_0^2 et y_1^2 représentant la fonction de coût (fonction d'erreur) est nulle lorsque les deux convertisseurs ne présentent pas d'erreur de bande passante. Sous l'hypothèse d'un premier ordre et pour un signal sinusoïdal à l'entrée, cette fonction s'exprime par :

$$\begin{aligned} loss[k] &= y_0^2[k] - y_1^2[k] \\ &= \frac{1}{2} \left\{ \frac{1}{1 + (\omega\tau_0)^2} - \frac{1}{1 + (\omega\tau_1)^2} \right\} \\ &\quad + \frac{1}{2(1 + (\omega\tau_0)^2)} \cos[2\omega T(kM + 0) - 2 \arctan(\omega\tau_0)] \\ &\quad - \frac{1}{2(1 + (\omega\tau_1)^2)} \cos[2\omega T(kM + 1) - 2 \arctan(\omega\tau_1)]. \end{aligned} \quad (5)$$

Qui peut être vue comme un signal DC + une fonction de moyenne nulle. Cette fonction d'erreur, une fois intégrée (sortie de l'intégrateur), va permettre d'extraire le DC qui comporte l'information de l'erreur de bande passante. En effet, à la sortie de l'intégrateur, la pente (notée Slope sur la figure) le représentant s'exprime par :

$$Slope = \frac{1}{2(1 + (\omega\tau_0)^2)} - \frac{1}{2(1 + (\omega\tau_1)^2)} \quad (6)$$

Autour de cette pente, le bruit intégré (représenté par la trace) dépend de l'erreur de la bande passante et de la fréquence d'entrée et définit le seuil de décision pour l'intégrateur. Lorsque la sortie de l'intégrateur dépasse ce seuil, nous prenons alors la décision de corriger l'une des deux voies dans et renvoyons le résultat à l'entrée de l'intégrateur jusqu'à ce que la pente devienne nulle.

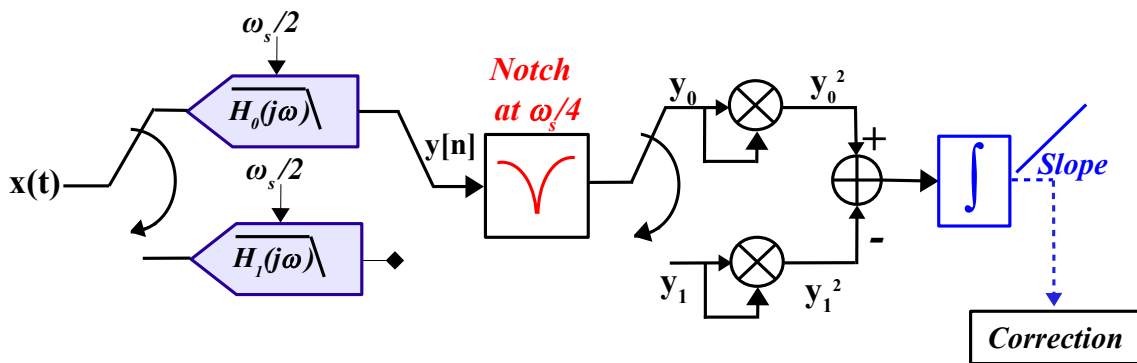


FIGURE 13 – Estimation de l'erreur de bande passante

Il est à noter que le but est de supprimer la raie due à l'entrelacement temporel. En conséquence pour un signal à la fréquence $\omega_s/4$, la raie de distortion apparaît à la même fréquence, ce qui rend son extraction impossible. D'où l'intérêt d'utiliser un filtre autour de cette fréquence afin de s'affranchir de ce problème (voir Figure. 13).

– b. Simulations et résultats

Le modèle implémentée pour l'estimation de l'erreur de bande passante a été évalué

tout d'abord par simulation puis un prototype réel a permis de valider la robustesse de la technique que nous avons proposé.

Le cas d'un signal CDMA a été traité par simulation et montre l'efficacité de cette solution. Les résultats sont représentés par la Figure. 14 où nous voyons une diminution des raies de distorsion et une amélioration du SFDR qui passe de 55 dB à 95 dB après correction analogique idéale de l'erreur extraite. Sur la Figure. 15, l'intégrateur converge après un certain temps vers la vraie valeur de l'erreur de bande (oscillation autour de zero). A noter que la figure 5.3.a est réalisée après le notch afin de voir son effet sur le signal de sortie. Cependant, la sortie utile du convertisseur se trouve avant le notch.

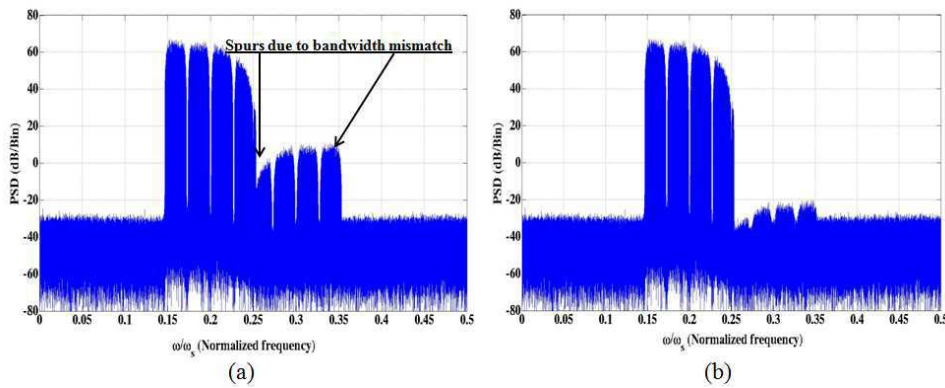


FIGURE 14 – Estimation de l'erreur de bande passante pour un signal CDMA.

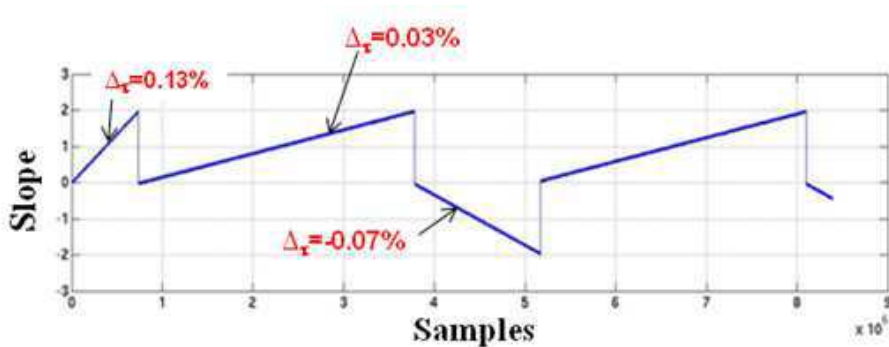


FIGURE 15 – Sortie de l'intégrateur pour le cas d'un signal CDMA.

Par ailleurs, nous avons considéré en début de cette étude que les erreurs de gain et de skew sont préalablement corrigées. En présence de ces dernières, cette solution est limitée par la présence d'une erreur de gain statique puisque elle basée sur l'extraction des puissances des deux convertisseurs, ce qui fausserait alors l'estimation de l'erreur de la bande passante. Cependant, il est à noter que l'erreur de gain statique provient principalement de disparité entre les alimentations des deux convertisseurs et nous pallions ce problème en utilisant alors une référence commune entre les voies du TIADC. De plus, il important de noter que la solution d'estimation proposée s'affranchit du problème de skew qui plus difficile à corriger. Après avoir validé la solution par simulation, nous avons réalisé un prototype qui

à l'aide de circuit réels afin de voir ses limitations en présence d'autres sources d'erreurs.

– *c. Prototype*

La validation de la solution proposée en utilisant des données d'un circuit en développement donne des résultats satisfaisants. Le circuit utilisé est composé de deux convertisseurs, chacun fonctionnant à 250 Msps. La première étape consiste en l'acquisition des échantillons à la sortie du convertisseur TIADC. Un post traitement est ensuite appliqué pour estimer l'erreur de la bande passante en utilisant la solution proposée. La Figure. 16 montre les résultats obtenus. La courbe en bleu représente la valeur extraite à l'aide de la solution proposée (basée sur le gain), quant à la courbe en rouge représente le calcul de l'erreur de la bande passante en se basant sur la mesure de la phase et après avoir supprimé l'erreur de skew qui peut être mesurée en basses fréquences. Comme nous pouvons le voir, la valeur extraite de la bande passante à partir de la solution proposée (courbe en bleu) varie avec la fréquence dans un intervalle [0.02%-0.05%], ce qui peut représenter une limitation pour l'extraction de l'erreur de bande pour des fréquences d'entrée très élevées. Le problème est identique pour la courbe rouge. Après une étude sur

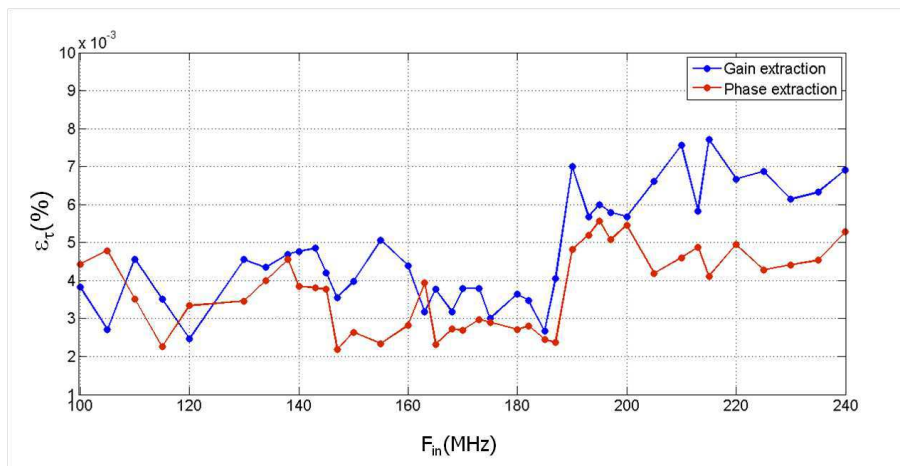


FIGURE 16 – Estimation de l'erreur de bande passante basée sur la solution proposée (courbe en bleu) versus calcul de l'erreur de bande à l'aide la mesure de la phase (courbe en rouge)

le circuit utilisé et des mesures de bande passante, nous avons constaté que ces fluctuations dans la bande passante sont dues aux retours de charges vers le circuit d'entrée, ce qui nécessite alors une adaptation d'impédance pour isoler le circuit TIADC. Ce travail représente une perspective pour les travaux futurs.

IV Conclusion

Afin de réaliser un convertisseur analogique numérique à hautes performances (vitesse et linéarité) pour une application large bande station de base, l'architecture à entrelacement temporel a été choisie. Elle permet d'atteindre des vitesses importantes en parallélisant plusieurs convertisseurs qui fonctionnent à une vitesse réduite tout en ayant une maîtrise sur la consommation globale du convertisseur. Cependant, cette architecture présente des

erreurs d'appariement entre les voies la constituant et qui réagissent différemment aux variations de l'environnement. Les erreurs les plus connues sont l'offset, le gain et le skew et qui sont largement traitées dans la littérature. Cependant, pour les applications larges bandes, l'erreur de la bande passante entre les voies devient visible et son impacte sur les performances en linéarité (SFDR) important. Nous avons alors montré que pour atteindre un SFDR >90 dB à 380MHz d'entrée, l'erreur de bande passante doit être inférieure à 0.02%, ce qui est difficile à réaliser. Très peu de travaux traitent cette erreur et nous nous sommes proposés d'apporter 2 solutions pour pallier ce problème. La première consiste à réduire l'impact de l'erreur de bande passante en randomisant les réseaux d'entrée du TIADC en ajoutant des circuits d'entrée supplémentaires. Ceci permet d'étaler les raies de distorsion sur toute la bande mais la puissance de bruit dans la bande reste constante. De ce fait, cette solution peut être utilisée en complément à d'autres solutions qui réduiraient l'erreur préalablement. Une solution d'estimation de l'erreur de bande passante a également été proposée. Elle est basée sur l'extraction de la contribution de gain. Cette solution a été validée par simulation à l'aide d'un signal large bande CDMA et un prototype de mesure a été mis en place et a permis de vérifier la robustesse de cette solution. Cependant, des réflexions dans la bande passante rendent l'extraction moins précise et de ce fait, il est important d'avoir des circuits bien adaptés avant d'utiliser des techniques d'extraction de la bande passante.

V Perspectives

La perspective principale à ce projet est de trouver une solution de séparation de toutes les erreurs afin d'avoir une estimation aveugle de celles-ci et permet de corriger les erreurs séparément dans le domaine analogique. Ce dernier constitue le travail le plus important. En effet, la correction analogique permet de consommer moins que la correction digitale et présente une meilleure résolution. De plus les variations de l'erreur de bande passante extraite représente un verrou technologique qu'il va falloir lever pour permettre une estimation précise. Enfin, la Figure. 17 donne une vision à moyen terme des travaux de recherche pour atteindre de meilleures performances avec des architectures à entrelacement temporel.

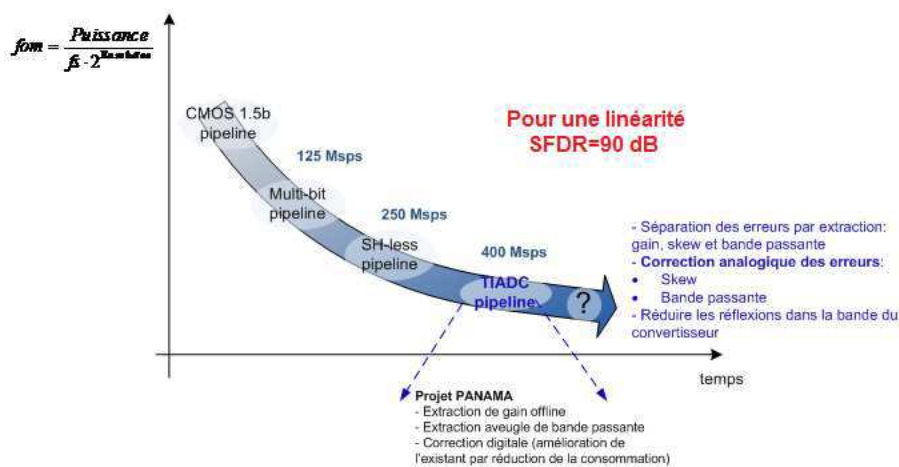


FIGURE 17 – perspectives pour les travaux futurs

Abstract

The rapid evolution of wireless communications pushes the analog-to-digital converter close to the antenna in order to address multistandard transceivers for Software Define Radio (SDR). In that case, wide band base stations require high speed, high resolution analog-to-digital converter (ADC). Time-interleaved ADC architecture (TI-ADC) is an efficient way to increase the sampling frequency. It consists of the parallelization of several channels; each one running at the overall data rate (f_s) divided by the number of channels M . However, due to IC process and temperature variations, mismatches between the channels generate errors which impact the linearity of the converter and hence degrade the SFDR. Several solutions deal with the problems of offset, gain and timing skew errors, when only few works have considered the bandwidth mismatch problem. This error comes from the fact that during the sampling period, the sampling networks behave differently as low pass filters. The difference between the cutoff frequencies of the channels input filters cause bandwidth mismatch error. This error intervenes as gain and phase modulation and these two components depend on the input frequency and are nonlinear dependent of the bandwidth mismatch error. For these two reasons, background calibration is necessary.

In this work, we have focused on the bandwidth mismatch error and proposed some solutions to deal with it. Two approaches have been proposed :

The first one consists of reducing the impact of the bandwidth mismatch error by randomizing the input sampling networks. In fact, mismatch error in a time-interleaved architecture is caused by a cyclic pattern and the easiest way to reduce this cyclic characteristic consists of randomizing the channels and spreading in that way the spurs over the bandwidth. A new implementation has been proposed using additional sample networks to achieve the randomization instead of entire channels. Compared to existing methods, the proposed implementation allows reducing power consumption and die area. Moreover, it is possible to compensate all errors due to switches mismatch such as timing skew error.

The second approach consists of compensating the bandwidth mismatch error using estimation and correction. We have focused on digital error estimation since it is very important to accurately extract the error. Bandwidth mismatch error is present in both ADC output gain and phase error components. A comparison between the two components has shown that the gain and phase errors due to bandwidth mismatch are comparable. consequently, the error can be estimation using either gain or phase extraction. Based on this analysis, a background estimation of the bandwidth mismatch using gain extraction has been proposed. It has the advantage to be free dependent from the clock skew mismatch but is impacted by the static gain error. This latter can be overcome either by design or using low frequencies offline compensation techniques. Nevertheless, the estimation of this static gain error can be done using the proposed solution. Moreover, thanks to this individual error estimation technique, either analog or digital correction can be applied. On the contrary, other existing solutions based on polynomial approximation address a global error including gain and skew which limits to calibration to digital correction. The proposed solution has been first validated by simulation, then robustness has been evaluated using a wide band WCDMA signal. This realistic use case has probabilistic properties avoiding the presence of two symmetrical signals at the same time. This latter configuration generates undesired spurs at the same frequencies which are not managed by the integrator for deterministic signals. Finally, the impact of measured intrinsic errors of the ADCs has been considered to validate the proposed estimation technique.

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Symbols and Abbreviations

Abbreviations

- **ADC** : Analog to Digital Converter.
 - **BiCMOS** : Bipolar Complementary metal oxide semiconductor.
 - **CMOS** : Complementary metal oxide semiconductor.
 - **CT** : Continuous Time.
 - **DAC** : Digital to Analog Converter.
 - **dBFS** : dB Full Scale.
 - **dBc** : Decibel relative to carrier.
 - **DNL** : Differential nonlinearity.
 - **DR** : Dynamic Range.
 - **DT** : Discrete Time.
 - **ENOB** : Effective number of bits .
 - **FFT** : Fast Fourier transform.
 - **FoM** : Figure of Merit.
 - **FPGA** : Field programmable gate array.
 - **HFB** : Hybrid Filter Bank.
 - **HD2** : Second Harmonic Distortion.
 - **HD3** : Third Harmonic Distortion.
 - **IF** : Intermediate frequency.
 - **INL** : Integral nonlinearity
 - **LSB** : Least Significant Bit.
 - **LNA** : Low Noise Amplifier.
 - **MDAC** : Multiplying Digital to Analog Converter.
 - **OSR** : Oversampling Ratio.
 - **OTA** : Operational Transconductance Amplifier.
 - **PA** : Power Amplifier.
 - **SAR** : Successive Approximation Register.
 - **SDR** : Software Defined Radio.
 - **SFDR** : Spurious Free Dynamic range.
 - **SHA** : Sample and Hold.
 - **SNDR** : Signal to Noise and Distortion Ratio.
 - **SNR** : Signal To Noise Ratio.
 - **THD** : Total Harmonic Distortion.
 - **WCDMA** : Wideband Code Division Multiple Access.
 - **WSS** : Wide Sense Stationary.
-

- **UMTS** : Universal Mobile Telecommunication System.
- **SQNR** : Signal to Quantization Noise Ratio.
- $\Sigma\Delta$: Sigma Delta

Symbols

- $\mathbf{x}(\cdot)$: Analog signal.
 - $\mathbf{x}_s(\cdot)$: Sampled signal.
 - $\mathbf{x}[\cdot]$: Digital signal.
 - $\mathbf{X}(\omega)$: Signal fourier transform.
 - K_{bol} : Boltzmann constant.
 - Δ_o : offset error.
 - Δ_g : gain error.
 - Δ_t : time skew error.
 - Δ_τ : time constant error.
 - $h_\tau(t)$: the impulse response.
 - $H_{\tau_i}(\omega)$: frequency response.
-

Résumé en français

La rapide évolution des standards pour la communication sans fil a fortement contribué à l'apparition de nouvelles architectures émetteurs-récepteurs reconfigurables, permettant d'adresser plusieurs standards en même temps. Ceci est d'autant plus attractif pour les applications stations de base où le coût de re-déploiement est très élevé. Ainsi grâce à la radio logicielle (SDR : Software Define Radio), la sélection des canaux de communication est réalisée par des unités logicielles, ce qui permet une très grande flexibilité des unités matérielles.

L'évolution grandissante de ces architectures impose alors de plus en plus de contraintes aux convertisseurs analogique-numérique (CAN) qui réalisent l'interface entre les mondes matériel et logiciel. Ils doivent être très rapides et très précis, ce qui est non sans conséquence sur la consommation, qui pour la plupart des applications représente la limite critique pour la réalisation d'un CAN.

Pour ce faire, les architectures parallèles sont un bon compromis permettant d'augmenter la vitesse d'échantillonnage des convertisseurs tout en ayant un contrôle sur la consommation, ce qui relaxe les contraintes sur le CAN à une voie. Le CAN à entrelacement temporel consiste en la parallélisation de plusieurs canaux, chacun fonctionnant à la vitesse globale divisée par le nombre de canaux. Le signal d'entrée est échantillonné puis converti par chacune des voie successivement pour enfin, être reconstitué dans le domaine digital. Cependant, les canaux constituant cette architecture ne réagissant pas de la même manière à des variations extérieures, les erreurs intrinsèques à chaque canal évoluent différemment, ce qui génère des erreurs d'appariement entre les canaux et dégrade les performances du convertisseur parallèle.

Les erreurs les plus connues sont : l'offset, le gain et l'erreur de phase des horloges d'échantillonnage. Celles-ci sont largement traitées dans la littérature et des techniques d'estimation et de correction ont été proposées tant analogiques que numériques. Toutefois les applications larges bandes comme les stations de base voient apparaître des erreurs de bande causées par le mésappariement entre les réseaux d'échantillonnage des canaux constituant le convertisseur à entrelacement temporel. Une étude de l'impact de cette erreur sur les performances du convertisseur a montré la nécessité de compenser cette erreur. Les caractéristiques de cette erreur de bandes montrent la difficulté à la compenser en temps réel pour les raisons suivantes : 1. d'une part, cette erreur dépend de la fréquence d'entrée du signal. Ce qui nécessite une compensation sur toute la bande à l'aide de filtres adaptatifs. 2. d'autre part, l'erreur de bande apparait dans le gain et la phase du signal de sortie. Ceci rend son extraction plus difficile notamment en présence des erreurs de gain statique et de phase linéaire.

Très peu de travaux traitent la calibration de cette erreur d'appariement de bandes pour les raisons susmentionnées. Ceci justifie le choix de cette problématique et place ce projet de thèse au coeur de l'innovation. La démarche suivie dans cette thèse est passée par différentes étapes :

1. Tout d'abord, un état de l'art des convertisseurs en général et des convertisseurs à entrelacement temporel en particulier a été réalisé. Pour cela, nous avons recensé les architectures existantes dans la littérature depuis 1998 et avons comparé leurs performances en vitesse, résolution et linéarité.
 2. Ensuite, Une étude approfondie sur les erreurs causées par un mésappariement entre
-

les voies d'un convertisseur à entrelacement temporel a permis de faire apparaître la nécessité de corriger les erreurs de bandes entre les voies en vue des applications large bandes visées, afin d'atteindre des performances en SFDR de 90 dB à 375 MHz de fréquence d'entrée.

3. Après avoir étudié les différentes techniques de compensation existantes, nous avons proposé deux solutions innovantes : la première, analogique consiste à randomiser les réseaux d'échantillonnage d'entrée qui sont responsables de cette erreur de bande. Ceci permet d'étaler les raies parasites sur toute la bande et ainsi améliorer le SFDR sans dégrader le SNDR. Une seconde démarche consiste à extraire l'erreur de bande d'une façon numérique et la corriger ; soit en analogique ou en numérique. Il n'existe à ce jour et à notre connaissance aucune solution qui permet d'estimer l'erreur de bande d'une manière aveugle. Nous avons alors proposé une technique d'estimation basée sur l'extraction de l'erreur de gain entre les deux voies. La validation de cette solution a été réalisée d'une part, par simulation pour un signal large bande CDMA. D'autre part et afin de vérifier la robustesse d'estimation de cette erreur de bande, des données provenant d'un circuit réel où toutes les erreurs intrinsèques au convertisseur sont présentes ont été utilisées.
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Introduction

Motivation

The rapid evolution of wireless communication systems is motivated by the explosion of market requirements in terms of devices and applications. It encourages the appearance of new standards offering multi-access services and the ability to increase the data rate. Nevertheless, the cohabitation of existing standards is needed to address all devices and optimizing the network according to the demand, this key role is vested in multi-standard receivers. Software defined radio (SDR) is a radio interface technology that consists of software reconfigurable hardware platform and software modules that can make flexible change in the hardware platform for a specific radio system application. Based on this principle, the objective of scalable RF systems is to push the analog-to-digital converter (ADC) close to the antenna in order to facilitate the digital processing. This key component is responsible of converting the analog received signal to digital signal without degrading the desired signal. Moreover, in order to realize SDR receivers, the channel selection must be done in the digital part which requires the ADC to treat wideband signals. According to this, the ADC is the most challenging component of the chain in terms of dynamic range and speed. The speed is related to the targeted bandwidth where the dynamic range concerns the accuracy of the ADC which sets the resolution of the converter.

Two existing categories of ADC architectures address different applications according to their requirements. The first one covers Nyquist ADCs which are better suited for wide band applications ; they include flash, SAR and pipeline architectures. The second family is based on oversampling and achieves higher resolutions ; it mainly consists of Sigma Delta modulators. However, wide band base station applications require high speed and high resolution ADCs. To break this bottleneck, time-interleaved converter (TI-ADC) which is an efficient way to increase the speed while maintaining a good accuracy is used. It consists of the parallelization of several channels ; each one running at the overall data rate (fs) divided by the number of channels M. The benefit of this approach is to increase the conversion bandwidth while maintaining the same operation frequency of the analog blocks. Moreover, it is important to notice that the power consumption of the TI-ADC is simply equals to M-times the power consumption of single ADC where it increases exponentially in function of the sampling frequency. For all these reasons, TI-ADC is the best suited architecture to the aimed requirements.

However, in the real world and due to process and environment variations, each channel behaves differently generating mismatch errors at the digital output. These mismatches create undesired spectral components and can significantly degrade the linearity (SFDR) and the resolution of the system. The spurs are basically caused by periodic mismatch factors such as offset, gain, timing and bandwidth and increase with the number of ADCs.

Nevertheless, offset and gain calibration are widely treated in the literature [1, 2, 3, 4] while clock skew mismatch error remains difficult to eliminate [5, 6, 7, 8, 9]. The impact of this error increases with the input frequency and the use of background calibrations is necessary to track the environment variations. In fact, offline calibration requires the ADC to be stopped and this is not appropriate for base station applications. Several techniques were proposed to calibrate this error online using either analog [10, 11, 12] or digital correction [13, 14, 15, 16] and offers promising achievements. Regarding the bandwidth mismatch, it consists of the difference between the input sampling circuits which behave like low pass filters [17, 18, 19]. The impact of this error becomes visible with the apparition of wideband applications where the input bandwidth is very large and leads for IF signals to increase this error impact which degrades drastically the linearity of the converter. For these reasons, background calibration is definitively needed and highly challenging.

The goal of the thesis is to develop and implement background calibration techniques for bandwidth mismatch error in a high speed TI-ADC (up to 500 Msps) in order to achieve a 90 dB of SFDR for high input frequencies (up to 385MHz) and up to 94 dB at low frequencies. Very few techniques address this problem because of two main reasons : first, this error depends on the input frequency. Second, the bandwidth mismatch error generates gain and phase components which are non-linear dependent of the bandwidth error. Consequently, the calibration is difficult and requires background solutions.

Organization

After introducing the motivation of the work, the thesis is organized as follows :

Chapter 1 explains how an ADC converts the signal from analog to digital part and highlights the different performance specifications in terms of noise and linearity. In order to choose the the best suited architecture for our requirements, a comparison of the existing architectures and their TI versions during the last decade has been presented. In the last subsection, the role of the ADC in the RF transceiver is explained and the different constraints responsible on the degradation of the ADC performances are highlighted. Finally, the required specifications to achieve a very high speed high resolution ADC for a base station application are provided.

Chapter 2 details the benefit of using time-interleaved architectures for wide band ADCs. The limitations of TI-ADCs are detailed in this chapter, including all errors : offset, gain, clock skew and bandwidth mismatch errors. Then, the impact of each error in the TI-ADC output is presented separately. this is done both in time and frequency domains. The latter analysis leads to quantify the degradation of the SFDR in function of the input frequency for each error. The last subsection is dedicated to quantify the degradation of the SFDR in presence of gain, skew and bandwidth mismatch and compare this combined error performance to the previous separate error analysis.

Chapter 3 gives an overview of existing calibration techniques for bandwidth mismatch error. First, a new implementation for randomization is proposed and compared to the existing solutions. Calibration techniques including estimation and correction are treated in this chapter. Moreover, we propose an easier implementation for the digital correction filters based on polynomial approximation method with some promising results. Regar-

ding the estimation, in the best of our knowledge only two methods propose bandwidth extraction ; the first one is semiblind while the second includes all other existing errors. the two techniques are detailed and their main drawbacks are presented. Finally, the last subsection highlights the necessity of choosing a good loss function beforehand in order to insure the desired error estimation.

Chapter 4 exposes the proposed solution for bandwidth mismatch error estimation in digital part. In order to validate the proposed solution, simulations for a sine wave input signal are presented. Then, the wide band input is treated using a WCDMA pattern. Moreover, the robustness of the proposed method is evaluated using a board for measurements. This one consists of two ADCs including all intrinsic errors.

Finally, in the last chapter, we conclude with some perspectives for the project.

Contributions

The main contributions of this work are :

– **Conferences :**

[*Conf1*] **F. Ghanem**, P. Desgreys, P. Loumeau, A. Biallais, P. Gandy ; A Background Extraction Technique for Bandwidth Mismatch Error in a Two-channel Time-Interleaved ADC ; IEEE International, NewCAS 2012.

[*Conf2*] **F. Ghanem**, C. Jabbour, P. Desgreys, P. Loumeau, C. Erdmann, P. Gandy ; A New Implementation of a Random Sampling Technique for Bandwidth Mismatch TI ADCs ; Designed Circuits for Integrated Systems, DCIS 2011 .

[*Conf3*] P. Degreys, **F. Ghanem**, Pham. G, H. Fakhoury, P.Loumeau ; Beyond 3G Wideband and High linearity ADCs ; IEEE International, Faible Tension Faible Consommation (FTFC) 2011 (Faible Tension Faible Consommation).

– **Invited presentations and posters :**

[*Presentation1*] **F. Ghanem** ; Mismatch Error Estimation in a Time Interleaved Analog-to-Digital converter Presentation GDR SoC SiP ; "Journée AMS et RF du 24 Mai 2012".

[*Poster1*] **F. Ghanem** ; Bandwidth Mismatch Error in a Two-channel Time-Interleaved ADC ; Poster NXP Semiconductors NCTC'Day 2012.

[*Poster2*] **F. Ghanem** ; Etude comparative des architectures Convertisseurs Analogique-numeriques hautes performances ; Poster JNRDM 2010.

– **Journals :**

F. Ghanem, P. Desgreys, P. Loumeau, A. Biallais, P. Gandy ; A Background Extraction Technique for Bandwidth Mismatch Error in a Two-channel Time-Interleaved ADC ; IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II ; journal paper in preparation

Chapitre 1

High Speed High Resolution Analog-to-Digital Converters

1.1 Introduction

The recent evolution in wireless communications encourages the development of the analog electronics. Software Defined Radio (SDR) aims to reduce the analog signal processing and moves the boundary between analog and digital parts closer to the antenna. The analog-to-digital converter (ADC), is the interface between the analog and digital worlds. It is a key element in almost all applications, so it is important to review the technology trend each few years. The communication industry has consistently pushed the boundaries of ADCs, and current evolution in ultra-wideband (UWB) and SDR continue the trend. Understanding the trend in ADC performance is the key for designers to predict the evolution of future communication systems especially SDR technology. Thereby, a set of ADCs is presented in this chapter to select the interesting architectures that can be suitable for the aimed applications.

This chapter is organized as follow : Section 1.2 explains how an ADC operates to convert the input signal. Because of the nonidealities of the circuitry, sampling and quantization limit the performances of the converter. The characterization of the device in terms of specifications is highlighted in Section 1.3. In Section 1.4, an overview of the mostly used analog-to-digital converters is presented : Flash, Pipeline, SAR and Sigma Delta. Then a general survey of the state-of-the-art is given for each architecture with a quantitative comparison in term of figure of merit to highlight the trade-off made between speed, resolution and power dissipation, which is exposed in Section 1.2. At the end of this section, a survey of the recent competitive ADCs highlights the sensitive areas of respective architectures that we need to improve in order to go higher in speed and performance. We focus particularly on parallel architecture which is the easiest way to improve the speed by parallelizing the converters. Finally, the conclusion presents the key elements of the chosen architecture to work on in order to achieve the aimed specification.

1.2 Analog-to-Digital Converters

1.2.1 Ideal Converters

An analog-to-digital converter transforms an analog voltage $x(t)$ to a digital signal $y[nT_s]$. It first samples the time axis with a certain period of time to give a series of sam-

pled values. These ones are then quantized with a certain resolution to provide a digitized code (Fig. 22). The successive processing of an ideal ADC is illustrated in Fig. 1.2 and each block function is explained below.

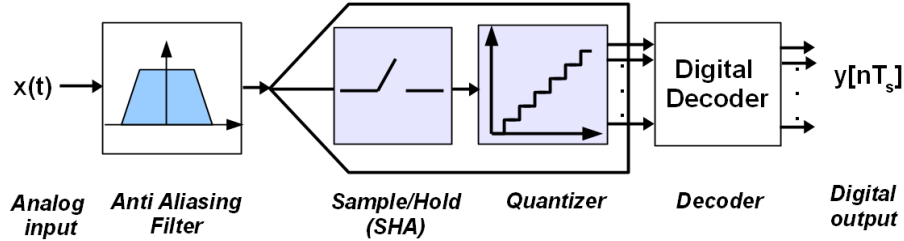


FIGURE 1.1 – Analog-to-digital converter blocks : anti-aliasing filter, sampling block, quantizer and decoder blocks.

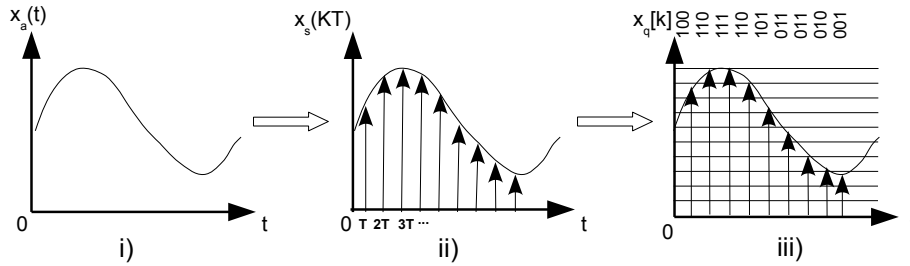


FIGURE 1.2 – (i) Analog signal, (ii) Sampled signal, (iii) Quantized signal

1.2.1.1 Sampler

In practice, Fig. 1.2 (b) is achieved by a sampling clock. At each front edge, a sample is get during a period of $T/2$ then the sample and hold (SHA) block holds the value during the following $T/2$ period. In switched capacitors circuits, the sampling is performed when the input switches S are "on", leading to charge the C_s capacitors ; see Fig. 1.3. The charge transfer starts when the Hold switches are "on" and the input switches are disconnected. Thanks to the amplifier, the charges are transferred from C_s capacitor into C_f capacitors during the period of $T/2$.

Analytically, the continuous time signal is multiplied by the train of pulses delayed by T leading to a sampled signal as follow

$$x_s(t) = \sum_{k=-\infty}^{+\infty} x(t)\delta(t - kT). \quad (1.1)$$

As a consequence, the output spectrum is periodic with a period of $F_s = 1/T$ as shown in Fig. 1.4, in which :

$$X_s(\omega) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} X(\omega - \frac{k}{T}). \quad (1.2)$$

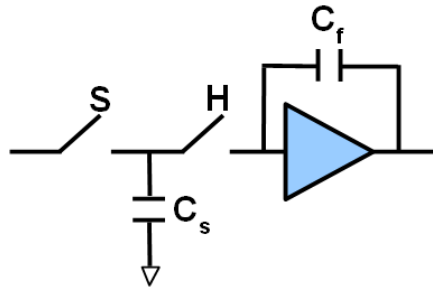


FIGURE 1.3 – Sample and Hold circuit

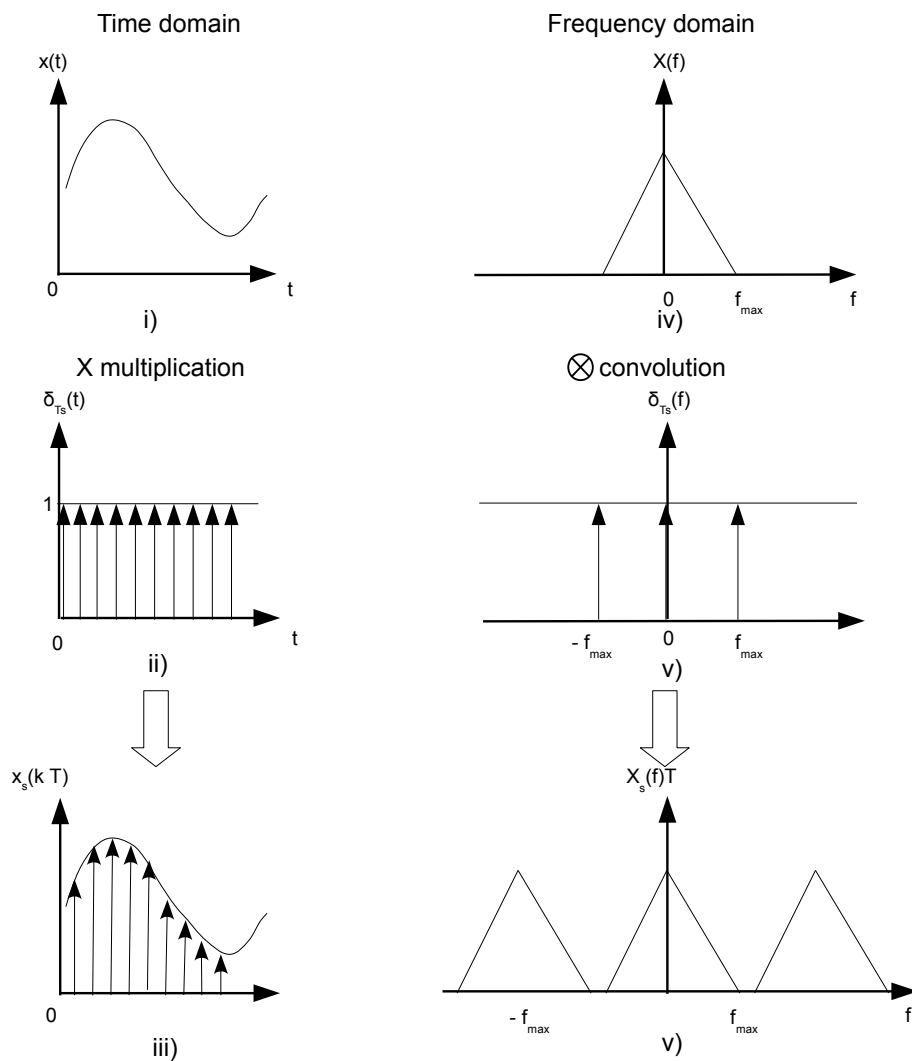


FIGURE 1.4 – sampling signal in time and frequency domains

If we denote by B , the bandwidth of the analog signal, aliasing occurs if Shannon criterion is not respected and consequently, the input signal cannot be reconstructed. This is

illustrated in Fig. 1.5 where $B > f_s/2$. To overcome this problem, an analog anti-aliasing filter is placed before the sampler block.

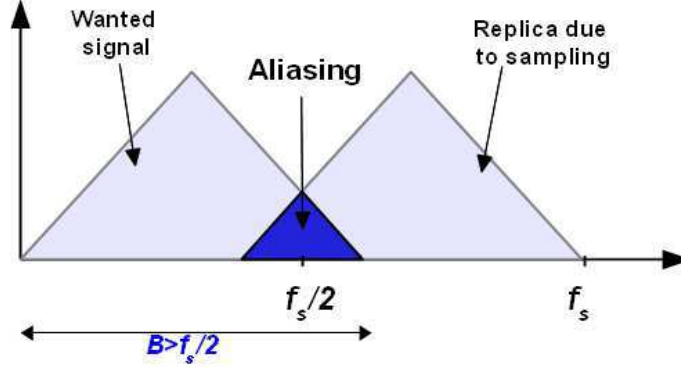


FIGURE 1.5 – Aliasing from the adjacent spectral band

1.2.1.2 Quantization

In order to treat the sampled signal in the digital domain, discretization of the amplitude values is required, this is called quantization. To do so, each analog sample value is approximated by a digital number and the number of bits that represents the digital value corresponds to the resolution of the ADC. Therefore, a N-bit ADC has a resolution of 2^N ; meaning that the analog value can be approximated using one value out of the 2^N possible quantized values. Fig. 1.6 illustrates the characteristic Input/Output of the ADC where V_{FS} , (the full scale voltage) represents the dynamic range of the input signal and the resolution is usually specified with respect to this value. Thereby, the quantization step is equal to $\frac{V_{FS}}{2^N-1}$ representing the least significant bit (LSB).

The digital approximation of the analog signal generates a quantization error. This latter represents the difference between the ideal In/Out characteristic and the quantized In/Out characteristic (Fig. 1.6). The quantization error cannot be avoided and appears as a white noise floor in the output spectrum. The effect of this error on the input signal can be evaluated by calculating a signal-to-noise ratio (SNR). By considering a sine wave input with an amplitude of A, the power of the signal P_s is then equal to $A^2/2$. Regarding the quantization noise, the power which represents the variance of the random quantization error comes out as

$$P_{\text{noise}} = \int_{-LSB/2}^{LSB/2} \frac{1}{LSB} e^2 de = \frac{LSB^2}{12} \quad (1.3)$$

where $LSB = \frac{V_{FS}}{2^N-1}$. This Gaussian noise has a certain density over a wanted bandwidth B. Hence, the power of noise is done by :

$$P_{\text{noise}} = \frac{1}{f_s} \int_{-\frac{B}{2}}^{\frac{B}{2}} \frac{LSB^2}{12} df \quad (1.4)$$

$$P_{\text{noise}} = \frac{B LSB^2}{f_s 12} \quad (1.5)$$

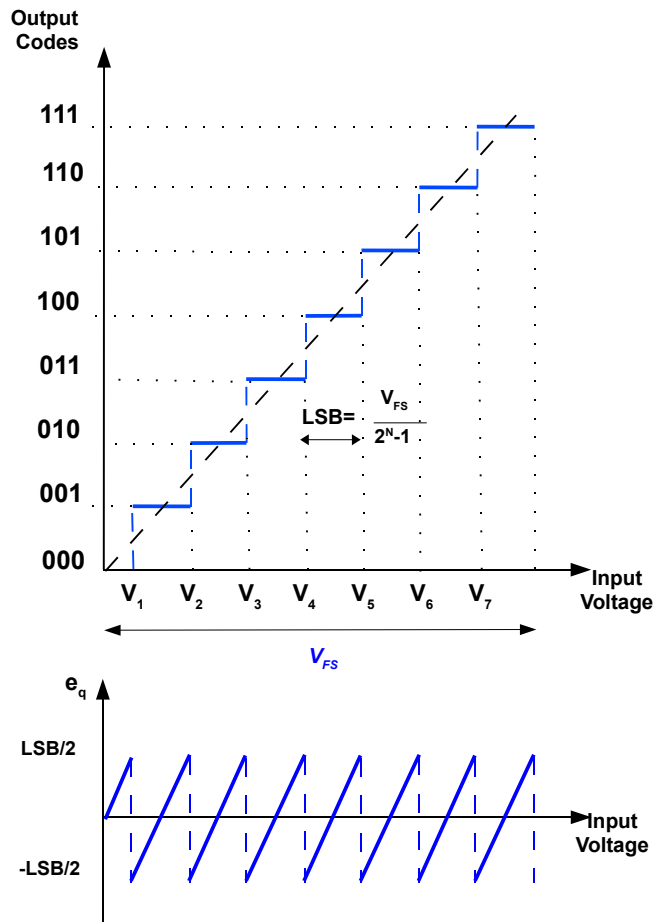


FIGURE 1.6 – (a) Quantizer In/Out characteristic and (b) quantization error

where the ratio $\frac{f_s}{B}$ is called the oversampling ratio OSR. Based on this, the signal to noise ratio is given by :

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}} \quad (1.6)$$

After some manipulations, the expression of the quantization SNR, commonly denoted by SQNR, can be expressed as

$$\text{SQNR}(\text{dB}) = 6.02N + 1.76 + 10\text{Log}(\text{OSR}) \quad (1.7)$$

where N is the number of bits. In this expression, one can note that the amplitude of the signal A is equal to $V_{FS}/2$. Moreover, for Nyquist converters, the OSR is equal to 1 which means that for each additional bit, the SNR is improved by 6 dB.

1.3 ADC versus Specifications

Besides quantization noise which cannot be avoided, the selection of the suitable ADC for the aimed application depends on the system performance. ADC specifications consist of : DC accuracy and dynamic or AC performance. The first one, also called static specification since it does not depend on the input signal frequency and the measured voltage, is related to some physical measurements. Nevertheless, for some applications, we are more interested on the performance of the ADC when the input signal changes because in most cases, the AC performance is not the same like DC one.

1.3.1 Static specifications

Static specifications include offset error, full-scale error, differential nonlinearity (DNL) and integral nonlinearity (INL), which determine the DC accuracy of the converter.

1.3.2 Offset and gain error

Offset error is a derivation of the bottom end point of the ADC characteristic from the ideal location. This error is independent of the input signal and saves the number of available codes. This is shown in Fig. 1.7 (a). Gain error is defined as a full-scale error when offset error is removed. It consists of an angular shift of the entire characteristic (Fig. 1.7 (b)). Positive shift from the ideal transfer function causes a lose in dynamic range and hence saturation in the output.

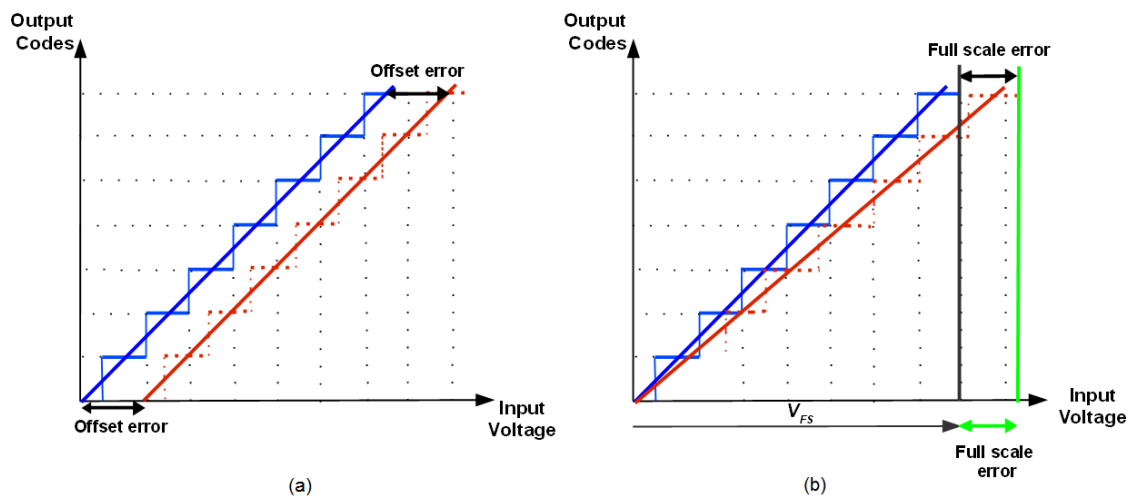


FIGURE 1.7 – (a) Offset Error, (b) Gain Error

1.3.3 Nonlinearity

Ideally, each code width (LSB) which is the difference between two successive codes should be the same. The differential nonlinearity (DNL) measures the deviation of the difference between two successive input voltage (in codes) from the LSB value as shown in Fig. 1.8. The DNL which is specified after static gain error has been removed is expressed

as follow

$$DNL = \frac{V_{n+1} - V_n}{LSB} - 1. \quad (1.8)$$

so that a DNL error needs to be less than 1 LSB to guarantee no missing codes.

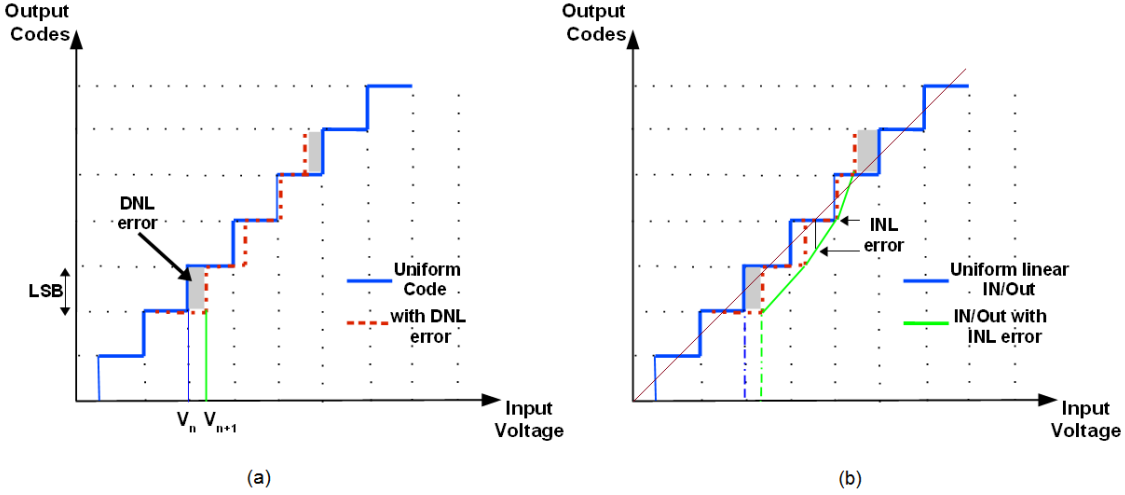


FIGURE 1.8 – (a) Differential nonlinearity (DNL) (b) Integral nonlinearity (INL).

Integral nonlinearity (INL) is defined as the integral of the DNL. It consists of the deviation of the transfer function from the ideal characteristic. It can be expressed as :

$$INL = \frac{V_{n+1} - V_0}{LSB} - \text{IdealCharacteristic}. \quad (1.9)$$

This is shown in Fig. 1.8, where it can be noticed that the deviation can be different from a code to another. Only the maximum value of these deviations is taken into account and needs to be less than 1LSB to guarantee a good DC linearity.

1.3.4 Dynamic specifications

Most of the applications consider AC performance of the converter especially for high input frequencies. Dynamic performances are obtained in the frequency domain where it is easier to evaluate the noise power and the distortion in the band. They include :

1. Signal to noise Ratio (SNR) :

Besides the quantization noise, other contributors intervene in the global noise power like thermal noise, $1/f$ noise and jitter.

- (a) Thermal noise : in switched capacitor circuits, thermal noise is generally fixed by the switches. It is stocked in the capacitors during the sampling phase, so that the thermal noise power is [20]

$$PSD_{\text{Thermal}} = \frac{K_{\text{bolt}}T^{(o)}}{C} \quad (1.10)$$

The same quantity is stored during the hold phase. Therefore, for differential circuit the overall thermal noise is multiplied by 4. Furthermore, it is common to fix the value of the tolerated thermal noise in order to determine the minimum value of the equivalent capacitor from the expression 1.10 [20].

- (b) Flicker noise : or 1/f noise is a form of noise that occurs in all electronics devices. It is in general shown as resistance fluctuations and increases at lower frequencies ; whereas, white noise is dominating for higher frequencies. It can then be neglected in the case of high input frequencies.
- (c) Jitter noise (phase noise) : theoretically, the exact period of the sampling clock is T . However, a statistical deviation occurs around the clock edges causing a so-called jitter noise. It is generally modelled as a Gaussian process with a zero mean value and a rms value of σ_{jitter} (Fig. 1.9). The noise power of the jitter can be expressed as [20]

$$\text{PSD}_{\text{jitter}} = 2\pi f_{in} \sigma_{\text{jitter}} \quad (1.11)$$

where f_{in} is the input frequency. In this expression the input amplitude is 1.

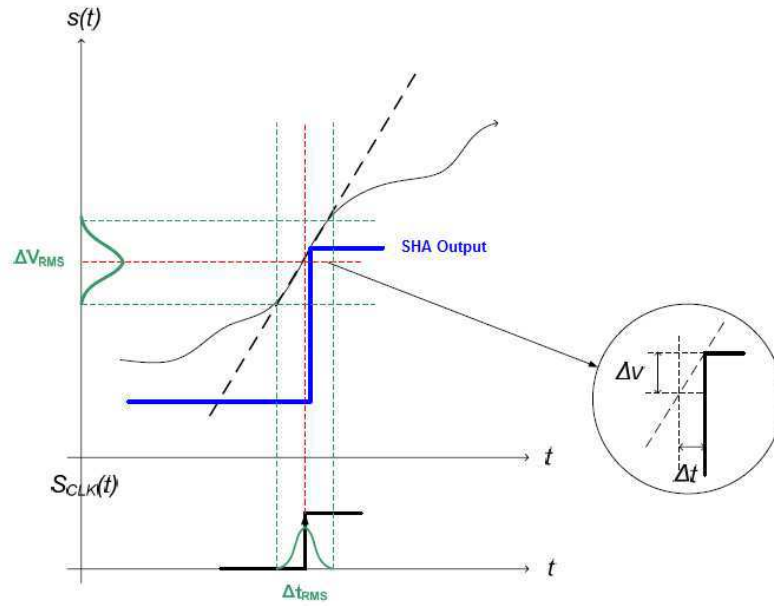


FIGURE 1.9 – Jitter effect.

Finally, the overall expression of the SNR including all cited errors is

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{Quantization}} + P_{\text{Thermal}} + P_{\text{jitter}}}. \quad (1.12)$$

Signal to Noise and Distortion Ratio (SNDR) is the SNR taking into account all types of distortion described below. This is used to measure the Effective Number Of Bits (ENOB) which is the effective resolution of the ADC

$$\text{ENOB}(\text{bits}) = \frac{\text{SNDR}_{\text{dB}} - 1.76}{6.02}. \quad (1.13)$$

2. Total Harmonic Distortion (THD) : non linear charge load causes nonideality of the In/Out characteristic of the ADC in the sense that a sine wave input signal $x(t) = \sin(\omega_{in}t)$ gives a series of harmonics of the fundamental

$$a_1x(t) + a_2x(t)^2 + a_3x(t)^3 + \dots = A_1 \sin(\omega_{in}t) + A_2 \sin(2\omega_{in}t) + A_3 \sin(3\omega_{in}t) + \dots \quad (1.14)$$

Consequently, additional tones appear at each kf_{in} , $k \in \{2, 3, \dots\}$. These undesired tones represent the so-called harmonics. Finally, in order to quantify the impact of the harmonics on the ADC performance, one can use the THD expression given by :

$$\text{THD} = \frac{\sqrt{\sum_{k=2}^{+\infty} A_k^2}}{\text{Fundamental}}. \quad (1.15)$$

This expression is usually done in dB. In addition, above a certain rank of the harmonic, its value can be neglected. In practice, we generally take the first five harmonics to calculate the THD.

3. Spurious Free Dynamic Range (SFDR) : this specification gives an information on the distortion of the analog signal in the ADC output. It is given by the difference between the fundamental and the maximum spur in the Nyquist zone :

$$\text{SFDR(dB)} = 20\text{Log}_{10} \frac{A_{\text{fundamental}}}{A_{\text{spurmax}}}. \quad (1.16)$$

The output spectrum is shown in Fig. 1.10. We denote by A_0 the amplitude of an offset error, A_k ; $k \in \{2, 3, \dots\}$, the harmonics tones and by *Spur*, an additional tone, the highest tone in this example. A is the amplitude of the fundamental.

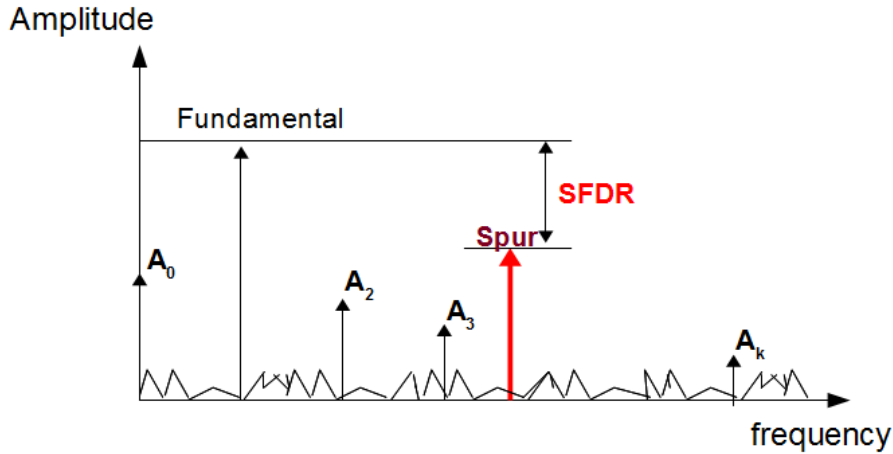


FIGURE 1.10 – Dynamic specifications at the output spectrum

1.4 Towards High Speed ADC Architectures

The above performances determine the choice of the converter in terms of specifications. Nevertheless, depending on the architecture, a trade-off between some parameters have to

	W7	W6	W5	W4	W3	W2	W1	Y2	Y1	Y0
$V_{in} < 0, 125V_{ref}$	0	0	0	0	0	0	0	0	0	0
$0, 125V_{ref} < V_{in} < 0, 250V_{ref}$	0	0	0	0	0	0	1	0	0	1
$0, 250V_{ref} < V_{in} < 0, 375V_{ref}$	0	0	0	0	0	1	1	0	1	0
$0, 375V_{ref} < V_{in} < 0, 500V_{ref}$	0	0	0	0	1	1	1	0	1	1
$0, 500V_{ref} < V_{in} < 0, 625V_{ref}$	0	0	0	1	1	1	1	1	0	0
$0, 625V_{ref} < V_{in} < 0, 750V_{ref}$	0	0	1	1	1	1	1	1	0	1
$0, 750V_{ref} < V_{in} < 0, 875V_{ref}$	0	1	1	1	1	1	1	1	1	0
$V_{in} > 0.875V_{ref}$	1	1	1	1	1	1	1	1	1	1

TABLE 1.1 – 3-bits flash ADC truth table

be taken into account to perform a good figure of merit. This section is dedicated to four high performance architectures and their applications. The first category is devoted to three Nyquist converters : the Flash ADC, Pipeline and Successive Approximation Converters. The second category concerns the oversampling converters like Sigma Delta converter.

1.4.1 Nyquist ADCs

1.4.1.1 Flash converters

Flash ADCs [21, 22, 23], are the fastest way to convert an analog signal to a digital signal and are suitable for applications requiring very large bandwidth. However, flash converters consume a lot of power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications such as data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives.

A n bit analog to digital flash converter requires, $2^n - 1$ comparators. 2^n resistors and one reference source V_{ref} which generates the $2^n - 1$ reference values used by the comparators to compare the sampled input values. Each comparator's output is set to '1' or '0' whether the sample is greater or smaller than the reference assigned to itself. This is known as thermometer code encoding and results in a digital output code.

As the comparators operate in parallel, the flash ADC is very fast and the conversion is achieved in one clock cycle. According to this, we can say that the speed of the ADC depends on the speed of the comparators.

A 3-bit flash converter is described in Fig 1.11. Seven comparators are required to achieve the conversion and the encoder converts the comparators outputs to a binary code. This is described in Tab.1.1.

The main drawback of this approach is that flash converters require a large number of comparators that must be carefully matched to ensure the linearity. Another limitation concerns the number of the comparators that increases exponentially with the resolution leading to high power consumption and die size and hence the price. In fact, additional bit almost doubles the size of the ADC core circuitry.

1.4.1.2 SAR ADCs

The Successive-Approximation-Register (SAR) ADC is commonly an architecture of choice for medium-to-high-resolution applications. It goes from 8 to 16 bits and provides

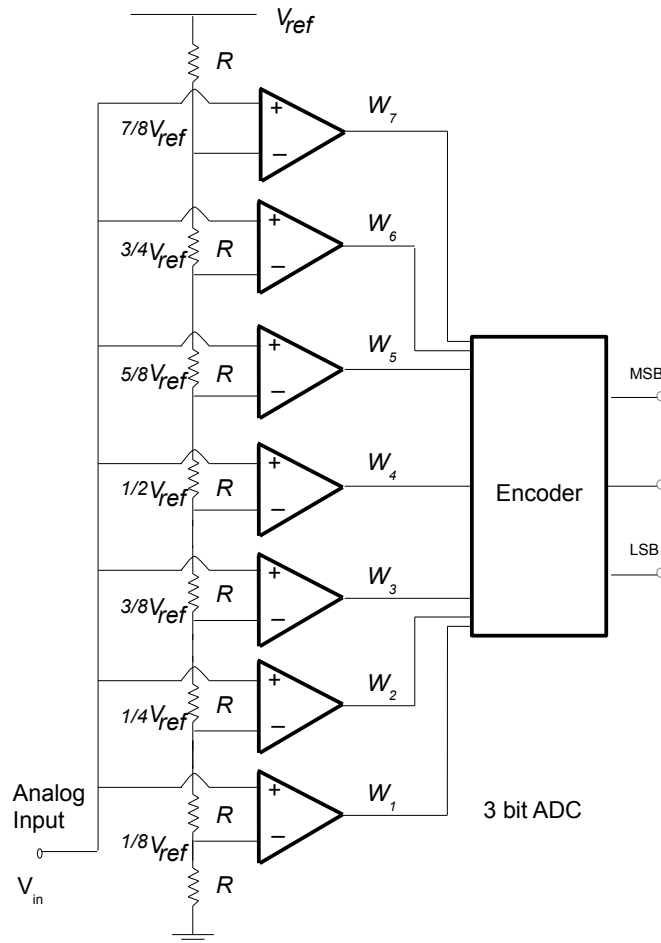


FIGURE 1.11 – A 3-bits flash ADC.

low power consumption. SAR converters are usually used for data/signal acquisition, industrial controls and portable/battery-powered instruments.

A SAR converter, conceptually uses a single comparator over many cycles to make a conversion. This is shown in Fig 1.12. The SAR register provides a binary code to the digital to analog converter (DAC) by trying all values of bits starting with the most significant bit and finishing at the LSB. Throughout the count process, the register monitors the comparator's output to see if the binary count is less or greater than the analog signal input. The DAC produces an analog signal that approximates the input signal. The first value provided is $V_{ref}/2$ which represents the most significant bit. If this value is smaller than the input sample, the $1/2$ scale is retained and the most significant bit (MSB) is set to 1. Otherwise it is removed and the MSB is equal to 0. The register sets the next bit to 1 and repeats the process. These series of steps is repeated n times, using successively smaller weights in binary progress until the desired resolution, n is attained.

One of the drawbacks of the SAR architecture is that there are many cycles for each

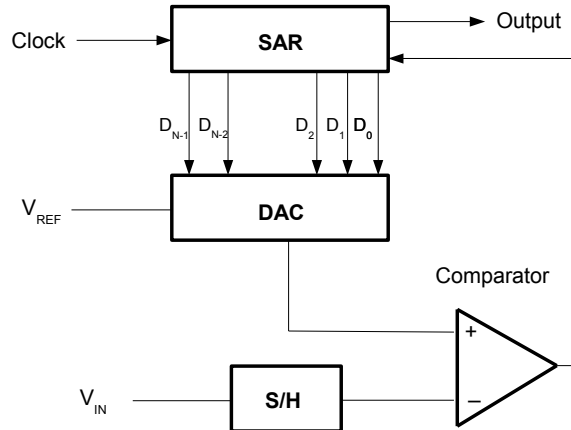


FIGURE 1.12 – Successive Approximation architecture

sample to be converted. In the n -bit converter, n approximations and comparisons must be performed in each sampling period compared to 1 cycle for flash converter. For this reason, SAR converters are more often used at lower speeds in high-resolution applications. Moreover, the DAC is the most critical component of the SAR, and it is difficult to design [24, 25]. In fact, the SAR ADC speed is mainly limited by the settling time of the DAC, which must settle to within the resolution of the overall converter. This makes the accuracy of the SAR ADC conversion imposed by the accuracy of the DAC [24].

1.4.1.3 Pipeline ADCs

Pipelined architecture effectively overcomes the limitations of the flash architecture. The converter divides the conversion task into several consecutive stages. Each of them consists of a sample and hold circuit, an m -bit sub-ADC (usually a flash ADC), and an m -bit D/A converter (DAC). The sample and hold, DAC, subtraction block and amplification form an arithmetic unit called the multiplying digital-to-analog converter (MDAC).

First, the sample and hold of the first stage requires the input signal. Then the n -bit flash converter converts the sampled signal to digital data. The conversion result forms the most significant bits of the digital output. This same digital output is sent to an m -bit digital to analog converter, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages are necessary to achieve the desired n resolution. The ADC architecture is described in Fig. 1.13. One redundant bit could be added to each stage to relax the quantization accuracy specifications in the sub-ADC [26, 27]. By adding a redundant bit, the stage resolution is increased by one bit minus one quantization level while the gain is kept the same. To perform an effective number of bit, the digital output bits from the stages are sent to a correction circuitry which consists of adding up the properly delayed stages outputs.

Due to pipelined architecture, the throughput rate of an ADC is independent of the number of the stages used and the hardware cost is approximately linear with resolution [28]. Another advantage of the pipeline architecture is that the accuracy requirements for the latter stages are greatly relaxed compared to the first few stages, making it possible to

reduce the total power consumption.

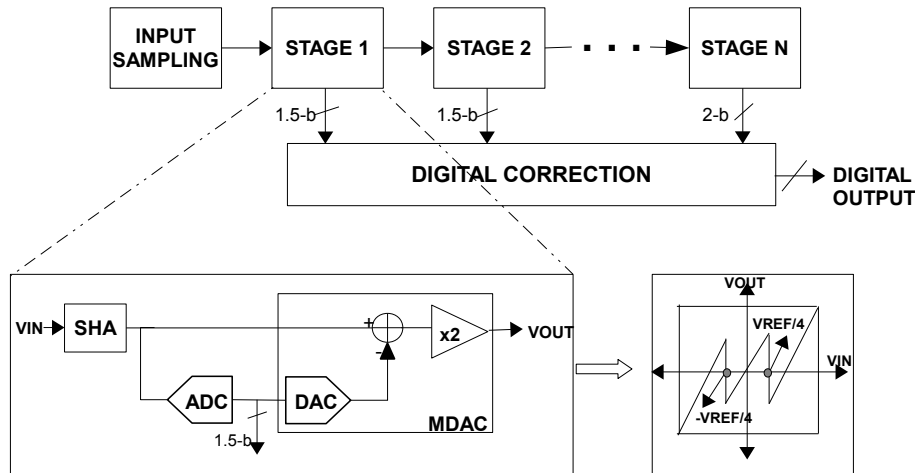


FIGURE 1.13 – Typical 10-bit (1.5-bit per stage) Pipeline ADC architecture

In pipeline ADCs, thermal noise is the fundamental source of errors, it basically comes from the sampling switches and the sample and hold amplifier. Thermal noise is random and the only way to reduce it is to increase the capacitor size which in turn increases the power consumption of amplifiers associated with charging and discharging capacitors. Another sources of errors in a pipeline ADC are offset errors (sample and hold, amplifier and comparator), gain error (sample and hold and amplifier). They can be eliminated by self-calibration techniques.

1.4.2 Oversampling ADCs

Oversampling is the best way to achieve higher resolution for analog to digital converters. Sigma Delta ADC uses this technique to improve by 1.5 bit the resolution for every doubling of the sampling rate frequency. Therefore, the oversampling is limited by the bandwidth since the clock frequency needs to be relatively high to provide the same resolution which is difficult to achieve. For this reason, Sigma Delta converters are usually suitable for applications requiring a trade-off between speed and resolution by oversampling; such as audio design, instrumentation and sonar.

Sigma Delta converter consists of a Sigma Delta ($\Sigma\Delta$) modulator followed by a digital decimation filter. The modulator shown in Fig. 1.14 samples the input signal at a rate much higher than the Nyquist frequency by the oversampling ratio (OSR). The digital output is fed back through a DAC and subtracted from the input signal. The result of the subtraction is accumulated in an integrator to finally be quantized by a coarse ADC. The quantization noise is high pass filtered to ensure a low noise at low frequencies. This process is called quantization noise shaping [29, 30]. Moreover, other types of errors originated from the non ideal circuit behavior such as analog noise can be partially removed by a digital filter before the signal is decimated to generate the final output of the converter.

Fig 1.14 shows a first order $\Sigma\Delta$ modulator since this one includes only one integrator. The resolution increases by 1.5 bit for every doubling of the sampling frequency, which means that the OSR is doubled. Thus to get a high resolution, a high OSR is needed at the cost of a low bandwidth. By adding more integrators in the loop, the order of the modulator increases leading to stringent noise shaping and then the OSR could be reduced.

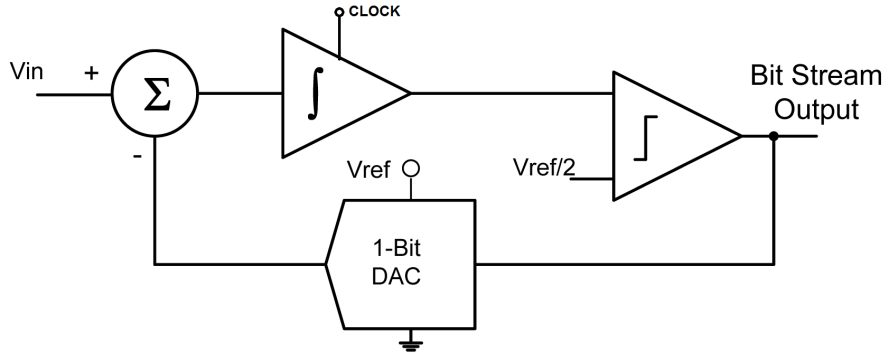


FIGURE 1.14 – First order $\Sigma\Delta$ modulator.

Thus the bandwidth could be larger. However the modulator may be unstable and the noise shaping, which is of the same order as the integrators number can increase the noise power.

The resolution of the modulator can also be increased by increasing the resolution of the quantizer. However, nonlinearity errors in the DAC will limit the performance while the 1-bit DAC have only offset and gain errors. This problem can be overcome using calibration techniques [31]. High noise shaping can also be achieved by cascading independent modulator stages avoiding the calibration [32]. The drawback of this technique is that mismatch between the analog and digital circuit limits the performance.

As the bandwidth is the principle limit of some ADC architectures such as the sigma Delta converter and the SAR ADC, several research works have been developed employing parallelism to widen the bandwidth of the converter. The well-known technique of parallelism is called time-interleaving method and is explained in the subsection below.

1.4.3 Time-interleaved ADCs

Nowadays, the performances of single analog to digital converter architectures are limited by high resolution, high speed and low power requirements to comply with new communications standards [33]. One possibility to overcome these performance limits is the use of parallelism. And the attractive way to increase the conversion rate of ADCs is the time-interleaving techniques where the input information is split into several parallel channels. Each channel operates independently, fed the output to the multiplexer to finally be recombined to a digital output. Fig. 1.15 illustrates the concept of the time-interleaved ADC using M parallel channels. Each channel operates at f_s/M , where f_s is the total sampling frequency rate of the time-interleaved converter. Thus, sampling with an ideal TI-ADC with M channels is equivalent to sampling with an ideal ADC with an M -times

higher sampling rate. The speed requirement of each channel is then relaxed by the factor of M . In addition, if we compare the power consumption to the single channel, Fig. 1.15 shows that up to a certain sampling frequency, the dependency to this one is linear then evolves exponentially. This is overcome thanks to the time interleaved architecture where the power consumption of the overall ADC is M -times the single channel consumption taking advantage of the linear dependency.

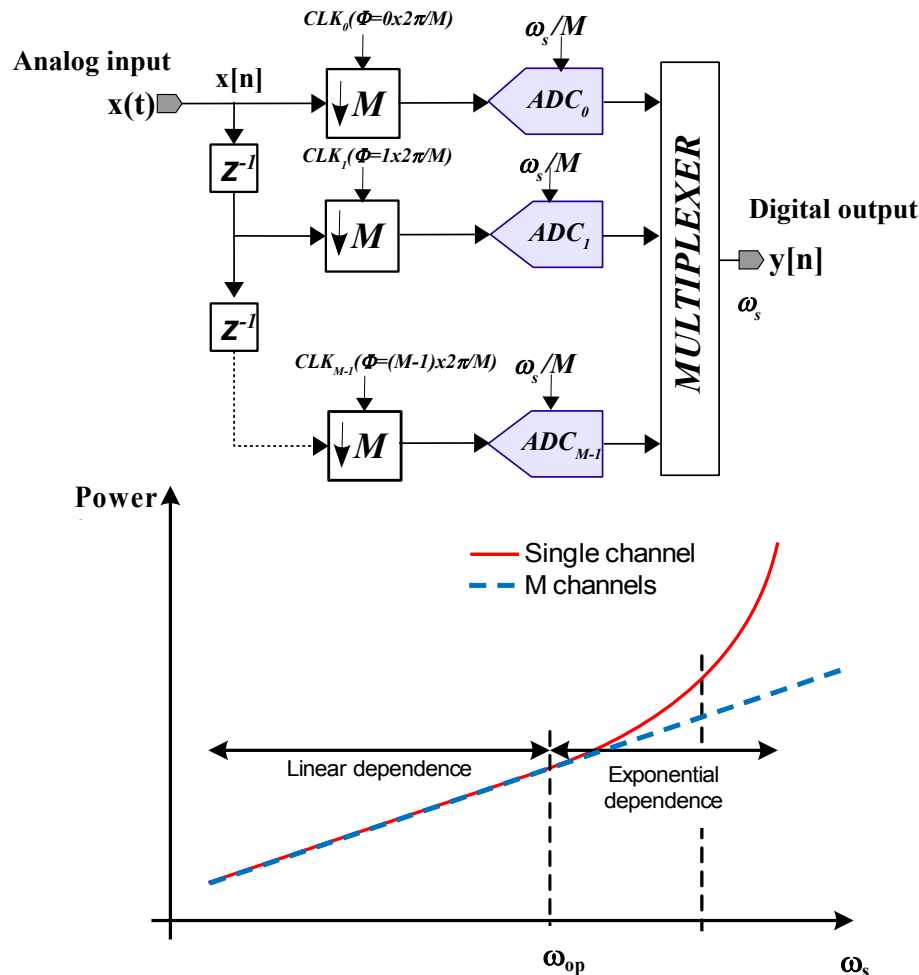


FIGURE 1.15 – Time-interleaved analog to digital converter.

The performance of the time interleaved converter is of course limited by the accuracy of the channel ADC but there are additional errors caused by the mismatch between the channels caused by IC and environment variation. At least four well-known impairments can limit the performance of the ADC : clock skew errors, gain and offset errors. The last one is the bandwidth mismatch, recently appeared with the very wide band applications. There are several techniques to reduce the effect of the three first ones. Offset and gain error can be removed by calibration [3, 34, 35, 36, 37]. However, phase skew errors are harder to compensate and lead to a more stringent limitation on TI architectures.[38, 5]. The most effective technique to overcome this problem is to use a single input sample and hold SHA circuit which usually needs an opamp that runs at the full speed of the ADC. Opamps are therefore power consuming parts of the ADC. However, their number can be

reduced by using opamp sharing techniques. It consists of using one opamp shared by a set of channels. This can reduce the number by the factor of 2 [39, 40]. However, this technique cannot be used for high speed application since the shared sampling network needs to work at full speed which is not possible in most cases.

Regarding bandwidth mismatch errors, which is the main subject of our interest, very few works have addressed this problem. This will be discussed along this document and some techniques are proposed.

The previous section gave an overview of Nyquist and oversampling converters mechanism, their performances and the applications they are suited for. Moreover, In order to widen a targeted bandwidth, a time-interleaved version was presented with some of the drawbacks this architecture can encounter. The following section illustrates the state of the art of each architecture and their time-interleaved versions. A comparison is given to point up the performances of each converter in the global state of the art.

1.5 ADC Trend

1.5.1 Global Converters trend from 1999 to 2012

A survey for Analog-to-Digital converters has been realized as a complement of the work in [41]. It allows to compare the different high performance converters described in the previous section and their time-interleaved versions. They are labelled in Fig. 1.16 where a trade-off between the resolution in terms of SNDR and bandwidth is shown. If we focus on the comparison between the architectures, we can notice that :

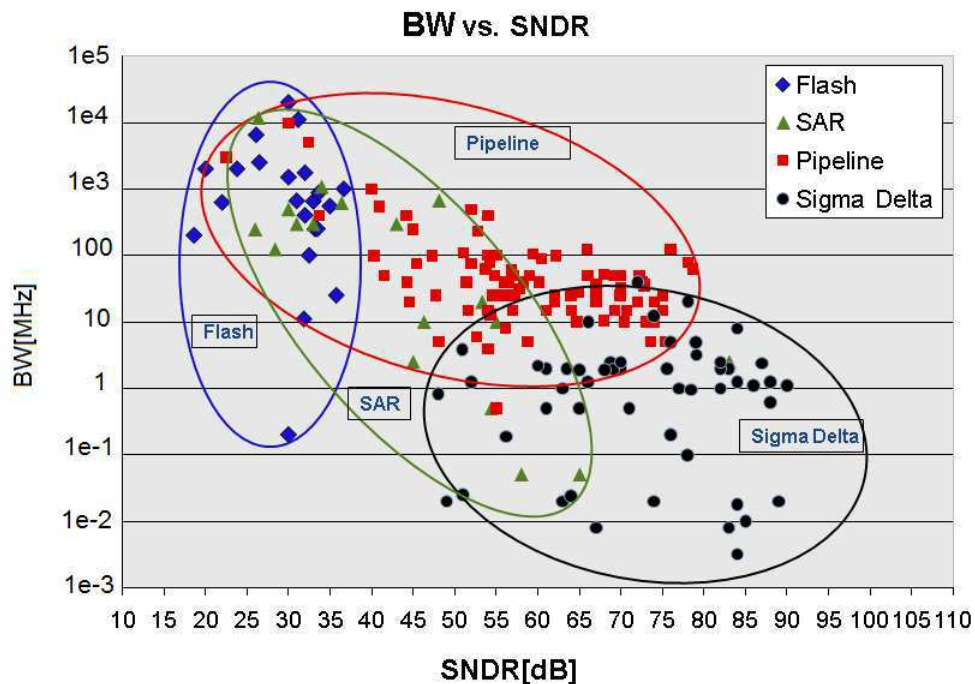


FIGURE 1.16 – State of the Art of high performance ADCs from 1999 to 2012.

- The flash ADCs are performed for very high sample rate up to several GHz (2.5GHz)

in the figure) and the resolution attains 7-bit in this survey.

For applications requiring much higher resolution, the flash converter is usually used in each pipeline stage at the cost of the bandwidth. The trend of the pipeline is then shown below.

- Pipeline ADCs spread over a large interval of bandwidth for resolutions going from 8 to 14 bits. The time-interleaved pipeline converter are essentially working at very high speed at the cost of the resolution.

Some recent pipeline architectures achieving high resolution, high speed and consuming less than 1W of power are listed in the Tab 1.3. Most of the ADCs today are based on the SHA-less technique in order to reduce the power dissipation and improve the linearity of the ADC. An example of one of the first circuits taking advantage of this approach achieves 78.6 dB of SNDR at 62.5 MHz of bandwidth and consumes 385 mW [42].

- For SAR converters, there is a trade-off to perform low to medium resolution for a bandwidth up to 12 GHz for time-interleaved SAR architecture. This latter works at very high speeds at the cost of low resolutions. However one architecture is distinguished by achieving 14-bit of resolution at 2.5 MHz of bandwidth. To do so, a non-binary technique is used [25, 43].
- Regarding oversampling architectures, the Sigma Delta converter is in general suited for applications requiring very high resolutions, up to 18 bit. The figure shows the trade-off made between speed and resolution. One can distinguishes for this architecture, continuous-time Sigma Delta from discrete-time version. The two architectures are different and do not have same requirements to achieve high performance as explained in [44]. The continuous-time converter works at higher bandwidth, when the discrete-time architecture achieves high resolution.

Tab 1.2 gives an overview of the trend of the different architectures described before. It gives a brief comparison of performance in term of speed, resolution and consumption.

	Flash	Pipeline	SAR	Sigma Delta
Speed	+++	+	--	---
Resolution	---	+	++	+++
Consumption	---	-	++	+

TABLE 1.2 – Analog to digital converters comparison.

From this analysis, we can choose the pipeline architecture which is better suited for base station application in terms of both speed and resolution. Time-interleaved architecture is an easy way in order to go higher in sampling frequency without increasing the power consumption. Fig. 1.17 highlights the time-interleaved architectures compared to a single channel. It is important to notice that due to mismatch errors in a parallel architecture, distortion occurs causing degradation in SNDR performance and hence gives lower resolution. That is why, the main work of the thesis focuses on calibration of these imperfections in order to push the time interleaved converters to higher resolutions.

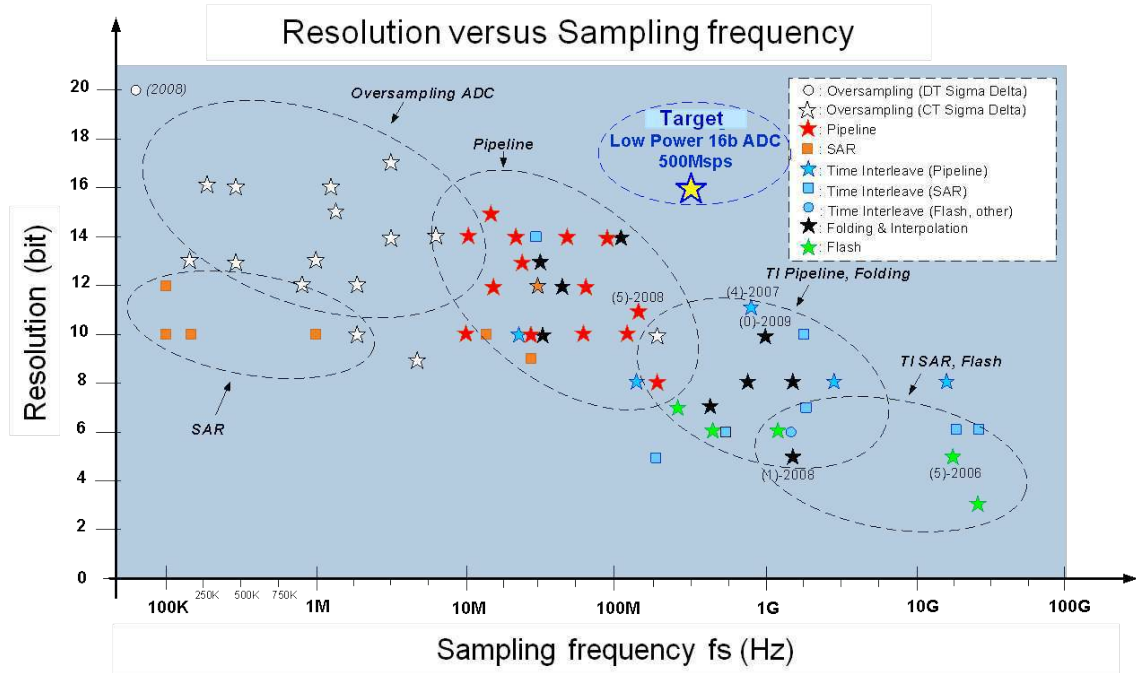


FIGURE 1.17 – State of the Art of high performance ADCs from 1999 to 2012 : Comparison Parallel architectures to Single channel ADCs.

1.5.2 Figure of merit

In order to make a choice between the presented high performance architectures and according to the aimed specification, a comparison including power consumption is necessary. First, from the survey shown in Fig. 1.16, an interesting area (more than 40dB of SNDR for more than 1MHz of bandwidth) gives a set of three high speed high resolution ADCs ; Pipeline, SAR and Sigma Delta. Power consumption, represents an important factor of choice of a good architecture, the study focuses on the factor of merit to select interesting architectures for the aimed application. The figure of merit, is widely used and defined as

$$\text{FOM} = \frac{P_{\text{diss}}}{(2^{\text{ENOB}} \cdot f_s)}. \quad (1.17)$$

Where, ENOB is the effective number of bits, f_s , the Nyquist frequency, and P_{diss} is the power dissipation. The figure of merit evaluates the power efficiency with resolution and speed.

Fig. 1.18 shows a comparison between the different ADCs described before in term of figure of merit in function of the resolution. SAR converters have a good figure of merits but have lower resolution compared to Pipeline and $\Sigma\Delta$ converters. Furthermore, it shows that $\Sigma\Delta$ presents the best trade-off between speed, resolution and consumption.

1.5.3 Some outstanding architectures

Tab. 1.3 shows a list of architectures from the literature that represents the best performances in terms of SNDR and sampling frequency. Moreover, power consumption and

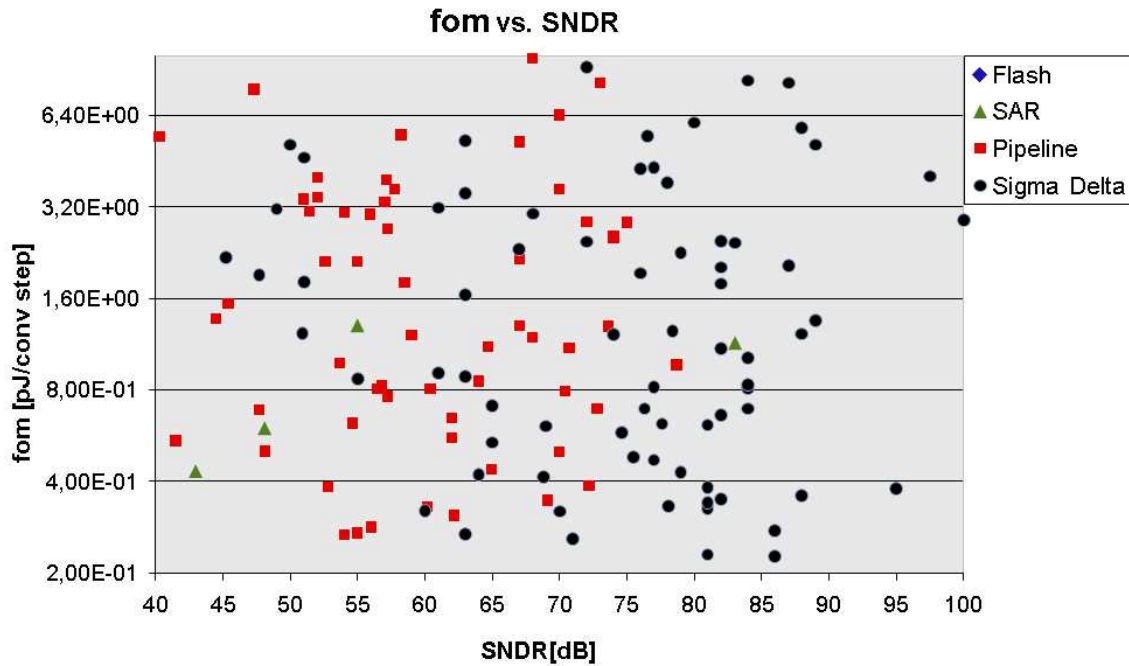


FIGURE 1.18 – ADCs performance in terms of the Factor of Merit and resolution.

Ref	Archi	Process (um)	SNDR (dB)	Fs (MSPS)	BW (MHz)	Power (mW)	FOM(pJ/conv step)
[45]	Pipeline	0.25 BiCMOS	78.1	160	80	1620	1.54
[42]	pipeline	0.18 CMOS	78.6	125	62.5	385	0.44
[46]	Pipeline	0.18 BiCMOS	76	250	125	1	0.78
[47]	TI-Pipeline	0.09 CMOS	54	800	400	350	1.07
[48]	TI-Pipeline	0.13 CMOS	52	1000	500	250	0.77
[49]	Pipeline	0.09 CMOS	62	50	25	4.5	0.087
[50]	SAR	0.09 CMOS	53.3	40	20	0.82	0.05
[51]	TI SAR	0.13 CMOS	81	40	2.5	66	0.18
[52]	SAR	0.13 CMOS	48.11	1350	675	168	0.60
[53]	TI SAR	0.045 CMOS	34	2500	1100	50	0.55
[54]	SDCT	0.13 CMOS	78.1	900	20	87	0.33
[55]	SDSC	0.065 CMOS	81	256	8	50	0.34
[30]	SDCT	0.13 CMOS	74	640	20	20	0.122
[56]	SDSC	0.13 BiCMOS	52	40000	120	1600	20.49

TABLE 1.3 – High performance ADCs gathered from the literature for CMOS and BiCMOS process (only the power consumption of the modulator is considered for $\Sigma\Delta$ converters in this table).

figure of merits parameters are taken in account in order to compare these converters such power consumption.

1.6 Wireless base station application

1.6.1 ADC performance requirements

Most of the wireless systems include a receiver (Rx) and a transmitter (Tx) in the same architecture in order to go towards convergence systems. The evolution of wireless communication systems leads to the development of flexible, multichannel transceiver architectures in order to address different standards. This is particularly relevant in base station applications where the deployment cost is significant [57, 58, 59].

Fig. 1.19 shows a simplified base station transceiver; the upper chain represents the receiver where the wideband RF signal from the base station antenna is filtered and amplified by the low noise amplifier (LNA). After that, the mixer shifts the signal into lower frequencies in order to be digitized by the ADC and be treated by the digital signal processing block. The voltage gain amplifier is mandatory in some architectures in order to regulate the input dynamic range of the ADC. This latter is the most stringent element of the chain. In fact, for wideband multi-carriers standards, the challenge is to push the converter as close as possible to the antenna in order to realize a multistandard receiver for software defined radio (SDR). In that case the channel selection is accomplished within digital domain. Consequently, for wideband signals, the ADC needs to go fast with large dynamic range [57, 60, 58, 61, 62]. The lower chain in Fig. 1.19 represents the transmitter part. From

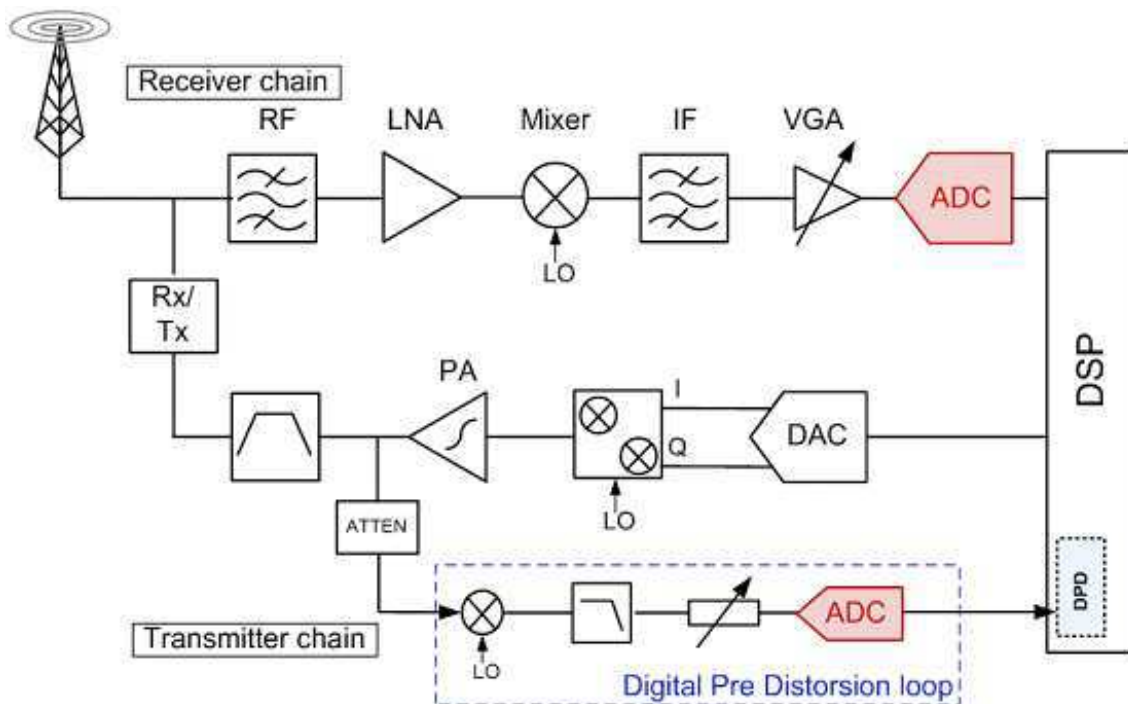


FIGURE 1.19 – ADC position in a base station transceiver

the digital part (DSP), first a conversion to the analog domain is necessary to send the signal through the analog blocks. The signal is shifted to higher frequencies using the I/Q mixers according to the aimed standard. However, due to the presence of other signals in the band of interest, coming from other equipments in the networks (base stations and user equipments), the transmitted signal is modulated generating undesired signals in the

Symbol	Parameters	Conditions	Value (Typic)
Speed			
f_s	Sampling frequency		500 Msps
Performances			
SNR	Signal to noise ratio	$f_{in} = 10MHz$ $f_{in} = 380MHz$	73 dBFS 71 dBFS
SFDR	Spurious Free Dynamic Range	$f_{in} = 10MHz$ $f_{in} = 380MHz$	94 dBFS 90 dBFS
Power consumption			
Power	Power consumption		< 650 mW

TABLE 1.4 – ADC specifications for a base station application. $A_{in} = -1dBFS$, jitter=80fs.

wanted band and hence distorts the signal. This effect is minimized using band pass filters which need to be steep enough to retrieve the wanted signal. This latter is amplified by the power amplifier module (PA) in order to send a strong signal to the antenna then in the air to prevent different attenuations that the signal undergoes before attaining the receivers. Nevertheless, due to modulation schemes, the PA is pushed to operate in its non-linear region which distorts the signal and generates undesired tones at the multiple of the input frequency. For wideband signals like WCDMA and multicarrier signals, this impact is more visible and the power efficiency of the transmission is minimized. In fact, addition wideband adjacent signals are generated due to the third and the fifth order of non linearity with high power levels. Moreover, with the apparition of SDR leading to the transmission of a wideband including multistandard bands, high linear PA requirements attract more attention in order to deliver the wanted signal properly.

Several works have addressed this problem and one of the most popular techniques consists of using a digital pre-distortion loop (DPD) [63]. It consists of pre distorting the signal in the digital domain and comparing the desired signal to the one at the PA output in order to evaluate the compensation. To do so, the output of the PA needs to be converted using an ADC (see Fig. 1.19) which is, in that case highly challenged in terms of speed and resolution, especially for wideband signals. In fact, the ADC digitizes a large signal including the wanted signal and adjacent interferers (3rd and 5th nonlinearity order of the PA) and for multi standards transmitters, the ADC needs to operate faster. In addition, the accuracy of the converter should be high enough to minimize the error between the feedback signal and the transmitted signal. For all these reasons, high speed, high resolution ADC converters are the good choice for such application.

The specifications of the ADC in terms of SNR and SFDR are limited by the requirements of the previous blocks in the transceiver chain. Tab. 1.4 sums up the specifications that we target in this thesis, they have been defined to challenge the existing ADC products in the market which are shown in Fig. 1.20, where is represented the different ADCs in terms of SFDR versus FoM.

1.7 Chapter Conclusion

In this chapter, a performance analysis of an ADC was provided. A quantization of 12 bit at minimum is needed to achieve the specification in Chapter 2 and do not degrade the SNR due to thermal noise. In order to choose the suited architecture, four high per-

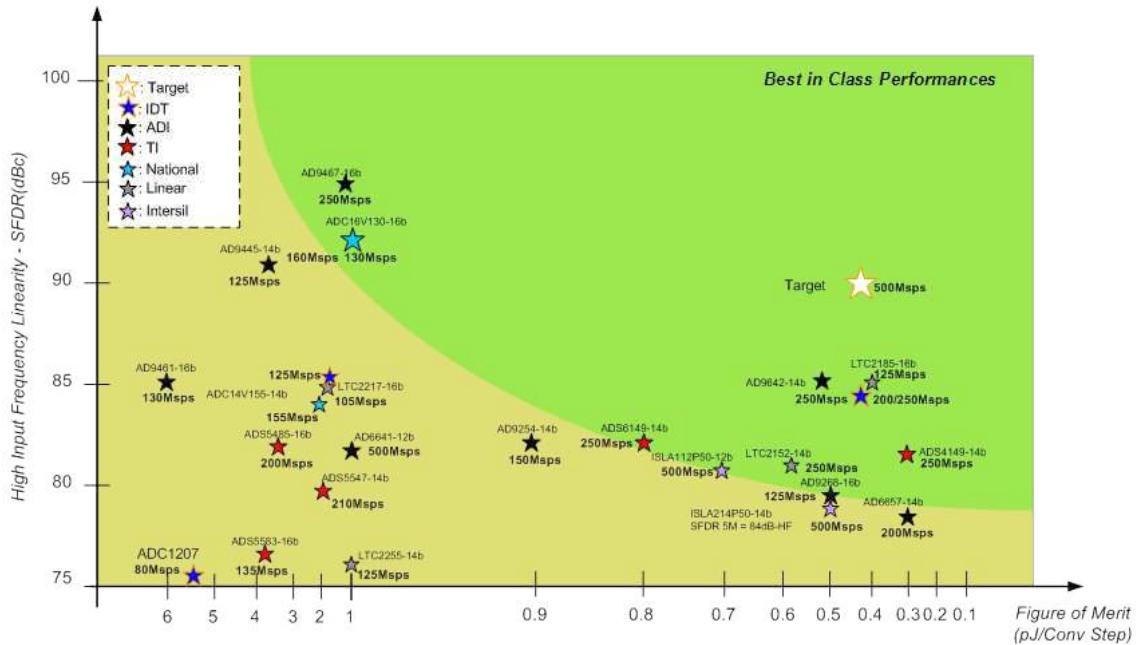


FIGURE 1.20 – Comparison of our targeted ADC with the existing competitor ADCs in terms of SFDR versus FoM

formance ADCs were presented; nyquist ADCs including flash, SAR and pipeline versus the oversampling ADCs presented by the $\Sigma\Delta$ converter. A performance analysis has been done for each architecture with a comparative trend using the figure of merit and taking into account the targeted specifications. In fact, a survey of these architectures has been done for the last decade and has shown that : flash ADCs are the fastest architecture but is limited in resolution due to exponential growth of the comparators number with the resolution. They are usually used in a pipeline architecture which cascades several stages to improve the resolution. Due to process limitations and the high number of OTA used, this architecture has a high power consumption. SAR architecture is suitable for applications that need a very low power consumption but limited in speed. However, this architecture can go faster using parallelism. It can also be used as a sub-ADC of pipeline stages for example. Finally, Sigma Delta ADC has the best figure of merit thanks to the very high provided SNR and taking into account the oversampling parameter.

In this comparison, time-interleaved architectures were considered for their capacity to improve the speed. It has been shown that time-interleaved pipeline ADC is the best choice for a base station application and the power consumption of the TI pipeline architecture is improved thanks to parallelism. However, this latter presents some drawbacks due to environment variations.

In the following chapters, time-interleaved architecture is chosen for study and calibration techniques are proposed to deal with the different limitations of this architecture.

Chapitre 2

Time-Interleaved ADCs

2.1 Introduction

In order to increase the sampling rate of an analog-to-digital converter (ADC) beyond a certain process technology limit, the use of a time-interleaved analog-to-digital converter (TI-ADC) has been proposed [64]. A TI-ADC has a parallel structure, where a number of ADCs successively sample the input signal. The input analog signal is sampled by each ADC in a cyclic manner, and the digital output is similarly taken from each ADC to reconstruct the signal stream in digital form. At the end, the overall sampling rate is multiplied by the number of ADCs. A TI-ADC finds its application in a multitude of electronic systems such as radar, direct digital receivers, base station receivers, and high-speed instrumentations.

A TI-ADC architecture is illustrated in Fig. 2.1, where M channels in parallel are operating at the same sampling rate ω_s/M , where ω_s is the overall sampling frequency. Each converter samples the input signal during $MT/2 = 2\pi/\omega_s \cdot M/2$, called the sampling phase and holds during the next $(M/2 - 1)T$ periods. After each sampling period, the next channel operates in the same way so that the channels have different sampling instants. Nevertheless all channels have the same period of MT .

The time-interleaved ADC system is a good way to increase the sample rate with relatively slow circuits. Ideally, the reconstructed digital output should be identical to an ADC output running at ω_s . However, in a real world, channel characteristics are different between individual ADCs in the time-interleaved architecture due to fabrication errors, circuit aging and temperature variations. This leads to create differences in terms of offset, gain and phase between the channels. Consequently, the so-called mismatch errors generate undesired spectral components and can significantly degrade the performances of the system such as the SFDR and hence the SNDR [33, 3, 34, 35, 65, 36, 37, 47, 66].

This chapter is divided as follow. First, the time-interleaved architecture is presented in Section 2.2, and analytic expressions are exposed in time and frequency domains. However, due to circuit imperfections, the channels are mismatched and the output performances are degraded. The consequence of these combined errors is expressed in this section as well. Then the errors are detailed separately in Section 2.3, where the impact in the output spectrum is illustrated. Section 2.4 is dedicated to the study of performance limitations including all errors where a SFDR budget is presented before any compensation. Then according to the existing compensation circuits in the literature regarding static gain and

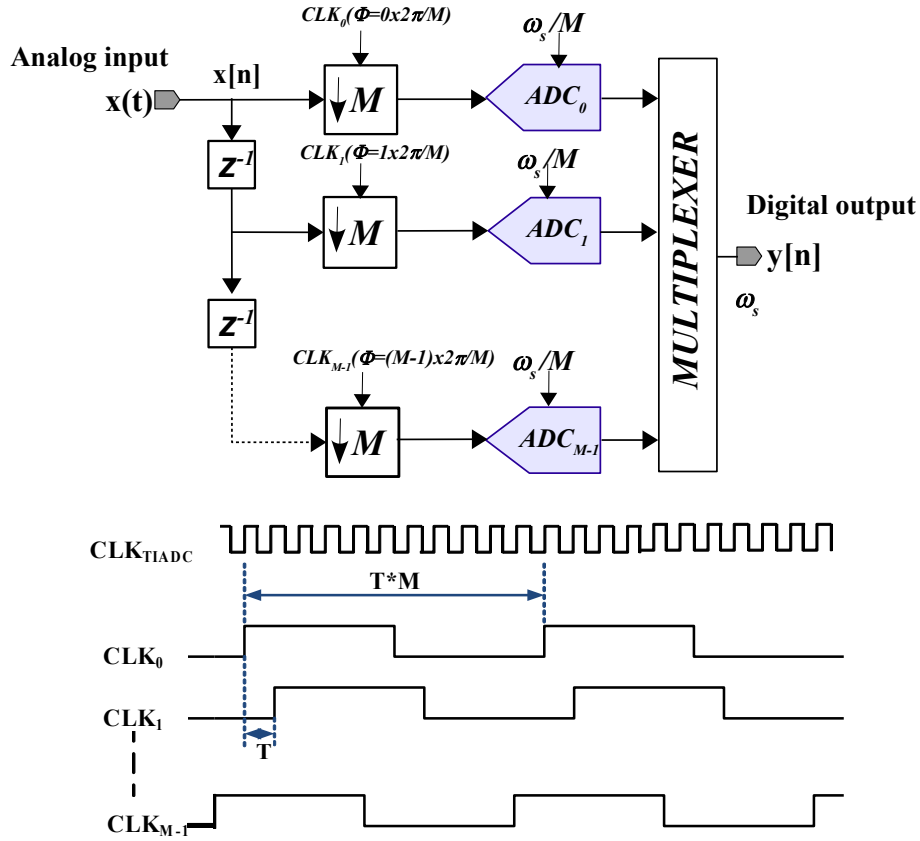


FIGURE 2.1 – M -channels time-interleaved ADC and sampling phase.

clock skew mismatch calibration, an evaluation of the targeted accuracy of the bandwidth mismatch error in order to reach a SFDR of 90dB is done.

2.2 Channel modelling

Fig. 2.2 models the i -th channel of the time-interleaved architecture including all the errors caused by environment variations, in which, offset mismatch error is the difference between the DC values of the channels whereas the static gain mismatch intervenes as the error in terms of amplitude. The clock skew which is a static deviation of the clock from the ideal edge creates a linear mismatch error in function of the input frequency if the deviation of each channel's clock is different in a TI-ADC. Finally, the bandwidth mismatch as illustrated in Fig. 2.2, comes from the difference between the time constants of the channels sampling networks. This error contributes as a non linear, frequency dependent error which distorts the gain and the phase of the signal. We will focus on this latest error in our work and propose a number of techniques to overcome these drawbacks in analog and digital domains.

In order to understand the impact of these errors on the output signal, we analyze the

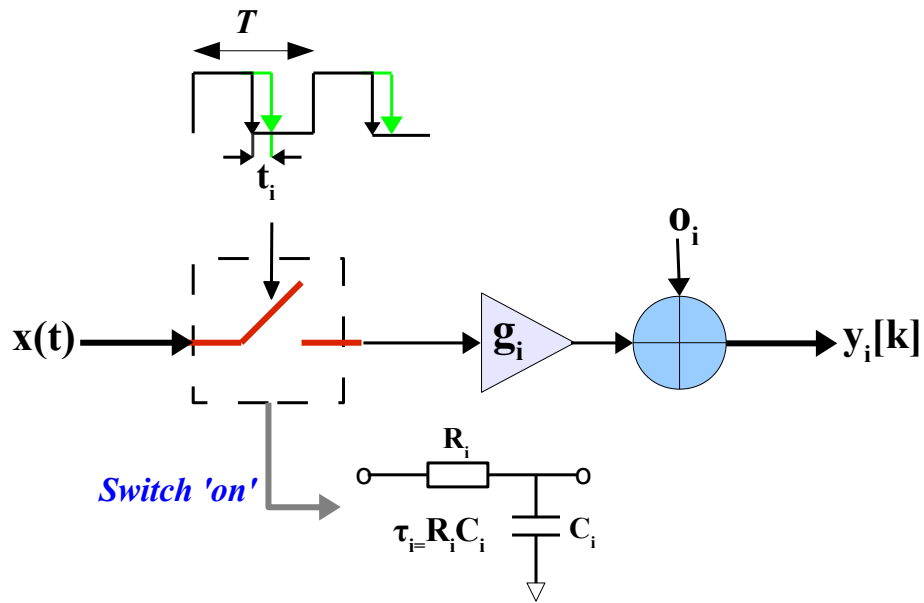


FIGURE 2.2 – i -th channel including distortion errors : offset, gain, skew and bandwidth mismatch.

overall TI-ADC output in time domain. Then, from the frequency analysis, we show the occurrence of undesired tones in the spectrum due to mismatch errors.

Fig. 2.3, shows a M channels time-interleaved architecture gathering all these errors. We

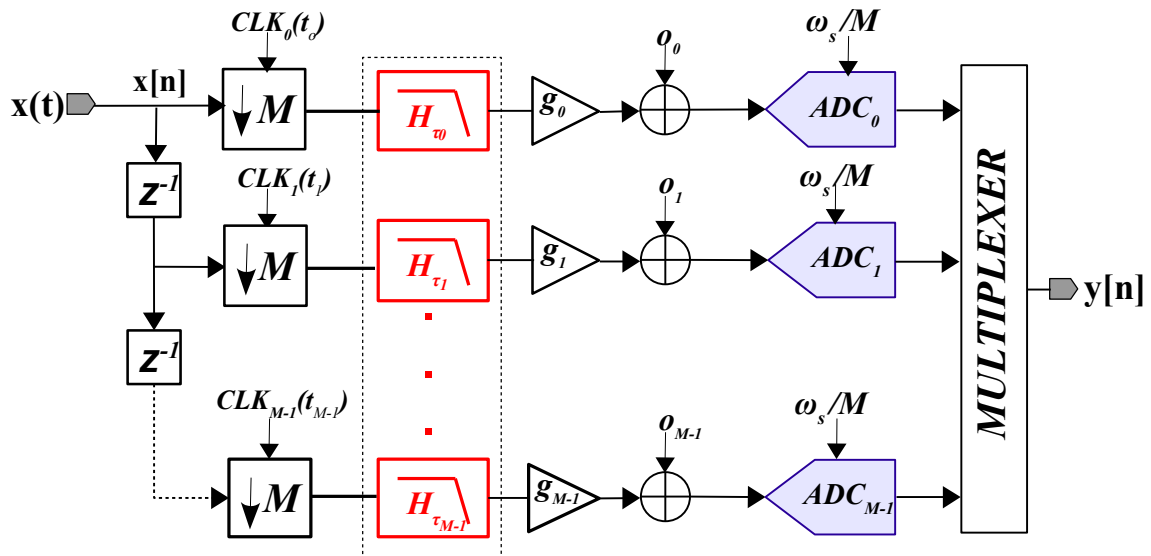


FIGURE 2.3 – Time-interleaved converter including all distortion errors : offset, gain, skew and bandwidth mismatch.

first consider the following notations which are used in the rest of the document.

1. Notations :

- Index i corresponds to the i -th channel, $i \in \{0; M - 1\}$
- Index r corresponds to the reference channel. We will use the 0-th channel as a reference,
- o_i : offset error of the i -th channel,
- g_i : gain error of the i -th channel,
- t_i : time error of the i -th channel,
- τ_i : time constant error of the i -th input filter, where $\tau_i = \tau_r(1 + \Delta_{\tau_i})$, the i -th time constant and τ_r the reference channel time constant,
- Δ_{τ_i}/τ_r : relative time constant mismatch error,
- $h_{\tau_i}(t)$: the impulse response of the i -th channel input filter.
- $H_{\tau_i}(\omega)$: frequency response of the i -th channel input filter ; Fourier transform of $h_{\tau_i}(t)$.
- $\delta(x)$: Dirac distribution,
- $x(t)$: analog input,
- y_i : i -th channel digital output.

2. Input considerations :

We denote by $x(t)$ the continuous time input signal and by $y_i[k]$, the i -th channel's output including the mismatch errors. The overall digital output is denoted by $y[k]$ as shown in 2.3. First, the signal has a wide spectral bandwidth, meaning that we can target several Nyquist zones. However, the signal is supposed to be bandlimited to $B < \pi/T$ in order to fulfill the Shannon criteria. In that case, the input spectrum $X(\omega)$ after sampling is periodic with period ω_s without aliasing and the input signal $x(t)$ can be reconstructed.

A sampled version of the input without errors can be expressed as :

$$x_d(t) = \sum_{k=-\infty}^{+\infty} x(t)\delta(t - kT). \quad (2.1)$$

The i -th channel output without errors at sample k can be expressed as :

$$y_i[k] = x((kM + i)T). \quad (2.2)$$

Considering all the errors in Fig. 2.2, the i -th channel's digital output can be expressed as :

$$y_i[k] = g_i x((kM + i)T - t_i) * h_{\tau_i}(t) + o_i. \quad (2.3)$$

The time expression of the i -th channel is done by summing the samples over the time axis as follows :

$$y_i(t) = \sum_{k=-\infty}^{+\infty} y_i[k] \delta(t - (kM + i)T). \quad (2.4)$$

$$y_i(t) = \sum_{k=-\infty}^{+\infty} (g_i x(t - t_i) * h_{\tau_i}(t) + o_i) \delta(t - (kM + i)T). \quad (2.5)$$

The overall output of the TI-ADC is given by :

$$y(t) = \sum_{i=0}^{M-1} y_i(t). \quad (2.6)$$

$$= \sum_{i=0}^{M-1} \sum_{k=-\infty}^{+\infty} \underbrace{(g_i h_{\tau_i}(t) * x(t - t_i) + o_i)}_{\hat{x}_i} \cdot \underbrace{\delta(t - (kM + i)T)}_{s_i}. \quad (2.7)$$

where \hat{x}_i is exactly the i -th channel including all errors, when s_i is a train of Dirac pulses. Consequently, the output spectrum is obtained by calculating the spectrum of each \hat{x}_i and s_i as follows :

$$S_i(e^{j\omega}) = \frac{2\pi}{MT} \sum_{k=-\infty}^{+\infty} \delta(\omega - k \frac{\omega_s}{M}) e^{-jki \frac{2\pi}{M}}. \quad (2.8)$$

and

$$\hat{X}_i(j\omega) = \underbrace{g_i}_{\text{Gain}} \underbrace{e^{-j\omega t_i}}_{\text{Timingskew}} \underbrace{H_i(j\omega)}_{\text{Bandwidth}} X(j\omega) + \underbrace{o_i \delta(\omega)}_{\text{Offset}}. \quad (2.9)$$

The overall output spectrum Y can then be expressed as

$$Y(e^{j\omega}) = \sum_{i=0}^{M-1} \frac{1}{2\pi} \hat{X}_i(j\omega) S_i(e^{j\omega}). \quad (2.10)$$

By including 2.9 and 2.8 into 2.10, one obtains

$$Y(e^{j\omega}) = \sum_{i=0}^{M-1} \sum_{k=-\infty}^{+\infty} \frac{1}{MT} [g_i H_i(j\omega) X(j\omega) e^{-j\omega t_i} + o_i \delta(\omega)] * \delta(\omega - k \frac{\omega_s}{M}) e^{-jki \frac{2\pi}{M}}. \quad (2.11)$$

Taking into account the following properties of the Dirac pulse :

$$\begin{cases} X(\omega) * \delta(\omega - \omega_0) = X(\omega - \omega_0) \\ X(\omega) \delta(\omega - \omega_0) = X(\omega_0) \delta(\omega - \omega_0). \end{cases} \quad (2.12)$$

Then the overall output spectrum of the TI-ADC including all the errors : offset, gain, timing skew and bandwidth mismatch errors is expressed as :

$$\begin{aligned} Y(e^{j\omega}) = & \frac{1}{T} \sum_{k=-\infty}^{+\infty} \left[\frac{1}{M} \sum_{i=0}^{M-1} g_i H_i(j(\omega - k \frac{\omega_s}{M})) e^{-j(\omega - k \frac{\omega_s}{M}) t_i} \cdot e^{-jki \frac{2\pi}{M}} \right] X(j(\omega - k \frac{\omega_s}{M})) \\ & + \frac{1}{T} \sum_{k=-\infty}^{+\infty} \frac{1}{M} \sum_{i=0}^{M-1} o_i e^{-jki \frac{2\pi}{M}} \delta(\omega - k \frac{\omega_s}{M}). \end{aligned} \quad (2.13)$$

This expression shows that, in the presence of all the errors, the input signal is modulated by the expression between brackets which combines gain, bandwidth and timing mismatch errors. These errors appear at each $\pm\omega_{\text{in}} + k\frac{\omega_s}{M}$ frequency, where ω_{in} is the input frequency. Additionally, the offset mismatch tones intervene as signal independent spurious tones at each $k\frac{\omega_s}{M}$. This is illustrated for two and four channels in fig. 2.4.

In the following parts, the effect of each error on the output spectrum is described se-

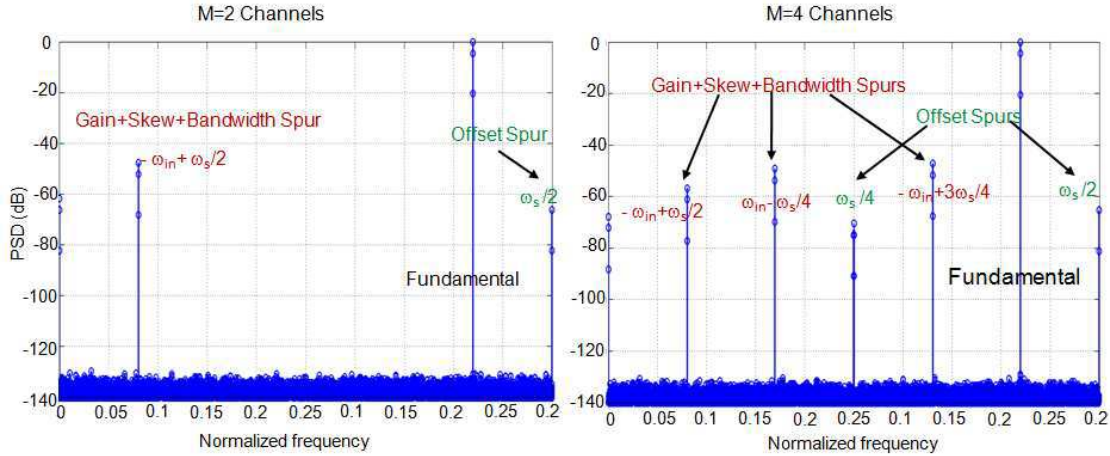


FIGURE 2.4 – Output spectrum including mismatch errors : offset, gain, skew and bandwidth for a 2 and 4 channels ADC

parately. We suppose for each error that other characteristics are identical. Moreover, a performance evaluation is done in each case. The global SFDR including all errors is the worse case among the SFDR degradation caused by offset error and the SFDR value calculated in the presence of the combined errors ; gain, timing skew and bandwidth mismatch error. This latest one is discussed at the end of this chapter.

2.3 Impact of the mismatch errors

2.3.1 Offset mismatch

Channel offset error causes fixed pattern noise in a ADC system. Each output code is shifted by the offset value from the initial code as shown in Chap. 3. The noise pattern is independent of the input signal in time and frequency domains.

By considering only offset error in Equation 2.3 ; (ie. $g_i = 0, t_i = 0$ and $h(t) = \delta(t)$), the i -th channel expression shows that the offset error is additive in the time domain :

$$y_i[k] = x((kM + i)T) + o_i. \quad (2.14)$$

Equation 2.6 leads to a global output expression

$$y(t) = x(t) + \sum_{i=0}^{M-1} \sum_{k=-\infty}^{+\infty} o_i \delta(t - (kM + i)T). \quad (2.15)$$

One can note the independence of the offset error from the input signal. This impact can also be observed in the frequency domain where Equation 2.13 is expressed as

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} X(j(\omega - k\frac{\omega_s}{M})) \left[\frac{1}{M} \sum_{i=0}^{M-1} e^{-jki\frac{2\pi}{M}} \right] \quad (2.16)$$

$$+ \frac{1}{T} \sum_{k=-\infty}^{+\infty} \frac{1}{M} \sum_{i=0}^{M-1} o_i e^{-jki\frac{2\pi}{M}} \delta(\omega - k\frac{\omega_s}{M}). \quad (2.17)$$

The term that multiplies the input signal can be reduced as :

$$\frac{1}{M} \sum_{i=0}^{M-1} e^{-jki\frac{2\pi}{M}} = \begin{cases} 1 & \text{if } k = 0[M] \\ 0 & \text{otherwise} \end{cases} \quad (2.18)$$

So that Equation 2.16 becomes :

$$Y(e^{j\omega}) \frac{1}{T} \sum_{k=-\infty}^{+\infty} X(j(\omega - k\omega_s)) + \underbrace{\frac{1}{T} \sum_{k=-\infty}^{+\infty} \frac{1}{M} \sum_{i=0}^{M-1} o_i e^{-jki\frac{2\pi}{M}} \delta(\omega - k\frac{\omega_s}{M})}_{A_{\text{offset}}} \quad (2.19)$$

From this equation, the so-called spurious tones appear at a multiple of ω_s/M .

It is important to notice that the spectrum is periodic. We focus on one period to show the impact of the offset mismatch error ; ie ; $-\pi < \omega_{in}T < \pi$.

For a 2 channels model, A_{offset} can then be expressed as :

$$A_{\text{offset}} = \frac{1}{2T}(o_0 + o_1)\delta(\omega) + \frac{1}{2T}(o_0 - o_1)\{\delta(\omega - \frac{\omega_s}{2}) + \delta(\omega + \frac{\omega_s}{2})\} \quad (2.20)$$

The impact of the offset mismatch error is illustrated for a sine wave input signal in Fig.

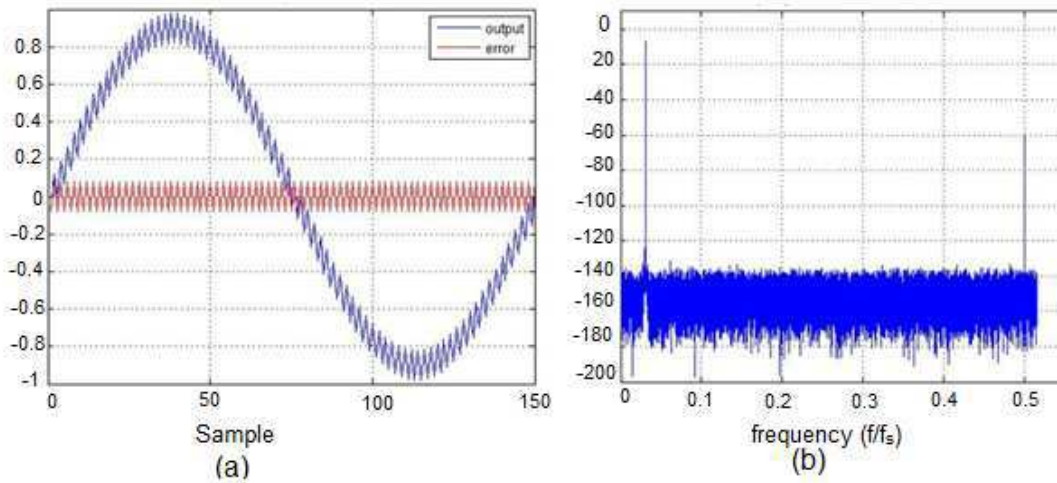


FIGURE 2.5 – Offset error impact on the 2 channels TI-ADC output in (a) time domain and (b) frequency domain.

2.5. Fig. 2.5 (a) represents the offset error in time domain. One can note the constant value

of the error. In Fig. 2.5 (b), the spectrum shows the additional tones at $\omega_s/2$. The DC in this case is a mean value of the two offset errors as explained previously. Consequently, the mismatch degrades the performance of the overall converter in terms of total noise power including distortion tones. This error is independent of the input signal which leads to a SFDR and SNDR constant regardless of the input frequency and the amplitude of the input signal.

2.3.2 Gain mismatch

Gain error in a channel appears as an angular deviation of the in/out characteristic from the ideal one as shown in Chap. 3. Gain error mainly results from OTA non-idealities and capacitors mismatch of the switched capacitor circuitry. This error is considered as constant since it depends on the circuit itself independently from the input signal. In a time-interleaved architecture, gain mismatch consists of the difference between the channels gain errors. If we consider that only gain error is present in the i -th channel and ignore the other contributions; (ie $o_i = 0, t_i = 0$ and $h_{\tau_i}(t) = \delta(t)$). Equation 2.3 becomes :

$$y(t) = \sum_{i=0}^{M-1} y_i(t) = \sum_{i=0}^{M-1} \sum_{k=-\infty}^{+\infty} g_i x(t) \delta(t - (kM + i)T). \quad (2.21)$$

This equation shows that the signal is modulated by the combination of the channels gain errors. As a consequence of this mismatch, undesired spurious tones appear in the spectrum dependently of the input frequency, and hence degrade the linearity performance. In fact, Equation 2.22 below, shows that the additional tones are present at each $\pm\omega_{in} + k\frac{\omega_s}{M}$ modulating the input signal. The wanted input signal is obtained for $k = 0$ which is multiplied by the mean value of all gain errors so that if the channels are perfectly matched, only the gain of one channel at this frequency will be observed.

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} \left[\frac{1}{M} \sum_{i=0}^{M-1} g_i e^{-jk\frac{2\pi}{M}} \right] X(j(\omega - k\frac{\omega_s}{M})). \quad (2.22)$$

Figure 2.6 illustrates the example of 2 channel TI-ADC with sine wave input in the presence of gain mismatch. One can note the modulated error in the time domain (Fig. 2.6. (a)), when Fig. 2.6. (b) shows additional tones in the spectrum. The degradation of the SFDR for 2 channels TI-ADC due to gain mismatch is obtain by considering a band limited input signal $X(\omega)$ where $-\pi < \omega_{in}T < \pi$ for a sine wave input. Equation 2.22 gives :

$$\begin{aligned} Y(e^{j\omega}) &= \frac{1}{2T} \underbrace{[g_0 + g_1]}_{\text{Input gain}} X(j\omega) \\ &+ \frac{1}{2T} \underbrace{[g_0 - g_1]}_{\text{spur gain}} \left\{ \delta(j(\omega - \frac{\omega_s}{2})) + \delta(j(\omega + \frac{\omega_s}{2})) \right\}. \end{aligned} \quad (2.23)$$

which leads to :

$$\text{SFDR(dB)} = -20\text{Log}_{10} \left(\frac{g_0 - g_1}{g_0 + g_1} \right). \quad (2.24)$$

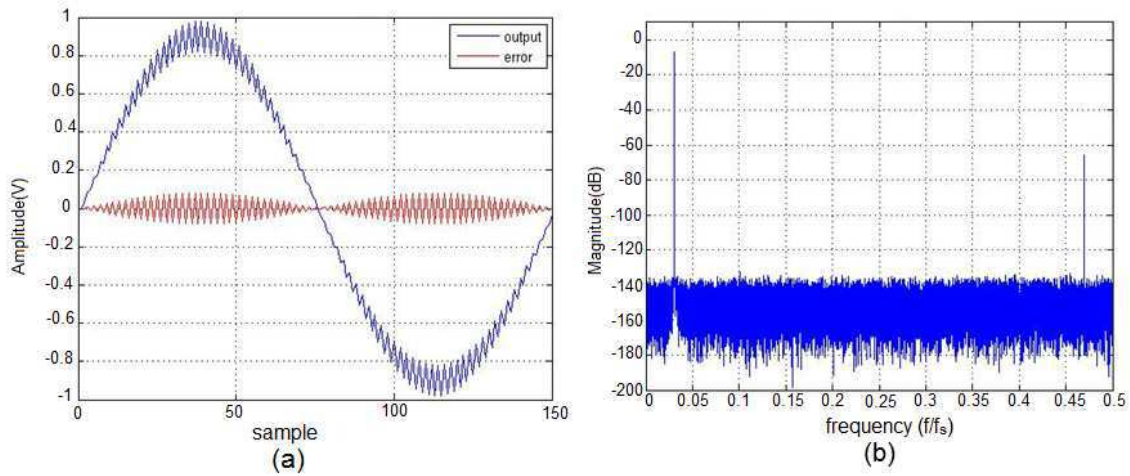


FIGURE 2.6 – Gain error mismatch on the output in time and frequency domain.

Fig. 2.7 shows that the required resolution to achieve 100 dB of SFDR is about 0.002%. Moreover, it is important to notice that the SFDR is independent of the input signal amplitude frequency and therefore can be treated easily.

Finally, depending on the resolution we can reach when compensating the gain, it is recommended to target less than 0.001% corresponding to an SFDR of 100 dB in order to have a sufficient margin of global error compensation.

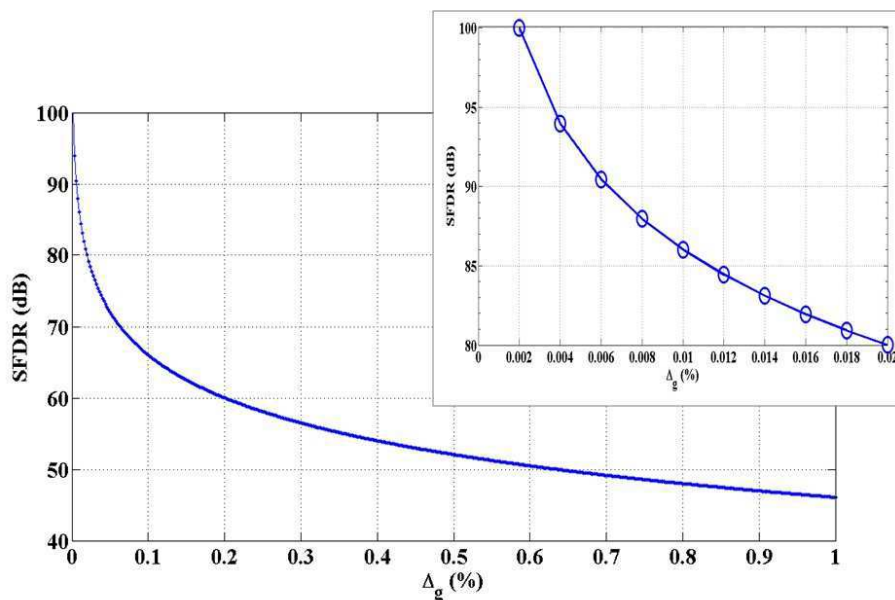


FIGURE 2.7 – SFDR versus gain mismatch error

Static gain mismatch quantification :

The predominant contributor of the gain mismatch error is the difference between the references of the channels in the TI-ADC. A channel reference is responsible of the dynamic

range of the ADC output which needs to be the same between all the channels. In order to realize the gain error value and the impact of the gain mismatch on the circuit, a Monte Carlo simulation has been done on a 2 channel TI-ADC. 500 runs have been realized ignoring the process variation which is supposed to be the same for the two channels. VDD is set to 1.8V and the input impedance is equal to 0 Ohm, which has no effect on the reference variation. The temperature is 25°C and the common mode is shared and equal to 0.9V.

The result of the simulation illustrated in Fig. 2.8, shows that the gain mismatch is about 0.88% for 1σ . At the end, the gain error due to references mismatch is about 2.64% which is impractical and therefore needs to be compensated.

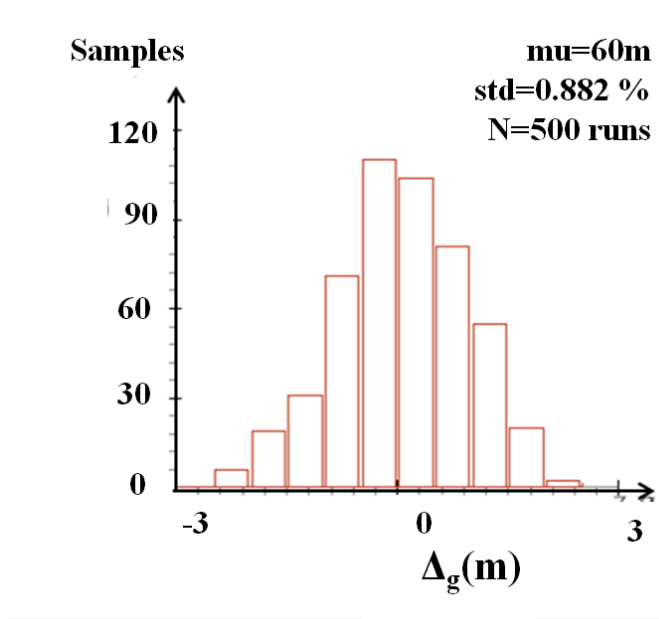


FIGURE 2.8 – Gain distribution of the two channels imposed by references' variations

This one can be avoided by sharing the same reference between the channels. The remaining error can be considered as an individual static gain error and does not generate additional spurious tones. We will expose at the end of this chapter how this error impact the bandwidth error extraction which is the target of our work.

2.3.3 Clock skew mismatch

Clock skew also called timing skew, phase skew or sample-time error is a static deviation of the clock signal from the one generated by the clock circuit. This can be caused by many contributors such as wire-interconnect length, temperature variation, gate propagation delay deviations, capacitive coupling and differences in input switch capacitors. In a time-interleaved architecture, each channel is delayed differently due the process and environment variations and consequently this creates mismatch error at the overall output. In addition, the jitter which is the phase noise of the clock can be seen as a Gaussian distribution of the sampling instants as shown in Fig. 2.9 [20].

In order to illustrate the impact of the clock skew mismatch on the performances of the

TI-ADC, we ignore the other mismatch errors and suppose that the i -th channel clock is deviated by t_i from the $(kM + i)T$ time instant which is expressed as :

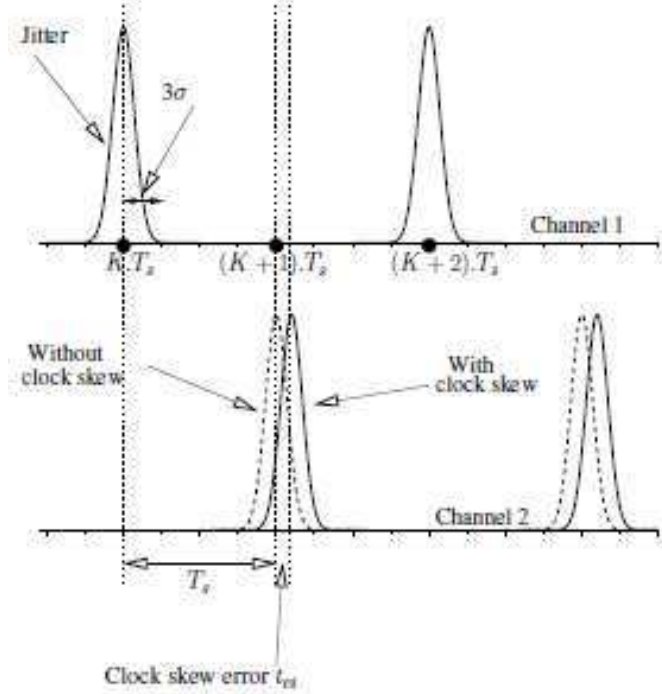


FIGURE 2.9 – SFDR Performance versus skew error

$$y_i[k] = x((kM + i)T - t_i). \quad (2.25)$$

Thus, the overall digital output formulation is :

$$\begin{aligned} y(t) &= \sum_{i=0}^{M-1} y_i(t) \\ &= \sum_{i=0}^{M-1} \sum_{k=-\infty}^{+\infty} x(t - t_i) \delta(t - (kM + i)T). \end{aligned} \quad (2.26)$$

The clock skew intervenes in the phase of the signal and the mismatch error appears in the output as a phase modulation. This can be observed through the following frequency transform. Undesired additional tones are generated by the mismatch error at each $\pm\omega_{in} + k\frac{\omega_s}{M}$ degrading the linearity performances of the TI-ADC, SFDR and therefore SNDR. Fig. 2.10 shows the impact of the skew error in the time and frequency domains. In fact, it is shown in Fig. 2.10 (a) that the skew causes noise in the ADC system, and in the time domain the largest error occurs when the input signal has the largest slew rate, or crosses zero which corresponds to a phase modulation (PM) noise. Hence, the envelope of the error signal is larger at the zero-crossings with a period of M/fs ; where M is the number of channels and fs is the sampling frequency. In the frequency domain, as with the gain mismatch case, the basic error occurs at $\pm\omega_{in} + k\frac{\omega_s}{M}$ (Fig. 2.10 (b)). Therefore, in the

presence of the timing mismatches, the output spectrum becomes :

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} \left[\frac{1}{M} \sum_{i=0}^{M-1} e^{-j(\omega - k\frac{\omega_s}{M})t_i} e^{-jk\frac{2\pi}{M}} \right] X(j(\omega - k\frac{\omega_s}{M})). \quad (2.27)$$

The degradation of the SFDR due to the clock skew mismatch error is obtained by consi-

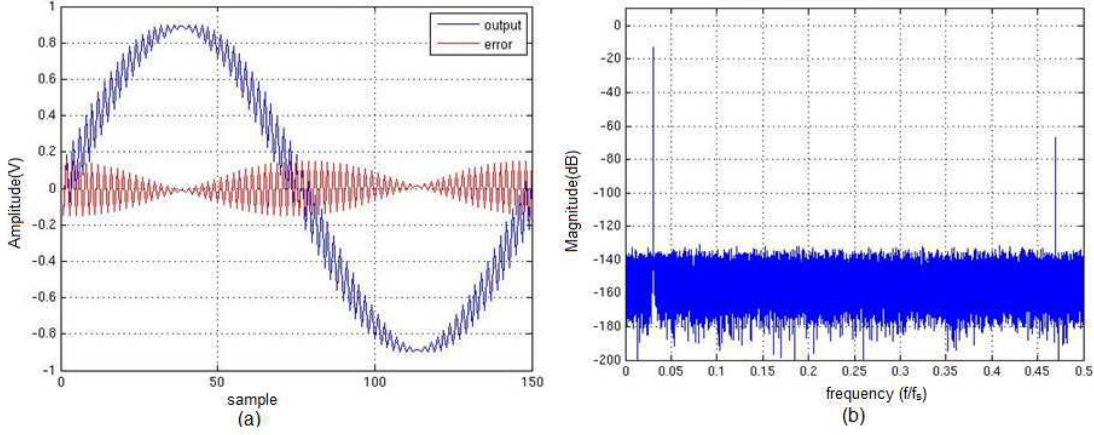


FIGURE 2.10 – Clock skew error on the output in time and frequency domain.

dering a bandlimited input signal $X(\omega)$, where $-\pi < \omega_{in}T < \pi$ for a sine wave input ($k \in \{0; 1\}$), equation 2.27 gives :

$$\begin{aligned} Y(e^{j\omega}) = & \frac{1}{2T} [e^{-j\omega t_0} + e^{-j\omega t_1}] X(j\omega) \\ & + \frac{1}{2T} [e^{-j(\omega - \frac{\omega_s}{M})t_0} - e^{-j(\omega - \frac{\omega_s}{M})t_1}] \delta(j(\omega - \frac{\omega_s}{2})) \\ & + \frac{1}{2T} [e^{-j(\omega + \frac{\omega_s}{M})t_0} - e^{-j(\omega + \frac{\omega_s}{M})t_1}] \delta(j(\omega + \frac{\omega_s}{2})). \end{aligned} \quad (2.28)$$

By assuming that the timing mismatch error is small, The SFDR can be expressed as :

$$\text{SFDR(dB)} = -20 \text{Log}_{10} \left[\frac{\omega_{in}}{2} (t_0 - t_1) \right] \quad (2.29)$$

Fig. 2.11 shows the variation of the SFDR in function of the input frequency versus the clock skew. One can note that a SFDR of 90dB can be achieved with a skew resolution of 20 fs up to 500 MHz of input frequency when the error can reach 60 ps using different dies. Nevertheless, a design effort can be made in order to control the clock skew before any calibration (less than 400 fs by design [67]). Much work have been done to compensate the skew error. However, there is no solution which is fully independent of the other errors, especially bandwidth mismatch error. In fact, we will see in the following that bandwidth mismatch error impacts the background calibration of the skew, which makes the existing solutions not usable.

2.3.4 Bandwidth mismatch

In switched capacitors ADCs, the input network behaves as a RC circuit during the sampling phase. In fact, when the switch is "on", it operates as a small on-resistance which

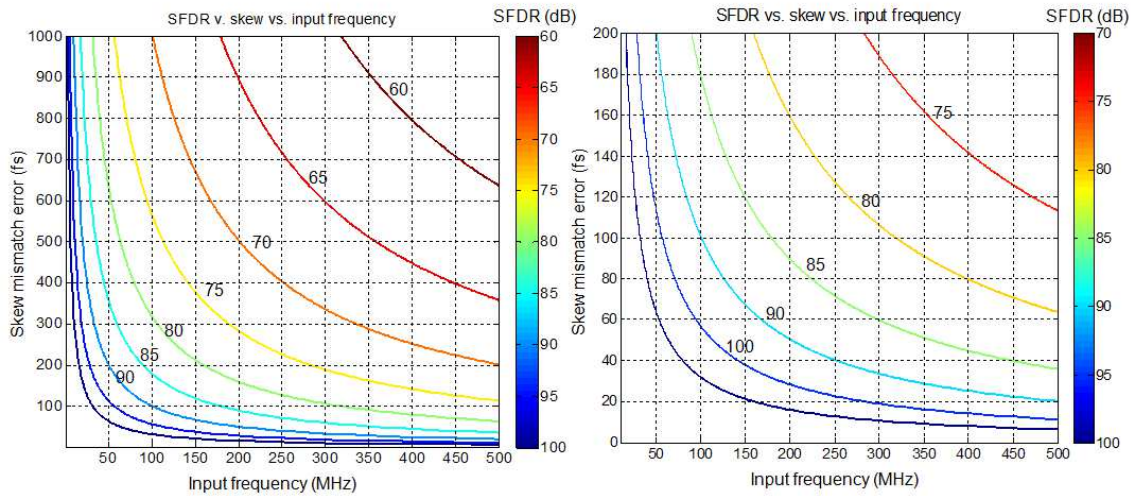


FIGURE 2.11 – SFDR Performance versus skew error.

have to be low enough to minimize the settling time [20] over the time constant. Fig 2.12 shows the input sampling network and its equivalent low-pass RC filter. R_i denotes the equivalent on-resistance of the i -th channels switches. At the end, the time constant of the filter is $\tau_i = R_i C_i$. It is relevant to notice that the input filter causes an attenuation of the input signal especially at high frequencies.

To simplify the analysis, it is assumed that the resistance of the MOS switch is constant,

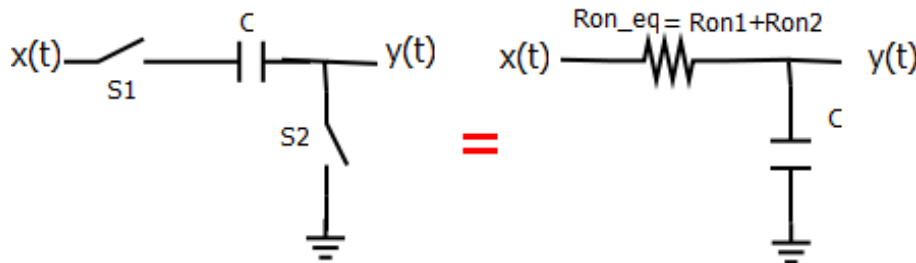


FIGURE 2.12 – Sampling network and its equivalent low pass filter when the switches are *On*.

which in practice may not be true. Indeed, since the source voltage of the switch is signal dependent, the resistance R is signal dependent as well and thus introduces nonlinear distortion in the output spectrum. Yet such nonlinearities may be minimized by using CMOS switches or by employing bootstrapping techniques [20]. Therefore, we can assume that the resistance is approximately constant since we can deal with the varying resistance problem without affecting the Sample and Hold RC model.

According to this, the input filter of the i -th channel can be described by the following equation :

$$x(t) = y_i(t) + \tau_i \frac{dy_i(t)}{dt}. \quad (2.30)$$

The output of the ADC can then be expressed as :

$$y_i(t) = h_i(t) * x(t). \quad (2.31)$$

where h_i is the impulse response of the continuous time input filter and $y_i(t)$ represents the continuous representation of the discrete time output signal. In Appendix A, measurements evaluate the order of the filter. For convenience, we first assume a first order input filter for each ADC. The transfer function of the i -th channel input can then be written as :

$$H_i(j\omega) = \frac{1}{1 + j\omega\tau_i} \quad (2.32)$$

$$= \frac{1}{\sqrt{1 + (\omega\tau_i)^2}} \angle -\arctan(\omega\tau_i). \quad (2.33)$$

In a time-interleaved architecture, the value of R and C may differ from a sampling network to the other due to imperfections in the IC manufacturing process. Therefore, this creates the so-called bandwidth mismatch error which impacts the gain and the phase of the signal and consequently degrades the linearity of the overall converter.

In order to highlight the effect of the bandwidth mismatch at the output spectrum and show the impact of this error on the performances, let us first ignore the other errors : offset, gain and timing skew. We will include these latter afterwards to budget the overall performance degradation.

From Equation 2.6, the TI-ADC output can then be expressed as :

$$y(t) = \sum_{i=0}^{M-1} y_i(t) = \sum_{i=0}^{M-1} \sum_{k=-\infty}^{+\infty} h_{\tau_i}(t) * x(t) \delta(t - (kM + i)T) \quad (2.34)$$

The impact of the bandwidth mismatch error on output spectrum is given by :

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} \underbrace{\left[\frac{1}{M} \sum_{i=0}^{M-1} H_i(j(\omega - k\frac{\omega_s}{M})) e^{-jki\frac{2\pi}{M}} \right]}_{\text{Bandwidth mismatch}} X(j(\omega - k\frac{\omega_s}{M})) \quad (2.35)$$

The equation shows that the bandwidth mismatch creates undesired additional spurious tones at each $\pm\omega_{in} + k\frac{\omega_s}{2}$ where the signal is affected both in gain and phase. Moreover, these latter depend on the input frequency. The error impact is shown in Fig. 2.13 for a two channels and a sine wave input where Fig. 2.13 (a) illustrates the attenuation caused by the input filters for each channel and shows that the mismatch error causes the shift in phase and gain. Fig. 2.13 (b) represents the output spectrum with the additional tone. In order to illustrate the impact of the bandwidth mismatch and estimate the resolution needed to achieve the specifications, the analytic expression of the SFDR for a two channels ADC is given by :

$$\text{SFDR} = -20\text{Log}_{10} \left[\frac{H_0(j\omega) - H_1(j\omega)}{H_0(j\omega) + H_1(j\omega)} \right]. \quad (2.36)$$

It has been evaluated in function of the input frequency, versus the bandwidth mismatch, see Fig. 2.14. The SFDR decreases for higher input frequency and obviously for higher bandwidth mismatch as well.

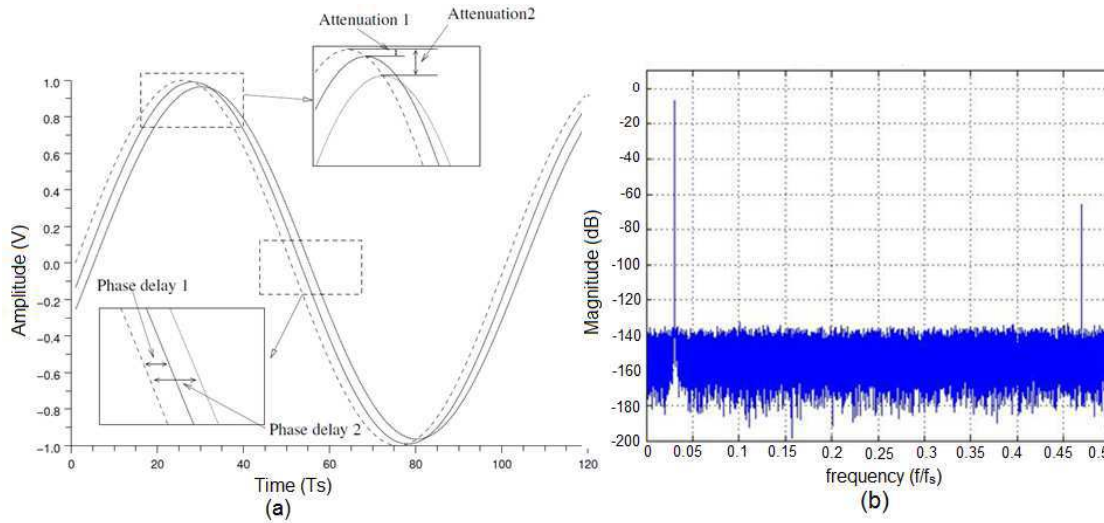


FIGURE 2.13 – Impact of the bandwidth mismatch error on the output in time and frequency domains

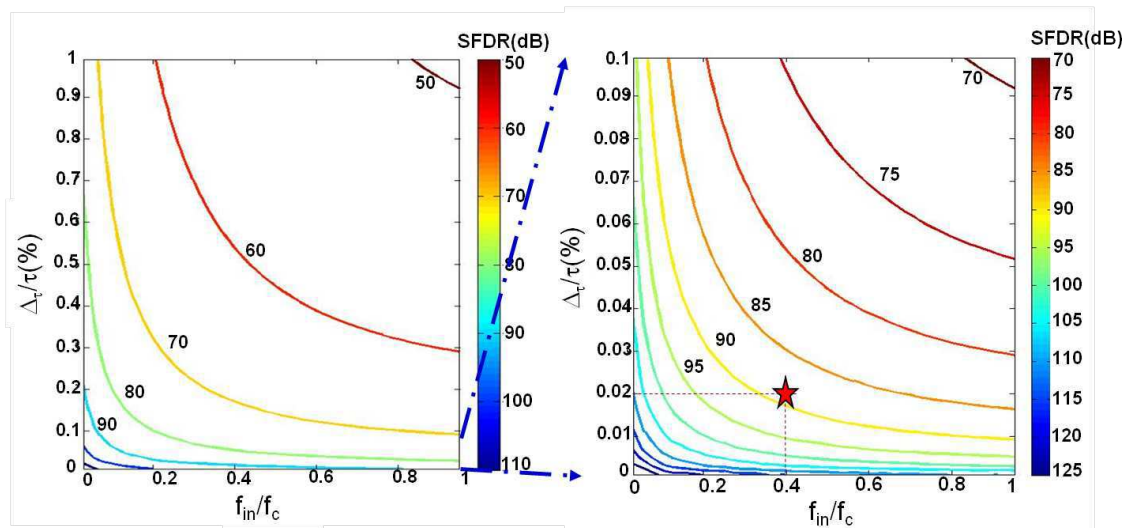


FIGURE 2.14 – SFDR Performance versus bandwidth mismatch error.

Bandwidth mismatch quantification :

An circuit simulation has been done by first neglecting the input impedance (Fig. 2.15) in order to evaluate the bandwidth mismatch between two sampling networks. A 500 Monte Carlo mismatch runs show that error is about 0.8% in the good conditions (distance between the circuits is supposed zero) which is impractical and proves the necessity to compensate this error to obtain the good performances. In Fig. 2.14, a SFDR of 94 dB is reached for very low frequencies where the mismatch is not visible. However, the aimed applications consider higher input frequencies, up to 375MHz which corresponds to an ω_{in}/ω_c equal to 0.4. In fact, by taking into account the input impedance of 50 Ohms, the average input bandwidth is approximatively 1.1 GHz as shown in Appendix A. Consequently, in order to reach a SFDR of 94 dB, the bandwidth mismatch error needs to be less than 0.02%.

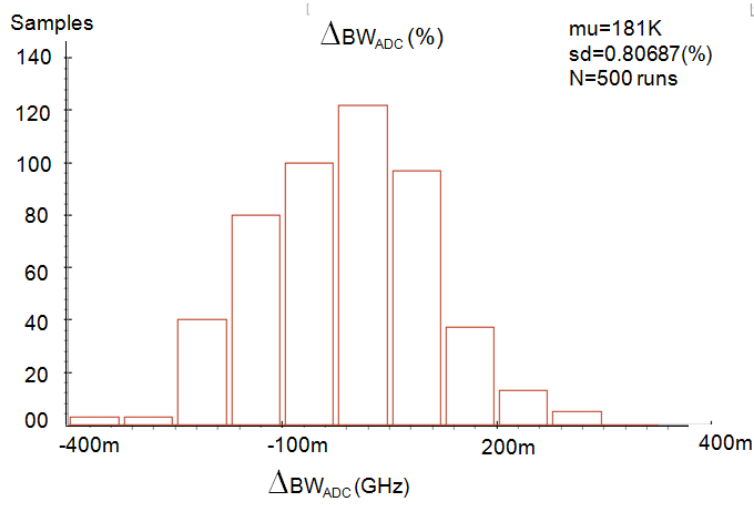


FIGURE 2.15 – Simulated Bandwidth distributions and mismatch quantification between two channels.

2.4 Overall Performance limitations

In this section, we evaluate the performance degradation including all the errors in order to point out how the compensation of the bandwidth mismatch is highly recommended.

The degradation of the SFDR, which is the highest undesired tone relative to the fundamental tone, can be calculated as the maximal tone level among the offset one; which appears at each $k\frac{\omega_s}{M}$ and the combined errors : gain, skew and bandwidth mismatch errors located at each $\pm\omega_{in} + k\frac{\omega_s}{M}$. where ω_{in} is the input frequency and k , an integer. Several works have addressed the problem of offset error which is easy to compensate because of the input independency of the error. Let us now consider the remaining errors assuming that the offset is corrected. At the end, the SFDR is expressed as :

$$\text{SFDR}(\text{dB}) = -20\text{Log}_{10} \left[\frac{g_0 e^{j(\omega)t_0} H_0(j(\omega)) - g_1 e^{j(\omega)t_1} H_1(j(\omega))}{g_0 e^{j\omega t_0} H_0(j\omega) + g_1 e^{j\omega t_1} H_1(j\omega)} \right]. \quad (2.37)$$

In [67], authors evaluated the timing skew by measurements for 400 fs for a 65 nm CMOS process. This represents 0.02% compared to the sampling frequency of 500 Msps. According to Fig. 2.11, this error leads to a SFDR below 66 dB for an input frequency of 375 MHz. Moreover, it has been shown in Fig. 2.8, that the gain mismatch is at least 2.6% which leads to a SFDR lower than 40 dB (Equation. 2.24). Finally, the bandwidth mismatch is approximately 1%, evaluated in good conditions, leading to a SFDR lower than 50 dB for the aimed application as shown in Fig. 2.14. It is important to notice that the degradations above are evaluated for separate errors.

Tab. 2.1 summarizes the SFDR regarding each contribution separately and then by taking into account all the errors obtained by using Equation 2.37. It is clear that these errors levels need to be reduced to improve the linearity.

Static gain and Clock skew errors have been treated in several works. The improvement of the clock skew error can nowadays reach 20 fs [67], which corresponds to a SFDR of 92 dB if no other error is present. In Fig 2.16 (a), the SFDR is evaluated in function of the gain

	Gain error (1%)	Skew error (0.02%)	Bandwidth error (1%)	Global error
SFDR (dB)	46	66	50	46.3

TABLE 2.1 – SFDR for separate errors and a global impact of the mismatch errors

and the bandwidth mismatch errors for a such timing skew correction. Regarding the gain, many works treat the compensation of this static error up to 0.002% of accuracy [67]. The SFDR is therefore equal to 100 dB which is reasonable. If we consider that only the gain is compensated at this resolution level, the improvement of the SFDR is then evaluated in function of the two remaining errors as illustrated in Fig. 2.16 (b).

It is usual to compensate the gain before the skew because of the dependency of the extrac-

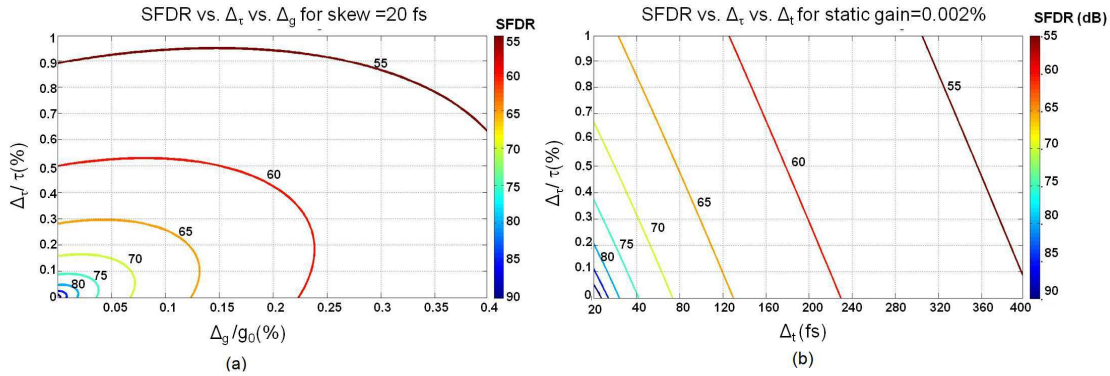


FIGURE 2.16 – SFDR Performance versus bandwidth mismatch error for (a) different static gain errors (b) different skew errors.

tion of the skew in the presence of the static gain [68]. Finally, the remaining bandwidth mismatch error degrades considerably the SFDR as it can be shown in Fig 2.17, where a compensation resolution of 0.02% leads to a SFDR of 85 dB instead of 94 dB as shown in Fig. 2.14.

Unfortunately, few works have addressed the problem of bandwidth mismatch due to the nonlinear characteristic and the input dependency. In the remaining of this document, we will focus on the compensation of this error in order to achieve the targeted SFDR performance. To do so, some techniques are proposed and then compared to what is done in the literature.

Finally, according to the compensation values described previously, the SFDR is summed up in Tab. 2.2 where the resolution of the bandwidth mismatch error needs to be less than 0.02% to reach the aimed SFDR.

2.5 Chapter Conclusion

In this chapter, we have described the errors responsible of the degradation of the TI-ADC linearity, characterized by the SFDR. Analytic expressions were exposed in time and

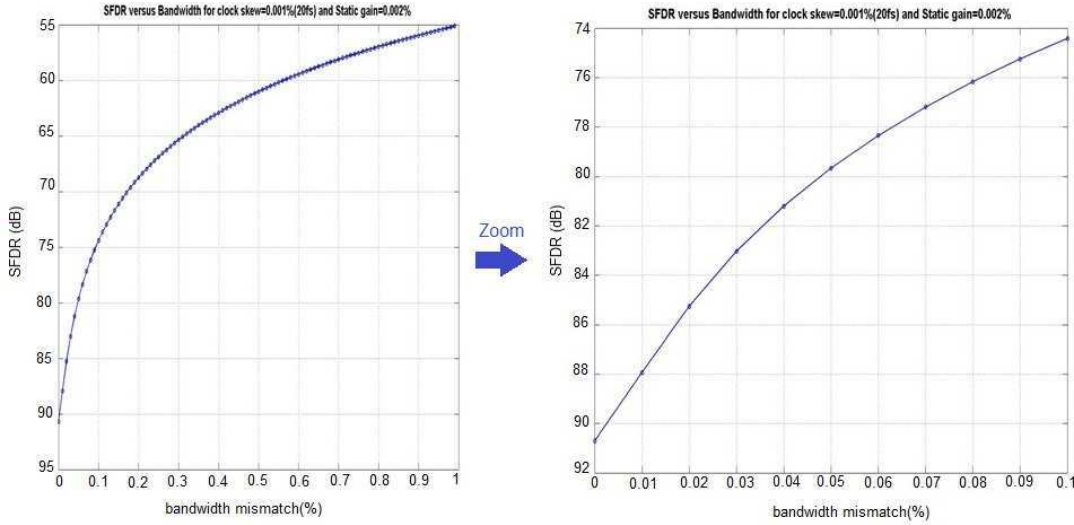


FIGURE 2.17 – SFDR Performance versus bandwidth mismatch error for a gain error=0.002% and a skew error = 20fs.

	Gain error (0.002%)	Skew error (0.001%)	Bandwidth error (aimed 0.02%)	Global error Global error
SFDR (dB)	100	92	94	88

TABLE 2.2 – SFDR including compensated errors : gain and clock skew. The bandwidth mismatch is remaining and needs to be corrected.

frequency domains to illustrate the impact of offset, gain, timing skew and the bandwidth mismatch on the TI-ADC output signal. Offset error is an additive error which creates undesired tones at each ω_s/M regardless the input frequency and hence can be dealt with easily. Regarding the remaining errors, amplitude and phase modulation occur which generate undesired spurious tones on the output spectrum dependently of the input frequency at each $\pm\omega_{in} + k\omega_s/M$. An evaluation of the SFDR by considering separate errors was been presented. It has been shown that by combining these latest errors, the SFDR is about 46 dB. By considering recent circuits, treating the gain and timing skew, the resolution of the bandwidth mismatch is highly challenged to be reach the targeted SFDR of 94 dB. This error is difficult to deal with because of its non linear dependency with the input frequency. Moreover, most of the existing works that treat the bandwidth mismatch error suppose the error already extracted. Very few techniques have been proposed to estimate this error due to the impact of other errors on its extraction. In the following chapters, we will focus on the bandwidth mismatch error compensation by first expose an analog solution that minimize its effect without any correction thanks to sampling randomization. After that, existing correction methods are presented and compared. Then, the two existing methods for error estimation are detailed to finally expose a proposed method of bandwidth mismatch error extraction in Chapter 4.

Chapitre 3

Bandwidth Mismatch Error Calibration

Up to date, only few works have treated the problem of bandwidth mismatch in the literature. This can be explained in one hand by the fact that this problem appeared recently because of very wideband applications such as base station. In the other hand, it has been shown in Section 2.3.4, that this mismatch causes frequency dependent, non linear gain and phase errors which make its compensation difficult to accomplish. Moreover, it is important to notice that we are focusing in our work on online error calibration preferred to the foreground techniques so that the ADC is not stopped during the calibration.

In this chapter we discuss the different classifications of bandwidth mismatch calibration techniques. In general, we are not interested in compensating mismatch errors but in reducing their impact on a particular figure of merit. This is usually achieved by sample randomization technique introduced in [1, 10, 6] targeting to improve the SFDR without degrading the SNDR. This approach will be discussed in Section 3.1 where a new implementation is proposed to overcome the problems of the existing randomization techniques. Another class of calibration aims to cancel the mismatch error by filtering. To do so, digital error identification is essential to evaluate the estimate of the mismatch error. In fact, if the identified parameter is inaccurately estimated, even the best reconstruction algorithms cannot improve the ADC performance. Unfortunately, very few methods have been proposed to estimate the bandwidth mismatch. One can mention the so-called semi blind estimation technique in [18] and the technique proposed in [69] based on polynomial approximation. This will be detailed in Section 2 where their limitations are highlighted. Then, at the end of this section, a solution based on autocorrelation is used to discuss the choice of the loss function used to extract the mismatch error. Once the mismatch identification is done, correction is performed using the extracted error. We will expose in Section 3.2.2, a comparison between the existing correction methods and show the advantage of using one of these techniques to validate the proposed extraction method in Chapter 4.

3.1 Random Sampling Technique

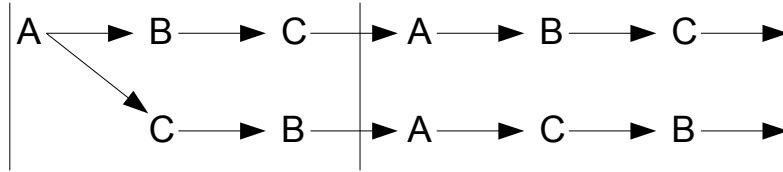
Mismatch error in a time-interleaved architecture is caused by cyclic patterns such as gain, timing and bandwidth contributions which lead to the generation of additional spurious tones in the output spectrum. In order to reduce this cyclic characteristic, channel

randomization can be performed [1, 70]. It basically consists of spreading the spurious tones over the bandwidth by randomizing the ADC channels without violating the time-interleaved constraints.

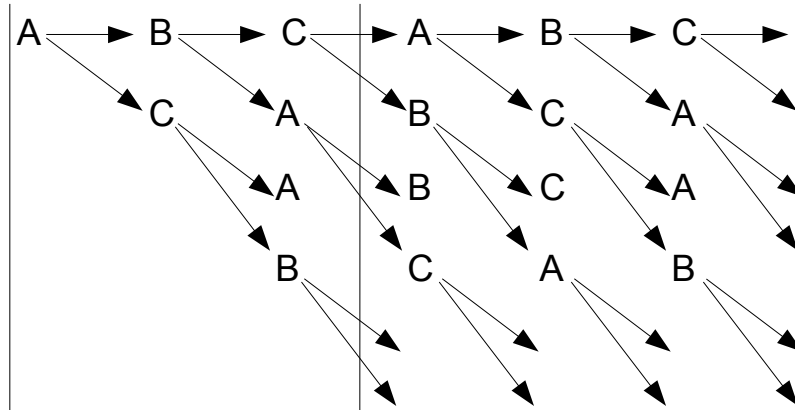
3.1.1 Literature review

In [71], a randomization method without adding ADCs has been proposed. It consists on delaying M samples from the input signal and randomizing their distributions between the M channels of the TI-ADC using an analog swap circuit. To do this, the architecture needs M analog interfaces to hold the samples at the input of the ADC channels, which add imperfections to the ADCs. This complexity was reduced in [72], where only one delay at the input is required to randomize the spurious components. The inconvenient of this method, as the one in [71], is that the added analog circuits undergo leakage of the held values and hence worsen the mismatches between the ADC channels. Consequently it increases the non-linearity of the real implementation.

Finally, an easy way to perform the randomization consists of adding at least one ADC to the effective TI architecture [70]. In the following, we consider R additional ADCs to the M existing ones. Each of the $M+R$ channels operates at ω_s/M sampling frequency so that at each time instant, one can chose among $R+1$ channels and afterwards, the TI-ADC samples are reconstructed after each M time instants.



(a) No additional ADC



(a) Single additional ADC

FIGURE 3.1 – Channel random sequence. (a)without additional ADC ($M=3$, $R=0$), (b)with additional channel ($M=2$, $R=1$)

Fig. 3.1 shows how randomization can be performed with respect to the time-interleaved architecture. It can be observed in Fig. 3.1 (a), that randomization cannot be achieved without additional converters. In fact, with three ADCs, the cyclic sequence $A \rightarrow B \rightarrow C$ or $A \rightarrow C \rightarrow B$ still appears in the way that the random characteristic is not respected. In Fig. 3.1 (b), a single ADC C ($R=1$) is added to a double sampling A B channels so that at each selection of the next ADC, there are always two available candidates. Based on this, different channels can be chosen to illustrate the random characteristic without affecting the time-interleaved behavior.

As a result of this randomization, the distortion tones due to mismatch errors are completely converted to random noise which improves considerably the SFDR. This is shown in Fig. 3.2, where a 12-bit time-interleaved ADC is considered. All errors are present in this example, the static gain mismatch is set to 0.1%, timing skew is 0.01% of the sample and bandwidth mismatch is about 0.1%.

The inconvenient of adding an entire channel is the increasing of the die area and hence increasing the consumption. To deal with this latter inconvenient, our proposed solution consists of achieving the random sampling by adding, not an entire channel but, only one or more samplers. This is detailed in the following.

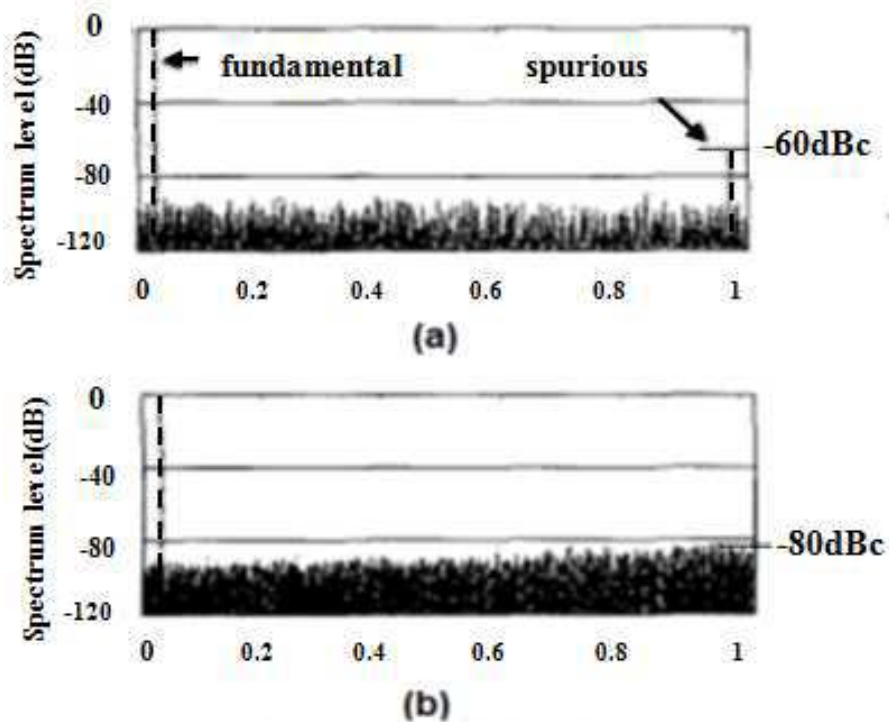


FIGURE 3.2 – TI-ADC with $M=2$, $R=1$, (a) before randomization, (b) after randomization. Spurs are spread over the bandwidth.

3.1.2 The proposed randomization technique using additional samplers

3.1.2.1 Concept

Let us consider a M -channel time-interleaved converter with R additional samplers. The m -th sample provided by one of the $R+1$ available samplers is sent to the m -th ADC converter. Consequently, this sampler cannot be chosen during the following $(M-1)T$ periods due to the time-interleaved architecture. Fig. 3.3 illustrates a case of three samplers ($M=2$, $R=1$) operating randomly to provide the sample alternatively to one of the two ADCs.

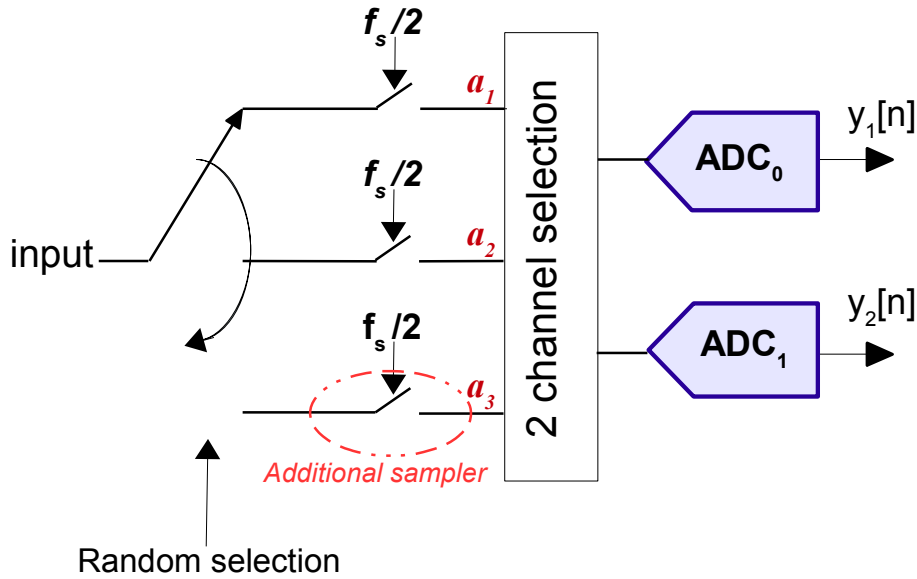


FIGURE 3.3 – 3 Samplers and 2 ADCs sampling.

Fig. 3.4 details the charge transfer in a 2-channel time-interleaved pipeline ADC using switched capacitor networks. The sampling phases are designed by S_i , where $i \in 1, 2, 3$ is the index of sampler. The charge transfer is performed by the H_{ij} switches where $j \in 1, 2$ denotes the index of the active converter. First, a random selection chooses a sampler that samples the input signal, let us say sampler 1. This latter sends the sample to the first MDAC to convert it when the H_{11} switch is "On". At the same time, a random selection of the next sampler between 2 and 3 is done and the sample switch of the chosen one is "On". The next hold phase concerns the second MDAC and hence the switches H_{i2} are "On", where i is the selected sampler (2 or 3 in this case). Thereby, at each sample time T , a sampler i is chosen differently from the one which is currently holding the previous sample.

The chronogram presented in Fig. 3.5 provides an example explaining the proposed random sampling method. It concerns the sequence 12132131. As it can be seen, the same sampler cannot be chosen twice in a period of $2T_s$ and then the TI characteristic is respected.

As a result of this randomization, the distortion tone is whitened throughout the bandwidth as illustrated in Fig. 3.6. Moreover, the advantage of this technique is that it can eliminate all kind of errors caused by mismatches between samplers like clock skew mismatch. However, if errors are present in the channel itself, this is not applicable and requires

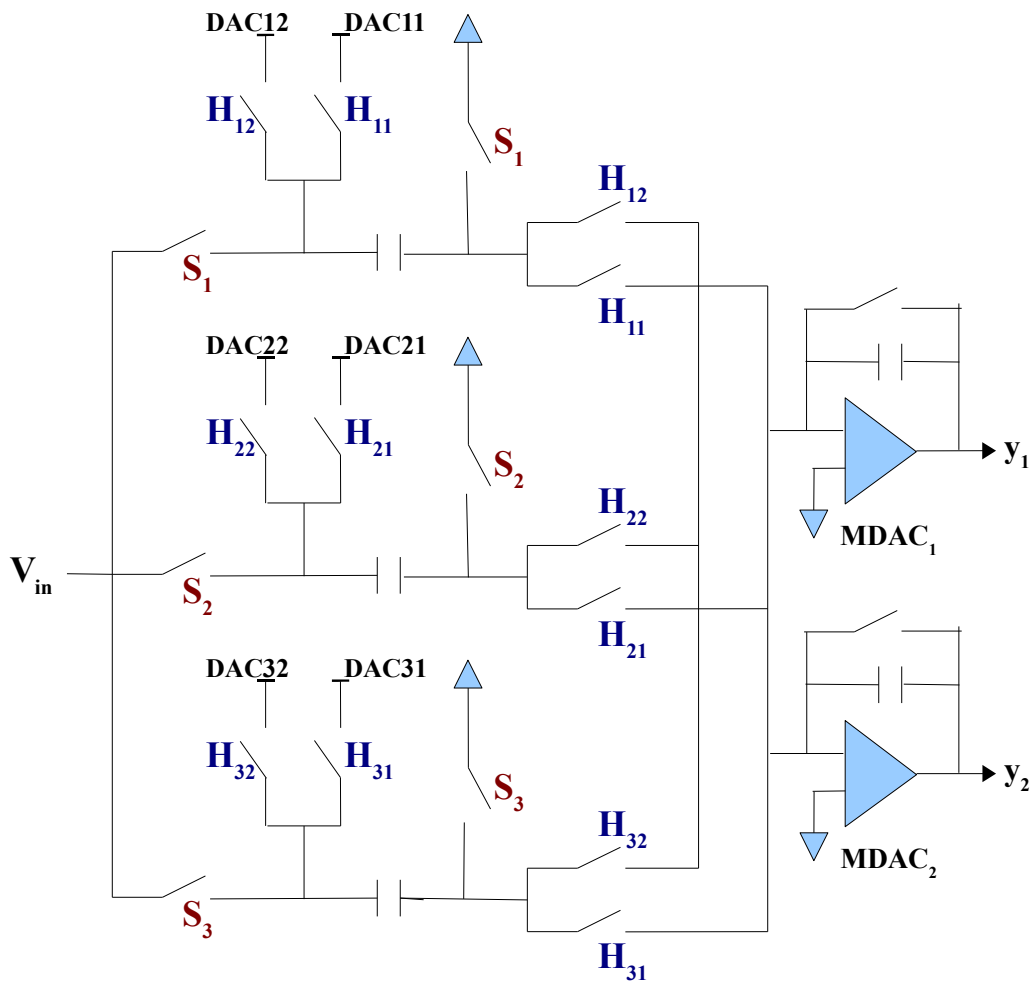


FIGURE 3.4 – 3 samplers for 2 ADCs Random sampling.

a one-channel calibration techniques. Finally, this technique does not require a large area, neither high power consumption since it brings into play only one additional sampler.

3.1.2.2 Impact of the number of additional samplers

The impact of the number of additional samplers is studied using a mismatch value of 1%. Fig. 3.7 shows the output spectrums of the 4-channels ADC with and without the employment of the proposed technique of compensation. The highest spur is about -60 dB before compensation due to bandwidth mismatch (Fig. 3.7 (a)). As it can be seen, the random sampling technique allows whitening the spurious tone correlated to the bandwidth mismatch. The SFDR is then highly improved without decreasing the SNDR of the converter and this is true whatever the number of channels and the number of additional samplers. In Fig. 3.7 (b), only one sampler is added to achieve the randomization. As a result, randomness is weakened and the noise becomes non-white. Nevertheless, it can be seen in Fig. 3.7 (c), in which $R=2$ that the noise is whiter. It remains true for higher number of additional sample networks. However, this does not much improve the SFDR. Finally, depending on the application and its noise ripple constraints, one additional sampler may be sufficient.

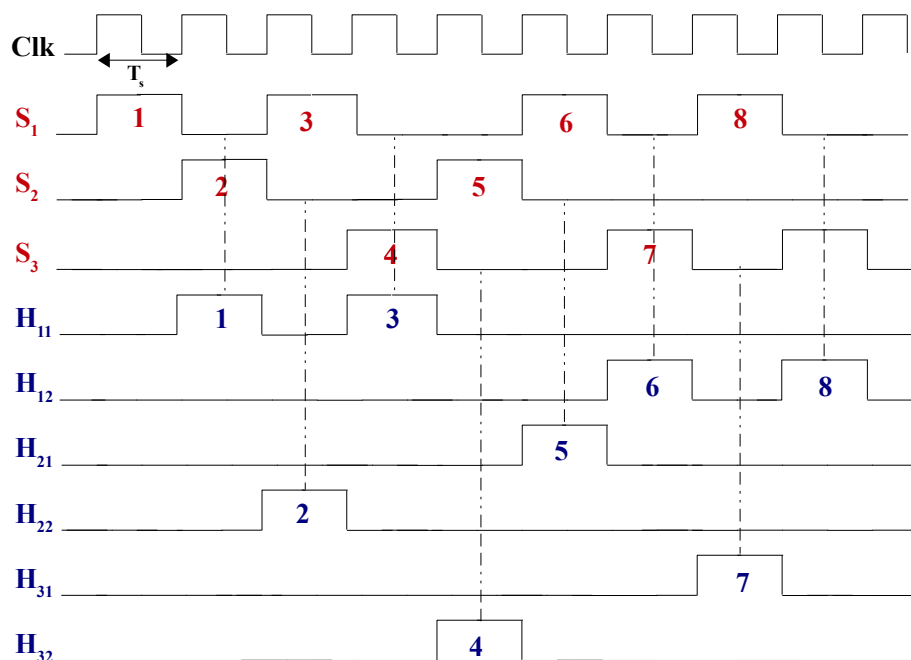


FIGURE 3.5 – Random sampling chronogram of the sequence 12132131.

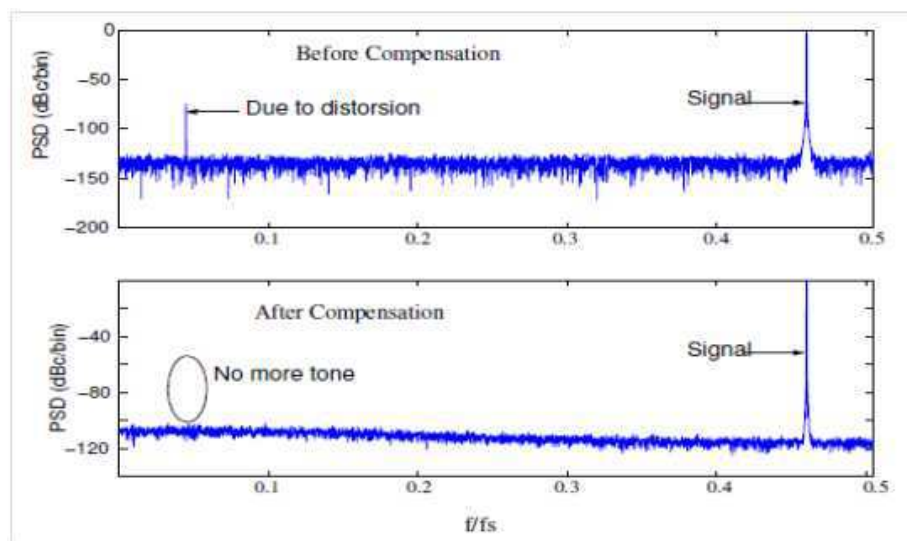


FIGURE 3.6 – Simulation for $M=2$, $R=1$ before and after randomization

The previous results show that by adding only one additional sampler, the desired result of suppressing the spurs can be sufficient. This was used in the experiment given by Fig. 3.8 to compare the values of SNR, SNDR and SFDR before and after compensation while using a pseudo random generator.

For a sine wave input signal, we choose $\omega_c/\omega_s = 3$ and illustrate the efficiency of the proposed solution for $M=4$ and $R= 1$. This is shown in Fig. 3.8. After compensation, the value of the SNDR remains the same as before using the random sampling technique. This is explained by the fact that the spurs have been converted into noise, and hence

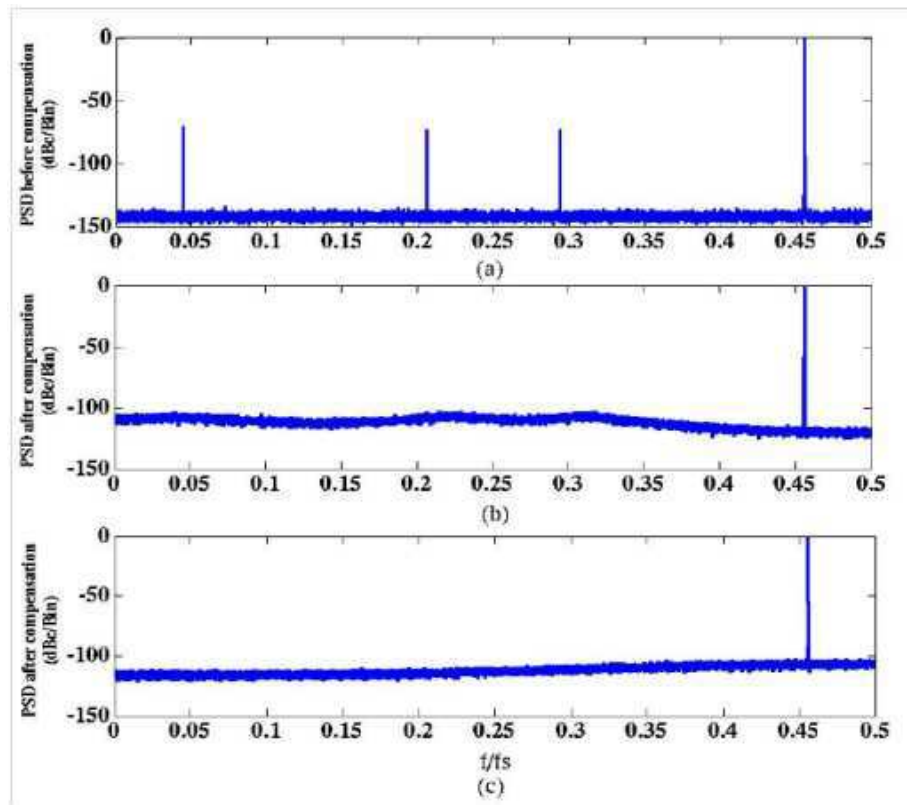


FIGURE 3.7 – Random sampling technique simulation (a) before compensation and after compensation for $M=4$ and (b) $N=1$ (b), (c) $N=2$.

the amount of global power remains the same. Moreover, the SNR after compensation is assimilated to the SNDR since no more tones appear. Finally, regarding the SFDR, the solution improves considerably its value up to 30 dB.

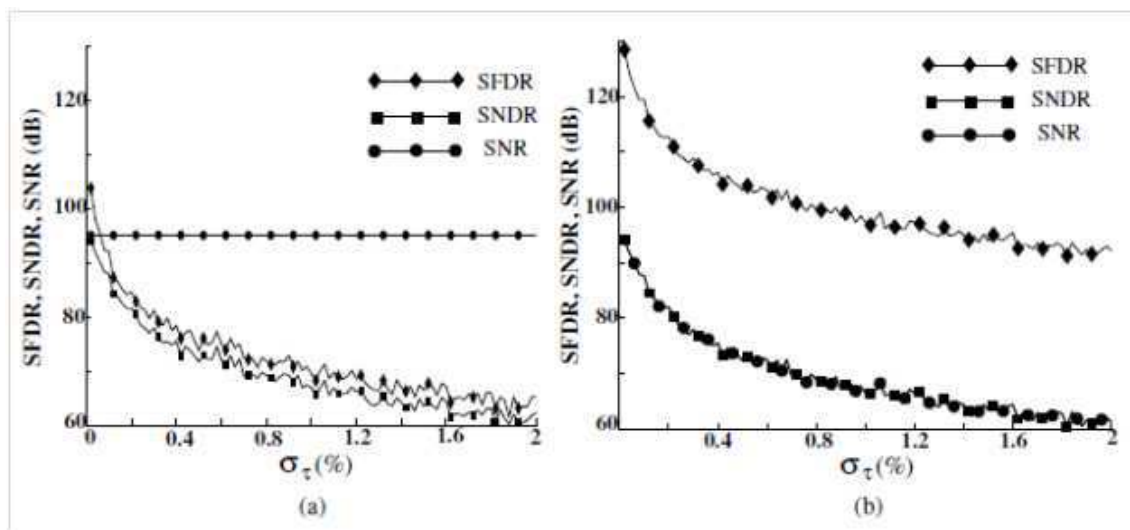


FIGURE 3.8 – SNR, SNDR and SFDR vs. $\sigma_{\tau}(\%)$, (a) before and (b) after compensation.

3.1.3 conclusion

In this section, a random sampling technique was discussed leading to reduce the impact of bandwidth mismatch error using additional samplers to spread the cyclic pattern over the frequency bandwidth. Compared to the existing methods, the proposed implementation allows reducing power consumption and the die area. It is also possible to compensate all errors due to switches' mismatch such as timing skew error. However, the generated noise degrades the SNR and must be shaped and filtered out of the bandwidth of interest. Nevertheless, this method can be used as a complementary solution where the errors are minimized beforehand and hence do not degrade the SNR.

3.2 Bandwidth Mismatch Calibration Techniques

3.2.1 Introduction

Apart from randomization method that leads simply to reduce the impact of the mismatch error, it is in general preferable to compensate this error between the channels. This is performed by first estimating this error and then using either digital adaptive filtering or tuning the input filters in the analog domain to achieve the correction. Fig. 3.9 shows the different scenarios. First one can notice that estimation is performed only in a digital part. In fact, the bandwidth mismatch is caused by the sampling networks so that the error appears in digital part. Moreover, for convenience we focus the development on digital correction techniques leading to compensate the output of any time-interleaved converter.

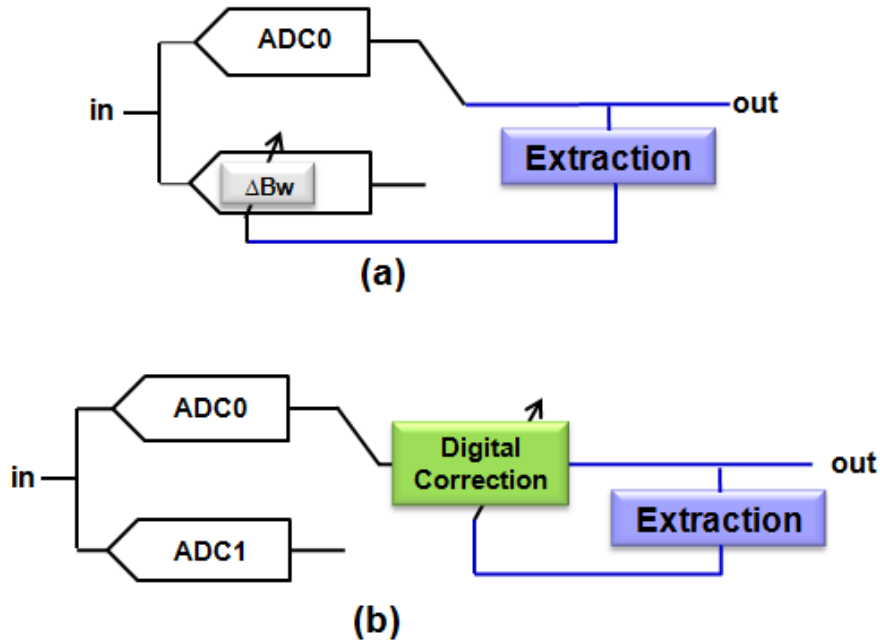


FIGURE 3.9 – Digital estimation and mixed correction model schemes for a bandwidth mismatch error (ΔBw) (a) Analog correction, (b) Digital correction.

In this section we will expose different background compensation methods by first comparing the existing techniques regarding error correction. Then, we will focus, in Sec.

3.2.2.2, on the error detection methods where two existing bandwidth mismatch estimation techniques are presented [18][69]. However, it will be highlighted that they present some drawbacks making them non usable for some correction methods. Finally, it will be shown at the end of this section the consequence of choosing a good loss function to estimate the error.

3.2.2 Background calibration techniques

3.2.2.1 Correction techniques

In the literature, very few analog techniques are proposed for bandwidth mismatch correction due to reliability and flexibility. One can refer to the recent work in [73] which consists of adjusting the voltage V_{gs} of the bootstrapped switch (responsible of sampling the input signal) and therefore varying the on-resistance of the sampling networks. However, it is difficult to attain very high accuracy by changing the voltage. Moreover, this can modify the delays of the clocks and generates additional clock skew. In addition, the circuit only achieves an SFDR of 75dB at 100 MHz of input signal which is not sufficient for our aimed specifications.

In the following, we focus on the digital correction techniques. First we propose an error analysis and consider linear phase compensation of the bandwidth mismatch. Then a comparison between different digital correction techniques is provided. Two existing approaches to deal with the bandwidth mismatch error are compared : the first one is based on Hybrid Filter Bank architecture where each input filter impact (called analysis filter) is compensated by its synthesis filter, so that the multiplication of the two filters provides a unity gain zero phase filter. The second family is based on a polynomial approximation filter. For this polynomial solution, a different approach is proposed to reduce the complexity of the existing solution.

1. *Linear compensation analysis for bandwidth mismatch error*

As discussed previously, bandwidth error due to mismatch between the input filters of the channels causes error in the gain and the phase of the output spectrum. The input filters can simply be modelled by first order low pass filters. Consequently, the gain and the phase components depend on the input frequency and are non linear dependent of the mismatch error. One can imagine to treat the bandwidth mismatch phase error as a timing skew error by linearization since the error is small. Fig. 3.10 shows a 2 channels TI-ADC in the presence of bandwidth mismatch between the two first order filters.

$H_i(\omega)$ which is the i -th channel input can be expressed as :

$$H_i(j\omega) = \frac{1}{1 + j\omega\tau_i} \quad (3.1)$$

$$= \frac{1}{\sqrt{1 + (\omega\tau_i)^2}} \angle -\arctan(\omega\tau_i). \quad (3.2)$$

Fig. 3.11 shows the evolution of the SFDR when compensating the nonlinear bandwidth phase with a linear phase $\omega\tau_i$ (as a timing skew error). The improvement (dash curve) is highly visible in very small error case and for low input frequencies. However, for higher input frequencies, this compensation becomes useless.

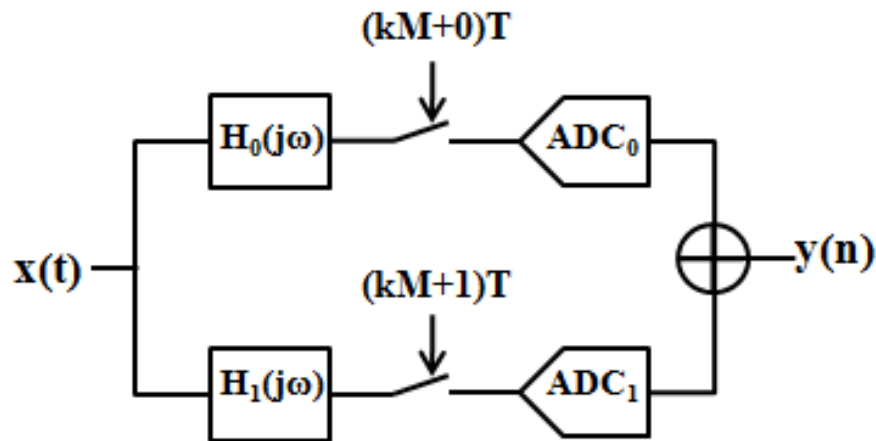


FIGURE 3.10 – 2-channels system model

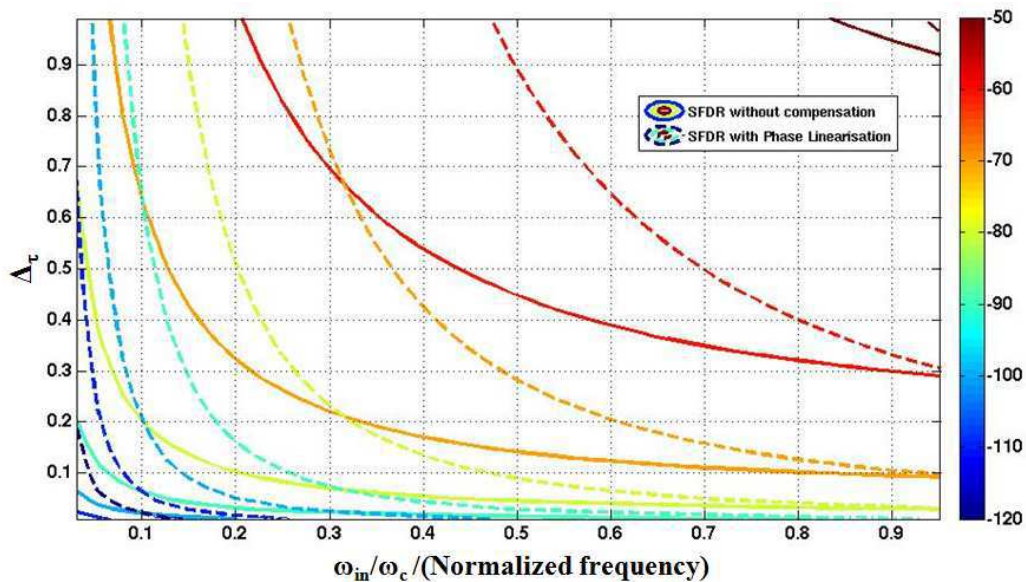


FIGURE 3.11 – SFDR Performance versus bandwidth mismatch error before and after linear compensation

Most of existing correction techniques treat the problem of bandwidth mismatch as a frequency response. This approach is preferred because of time varying characteristic of the input filters. In addition, one can note that, in frequency domain, the output is easily modelled as the input signal multiplied by a gain error function while the phase error is added to the phase of the input signal. This allows to correct one channel compared with a reference one, so that transfer functions are divided in order to characterize only one compensation error filter.

2. Individual channel corrections

Adaptive filters require computation of the coefficients whenever the error changes

because of environment variations. Fig. 3.12 shows two digital correction filters, F_0

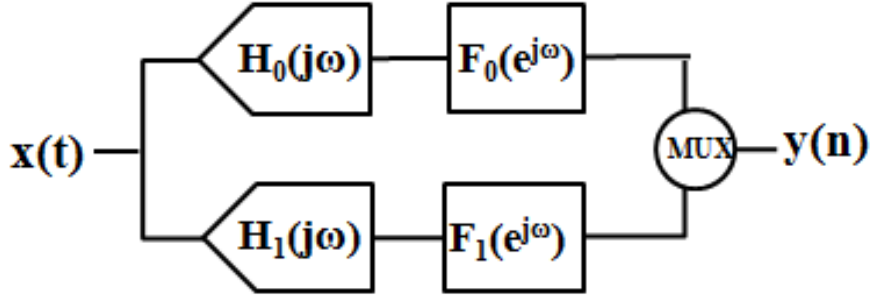


FIGURE 3.12 – Correction of each channel using high pass filters

and F_1 , where each one leads to compensate the filtering effect of the analog input filters H_0 and H_1 of Fig. 4.1, respectively. One can imagine the correction filters as high pass filters where the product $H_i(j\omega)F_i(j\omega)$, $i \in \{0, 1\}$, should give a unity gain, zero phase shift at ω_{in} , while eliminating the image spurious at $\omega_s/2 - \omega_{in}$. In [74], the authors elaborate the following system in respect with the previous conditions so that :

$$\begin{cases} H_0(j\omega_{in})F_0(e^{j\omega_{in}}) + H_1(j\omega_{in})F_1(e^{j\omega_{in}}) = 2 \\ H_0(j(\omega_{in} - \frac{\omega_s}{2}))F_0(e^{j\omega_{in}}) + H_1(j(\omega_{in} - \frac{\omega_s}{2}))F_1(e^{j\omega_{in}}) = 0 \end{cases} \quad (3.3)$$

It is important to notice that the F_i filters are digital filters and the H_i are analog filters. Therefore, the discrete-time filters F_i are valid for $-\omega_s/2 < \omega < \omega_s/2$ and periodic with period ω_s .

Based on this, several techniques have been proposed to determine the inverse system for the time-varying time-interleaved architecture [17]. These filters require the computation of the coefficients using windowing techniques which include inverse Fourier transforms [74], matrix inversions [75, 76] and numerical optimization which is complex and time consuming. Moreover, this may comply with offline filters design which is not acceptable when compensating the bandwidth mismatch error because of input frequency dependency.

For all these reasons, this solution has not been chosen and relative error compensation between the two channels is preferred.

3. Polynomial approximation technique : proposed implementation

To overcome the previous problem, another approach consists of compensating only one channel compared to a reference channel, so that the lower channel contains the relative bandwidth error, as shown in Fig. 3.13. Therefore, if the two channels are identical, the second channel's filter will be equal to one and the overall output corresponds to the input signal multiplied by the upper channel filter.

Recently, solutions based on polynomial approximation have been widely studied [77, 76, 78]. The main idea consists of using farrow filters instead of all adaptive filters to achieve the calibration. A Farrow filter is basically used for an efficient realization of adjustable fractional-delay FIR filters [78]. This will be explained below.

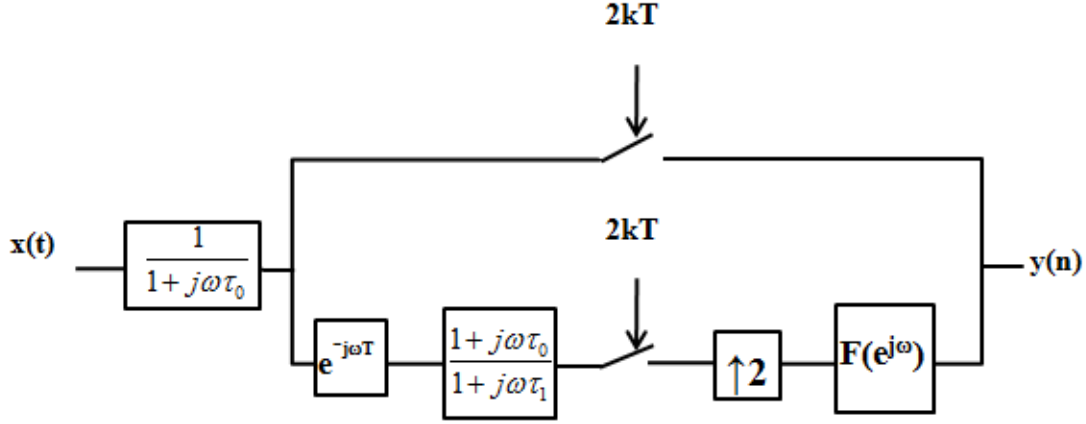


FIGURE 3.13 – Correction of a 2 channel TI-ADC using relative adaptive filter

Let us denote by $H(j\omega)$, the analog error filter in Fig. 3.13, which is expressed as :

$$H(j\omega) = \frac{1 + j\omega\tau_0}{1 + j\omega\tau_1}. \quad (3.4)$$

The challenge of the digital filter $F(e^{j\omega})$ is to compensate the analog filter $H(j\omega)$ to match better with a unity gain, zero phase filter. The idea is then to design the filter F as the inverse of H , so that :

$$F(e^{j\omega})H(j\omega) = 1. \quad (3.5)$$

Hence,

$$F(e^{j\omega}) = \frac{1 + j\omega\tau_1}{1 + j\omega\tau_0}. \quad (3.6)$$

Bilinear transformation can be used to design the digital filter using the above analog expression. The analog frequency axis is warped into a limited band $[-\omega_s/2; \omega_s/2]$ to avoid aliasing. In fact, due to sampling, replicas of the Nyquist band are created along the frequency axis and aliasing can be generated. This can be a drawback for wideband applications where the signal band is not limited to a Nyquist band.

The exposed solution is based on a Taylor approximation applied to F , since realistic values of the bandwidth mismatch are around 1% which is small enough [77]. Therefore, a third order polynomial approximation can be expressed as :

$$\begin{aligned} F(e^{j\omega}) &= (1 + j\omega\tau_1)[1 - (j\omega\tau_0)^1 + (j\omega\tau_0)^2 - (j\omega\tau_0)^3] \\ &= 1 - j\omega(\tau_0 - \tau_1) + (j\omega)^2\tau_0(\tau_0 - \tau_1) - (j\omega)^2(\tau_0^2)(\tau_0 - \tau_1) \end{aligned} \quad (3.7)$$

Therefore

$$F(e^{j\omega}) = 1 + \epsilon_\tau(j\omega\tau_0)^1 + \epsilon_\tau(j\omega\tau_0)^2 + \epsilon_\tau(j\omega\tau_0)^3 \quad (3.8)$$

in which $\epsilon_\tau = \frac{\Delta\tau}{\tau_0}$ denotes the relative bandwidth error that need to be equal to zero to match the two channels.

The structure in Equation 3.12 is called Farrow filter and the differential filters $(j\omega\tau_0)^p$, (where $p = 1, 2, 3$ in this example), are designed beforehand. It is important to notice that F is a digital filter, meaning that the differentiators are FIR or IIR filters and can be designed offline as a set of fixed digital differentiators $G_p = (j\omega)^p$ followed by the constant coefficients $a_p = \tau_0^p$. The impulse response of $G_p = (j\omega)^p$ can be expressed as :

$$g_p(n) = \frac{1}{2\pi} \int_{-\pi}^{\pi} G_p e^{j\omega n} d\omega. \quad (3.9)$$

$$= \frac{1}{2\pi} \int_{-\pi}^{\pi} (j\omega)^p e^{j\omega n} d\omega. \quad (3.10)$$

$$= \frac{(j\pi)^{p-1}}{n} \cos(\pi n - \frac{\pi}{2}(p-1)) - \frac{p}{2\pi n} g_{p-1}(n). \quad (3.11)$$

for $p = 1, 2, 3$, the impulse responses are given by :

$$g_1(n) = \frac{\cos(\pi n)}{n}. \quad (3.12)$$

$$g_2(n) = -\frac{2}{n} g_1(n). \quad (3.13)$$

$$g_3(n) = -\pi^2 \frac{\cos(\pi n)}{n} - \frac{3}{n} g_2(n). \quad (3.14)$$

$$(3.15)$$

The scheme of the global correction filter is illustrated in Fig. 3.14. The mismatch coefficient ϵ_τ multiplies each differentiator. They are comparable to the ones calculated in [77] with the difference of having τ_1 instead of τ_0 in Equation 3.12. It is important to note from this structure that the error is multiplied by fixed filters which have been designed beforehand. This is simpler than the proposed one in [77] where an additional calculation of the power values of this parameter is required which increase the complexity of the implementation.

ϵ_τ needs to be estimated with a desired accuracy to achieve a good correction. Let us consider an example of iterative correction so that the value of ϵ_τ increases with a resolution step of 0.1% until the performance is attained. The initial error is 0.53% between the two channels and only the second channel is modified thanks to the farrow filter. Fig. 3.15 illustrates the evolution of the SFDR with the error (i.e., when changing ϵ_τ) along the bandwidth. Before correction, the SFDR degrades significantly with the input frequency and tends to a value of 85dB when ϵ_τ approach the error (0.53%).

In this simulation, we assume ideal design of the differentiators. The impulse responses are calculated using the inverse Fourier transforms of the frequency transforms of each $(j\omega)^i$, where i is an integer. The complexity of this solution is then related to the implementation of these filters. Moreover, it is important to notice that if the errors are important, then the polynomial approximation will be limited and hence high SFDR could not be achieved. Finally, the technique is adaptable in the presence of all other errors ; especially gain and clock skew and best fit with polynomial estimation of the global error [69].

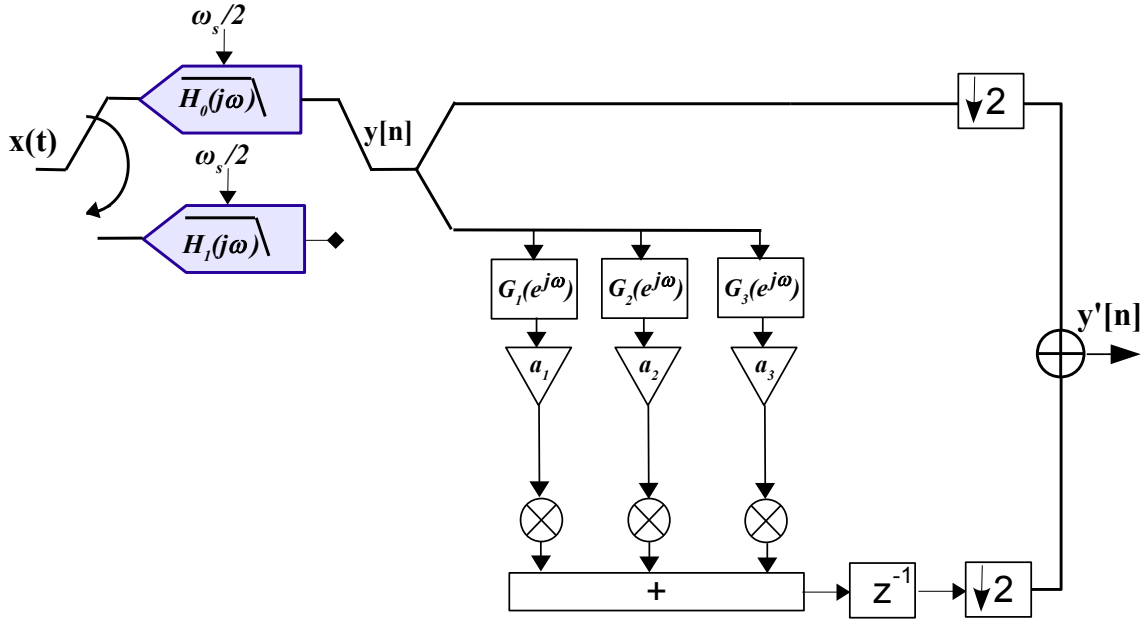


FIGURE 3.14 – Correction of a 2 channel TI-ADC using relative adaptive filter : polynomial approximation structure.

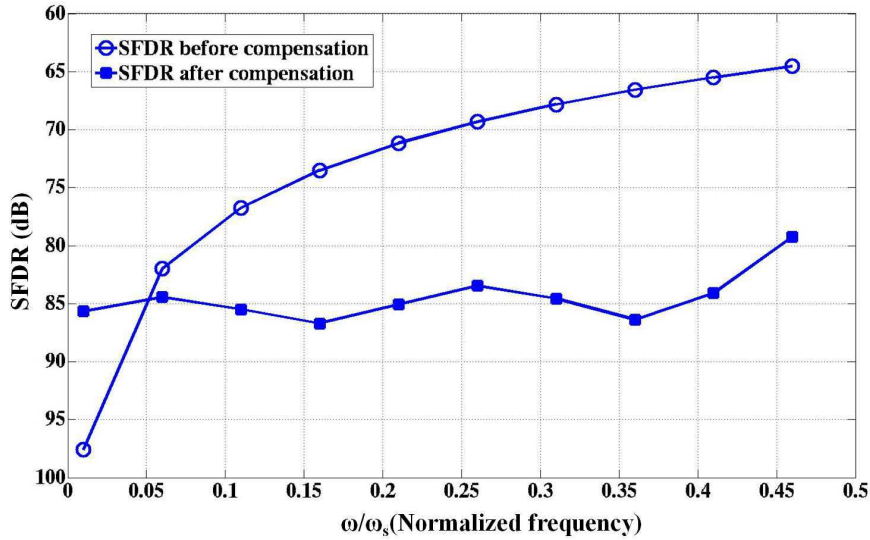


FIGURE 3.15 – SFDR before and after polynomial filtering.

3.2.2.2 Background detection techniques

In the best of our knowledge, no estimation technique or circuit exists to blindly determine the bandwidth mismatch error because of the nonlinear, frequency dependency of this generated error. We can classify the background error estimation into in one hand a semi blind estimation technique, proposed in [18], where an additional signal is needed to evaluate the error. A second approach consists of estimating the global error using polynomial approximation proposed in [69]. This will introduce the discussion about the loss function choice which is detailed at the end of this section. This is important to reach

a good estimate of the desired error. Finally, this one is retrieved using some proposed algorithms detailed in chapter 4.

1. *Semiblind estimation*

The semi blind estimation technique proposed in [18] aims to estimate the relative error between time constants of two channels in a TI architecture. It consists of the injection of a small signal in a narrow band given by $[(1 - \epsilon)\omega_s/2; \omega_s/2]$, as shown in Fig. 3.16. Due to mismatch errors in a time-interleaved architecture, a spurious tone appears in the $[-\epsilon\omega_s/2; \epsilon\omega_s/2]$ region. After that the generated error is extracted by filtering.

According to the authors, two conditions are required to properly extract the band-

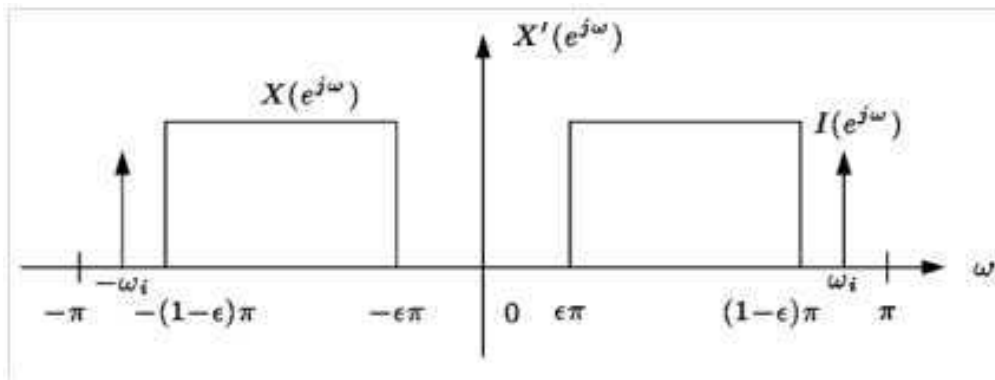


FIGURE 3.16 – Spectral representation of the injected test signal in $[(1 - \epsilon)\omega_s/2; \omega_s/2]$. mismatch error is extracted around zero.

width mismatch error : 1) the first one assumes that the input signal has no frequency content in a small band around zero frequency $[-\epsilon\omega_s/2; \epsilon\omega_s/2]$ so as only the spurious tone caused by the test signal would be extracted in this band. 2) the second condition consists of initially having some energy in a matching band, just below a first Nyquist band, meaning $[(1 - \epsilon)\omega_s/2; \pi]$ shown in Fig. 3.16. However, if the input signal is oversampled, this condition is satisfied by injecting a test signal. This is employed to estimate the bandwidth mismatch, and possibly other mismatch parameters, without interfering with the ADC operation. According to this, the test signal should be small enough compared to the desired signal to ensure that it does not reduce significantly the ADC's dynamic range. Afterwards, the injected signal can be removed digitally by bandpass filtering the ADC output after correction.

One can note that the estimation algorithm proposed in [18] for bandwidth mismatch error is semi blind in the sense that it does not require any knowledge of either the input signal or the test signal which is waited for. Nevertheless, the presence of the additional signal represents limitations. In fact, authors suggest using a square wave as a test signal, easily generated by a clock signal. However, this generates additional harmonics which can require the anti-aliasing filter of the ADC to be sufficiently accurate. It can also be mentioned that due to the power condition of the injected signal, the spurious tone is very small which makes the detection accuracy difficult to achieve. Moreover, test signal generation requires extra power which can be controlled

by turning off this signal outside the estimation phases but increases the convergence time of the estimator. The last inconvenient that can be noted about this technique is the complexity of the considered filters for bandwidth extraction and the approximations made to assume that the error is small enough.

Besides the mentioned limitations, we are particularly interested in our work on on-line calibration techniques without any additional signal. This is discussed bellow.

2. *Polynomial estimation*

The second approach which is blind consists of estimating a global error using polynomial approximation at the ADC output. A global error may include gain, timing skew and bandwidth mismatch. This solution was proposed in [69] where the authors use the property of a cyclostationary output signal in time-interleaved architecture to define the loss function that should be minimized to extract the error. This work tends to estimate at the same time, gain and timing skew errors by unique parameter identification.

Cyclostationary process is a signal having statistical properties that varies cyclically with time. One of the cyclostationarity properties is the the autocorrelation (meaning second order statistics) is periodic in time. Non-stationary part of the signal autocorrelation is then smoothed out by averaging in time instead of stochastic expectation. These are called wide-sens cyclostationary signal which is assumed for convenience in most of practical cases.

The analysis is based on the model shown in Fig. 3.17 (a). In order to estimate the error between the two channels, it is preferable to consider the frequency response ratio as shown in Fig. 3.17 (b). If the channels are perfectly matched then $H(j\omega) = 1$ and the input signal can be considered as cyclostationary with a period T , where T is the overall period of the TI-ADC. This is a so-called Wide Sens Stationary (WSS) signal and for a perfect matched system without errors, an input WSS signal $x(t)$ leads to a WSS output signal as well. However and in the presence of mismatches, the basic idea consists of using the correction block in Fig. 3.17 (b) to make the output z wide-sense cyclostationary. This approach imposes to define analytically the autocorrelation function of the corrected output in order to specify the loss function used to extract the error.

To do so, a decomposition of $H(j\omega)$ can be written as :

$$H(j\omega) = (1 + g(\omega))e^{j\phi(\omega)} \quad (3.16)$$

where $g(\omega)$ and $\phi(\omega)$ are general gain and phase mismatch respectively.

From this and under small mismatch assumption, one obtains the approximation model using the first taylor order expansion :

$$H(j\omega) = 1 + g(\omega) + j\phi(\omega) \quad (3.17)$$

The frequency response polynomial approximation leads to :

$$g(\omega) = \sum_{k=0}^Q a_k \omega^k, \phi(\omega) = \sum_{k=0}^Q b_k \omega^k \quad (3.18)$$

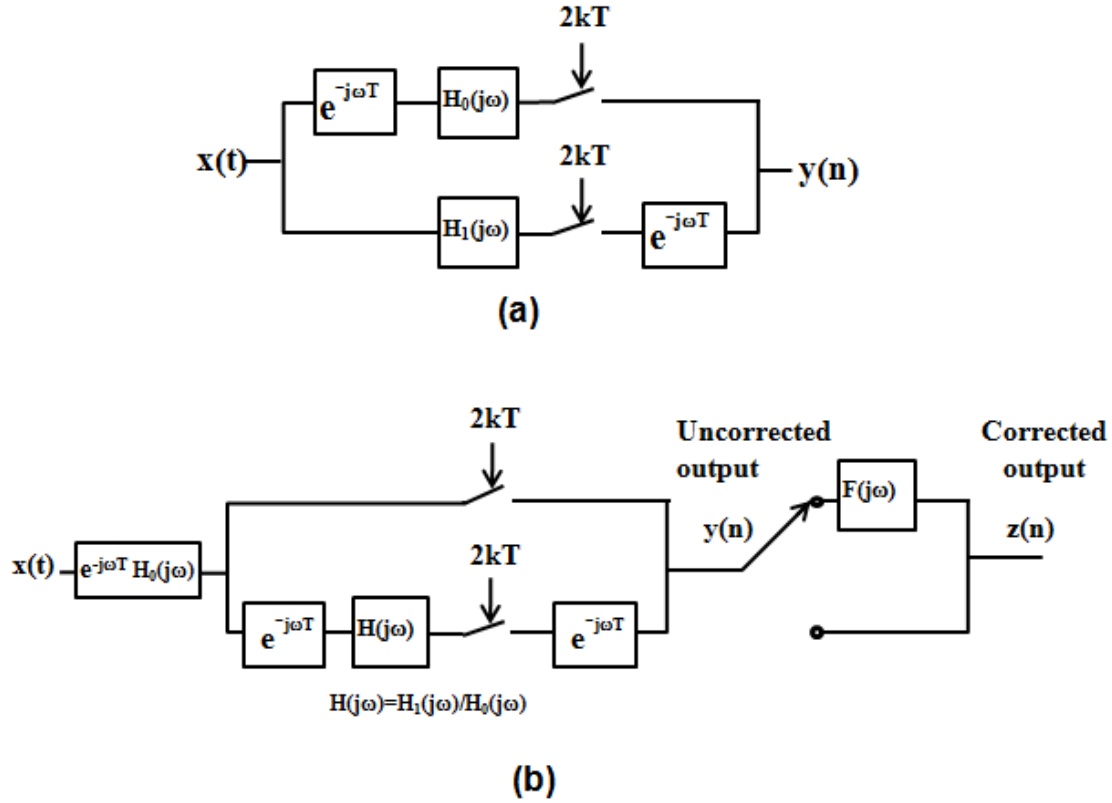


FIGURE 3.17 – 2-channel TI ADC model (a) conventional system (b) normalized system.

where a and b represent the coefficients containing the gain error and the phase error respectively. Q is the polynomial order.

By plugging Equation 3.18 into 3.17 with Fourier inverse calculation, the impulse response is :

$$h[n] = \delta[n] + \sum_{k=0}^Q \alpha_k h_k[n] \quad (3.19)$$

where α_k is a combination of the parameters a_k and b_k in Equation 3.19. The estimation of the mismatch error yields to α_k , which is the estimate of α_k . To do so, thanks to the correction filter F , a perfect reconstruction consists of minimizing the error well enough to restore the WSS signal property. This is achieved when the autocorrelation depends on the difference between the samples rather than the sample itself. Consequently, for any delay u ; the autocorrelations $R_z[u+1, 1]$ and $R_z[u, 0]$ are equal. Therefore, the following error function needs to be minimized :

$$J = \sum_{u=0}^{U_{max}} (R_z[u+1, 1] - R_z[u, 0])^2 \quad (3.20)$$

where U_{max} is the maximum time lag to consider. Fig. 3.18 shows the different terms of J for each u delay ($U_{max} = 2$). It can be noticed that the output can be split into odd samples represented by 0 in the figure which corresponds to channel '0' and even

samples represented by '1'. Each channel output can be viewed separately as a WSS signal. Consequently, $R_z[m, n] = R_z[m + 2, n + 2]$; for all m, n . It can be shown that

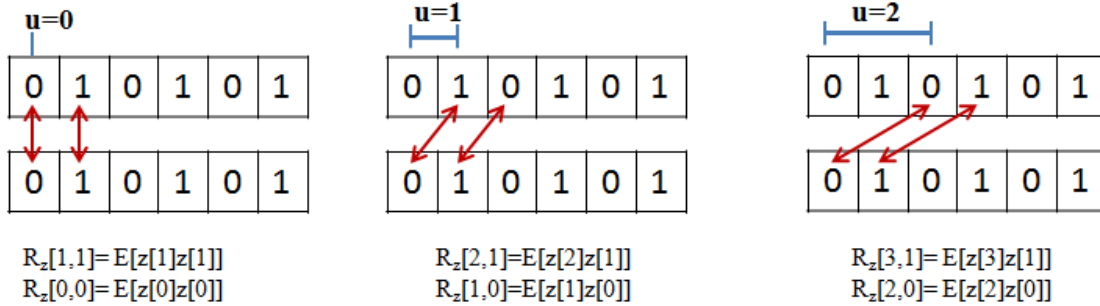


FIGURE 3.18 – corrected output autocorrelation for different delays $u \in 0, 1, 2$.

for even values of u , the loss function consists of the difference between the power values of the two channels. The odd values give the difference between the shifted cross correlations between the two channels which aims to extract the phase error. At the end, the minimization of the loss function J is obtained by zeroing its gradient $\frac{dJ}{d\hat{\alpha}}$ which can be performed iteratively using the Least Mean Square schemes (LMS). The complexity of this solution resides in the double-convolution required to calculate the autocorrelations $R_z[u + 1, 1]$ and $R_z[u, 0]$. Moreover, this solution is based on polynomial approximation which can highly limit the accuracy of the obtained results if the mismatch error is high which is not discussed by the authors. This limitation has been discussed in Sec. 3, where the SFDR is limited by the polynomial approximation. Finally, the main drawback of this solution is that the result of estimation merges global gain and phase errors without any possible distinction meaning that analog correction is not possible. In fact, tuning separately the mismatch parameters cannot be distinguished in the loss function error and hence its impact cannot be evaluated.

In the following part, we discuss the consequence of choosing an inappropriate loss function and then we propose an alternative method to extract the bandwidth mismatch error.

3. Loss function study and requirement

The choice of a good loss function is the most important part of error extraction. In fact, the existing algorithms lead to find an estimate of the desired parameter by minimizing a certain function. This latter is called loss function because it represents an error. Nevertheless, a bad choice of this loss function can give local minimums and consequently alter the estimation. Let us consider in this section a linear phase error to highlight the choice of the loss function. Afterwards, bandwidth mismatch error including non linear parts will be exposed to introduce the usage of the proposed a new estimator detailed in Chapter 4.

For a linear phase error denoted by Δ_t , a sine wave input signal leads to :

$$y_i[k] = \cos(\omega T(kM + i + \Delta_{t_i})). \quad (3.21)$$

For each channel i of a two-channels time-interleaved architecture. The autocorrelation for each sample n calculated for N samples is expressed as :

$$R_{y_i}[n] = \frac{1}{N} \sum_{k=1}^N y_i[k]y_i[k+n]. \quad (3.22)$$

Each channel's output in a TI architecture is a cyclostationary process [69] and therefore, the autocorrelation depends only on the difference between the samples n and $n+k$. For an input frequency ω_{in} , one has :

$$R_{y_i}[n] = \frac{1}{N} \sum_{k=1}^N \cos(\omega_{in}T(kM+i) + \Delta_{t_i}) \cos(\omega_{in}T(kM+i+nM) + \Delta_{t_i}). \quad (3.23)$$

Finally, the i -th channel autocorrelation gives :

$$R_{y_i}[n] = \frac{1}{2} \cos(nM\pi\omega_{in}) + \frac{1}{2N} \frac{\sin(\omega_{in}T.NM)}{\sin\left(\pi\frac{N_{in}}{N}M\right)} \cos(\omega_{in}T\{(N-1)M+nM+2i+2\Delta_{t_i}\}).$$

If the two channels are perfectly matched, the autocorrelations must be the same. The maximum value of the autocorrelation is obtained for a delay of $n=0$. The loss function can be then obtained by subtracting the two channels autocorrelations.

$$V_{loss_1} = (R_{y_j}[0] - R_{y_i}[0])^2. \quad (3.24)$$

in which :

$$R_{y_j}[0] - R_{y_i}[0] = \frac{1}{N} \frac{\sin(\omega_{in}TNM)}{\sin(\omega_{in}TM)} \sin(\omega_{in}T\{j-i+(\Delta_{t_j} - \Delta_{t_i})\}) \quad (3.25)$$

$$\sin(\omega_{in}T\{(N-1)M+nM+(i+j)+\Delta_{t_j}+\Delta_{t_i}\}). \quad (3.26)$$

From this expression, it can be seen that for $N \rightarrow \infty$, the difference tends to 0, imposing the accuracy of the extraction to be very high. Fig. 3.19 shows the loss function of Equation 3.24 versus the mismatch error. This is done for different input frequencies. This loss function presents different local minimums around the desired mismatch error which is impractical for unique error estimation. Moreover, the value of the loss function at $\Delta_{t_0} = -0.2\%$ is too small to be extracted. This is shown in Fig. 3.20 which represents the zoom figure of Fig. 3.19 around this error value. It is important to note that a minimum of -0.8% in Fig. 3.19 comes from the fact that one sample separates the two successive channels, and can be observed in the first term of Equation 3.24 ($i-j+\Delta_{t_j}-\Delta_{t_i}=-1+0.2$).

To overcome these problems, one can refer to [79], where the authors define an additional loss function which owns the same global error and posses orthogonal values for each local minimum with Equation 3.24. The sum of the two functions leads then to the extraction of the unique global error. The complexity of this approach is to find the complementary function taking into account different parameters (input frequency, mismatch error).

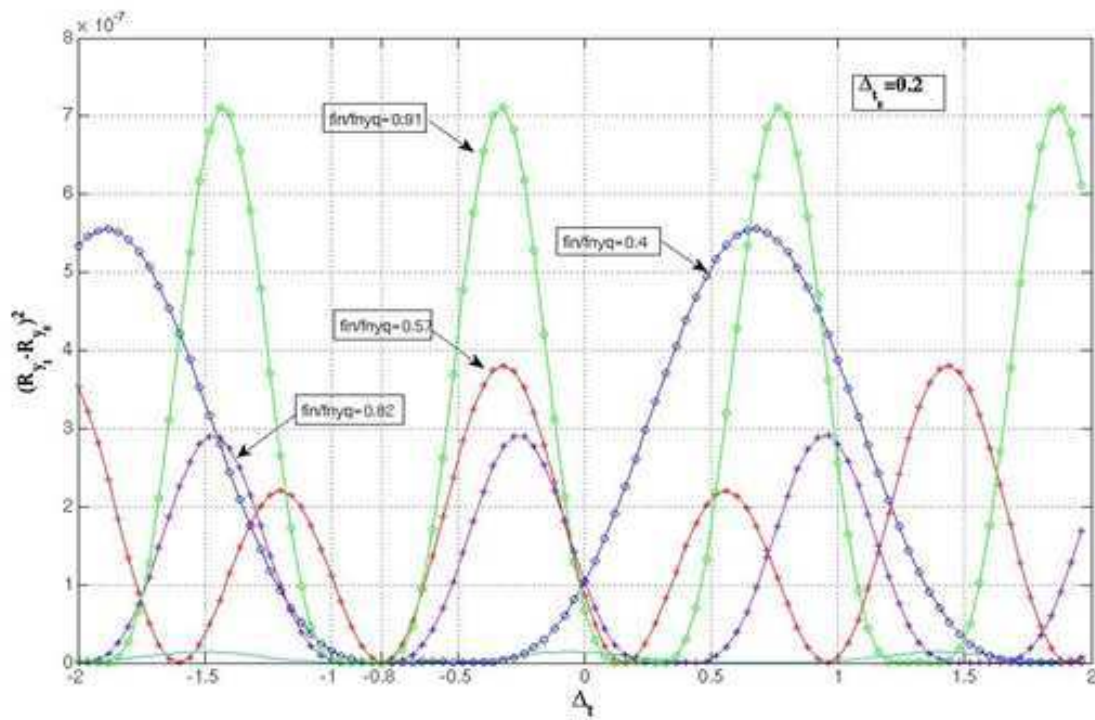


FIGURE 3.19 – V_{loss_1} : Difference between the two autocorrelation versus the phase mismatch.

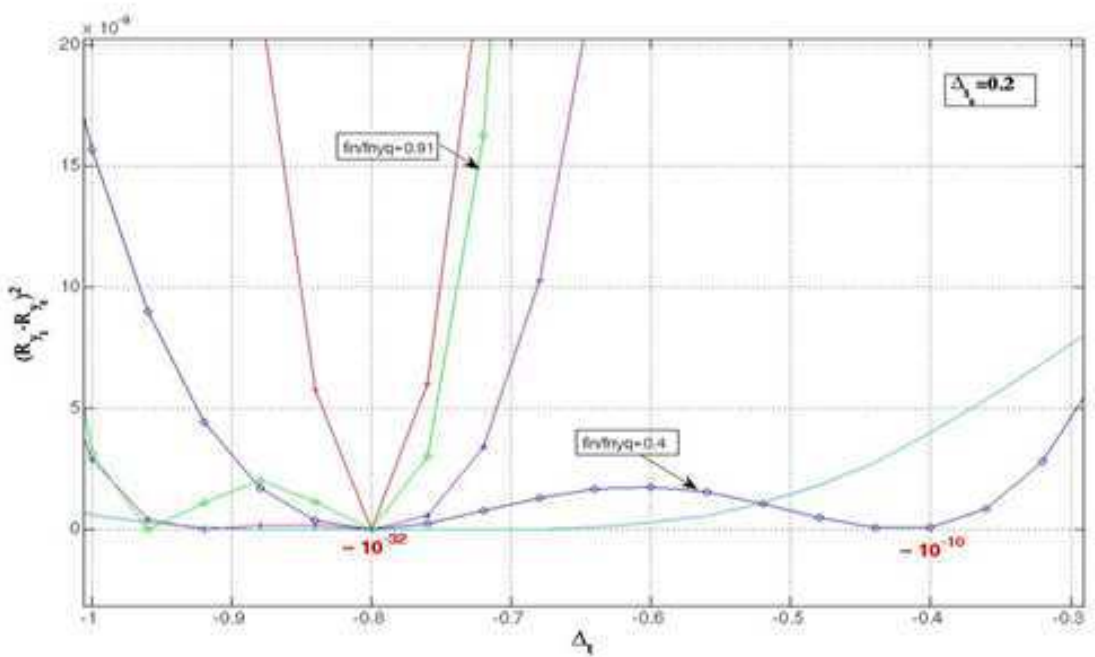


FIGURE 3.20 – V_{loss_1} : Zoom figure of Fig. 3.19 around the global minimum.

A second approach consists of the definition of the proficient loss function using cross correlation between channels. It can be expressed by considering N samples as

$$R_{y_i y_j}[n] = \frac{1}{2} \cos(\omega_{in} T \{(j-i) + (\Delta_{t_j} - \Delta_{t_i})\}) + \frac{\sin(\omega_{in} T N M)}{\sin(\omega_{in} T M)} \frac{1}{2N} \cos(\omega_{in} T \{(N-1)M + nM + (i+j) + \Delta_{t_j} + \Delta_{t_i}\}). \quad (3.27)$$

In this equation, only the second term is multiplied by $1/N$ so that for a high number of samplers, the first term is extracted. This one contains the error mismatch between the two channels. If these latter are matched, the cross correlation tends to one of the channel autocorrelation function. To minimize the error between the two functions, the loss function is defined as the difference between the cross correlation in Equation 3.27 and the mean value of the autocorrelations of the two channels i and j (Equation 3.24).

$$V_{loss_2} = \left(R_{y_i y_j}[0] - \frac{R_{y_j}[0] - R_{y_i}[0]}{2} \right)^2. \quad (3.28)$$

After some manipulations, one obtains :

$$R_{y_i y_j}[0] - \frac{R_{y_j}[0] - R_{y_i}[0]}{2} = \frac{1}{2} \left\{ \cos(\omega_{in} T \{(j-i) + (\Delta_{t_j} - \Delta_{t_i})\}) - 1 \right\} \left\{ 1 - \frac{1}{2N} \frac{\sin(\omega_{in} T N M)}{\sin(\omega_{in} T M)} \cos(\omega_{in} T \{(N-1)M + nM + (i+j) + (\Delta_{t_j} + \Delta_{t_i})\}) \right\}.$$

For $N \rightarrow \infty$, the second term tends to zero when the first term gives the following mismatch :

$$R_{y_i y_j}[0] - \frac{R_{y_j}[0] - R_{y_i}[0]}{2} \rightarrow \frac{1}{2} \left\{ \cos(\omega_{in} T \{(j-i) + (\Delta_{t_j} - \Delta_{t_i})\}) - 1 \right\}. \quad (3.29)$$

It can be seen in Fig. 3.21 that in the range of one sample $\Delta \in [-1; 0]$, the function in Equation 3.28 owns a unique minimum which can be considered as global in this interval. Now, let us consider the non linear, frequency dependent gain and phase errors due to bandwidth mismatch. It is shown in Fig. 3.22 that the first loss function, difference between the two channels autocorrelation functions owns a unique global minimum at the value and particularly, the loss function values are higher compared to Fig. 3.19, where the maximum value of the loss function is about 10^{-7} . Once the loss function is well defined, it is essential to choose the right minimizing algorithm. LMS algorithms are in general preferred in literature in [79]. In the next chapter, we expose another approach to address the problem of loss function minimization once the loss function is chosen.

3.2.3 Conclusion

In this section, a classification of bandwidth mismatch compensation techniques has been discussed. First, a comparison between existing correction techniques has been shown

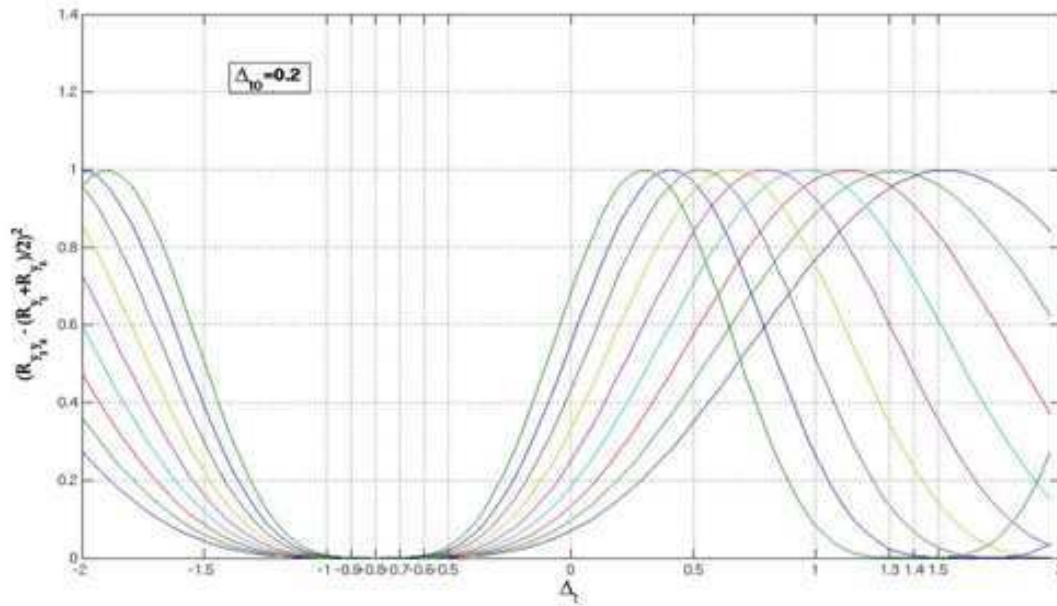


FIGURE 3.21 – V_{loss_2} versus mismatch for different ω_{in}/ω_{nyq}

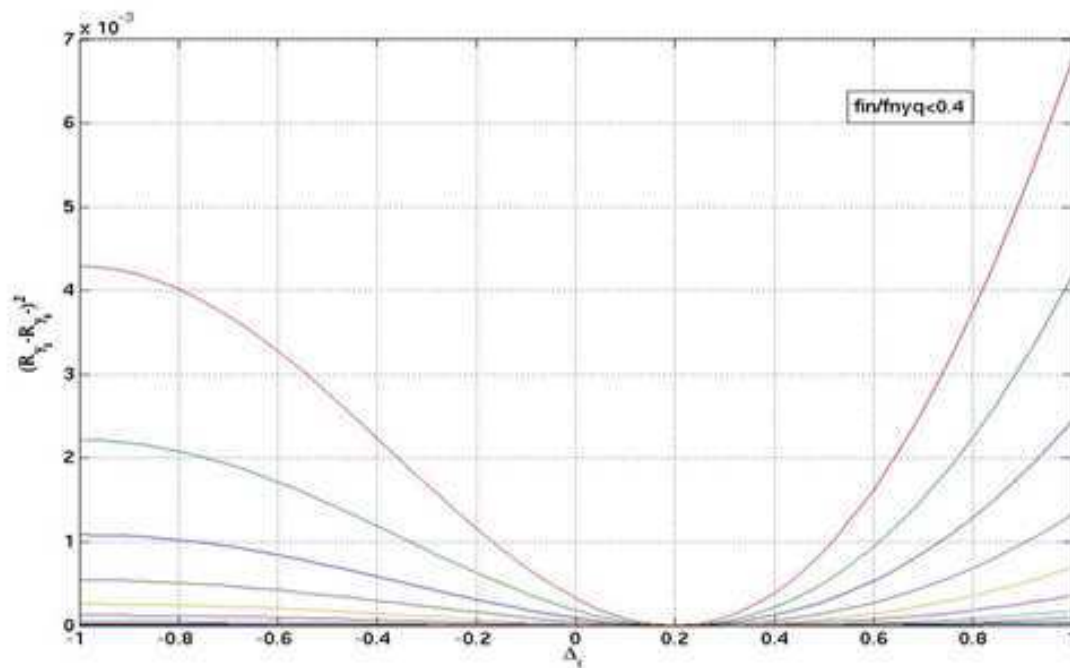


FIGURE 3.22 – V_{loss_1} versus nonlinear mismatch error

by highlighting their limitations. Then, we have focused on the detection block which is very important in the sense that wrong identification can degrade dramatically the per-

formances. To the best of our knowledge, only two solutions have been proposed in the literature. The first one addresses the problem by adding a small signal and leads to extract the mismatch error. However, we rather aim to extract the error blindly. The second approach addresses the problem globally so that the errors are not separated, in that case, only digital correction can be applied. Finally, we have detailed the use of autocorrelation to define a good loss function which needs to be minimized to estimate the error.

3.3 Chapter conclusion

In this chapter, two ways to address the problem of bandwidth mismatch have been exposed. First, random sampling method is an easy way to minimize the effect of the mismatch between the channels. It consists of adding identical analog circuits to achieve the randomization leading to spread the undesired spurs over the bandwidth. A new implementation has been proposed. It is based on randomizing only the input sampling networks rather than the overall channels. This allows to save power consumption and die area. The limitation of this approach resides in the fact that the overall noise power remains the same so that the SNDR is not improved.

In the second part of this chapter, bandwidth mismatch error calibration has been split into digital estimation and error correction. A comparison of existing digital correction methods show the difficulty to calibrate the bandwidth mismatch error because of the nonlinearity and input dependency characteristic. It has been shown that correction using linear compensation is not sufficient for high frequency and high errors. In this part, a polynomial approach has been evaluated and a simpler implementation has been proposed compared to the one proposed in [77]. After that, existing estimation techniques have been compared, two solutions are highlighted. The first one is based on semiblind estimation where a test signal is used to extract the error. The second method is uses polynomial approximation of the error and tends to estimate a global error which is not useful for mixed calibration techniques. Finally, the choice of a good loss function has been discussed and introduces the following chapter where an extraction solution for bandwidth mismatch error is proposed and detailed.

Chapitre 4

Proposed Detection Technique : Bandwidth Mismatch Estimation

4.1 Introduction

It has been shown in Section 2.3.4 that the bandwidth mismatch error intervenes in both the gain and the phase of the output signal. In the presence of all other errors, the gain error component is combined to the static gain error when the phase error component is additionally combined with the clock skew error. Furthermore, these components are non linear and depend on the input frequency. As a consequence, errors separation becomes unfeasible and error variation makes an online extraction more difficult but necessary. Based on the proposed phase extraction and autocorrelation in Section 3, the loss function owns a unique minimum in the sample interval. This minimum value corresponds to the bandwidth mismatch error. Nevertheless, in the presence of the clock skew error which is more difficult to compensate, this method presents a significant drawback of error correlation. In this chapter, we proposed a bandwidth mismatch estimation technique using gain extraction. This approach will be explained in the second subsection, where a comparison with phase extraction is provided. Subsection 4.2.1.2 is dedicated to the validation of the solution by simulation using a sine wave signal and a CDMA pattern. Furthermore, the impact of static gain and clock skew errors on the estimation is evaluated. The last section takes into account all intrinsic errors in the ADC, a prototype using two ADCs from the market is used as an illustration and measurements at different frequencies are used to validate the proposed estimation technique.

4.2 Proposed Technique Overview

Let us consider a two-channel time-interleaved ADC in order to explain the proposed estimation technique. Nevertheless, the solution can be extended to an M-channel TI-ADC, which can be done by considering one reference channel and estimate the error of each channel compared to this reference. However, some considerations have to be respected, they are explained at the end of this section. We first suppose in this section that all errors, except bandwidth mismatch are already corrected. The impact of gain and time skew error on the proposed technique is discussed after that.

4.2.1 Proposed extraction technique

4.2.1.1 System model

It has been discussed in Section 2.3.4 that during the sampling phase of the i -th channel, the sampling network behaves as a low pass filter imposed by the equivalent R_{on} of the switches and the equivalent capacitor. For simplicity, we consider in our study a first order low pass input filter. Fig. 4.1 illustrates a system model with two channels input filters denoted by H_0 and H_1 followed by the converters ADC_0 and ADC_1 , respectively. Each channel is filtered then sampled at $(kM + i)T$, where i is equal to zero for the top channel and one for the bottom one. M is the number of channels (2 in this case) and k represents the discrete time index. The overall sampling frequency is denoted by $1/T$ and the input signal is bandlimited to π/T , so that the Nyquist criterion is fulfilled.

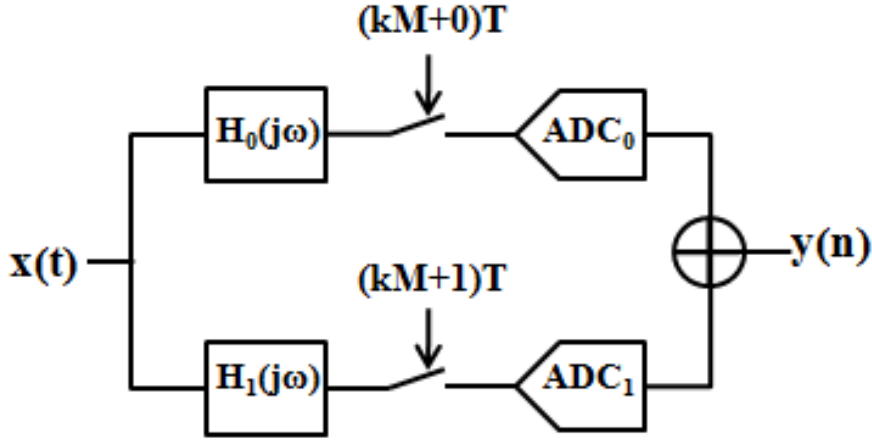


FIGURE 4.1 – 2-channels system model.

Therefore, the i -th channel output can be expressed as :

$$y_i[k] = (1 + g(\epsilon_{\tau_i}))x((kM + i)T + f(\epsilon_{\tau_i})). \quad (4.1)$$

where, $1 + g(\epsilon_{\tau_i})$ and $f(\epsilon_{\tau_i})$ are respectively the gain and the phase of the channel output, T represents the overall sampling period and $\epsilon_{\tau_i} = (\tau_i - \tau_r)/\tau_r$ is the relative time constant error, where τ_r denotes the reference time constant among the channels.

For a first order input filter, one has :

$$\begin{cases} 1 + g(\epsilon_{\tau_i}) &= \frac{1}{\sqrt{1 + (\omega\tau_r(1 + \epsilon_{\tau_i}))^2}}, \\ f(\epsilon_{\tau_i}) &= -\arctan(\omega\tau_r(1 + \epsilon_{\tau_i})). \end{cases} \quad (4.2)$$

in which, ω refers to the input frequency.

For a sine wave input signal, Equation 4.1 can be written as :

$$y_i[k] = \frac{1}{\sqrt{1 + (\omega\tau_i)^2}} \cos[\omega T(kM + i) - \arctan(\omega\tau_i)]. \quad (4.3)$$

In order to highlight how can the gain and the phase contributions separately impact the input signal, let us develop the expression in Equation 4.3 :

$$y_i[k] = \frac{1}{\sqrt{1 + (\omega\tau_i)^2}} \left\{ \cos[\omega T(kM + i)] \cos[\arctan(\omega\tau_i)] + \sin[\omega T(kM + i)] \sin[\arctan(\omega\tau_i)] \right\}. \quad (4.4)$$

where,

$$\cos(\arctan(\omega\tau_i)) = \frac{1}{\sqrt{1 + (\omega\tau_i)^2}}, \sin(\arctan(\omega\tau_i)) = \frac{\omega\tau_i}{\sqrt{1 + (\omega\tau_i)^2}}. \quad (4.5)$$

This is valid only when $-\pi/2 < \omega\tau_i < \pi/2$, which is the case since $\omega\tau_i$ is always less than 1. By plugging Equation 4.5 into Equation 4.4, one obtains :

$$y_i[k] = \frac{1}{1 + (\omega\tau_i)^2} \underbrace{\cos[\omega T(kM + i)]}_{\text{input signal}} + \frac{\omega\tau_i}{1 + (\omega\tau_i)^2} \underbrace{\sin[\omega T(kM + i)]}_{\text{input signal shifted by } \frac{\pi}{2}}. \quad (4.6)$$

According to Equation 4.2, the gain and the phase components due to a channel bandwidth error are frequency dependent and nonlinear dependent of the time constant, which makes the bandwidth extraction more complicated and hence the error accuracy difficult to achieve. In Equation 4.6, it can be seen that by combining the gain and the phase, the channel input filter contribution can be divided into two components. The first one is in phase with the input signal and corresponds to the squared value of the gain, when the second component is observed by shifting the input by $\pi/2$.

Consequently, the bandwidth mismatch error between the two channels which is represented by the difference between the time constants of the two channels can be obtained by estimating each time constant. The latter is retrieved by extracting either the gain or the phase from the channel output as shown in Equation 4.6. One can deduce this result in the frequency domain analysis. In fact, the complex version of the transfer function of the channel i can be expressed as :

$$H_i(j\omega) = g(\epsilon_{\tau_i}) e^{f(\epsilon_{\tau_i})} \quad (4.7)$$

$$= \frac{1}{\sqrt{1 + (\omega\tau_i)^2}} e^{(-\arctan(\omega\tau_i))}. \quad (4.8)$$

The error between the two channels in the frequency domain is the ratio between the two transfer functions, which leads to :

$$\frac{H_i(j\omega)}{H_j(j\omega)} = \frac{\sqrt{1 + (\omega\tau_j)^2}}{\sqrt{1 + (\omega\tau_i)^2}} e^{(\arctan(\omega\tau_j) - \arctan(\omega\tau_i))}. \quad (4.9)$$

If the channels are perfectly matched then :

$$\begin{cases} \frac{\sqrt{1 + (\omega\tau_j)^2}}{\sqrt{1 + (\omega\tau_i)^2}} = 1, \\ \arctan(\omega\tau_j) - \arctan(\omega\tau_i) = 0. \end{cases} \quad (4.10)$$

The first condition means that the two input filter gains are equal and the second one refers to identical phase contributions. Consequently, the bandwidth mismatch error can

be estimated using either gain error extraction or phase error extraction. However, when including all other errors, these components are combined to the static gain and the clock skew errors respectively. Consequently, the errors separation becomes unfeasible.

If we suppose that the static gain and the clock skew are previously compensated, the resolution of these ones needs to be less than the contribution of the bandwidth mismatch error to allow the extraction of this later.

In Fig. 4.2, a comparison between the contribution of the gain error component and the phase component has been illustrated. It shows that along the Nyquist band, the two components are comparable for 0.02% of a bandwidth mismatch error. This accuracy corresponds to the targeted performance of 90dB of SFDR at high frequencies. From these observations, mismatch error estimation can be retrieved from either gain or phase extraction. However, other errors need to be corrected beforehand; static gain mismatch error when the estimation is based on gain extraction and clock skew error if the estimation uses phase extraction. Nevertheless, static gain error is easier to compensate when sharing the same reference between the two channels as discussed in Section 2.3.2.

In the following, we develop the proposed bandwidth estimation method based on gain extraction. First, the squared expression of the i -th channel output represents the power

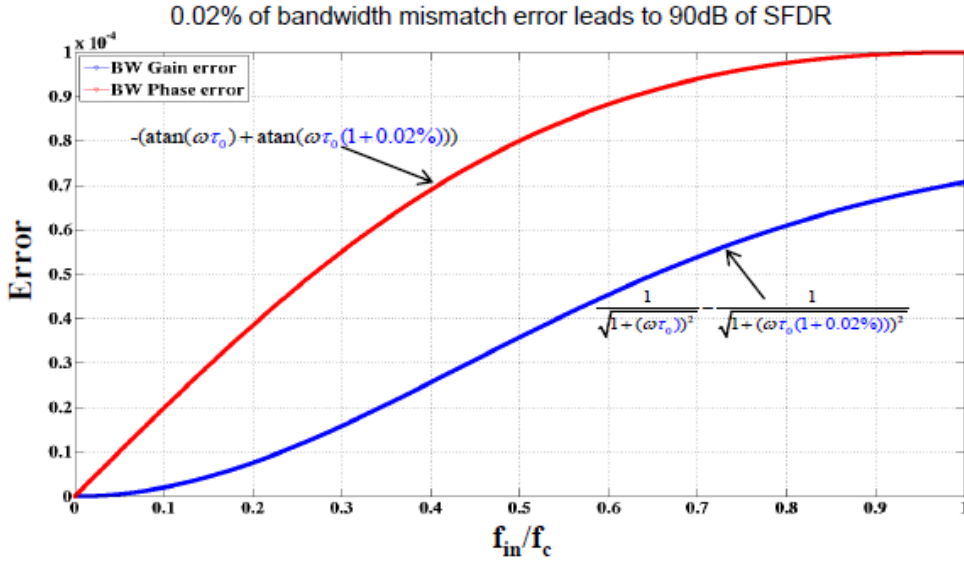


FIGURE 4.2 – comparison between the gain error component and the phase error components due to bandwidth mismatch for $\frac{\Delta\tau}{\tau} = 0.02\%$.

of the signal and is expressed as :

$$y_i^2[k] = \frac{1}{1 + (\omega\tau_i)^2} + \frac{1}{1 + (\omega\tau_i)^2} \cos[2\omega T(kM + i) - 2 \arctan(\omega\tau_i)]. \quad (4.11)$$

where, $i \in \{0; 1\}$. In this equation, the left expression is independent of the input signal meaning that it will appear at the zero frequency as an offset. This term contains the time constant value which is needed to estimate the error. In addition, the term in the right depends on the input signal and the average value is zero if we suppose that the offset is removed beforehand. Furthermore, one can note that if the channels are perfectly matched

the term in the left will be the same for the two channels.

The challenge is then to minimize the difference between the two channels powers which represents the loss function of our model. It is expressed as :

$$\begin{aligned}
 loss[k] &= y_0^2[k] - y_1^2[k] \\
 &= \frac{1}{2} \left\{ \frac{1}{1 + (\omega\tau_0)^2} - \frac{1}{1 + (\omega\tau_1)^2} \right\} \\
 &\quad + \frac{1}{2(1 + (\omega\tau_0)^2)} \cos[2\omega T(kM + 0) - 2 \arctan(\omega\tau_0)] \\
 &\quad - \frac{1}{2(1 + (\omega\tau_1)^2)} \cos[2\omega T(kM + 1) - 2 \arctan(\omega\tau_1)]. \tag{4.12}
 \end{aligned}$$

As already discussed, the first term represents the DC value and highlights the mismatch error between channels. The approach consists of averaging the second term thanks to the sine wave expression to extract the DC term.

Fig. 4.3 illustrates the proposed solution. It is important to notice that the TI characteristic is respected and only the second term in Equation 4.11 is different between the channels since the samples are alternated. However, thanks to averaging, this does not impact the extraction.

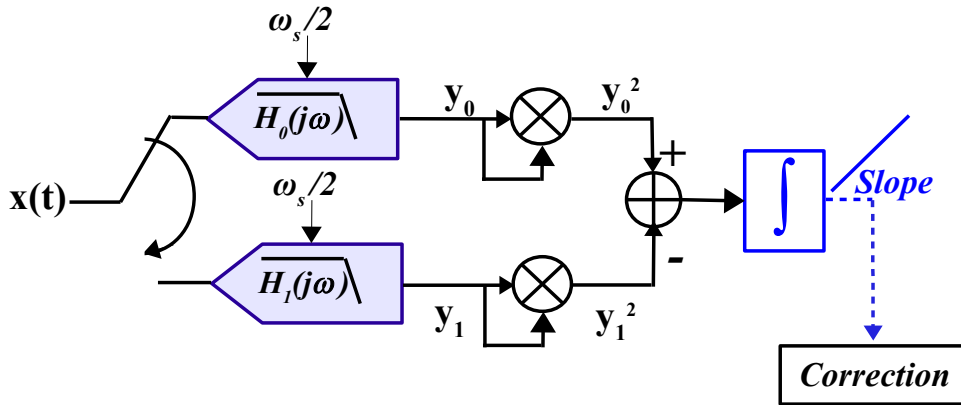


FIGURE 4.3 – The proposed bandwidth mismatch extraction scheme.

1. *Integrator characteristics :*

The averaging of the expression in Equation 4.12 is performed using an integrator. The output of this integrator is characterized by a slope and a trace around this slope. These two functions are described in the following :

- The slope is the difference between the squared channels DC values. From Equation 4.12, we can express the slope as :

$$Slope = \frac{1}{2(1 + (\omega\tau_0)^2)} - \frac{1}{2(1 + (\omega\tau_1)^2)} \tag{4.13}$$

To make the channels perfectly matched, it is clear that the slope must be equal to zero. Therefore, the slope gives an information of how the channels are identical and the latency of the integrator corresponds to the time taken by the integrator to

attain the desired resolution. Regarding the correction, this can be done by tuning the input filters in the analog domain. However this is tricky to reach the precision of 0.02% of mismatch in CMOS technologies. To overcome this limitation, digital correction can be applied at the cost of power consumption and complexity of development.

- The trace of the loss function is represented by the second term in Equation 4.12 and is expressed as :

$$\begin{aligned} \text{Trace}(\tau_0, \tau_1, \omega, k) = & \frac{1}{N} \sum_{k=0}^N \left\{ \frac{1}{2(1 + (\omega\tau_0)^2)} \cos[2\omega T(kM + 0) - 2 \arctan(\omega\tau_0)] \right. \\ & \left. - \frac{1}{2(1 + (\omega\tau_1)^2)} \cos[2\omega T(kM + 1) - 2 \arctan(\omega\tau_1)] \right\}. \quad (4.14) \end{aligned}$$

where N is the number of samples. It is function of the mismatch error and the input frequency. The maximum thickness of this trace fixes the minimum threshold value that must be chosen for the integrator and defines the convergence time of the integrator. In fact, in order to make the trace equal to zero, at minimum one period is needed to zeroing the sine wave average and then retrieving the right estimate value of the slope. Nevertheless, it is preferable to take more than one period to minimize the trace. This stretch of time determines how long do the slope take to reach the threshold. Finally, the convergence time of the integrator tell us how long do the slope take to approach the zero after correction.

2. Limitations :

The main limitation of the model proposed in Fig. 4.3 appears at the input frequency $\omega_{\text{in}} = \omega_s/4$ where the input signal and the spur generated by TI structure overlap (spur at $\omega_s/2 - \omega_{\text{in}} = \omega_s/4$). Consequently, the integrator does not distinguish the signal from the undesired tone and hence diverges. Therefore, the input signal at $\omega_s/4$ cannot be treated by the integrator and needs to be filtered. Especially because the estimation needs to operate online, meaning that no information is provided to avoid this problem. To do so, a notch filter is set before integration, around $\omega_s/4$ as shown in Fig. 4.4.

Besides this limitation, the notch filter allows to deal with the high values of the

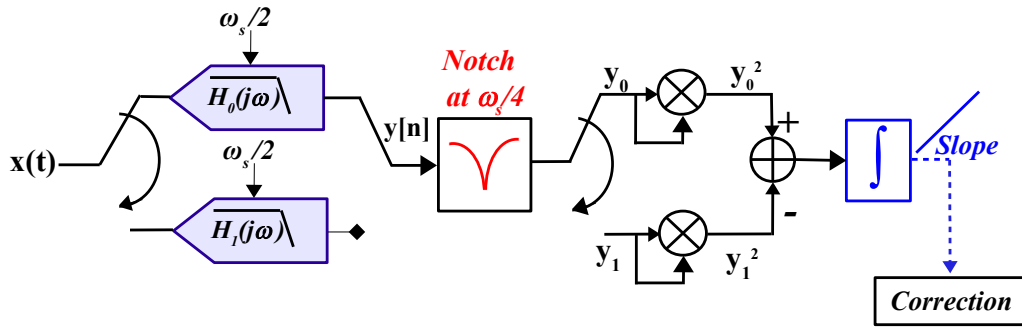


FIGURE 4.4 – The proposed bandwidth mismatch extraction scheme including the notch filter around $\omega_s/4$.

threshold around $\omega_s/4$. In fact, at this frequency, $\omega_{\text{in}}T = \pi/2$ which leads to : $\sin(2\omega_{\text{in}}T(kM + i)) = 0$ and $\cos(2\omega_{\text{in}}T(kM + i)) = \pm 1$ depending on whether i refers to channel 0 or 1. Consequently, the trace becomes :

$$\begin{aligned} \text{Trace}(\tau_0, \tau_1, \omega_s/4, k) = \frac{1}{N} \sum_{k=0}^N 1 \left\{ \frac{1}{2(1 + (\omega_s\tau_0)^2)} \cos[2k\pi - 2 \arctan(\omega_s\tau_0)] \right. \\ \left. - \frac{1}{2(1 + (\omega_s\tau_1)^2)} \cos[\pi(2k + 1) - 2 \arctan(\omega_s\tau_1)] \right\}. \end{aligned} \quad (4.15)$$

where :

$$\begin{cases} \cos[2k\pi - 2 \arctan(\omega_s\tau_0)] = \cos[2 \arctan(\omega_s\tau_0)] \\ \cos[\pi(2k + 1) - 2 \arctan(\omega_s\tau_1)] = -\cos[2 \arctan(\omega_s\tau_1)]. \end{cases} \quad (4.16)$$

This leads to an expression, independent of the sample. The trace is then expressed as :

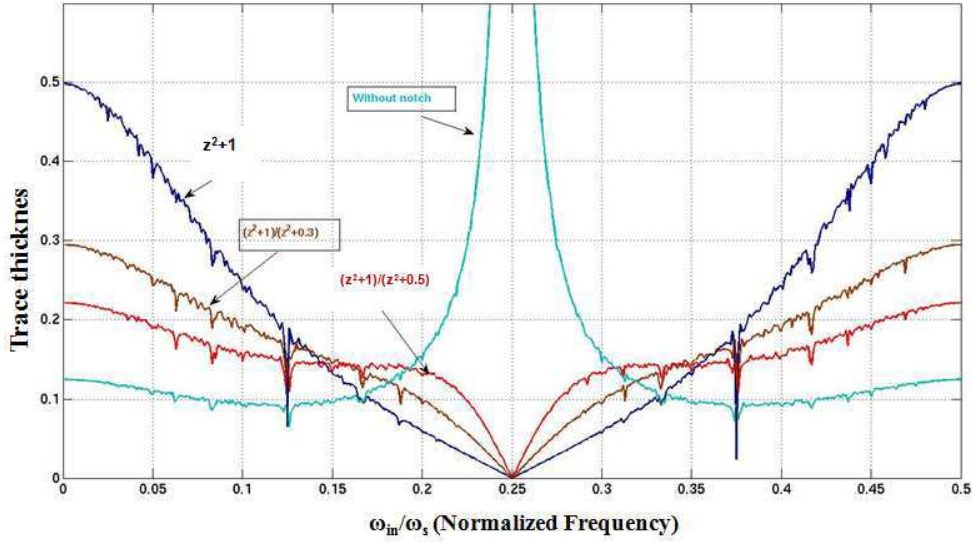
$$\begin{aligned} \text{Trace}(\tau_0, \tau_1, \omega_s/4) = \\ \frac{1}{2(1 + (\omega_s\tau_0)^2)} \cos[2 \arctan(\omega_s\tau_0)] + \frac{1}{2(1 + (\omega_s\tau_1)^2)} \cos[2 \arctan(\omega_s\tau_1)]. \end{aligned} \quad (4.17)$$

Finally, after some manipulations based on Equation 4.5, the trace is constant and is equal to :

$$\text{Trace}(\tau_0, \tau_1, \omega_s/4) = \frac{1 - (\omega_s\tau_0)^2}{2(1 + (\omega_s\tau_0)^2)^2} + \frac{1 - (\omega_s\tau_1)^2}{2(1 + (\omega_s\tau_1)^2)^2}. \quad (4.18)$$

This is the maximum value of the trace since the sine expressions in Equation 4.16 are maximum. According to this, the trace thickness is maximum and the threshold needs to be very high at $\omega_s/4$. To overcome this problem, the notch filter make the trace thickness figure as flat as possible and fix beforehand the threshold value. In Fig. 4.5, cyan curve represents the trace thickness along the input frequencies. As explained before, its value is maximum around $\omega_s/4$ which would make the threshold variable if we want to minimize the convergence time. In Fig. 4.5, different filters were applied in order to remove the narrowest band around $\omega_s/4$ in one hand and make sure to choose a constant threshold in the other hand. The simplified notch filter $1 + z^{-2}$ has been used in [37, 36] and can be sufficient to overcome this problem, however a large band around $\omega_s/4$ is filtered which is not desired. Indeed, in that case the signal is attenuated which can make small accuracies difficult to obtain.

One can note that the exposed problem is a special case of a two input frequencies, the first one is set at ω_{in} and the second one is set at $\omega_s/2 - \omega_{\text{in}}$. In that case, each input signal overlays with the spurious tone of the second one. Unfortunately, it is not possible to deal with this problem online, in fact, one can imagine first treating the band $[0, \omega_s/4]$ to avoid the spurious tones of the second band $[\omega_s/4, \omega_s/2]$. To do so, filtering has to be done before the presence of the spurious components in the wanted bandwidth which is only possible in the analog part. However, this solution is more complicated and causes additional errors in the system. It will be shown in the following section that statistical behavior of the CDMA signal can be benefic to

FIGURE 4.5 – Notch Filter at $\omega_s/4$

avoid such problems. In fact, as the presence of each signal in the bandwidth has its own probability, one can imagine that the two signals are rarely present at the same time for a long time.

In this section, we have considered the presence of unique bandwidth mismatch error. The validation is provided in the following section using in one hand a sine wave signal, then a CDMA as an input signal in the other hand. After that, the impact of other errors is discussed. It consists of the impact of the static gain error and the clock skew error on the extraction.

4.2.1.2 Simulation and validation

In this section, we present the performances of the proposed extraction technique for a two-channel 16-bit time-interleaved converter. First we consider an ideal correction equivalent to tuning the analog filters. In this study, static gain and clock skew are assumed to be previously compensated. Bandwidth mismatch is set to 0.53% and the cut-off frequency of the 0-th channel input filter is given by $\omega_c = \omega_s/2$ in this example.

– Sine wave input use case :

This first example illustrates the case of a sinusoidal input at $\omega_{in} = 0.2\omega_s$. The threshold is equal to three times the trace thickness in this example and the correction step is 0.1%. The filter coefficients updates change the slope value when this one exceeds the threshold to finally swing around zero after about 25000 samples as shown in Fig. 4.6. The mismatch error between the two channels reaches 0.03% equivalent to a 95 dB of SFDR for this input frequency (see Fig. 4.7).

– CDMA use case :

The second use case concerns a CDMA input signal. This example shows that the algorithm limitations, previously pointed do not impact the error extraction. Basically, the CDMA signal can be considered as a multi sine wave with a certain probability

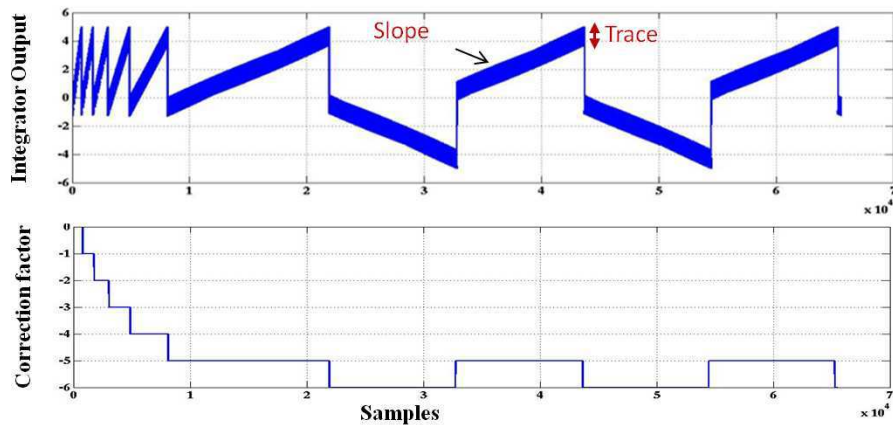


FIGURE 4.6 – Integrator output for a sine wave case

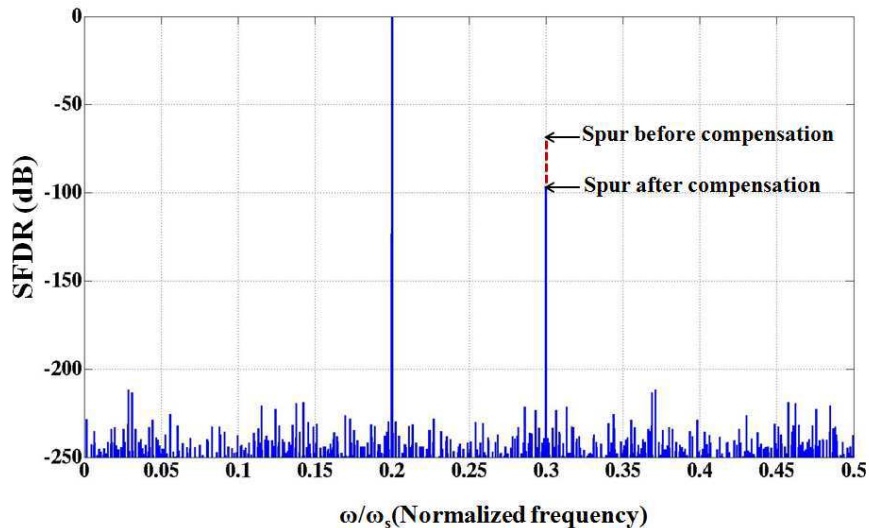


FIGURE 4.7 – Improvement of the SFDR after Compensation from 70 dB to 95 dB

for each signal. Fig. 4.8(a) shows a four-pattern CDMA signal sampled at 184 Msp s around $0.2\omega_s$. One can see the presence of the signal around $\omega_s/4$ which generates overlapped signal with spurious tones and hence the estimator diverges without the notch filter. In Fig. 4.8, the notch filter is present. We can see the presence of the spurious tones due to bandwidth mismatch errors corresponding to $\omega \pm \omega_s/2$. The mismatch before compensation is set to 1.3% in this example. In Fig. 4.9, the convergence of the integrator can be seen in the presence of the notch filter. Moreover, the SFDR is then improved up to 95 dB after the correction as shown in Fig. 4.7 (b).

Since we have proven the use of the proposed bandwidth mismatch error estimation technique, let us first discuss the impact of the gain and timing skew error on this extraction. The presence of other errors such as aliasing and harmonic distortion errors is considered in part 2 using measured data.

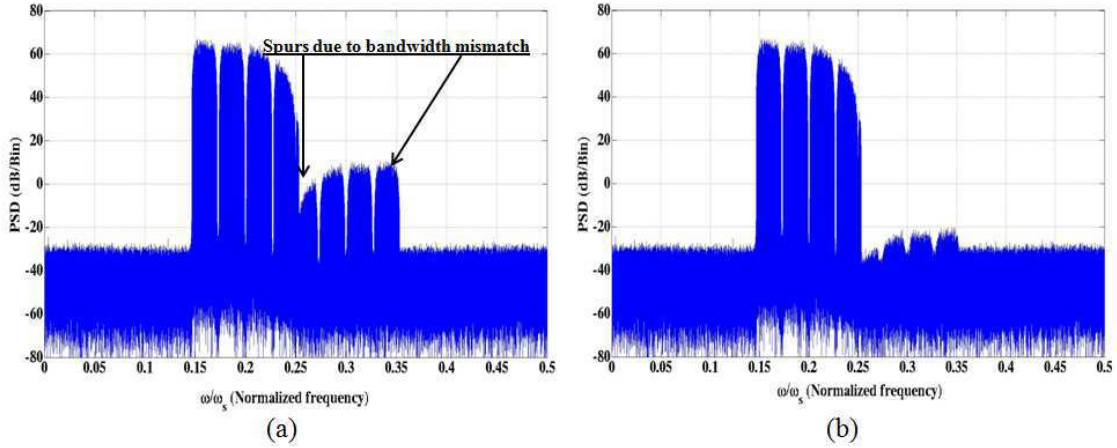


FIGURE 4.8 – CDMA signal input after the notch filter (a) before compensation (b) after compensation.

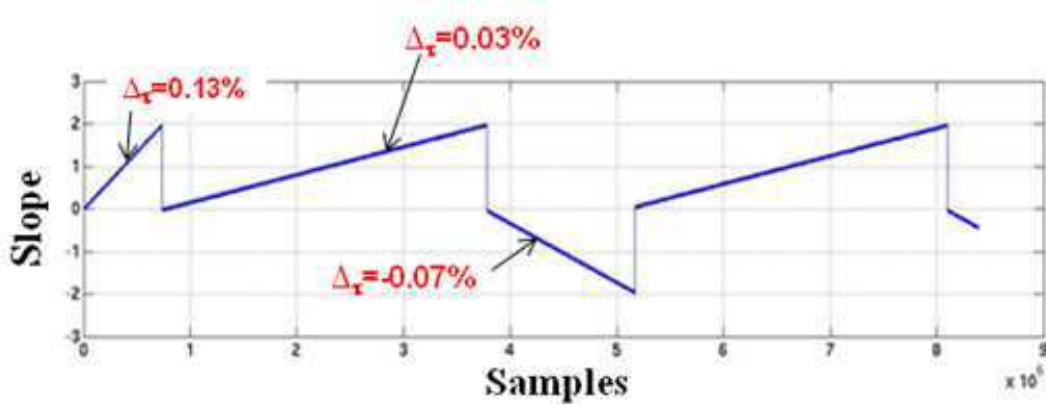


FIGURE 4.9 – Integrator output for a cdma use case.

4.2.2 Static gain and clock skew impact on the extraction

The bandwidth error estimation technique proposed in this chapter is based on gain extraction. The advantage of this approach is that static gain errors are easier to compensate than clock skew errors. In addition, as the best of our knowledge, most of the estimation techniques based on phase extraction need gain calibration beforehand [37, 36, 66, 80, 81]. In Fig. 4.10, the impact of the static gain error on the bandwidth mismatch error estimation is illustrated. We assume that only a static gain error is present (1% in this example) and the two channels are matched in terms of bandwidth and clock skew. In that case, the estimator detects a bandwidth error and consequently the correction block compensates the static gain but generates a phase error, which more degrades the SFDR even more. As discussed in Section 2.3.2, the static gain comes mainly from different reference generators and by sharing the same reference minimizes the presence of this error. Moreover, this error is independent of the input frequency and can be calibrated by either offline or by design. Regarding the impact of clock skew, it is straightforward that this error does not alter the on the proposed bandwidth mismatch estimation since the latter is based on gain extraction. This is illustrated in Fig. 4.11 where the static gain is supposed to

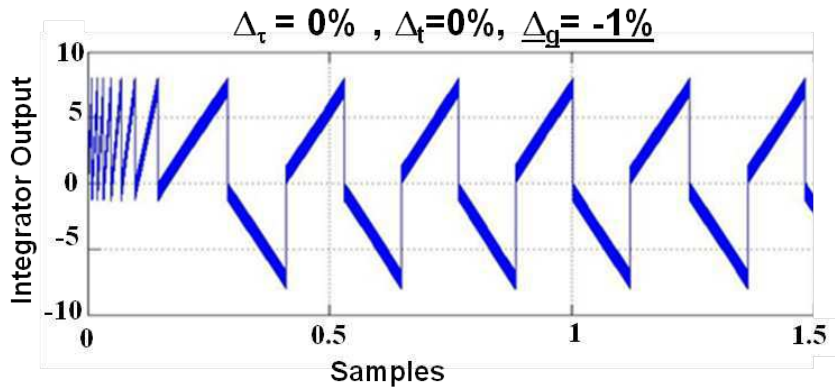


FIGURE 4.10 – Impact of the static gain on the bandwidth mismatch extraction.

be compensated. Bandwidth mismatch error is set to 0.53% and different values of clock skew mismatches are set to : -1% , 0% and 1% compared to the sampling frequency. The convergence of the integrator is identical for the three cases and clock skew errors remain the same while bandwidth mismatch can better be corrected in analog part in this case.

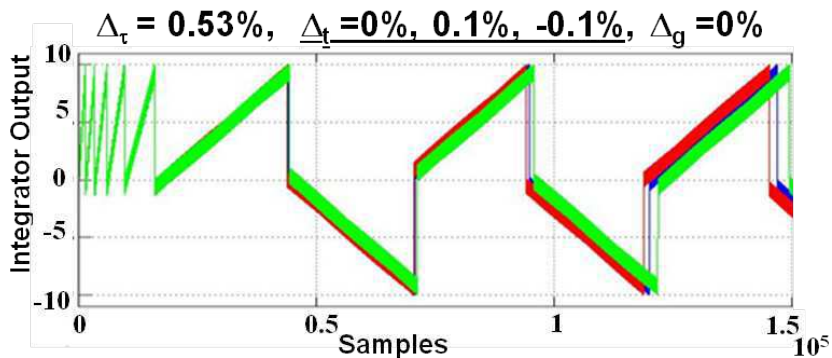


FIGURE 4.11 – Impact of the static gain on the bandwidth mismatch extraction.

4.2.3 Conclusion

In this section, an online estimation technique for a bandwidth mismatch error has been provided. It is based on gain extraction and the minimization of the power difference between the two channels. In fact, the comparison between the gain and the phase error components due to bandwidth error shows that they are comparable at the desired accuracy of 0.02%. Consequently, bandwidth error can either be retrieved from gain or phase error. However this requires the static gain mismatch error to be corrected beforehand, which can be done using offline calibrations or can be highly minimized by design.

The proposed method requires the use of notch filter around the frequency $\omega_s/4$ because the input signal and its generated spur appear at the same frequency and the integrator cannot distinguish between them. It is important to notice that for an M-channels TI-ADCs, the filter must be designed to present notches at multiple of $\omega_s/2M$ which requires more attention in its design.

The proposed solution has been validated using at first a sine wave signal. Then a wide-band signal, CDMA to override the issue of two symmetrical signals thanks to its statistical characteristic.

Finally, the impact of static gain and clock skew mismatch errors have been discussed in the last section and consolidate the need of static gain calibration before applying the algorithm to bandwidth mismatch estimation.

In the next section, the validation of the proposed technique is performed using a board prototype with two ADCs from the market. This includes intrinsic errors of each ADC and therefore measure the robustness of the proposed solution.

4.3 Prototype

4.3.1 Introduction

Initially, the implementation of the proposed solution would be done using a FPGA at the output of 2-channels TI-ADC on the same board ; each one running at 250 Msps in order to achieve the desired 500 Msps. Unfortunately and because the unavailability of the board in time, the validation of the proposed estimation technique has been done by post processing the measured data coming from two channels on the same board with different inputs. As discussed in the previous section, bandwidth mismatch estimation requires static gain compensation beforehand. Moreover, for data acquisition, a great care must be done regarding the employed equipments. After a brief description of the board, the optimized test setup with the different equipments is described in Subsection 4.3.2. The last subsection is dedicated to the results obtained by post processing the measured data.

4.3.2 Board description and test setup

Fig. 4.12 corresponds to the board used for the validation of the proposed estimation technique. It consists of two ADCs, each one running at 153.6 Msps with a resolution of 14 bits. Therefore, in order to respect the time-interleaved architecture the clocks of the two ADCS are in opposition of phase so that the global input signal is finally sampled at 307.2 Msps.

In the following, test setup considerations are exposed and the steps that allow to measure the TI-ADC output signal are provided.

The prototype used to measure the TI-ADC output is described in Fig. 4.13 where the various equipments are explained as :

- The signal generator needs to have low jitter especially for very high input frequencies (above 300-400 MHz).
 - The 2 signal generators need to be synchronized to share the same reference signal (10 MHz) as an input and ensure a coherency for both signals.
 - The band-pass filters are mandatory for input signal frequency to get rid of the harmonics generated by the signal generator and obtain a pure sine-wave at the
-

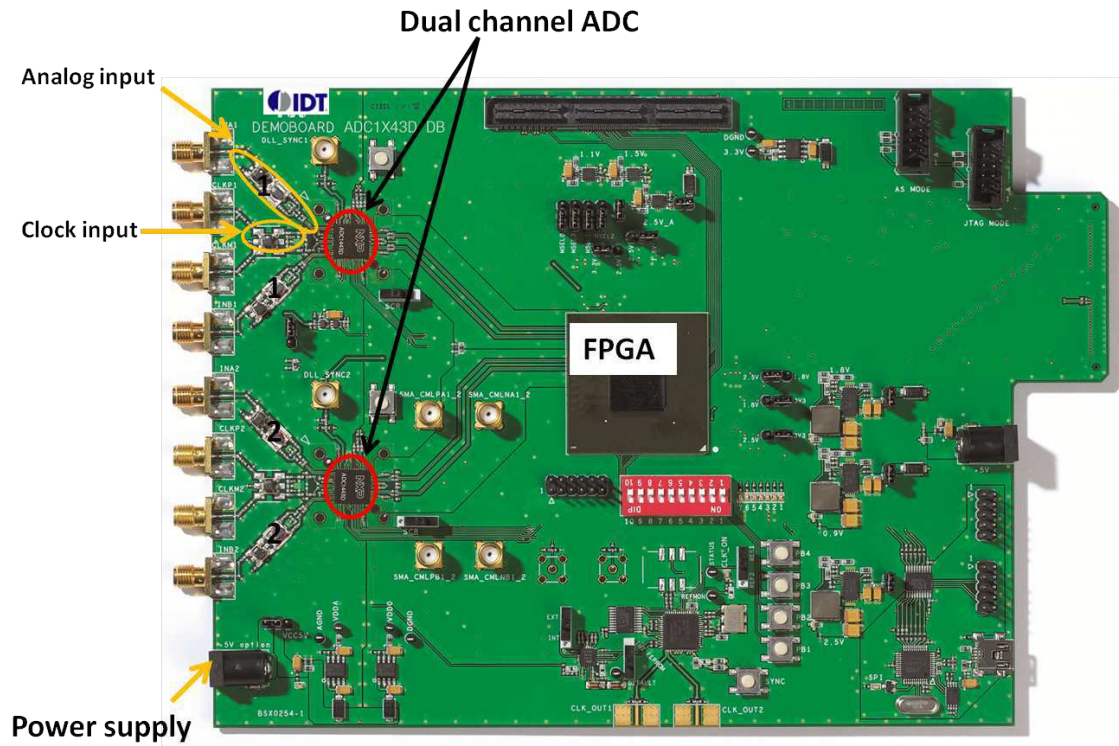


FIGURE 4.12 – Board of measurement including 2 ADCs used for a 2 channel TI-ADC

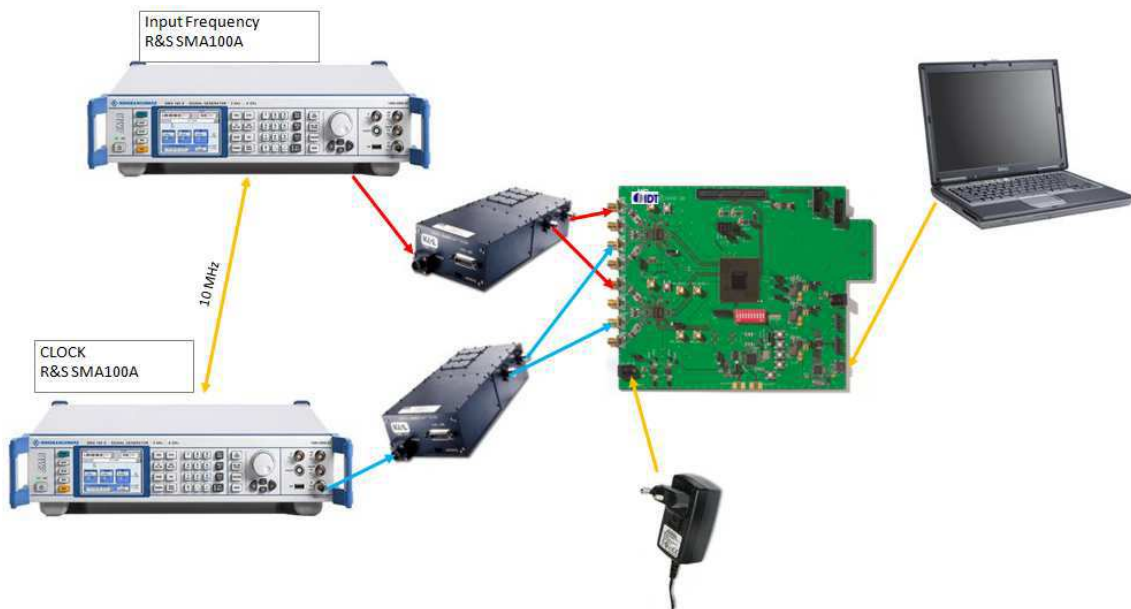


FIGURE 4.13 – Lab environment and test setup considerations

input of the ADC. The band-pass filter for the sampling frequency is required to minimize the noise for high resolution ADC (= 14 bit).

- The Personal Computer is used to collect the measured data for post processing (calibration and bandwidth estimation).

Finally, the chosen settings for measurements are :

- The sampling frequency is fixed to $F_s=307.2$ Msps (each clock generates a 157.6 Msps).
- The input signal amplitude is set to -1 dBFS.
- The input impedance of each ADC is two times the impedance of a single ADC because the same signal is shared between the two channels. Consequently, the input bandwidth of the TI-ADC is divided by 2 and is approximatively equal to 600 MHz.

4.3.3 Measurements results

Acquisitions at several input frequencies have been done. First, the process at low frequencies allows the extraction of the static gain mismatch error (step 2). Then, at high frequencies the proposed estimation method is applied for bandwidth mismatch extraction. The steps in Fig. ?? are described in the following :

- First, the offset mismatch error due to TI-ADC is easily removed by subtracting the mean value of each channel whatever the input frequency.
- Then, the static gain error is extracted at low frequencies. The input frequency $f_{in} = 4.43MHz$ was chosen for this first post processing where the generated spur level at $\frac{f_s}{2} - f_{in}$ is equal to 70dB as illustrated in Fig. 4.14. One can note that, the ratio $\frac{f_{in}}{f_c} = \frac{4.43MHz}{600M}$ is equal to 0.0073 and hence the bandwidth mismatch effect is neglected (see Section 2.3.4 Fig. 2.14).

In order to extract the static gain mismatch between the two ADCs, the proposed solution for bandwidth mismatch estimation can be used since it is based on the gain extraction. In that case, the static gain error was estimated using a feedback loop factor. In fact, The lower channel is multiplied by a certain correction gain iteratively until the slope is sufficiently minimized. The chosen step for this operation is set to 0.002% corresponding to an SFDR due to gain mismatch error equal to 100 dB as shown in Section 2.3.2 Fig. 2.7. Finally, the convergence leads to a static gain resolution equal to 0.056% which improves the spur from 70 to 75 dBc as shown in Fig. 4.15. This extracted value will be considered as constant at high frequencies.

- Contrary to the bandwidth mismatch error, the clock skew can be extracted at low frequencies. In fact, once the static gain is compensated, the phase difference between the fundamental and the remaining spur is approximatively equal to 90° . It corresponds to the clock skew mismatch error as already explained in Subsection 4.2.1.1 and labelled in Fig. 4.15 as "*spur wo gain*" and is equal to 75 dB.

In order to extract the value of the clock skew error, Equation 2.29 is used and the calculated mismatch error is 12.75 ps. This value does not depend on the input frequency and hence can be used at high frequencies to highlight the remaining bandwidth mismatch error at the TI-ADC output. The technique exposed in [36] has been used and allows to compensate the spur by 21 dB going from 75 to 96 dB without the bandwidth mismatch error.

- After DC gain and clock skew compensation, the remaining error is assumed to be due to bandwidth mismatch which degrades with high input frequencies. The input frequency is set to 120 MHz in this test, which leads to an additional spur due to

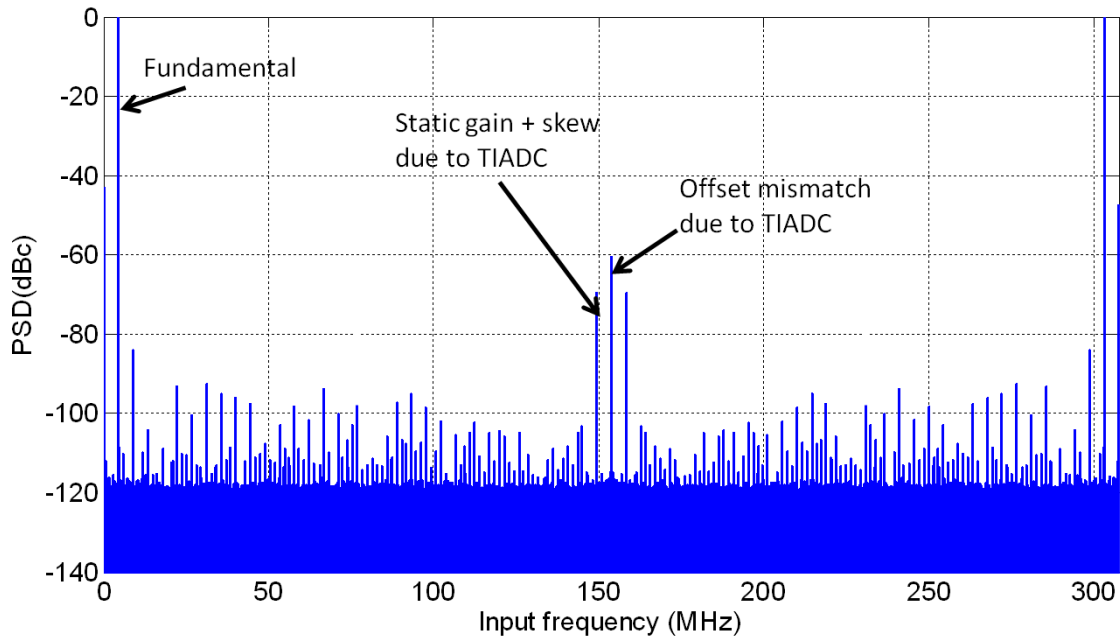


FIGURE 4.14 – Spectrum at the TI-ADC output for $f_{in} = 4.43$ MHz.

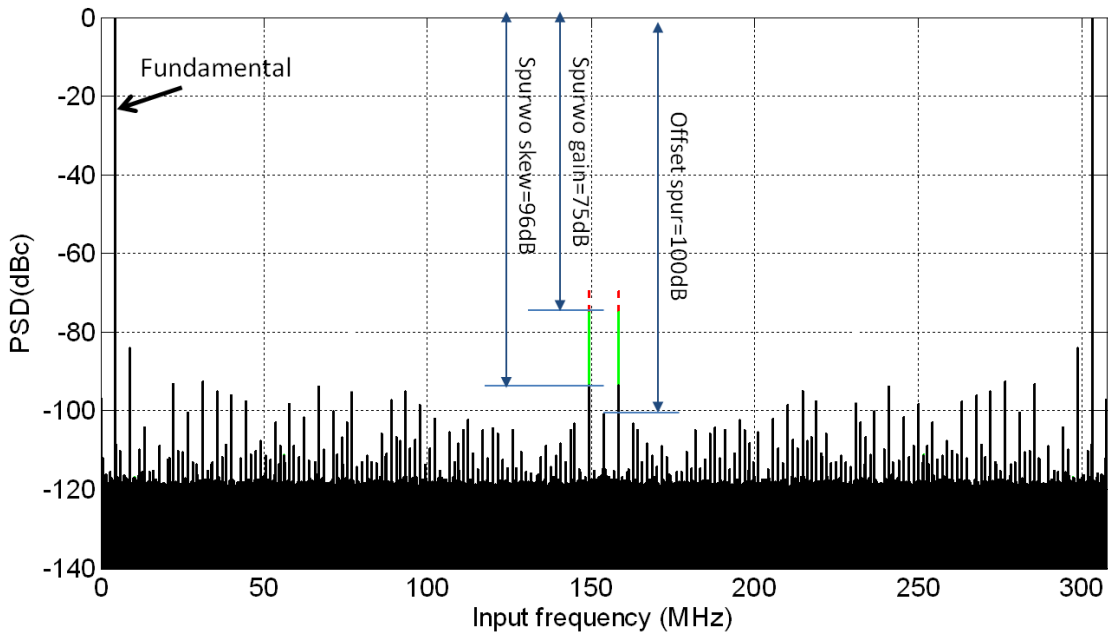


FIGURE 4.15 – Spectrum at the TI-ADC output for $f_{in} = 4.43$ MHz after static gain and clock skew correction and without offset mismatch error due to the TI-ADC.

gain, clock skew and bandwidth mismatches at 33.6 MHz, equal to 46 dB before correction. Fig. 4.16 shows the spectrum at the output of the TI-ADC. The impact of the gain is very small and only 0.01 dB of improvement has been observed after static gain compensation (the extracted factor of 0.056% has been used). In order to estimate the bandwidth mismatch error, some assumptions are taken into account :

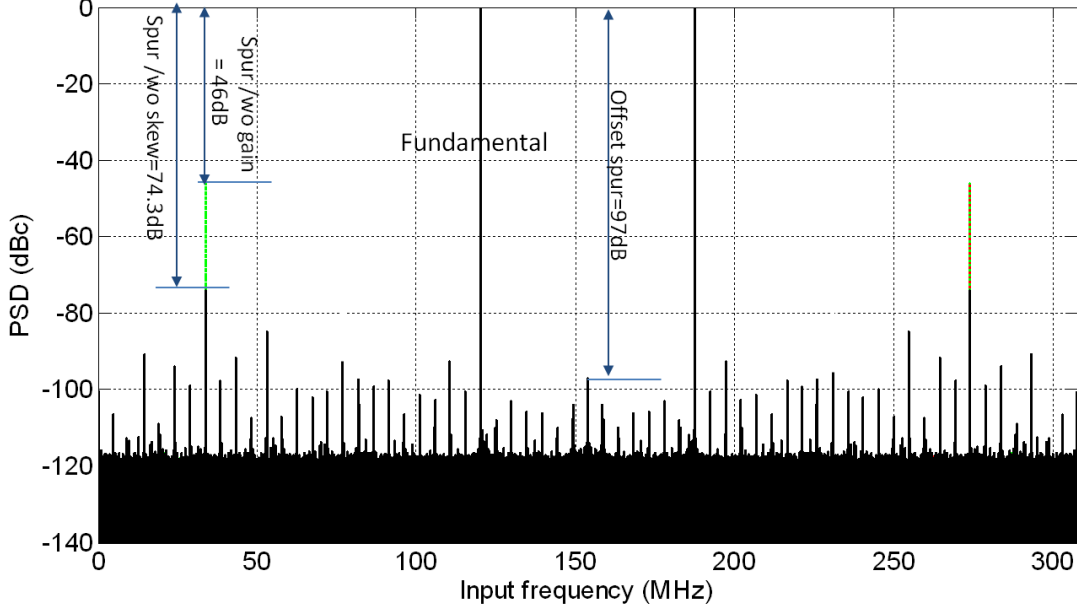


FIGURE 4.16 – Spectrum at the TI-ADC output for $f_{in} = 120$ MHz after static gain and clock skew correction. The remaining error corresponds to the bandwidth mismatch error.

- First, we assume that the spurious tone includes only the bandwidth mismatch error.
- Then in order to apply the proposed technique in Section 4.2, we consider a first order input filters.

Therefore, the slope at the integrator output in Equation 4.13 is expressed as :

$$Slope = A_{max}^2 \frac{1}{2(1 + (f_{in}/f_c)^2)} - \frac{1}{2(1 + (f_{in}/f_c(1 + \epsilon_{tau}))^2)} \quad (4.19)$$

where f_c represents the bandwidth of the overall ADC, ϵ_{tau} denotes the relative bandwidth mismatch error and A_{max} is the amplitude max of the output signal.

From the equation above, one can deduce the expression of ϵ_{tau} , which is :

$$\epsilon_{tau} = \frac{f_c}{f_{in}} \sqrt{\frac{1}{\frac{1}{1 + (\frac{f_{in}}{f_c})^2} - 2 \frac{Slope}{A_{max}^2}} - 1} - 1 \quad (4.20)$$

In order to validate the uniqueness of the extracted value, it is measured for different input frequencies using expression in Equation 4.13. In this test, $A_{max} = 3.62V$ and the cut-off frequency is equal to 600 MHz. Fig. 4.17 illustrates the integrator output in which the measured slope is done for two input frequencies $f_{in} = 120$ MHz and $f_{in} = 180$ MHz. In one hand, Fig. 4.17 (a) shows the measured slope for $f_{in} = 120$ MHz which is equal to $0.0023 V^2$. This corresponds to an extracted bandwidth mismatch error of 0.47 % leading to a spur level of 66 dB. In the other hand, the measured slope for $f_{in} = 180$ MHz (Fig. 4.17 (b)) is equal to 0.0048 % and leads to an estimated bandwidth mismatch error of 0.48% (spur level=63 dB) which perfectly match with

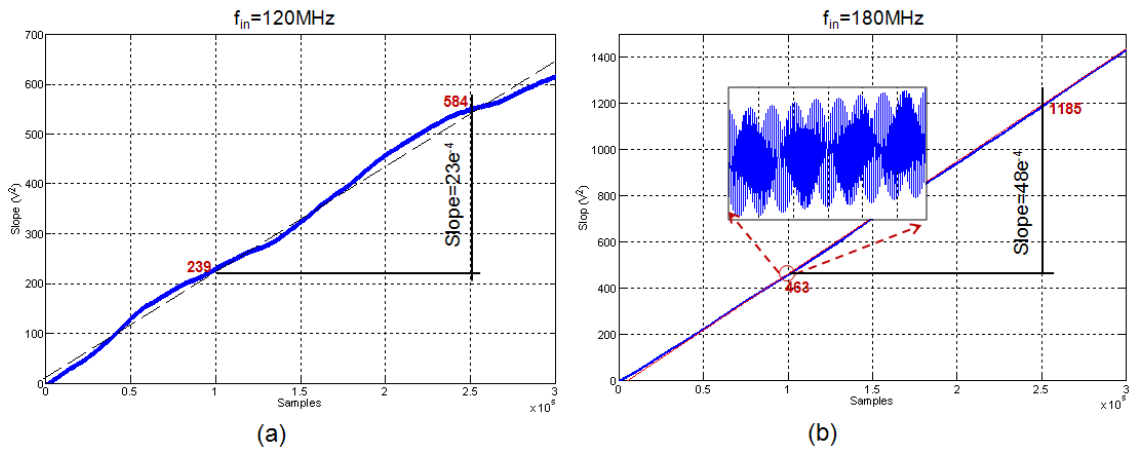


FIGURE 4.17 – Integrator output for two input frequencies : (a) $f_{in} = 120$ MHz and (b) $f_{in} = 180$ MHz.

the previous test.

Finally, the proposed method based on gain extraction can be compared to the bandwidth mismatch error estimated using the phase extraction. In fact, the skew can also be measured in low frequencies, the remaining phase error refers to the bandwidth error. Fig. 4.18 shows variations in the measurements, which is problematic for exact bandwidth estimation. This can be explained by the fact that the two channels have different references on one hand which leads to a variation of the static gain. On the other hand, kickback of the charges changes the phase of the signals and causes variation on the skew between the channels. However, these two problems can be overcome by using the same reference for gain error reduction and use an input buffer for impedance matching.

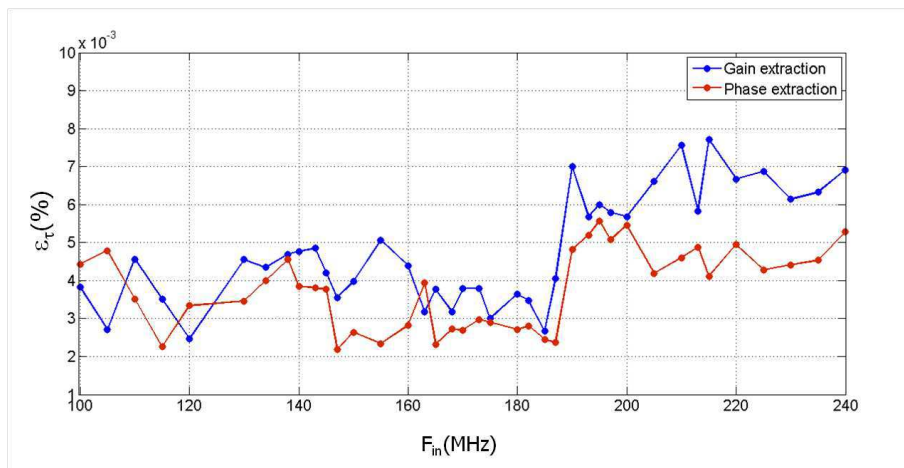


FIGURE 4.18 – bandwidth mismatch estimation based on the proposed solution (blue curve) and error calculation using phase measurements (red curve)

Now that we have estimated the spur level at 120 MHz due to bandwidth mismatch, let us compare this value to the remaining error after clock skew compensation using the technique in [36]. The results are summed up in Tab. 4.1. The authors propose

to shift the input signal by 90° in order to estimate then compensate the generated spur. However, the bandwidth mismatch impacts this digital compensation. In fact, when applying this, the remaining error for bandwidth mismatch is about 74 dB meaning that part of the phase component due to bandwidth mismatch is compensated. Nevertheless, this impact can be overcome using analog correction for both clock skew and bandwidth mismatch errors.

f_{in} (MHz)	offset	spur	$spur_{wogain}$	$\hat{\epsilon}_\tau$	ϵ_τ [36]
4.43	60 dB	70 dB	75dBc	>96 dB	>96 dB
120	60 dB	45.99 dB	46 dB	66dB	74.3 dB

TABLE 4.1 – Mismatch spur before and after static gain and clock skew mismatch compensation

where :

- *offset* : Offset mismatch spur due to TI-ADC.
- *spur* : Gain+skew+bandwidth mismatch spur due to TI-ADC.
- *spur_{wogain}* : Skew+bandwidth mismatch spur due to TI-ADC.
- $\hat{\sigma}_\tau$: Estimated Bandwidth using the proposed solution in this chapter.
- σ_τ : Bandwidth error after skew correction proposed in [36].

4.4 Chapter conclusion

In this chapter, we have proposed a new bandwidth mismatch estimation technique. It is based on the extraction of the gain component and error. This chapter is divided into two sections : in the first section, we have detailed the proposed solution. A comparison between the gain and the phase components due bandwidth mismatch error shows that they are comparable for the desired error accuracy. However, in the presence of other errors due to static gain and clock skew mismatches, the estimation becomes more difficult. Nevertheless, static gain error is easier to compensate than the clock skew which generates a nonlinear error regarding the input signal. Therefore, the static gain is compensated either offline or by design before applying the estimation of the bandwidth error.

It has been shown in this section the necessity of using a notch filter around the frequency $\omega_s/4$ where the signal and its generated spur appear at the same frequency. This is extendable to M channels TI-ADC where notches at each frequency multiple of $\omega_s/2M$ are needed. Simulations have been provided to validate the proposed technique using a sine wave signal and a WCDMA pattern has proven that the extraction is not impacted by the presence of symmetrical signals which overlays with the spurs. At the end of this first section, the impact of the static gain on the estimation has been highlighted when the clock skew mismatch error does not intervene on the extraction.

In the second section, a prototype was presented to validate the proposed solution where all intrinsic errors of two ADCs have been taken into account. The test setup conditions have been presented and the board has been described. The static gain error was firstly compensated at low frequencies (4.43 MHz) using the same technique explained in the first section. The remaining spur at this frequency includes only the clock skew mismatch error which has been calculated thanks to the expression in Equation 2.29. After that, the

processing at high frequencies allows to extract the bandwidth mismatch error using the proposed estimation technique.

As a result, after compensating a static gain error of 0.056%, the remaining spur level at $f_{in} = 120$ MHz is equal to 46 dB where 66dB corresponds to bandwidth mismatch error estimation using the proposed solution. This one leads to an error of about 0.47%.

Conclusion and Perspectives

Conclusion

The evolution of wireless communications moves towards higher data rate analog to digital converters (ADCs). To break this bottleneck, time interleaving is an efficient way to increase the speed while maintaining a good accuracy. Its main idea consists of distributing signal samples between M ADCs operating each at the overall sampling frequency divided by the number of channels. The benefit of this approach is to increase the conversion rate while maintaining the same operation frequency of the analog blocks. An important condition to achieve a good reconstruction of the signal at the digital back-end in TI architecture is that all channels must be identical. Unfortunately, due to process and environment variations, each channel has a different behavior. These mismatches among channels generate undesired spectral components and can significantly degrade the linearity (SFDR) and the resolution (SNR) of the system. These distortions are created by periodic mismatch factors such as offset, gain, timing and bandwidth which increase with the number of ADCs. We have been interested in this thesis on the last error which is more complicated to compensate and less studied than other errors.

First, the introduction details the motivations of the thesis and provides the list of the different contributions during this thesis.

Then, Chapter 1 explains the different performance parameters of an ADC including static and dynamic specifications. These latter were useful to compare the performances of existing architectures in terms of resolution, speed and power consumption. Compared to other architectures including flash, SAR and Sigma Delta ADCs, it has been shown that pipeline ADC is the best suited for the targeted base station application. Furthermore, in order to go faster, time-interleaved pipeline architecture can be used. In fact, parallelization of the ADCs improves certainly the speed and maintains a reasonable power consumption and consequently improves the figure of merit of the ADC. At the end of this chapter, the need of high speed, high resolution ADC in a wireless base station transceiver has been justified by highlighting the impact of the different blocks in the RF chain on the ADC which is the last analog (mixed signal) block and hence the most challenged element. Finally, the desired specifications have been summed up in this chapter.

The second chapter has been dedicated to the TI architecture. Due to process and environment variations, mismatches occur between the different channels. Firstly, a global model has been provided and has shown the impact of the these different errors of the TI-ADC in time and frequency domains. Then, each error has been detailed separately in order to highlight the degradation of the SFDR in the presence of each error. Moreover, a

quantification of the bandwidth mismatch errors was provided and shows the importance of compensating this error. It has also been shown that bandwidth mismatch error combines frequency dependent and non linear gain and phase components, which makes its extraction difficult especially, in the presence of other errors such as static gain and clock skew mismatch errors. The last subsection of this chapter shows the degradation of the SFDR when all errors are combined : static gain, clock skew and bandwidth mismatch. In addition, based on existing calibration circuits for gain and clock skew errors, an analysis for the remaining degradation including mainly bandwidth mismatch error was provided.

In Chapter 3, an overview of existing calibration techniques for the bandwidth mismatch error has been done. Calibration includes estimation and correction. When estimation is generally achieved in digital part, correction can be done either in digital or analog domain. This latter is preferred to digital solution for its low power consumption, however, it is difficult to attain very high accuracies with actual technologies. It has been shown in correction subsection that compensating the non linear phase due to bandwidth mismatch using linear factor may not be sufficient and correction requires more complex filters. A simpler development of polynomial approximation filters based on farrow structure has been proposed and the simulation results are very promising.

Regarding the estimation, very few solutions have been proposed in the literature. As the best of our knowledge, only two techniques exist and were detailed in this chapter. The first one called semi-blind technique, consists of adding a test signal that is used to extract the mismatch error. Its main drawback is the generation of the test signal which is difficult to obtain due to jitter and skew errors. Moreover, such a solution cannot be used for integrated ADCs where full background calibration is required, however it can be suitable for instrumentation. The second solution is based on polynomial approximation where a global error is extracted. However, analog correction cannot be applied since the errors cannot be distinguished. Finally, the requirements for a good choice of the loss function were studied and have been validated by simulation.

Chapter 4 provided a new solution based on gain extraction, that is used to estimate the bandwidth mismatch error. In the first section, this choice has been justified by comparing the gain component to the phase mismatch component due to the bandwidth mismatch error. Then the proposed solution has been detailed and some limitations have been highlighted. The first concerns the fact that at an input frequency equal to $\omega_s/4$, the generated spur appears at the same frequency and hence the integrator which is responsible of averaging the loss function diverges. The second limitation comes from the presence of symmetrical signals at the same time which generate spurs at the same frequencies as well. Nevertheless, the simulation using the CDMA pattern shows that the latter limitation do not impact the estimation.

In the second section, the proposed method has been validated using two ADCs from the market where all intrinsic errors are present. The static gain has been removed beforehand at low frequencies because it impacts the bandwidth error extraction. By using several input frequencies, the estimation method converges to a value of 0.47% of bandwidth mismatch error. Finally, it is important to notice that this value is the minimum mismatch we can obtain since first order filters are considered in the proposed estimation technique.

Perspectives

As a short term perspectives, we will focus on implementing the proposed solution on an FPGA. The complexity of the implementation would be evaluated according to : 1)the number of samples needed to achieve the desired accuracy. This will define the convergence time of the integrator. 2)the complexity of the notch filter including the filter order and the number of taps.

In addition, these requirements are imposed by the power consumption of the system which needs to be quantified.

Regarding the correction, the implementation of the proposed solution in Chapter 3. the solution proposed in Subsection 3 needs to be deeply studied in order to determine the real limitation of the approximations. In fact, the differentiators proposed in this section were calculated ideally using inverse fourier transforms which is not realistic. Based on the ideal filters, it has been shown that the correction is bounded by and SFDR equal to 85 dB. Therefore, the challenge is to design the differentiators as close as possible to the ideal configuration.

On the long view, two objectives are planned to be achieved. The first one concerns the static gain calibration, which needs to be done online without altering the estimation of the bandwidth mismatch error. Moreover, the proposed estimation solution is best suited to analog correction. The second challenge for this work is to propose an analog correction technique able to attain very high accuracies thanks to good estimation of the bandwidth mismatch error.

Appendix A

This appendix is dedicated to measure the bandwidth of the ADC. This information is essential to estimate the bandwidth mismatch error since this one is more visible when we work close to the cut-off frequency. Moreover, the bandwidth mismatch error is exactly the difference between the two cut-off frequencies of two channels in a TI-ADC. We will highlight in this appendix some limitations for bandwidth and error measurements and show how to deal with them.

Bandwidth measurements

The measurements setting are described in the following :

- First of all, the impedance matching is necessary to obtain the maximum power transfer from the source to the ADC. One can note that because of differential functioning, the chosen differential matching resistance is then equal to 100 Ohm.
- At each input frequency, the gain is measured at the ADC output. Here, the input voltage is fixed to -1dBFS.
- For a fixed sampling frequency of 80Msps, a frequency sweep is realized in the range [10MHz ; 1300MHz].

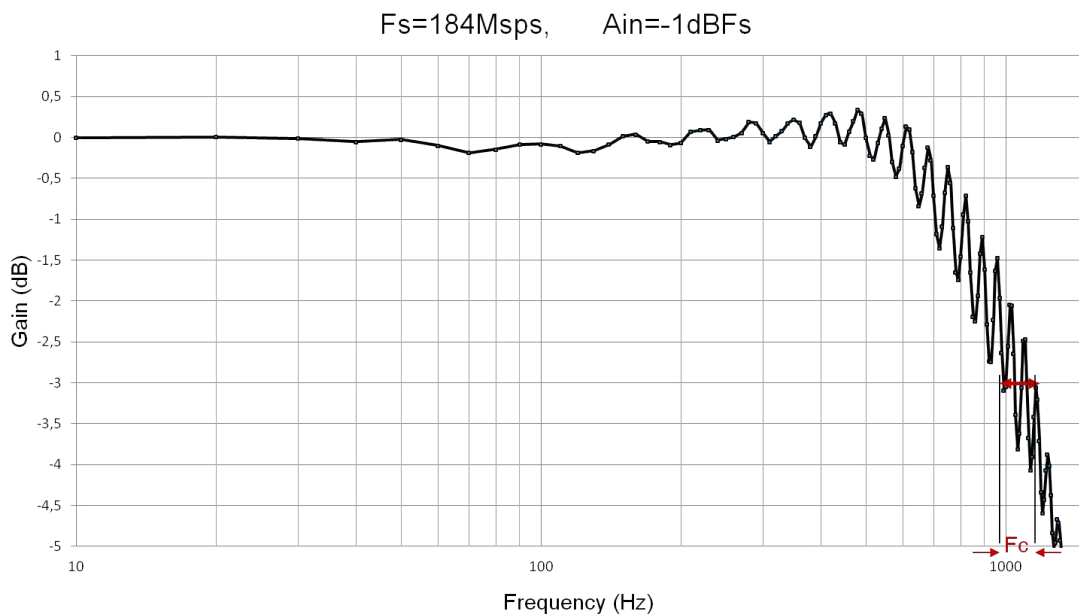


FIGURE 19 – Bandwidth measurements at the ADC output.

The result of this first set of measurements is shown in Fig. 19. The oscillations in the band are caused by two phenomena :

1. Signal reflection due to imperfections in the impedance matching. In fact, when high-frequency signals are carried on transmission lines of any significant length, care must be taken that the transmission medium is matched to its terminations. The source and load impedances should equal the characteristic impedance of the transmission line, as this minimizes signal reflections. However, since the input network of the ADC contains resistances and capacitances, the chosen matching impedance have to compensate both the resistive and the capacitive effect. The latter is more difficult to obtain because its dependency of the input frequency.
2. The second phenomenon is called a kick-back effect and corresponds to the charge injection in the ADC architecture when using input switched capacitor network. When the switch is open, the charge on capacitor C is fixed but the signal is still changing at the input (illustrated in Fig. 20 (a)). Then when the switch is closed, the level at the capacitor C will change suddenly and it will create a charge injection in the application (see Fig. 20 (b)). Consequently, some energy is returned to the source and can cause reflections and ringing in the cable.

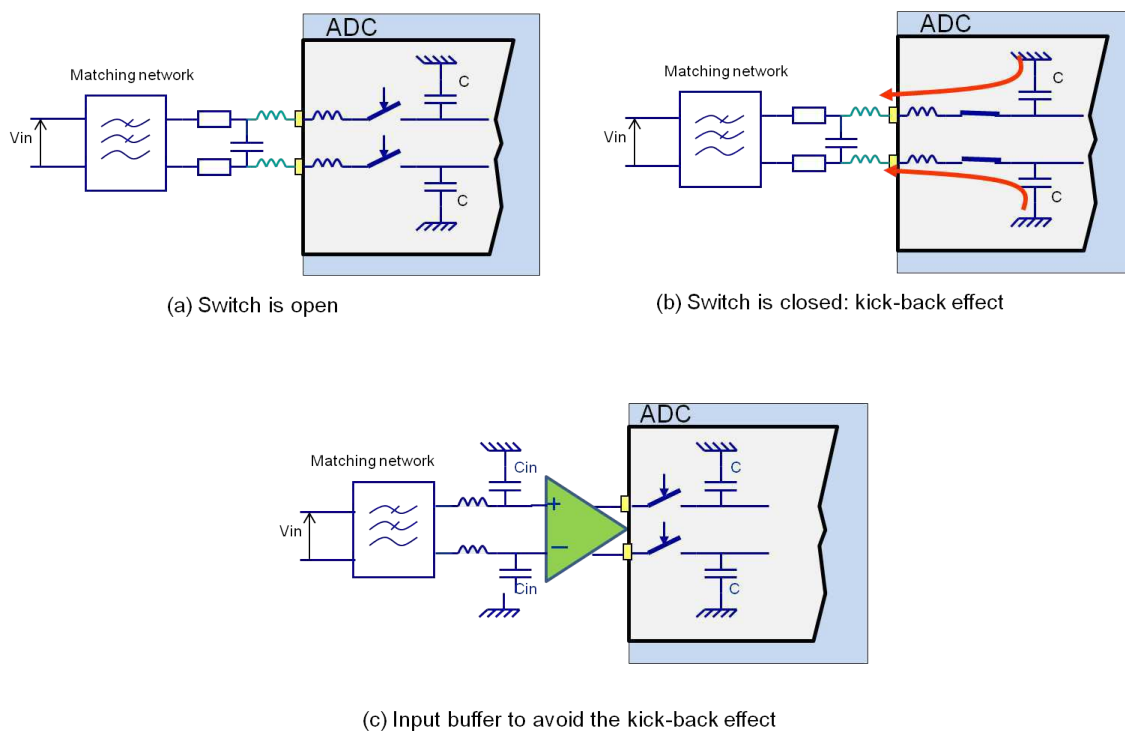


FIGURE 20 – impedance matching block at the ADC input when (a)the switch is open, (b) the switch is closed generates kick-back effect, (c) input buffer eliminates kick-back effect

To avoid the effect of kick-backing, it is mandatory to isolate the switched capacitance inputs of the ADC from the input. To do so, a driver (also called input-buffer filter) is required to isolate the ADC from the input circuit. In that way, the impedance matching is only performed at the input of the driver as shown in Fig. 20 (c). Furthermore, since the impedance at output of the driver is very large, this do not allow the charges to be

injected into the input and hence minimizes the ringing in the circuit.

In order to measure the bandwidth of the ADC avoiding ringing in the band in an easier way, an attenuator (-10 dB) is placed at the input of the circuit to absorb the reflection. This measurement is provided in Fig. 21 where we obtain a bandwidth around 1.1 GHz.

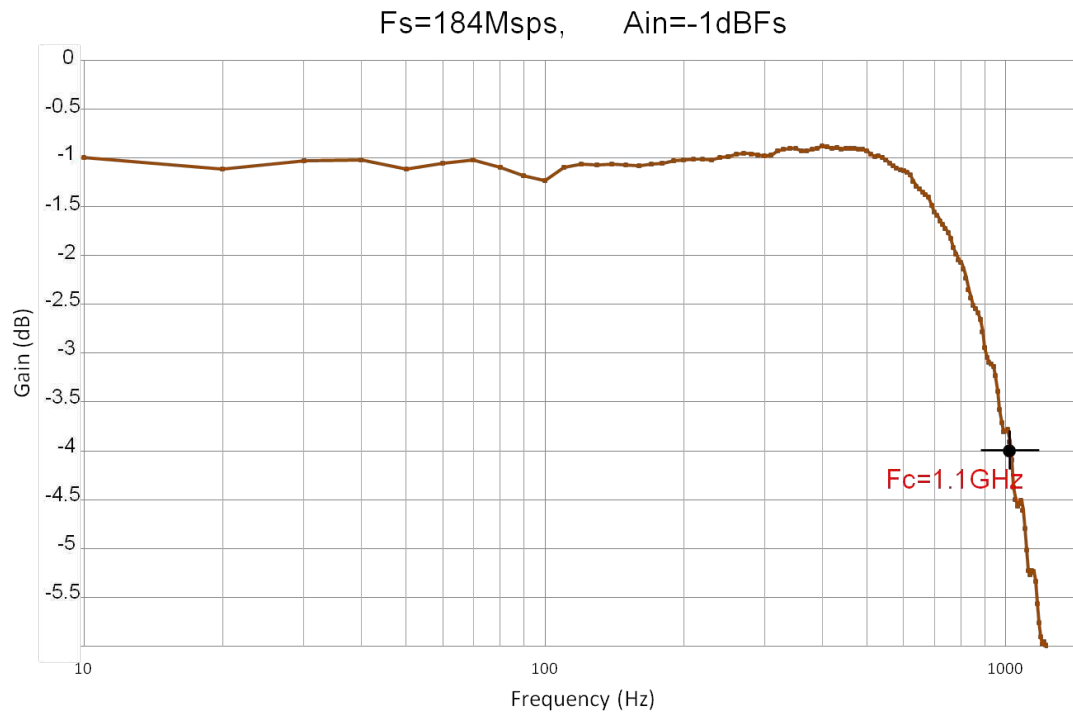


FIGURE 21 – Bandwidth measurement at the ADC output.

Bandwidth mismatch simulation

Regarding the bandwidth mismatch error measurement, the ringing in the band alters the result. Nevertheless, the two ADCs have been simulated and the results are shown in Fig. 2.14. Each ADC has a cut-off frequency of 1.1 GHz (Fig. 2.14(a) and (b)). Fig. 2.14 (c) shows that the bandwidth mismatch is 889 MHz which corresponds to a mismatch of 0.8% for 1σ or 2.4% for 3σ .

1. We have used this approach instead of the input-buffer because of the unavailability of this one in the circuit. However, the measurements are on going

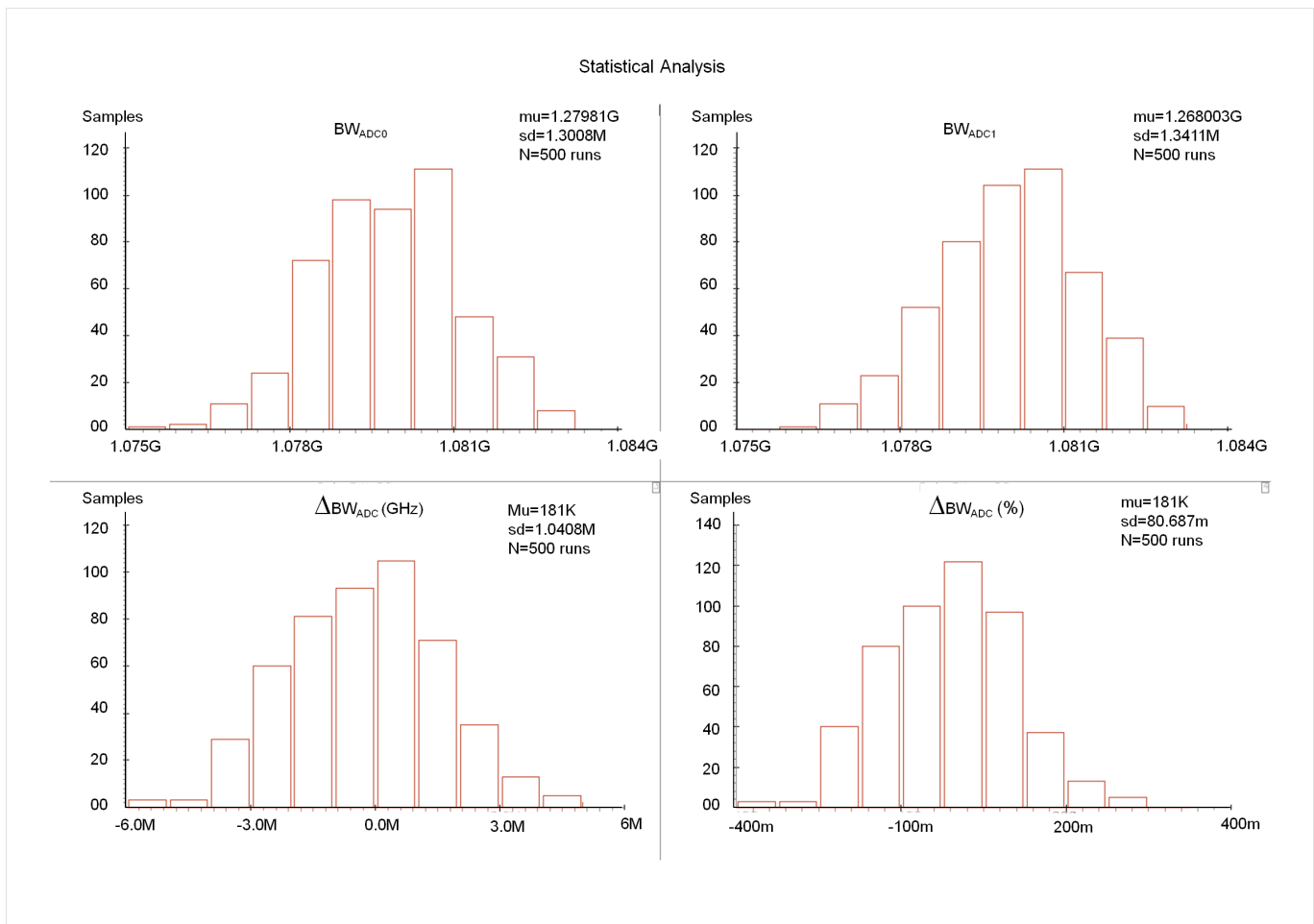


FIGURE 22 – Bandwidth mismatch between the two sampling networks ADC_0 and ADC_1 .

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