

Modulateur Sigma Delta Passe-Haut et son application au convertisseur Sigma Delta à l'entrelacement temporel

van Tam Nguyen

▶ **To cite this version:**

van Tam Nguyen. Modulateur Sigma Delta Passe-Haut et son application au convertisseur Sigma Delta à l'entrelacement temporel. domain_other. Télécom ParisTech, 2004. English. NNT : . pastel-00000929

HAL Id: pastel-00000929
https://pastel.hal.science/pastel-00000929

Submitted on 3 Feb 2005

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

High-Pass $\Delta\Sigma$ Modulator and its Application to Time-Interleaved $\Delta\Sigma$ Converter

Van Tam Nguyen

COMELEC Departement

Ecole Nationale Supérieure des Télécommunications

Remerciements

Cette thèse a été effectuée au sein du département Communications et électronique de l'Ecole Nationale Supérieure des Télécommunications. Je tiens tout particulièrement à remercier mes deux directeurs de thèse Monsieur Patrick Loumeau et Monsieur Jean-François Naviner de m'avoir accueilli et accordé une totale confiance au cours de son développement. Le sujet était très ambitieux, et ils m'ont permis par leur connaissance et leur lucidité sur le sujet, de mener à bien cette recherche.

J'exprime toute ma gratitude à Monsieur Pierre Duhamel, Directeur de Recherche de CNRS, pour avoir accepté de présider le Jury de thèse.

Je suis très honoré que Monsieur le Professeur José Luis Huertas et Monsieur le Professeur Denis Flandre, aient acceptés d'être les deux rapporteurs de cette thèse. Je les remercie de cet engagement dans cette lourde tâche, d'autant que je sais leur emploi du temps extrêmement chargé.

Mes remerciements s'adressent également à François Barbara, Ingénieur de Schlumberger, d'avoir bien voulu d'examiner ce travail et pour les échanges que j'ai pu avoir avec lui.

J'associe toutes les personnes qui font partie du département à ces remerciements et plus particulièrement Monsieur Hervé Petit pour ses apports constructifs et son aide pour le banc de test, Monsieur Jean-François Naviner pour son aide à l'utilisation et la gestion des outils de conception et Madame Patricia Desgreys pour son aide au développement des modèles en VHDL-AMS. Je ne peux omettre Monsieur Karim Benkalaia pour son aide à la conception de la carte de test du circuit et Monsieur Jacky Porte pour son aide de l'utilisation de l'outil OCEANE, ainsi que Madame Chantal Cadiat pour sa disponibilité et sa gentillesse.

Comment oublier tous les thésards et les stagiaires avec qui j'ai partagé de longs moments et surtout un projet commun. Leur confort et leur présence ont tout

© Van Tam Nguyen, Telecom Paris - July 2004

simplement rendu agréable ces années de thèse. J'adresse mes amitiés et renouvelle mes remerciements à Frédéric, mon partenaire du projet, ainsi que Bilal, Elisabeth, Elisabette, Kae, Sabeur, Mohamed, David, Richard, Nesrine, Sonia et Maryam. J'espère que nous gardons le contact par la suite.

Je pense enfin à toute ma famille, et en particulier mes parents, mon frère et ma sœur, qui m'ont donné le courage de faire cette thèse. Un remerciement spécial pour mon épouse Nguyên, qui m'a soutenu tout au long de ce travail, et qui a su apporter avec talent et enthousiasme les touches finales à ce manuscrit. Cette thèse est donc aussi la leur.

Projet SPRING

Ma thèse est effectuée dans le cadre d'un projet de recherche européen intitulé SPRING. Ce projet est coordonné par Schlumberger Industries (France) avec la participation de trois partenaires universitaires:

- Université Catholique de Louvain (UCL - Belgique);
- Centro Nacional de Microelectronica (CNM - Espagne);
- Ecole Nationale Supérieure des Télécommunications (ENST - France).

Ce projet propose la création d'un réseau de recherches et de formation recueillant les partenaires universitaires (CNM, ENST, et UCL) et l'industrie (Schlumberger) pour établir et échanger les connaissances. Le réseau s'est concentré sur le transfert des technologies entre les partenaires (à travers les thèse doctorales) et sur la formation mutuelle et complémentaire de tous les partenaires.

Cette thèse a donc la privilège d'être suivie et encadrée par des industriels, avec leurs points de vue réalistes et critiques dans les différentes phases de son dévellopement. Je tiens donc à remercier Messieurs Lionel Beneteau, François Barbara, Matthias Sicard et Gilles Picard qui ont participé activement au bon déroulement de cette thèse.

Le rapport de thèse fait partie des deliverables du projet. C'est la raison pour laquelle il est écrit en anglais.

Résumé

Le convertisseur analogique-numérique fondé sur le principe de modulation $\Sigma\Delta$ est capable de fournir une très haute résolution. Bien qu'il nécessite un suréchantillonnage, il est peu sensible aux imperfections des composants. Le modulateur $\Sigma\Delta$ classique est donc très populaire pour les applications de bande étroite demandant une très haute résolution.

Dans cette thèse, nous nous sommes intéressés à l'extension des applications du modulateur $\Sigma\Delta$ vers une bande passante plus large. Nous avons tout d'abord étudié l'architecture parallèle basant sur la modulation $\Sigma\Delta$ et proposé une nouvelle architecture basant sur la modulation $\Sigma\Delta$ passe-haut et l'entrelacement temporel permettant de réduire de façon significative le problème caractéristique du parallélisme, à savoir la disparité entre les canaux.

Nous avons ensuite étudié le modulateur $\Sigma\Delta$ passe-haut et proposé une implémentation en technique des capacités commutées. Ce nouveau modulateur, contrairement au modulateur classique, est complètement immune au bruit de basse fréquence et peut être utilisé non seulement dans une architecture parallèle, mais aussi de façon autonome.

Nous avons aussi modélisé la plupart de non-idéalités du modulateur en VHDL-AMS pour finalement arriver à une méthodologie de conception descendante qui permet de dériver les spécifications de tous les blocs du circuit à partir de performance visée pour le système complet. L'implémentation d'un modulateur $\Sigma\Delta$ passe-haut d'ordre 2 et un convertisseur $\Sigma\Delta$ passe-haut en combinant avec l'entrelacement temporel a été réalisée en technologie CMOS 0,35 μm.

Enfin, notre travail nous a permis de démontrer non seulement l'avantage du modulateur $\Sigma\Delta$ passe-haut, mais aussi un perspective prometteur du modulateur $\Sigma\Delta$ parallèle pour les applications de très large bande.

© Van Tam Nguyen, Telecom Paris - July 2004

Abstract

The analog-to-digital converter based on the $\Delta\Sigma$ modulation is capable of providing a very high resolution. Although it requires an oversampling, it is not sensitive to the imperfections of the components. The conventional $\Delta\Sigma$ modulator is thus very popular for narrowband applications requiring a very high resolution.

In this thesis, we consider the extension of the $\Delta\Sigma$ modulators towards wideband applications. First, we studied parallel architectures basing on the $\Delta\Sigma$ modulation and proposed a new architecture basing on the high-pass $\Delta\Sigma$ modulation and time-interleaved allowing to reduce significantly the characteristic problem of parallelism, namely the channel mismatch.

We then studied the high-pass $\Delta\Sigma$ modulator and proposed an implementation in switched-capacitor technique. This new modulator, contrary to the conventional modulator, is completely immune to the low frequency noise and can be used not only in a parallel architecture, but also as stand-alone modulator.

We also modelled the main non-idealities of the $\Delta\Sigma$ modulator in VHDL-AMS for finally arriving at a top-down design methodology which makes it possible to derive the specifications of all the circuit blocks from the performance aimed for the complete system. The implementation of a high-pass second order $\Delta\Sigma$ modulator and a time-interleaved high-pass $\Delta\Sigma$ converter was carried out in 0.35 μm CMOS technology.

Finally, our work allowed us to demonstrate, not only the advantages of the high-pass $\Delta\Sigma$ modulator, but also a promising prospect of the parallel $\Delta\Sigma$ modulators for the wide band applications.

© Van Tam Nguyen, Telecom Paris - July 2004

Contents

Remerciements i

Résumé v

Abstract vii

Contents xiii

List of Figures xxi

List of Tables xxiv

Listings xxv

Abbreviations xxvii

1 Introduction **1**

1.1 Motivations and Objectives 1

1.2 Organization 2

2 Analog-to-Digital Converter Architectures **5**

2.1 Introduction 5

2.2 Flash Converter 5

2.3 Successive Approximation ADC 9

2.4 Pipeline Converter 10

2.5 Time-Interleaved ADC 11

2.6 Hybrid Filter Bank ADC 13

© Van Tam Nguyen, Telecom Paris - July 2004

2.7 $\Delta\Sigma$ Converter 14
2.8 Conclusion 15

3 High-Pass Delta Sigma Modulator 17

3.1 Introduction 17
3.2 Conventional $\Delta\Sigma$ Modulator 19
3.3 Presence of Low Frequency Noise 27
3.4 Principle of high-pass $\Delta\Sigma$ Modulator 30
3.5 Performance of high-pass $\Delta\Sigma$ Modulator 34
3.6 Switched-Capacitor Basis Block Implementation 38
3.7 Modulator Stability 42
3.8 Conclusion 50

4 Time-Interleaved $\Delta\Sigma$ Converter 53

4.1 Introduction 53
4.2 Architecture 54
4.3 Theoretical Performance 58
4.3.1 Overall Useful Signal 59
4.3.2 Overall Quantization Error 61
4.3.3 Optimal Channel Filter 63
4.3.4 Ideal Performance Obtainable 66
4.3.5 Minimal Filter Length of the Optimal Filter 68
4.4 Sensitivity to Nonideal Circuit Behavior 71
4.5 Time-Interleaved High-Pass $\Delta\Sigma$ ADC 74
4.6 Adaptive Equalization of Channel Gain Mismatch 79
4.7 Conclusion 83

5 Design Methodology with VHDL-AMS **87**

5.1 Introduction 87

5.2 VHDL-AMS Overview 88

5.3 Top-Down Methodology with VHDL-AMS 90

5.4 Component models 93

5.4.1 Clock Jitter Noise 94

5.4.2 Switch Noise 96

5.4.3 Operational Amplifier Noise 97

5.4.4 White Noise Model 98

5.4.5 $1/f$ Noise Model 101

5.4.6 Switch Model 102

5.4.7 Operational Amplifier Model 105

5.4.8 Complete Filter Model 108

5.4.9 Comparator 109

5.5 Simulation Results 109

5.5.1 Noise Effect 110

5.5.2 Nonideality Effect 115

5.5.3 Block Specification Summary 118

5.6 Conclusion 118

6 Implementation **121**

6.1 Introduction 121

6.2 Switched-Capacitor High-Filter 122

6.3 Circuit Design 123

6.3.1 Operational Amplifier 123

6.3.2 Switch 131

6.3.3 Capacitors . . . 132
6.3.4 Comparator . . . 133
6.3.5 Chopper . . . 135
6.3.6 Clock Generator . . . 137
6.3.7 Clock Buffer . . . 137
6.3.8 Real Inband Noise Effect . . . 137
6.4 Conclusion . . . 141

7 Layout and Test Setup **143**
7.1 Layout . . . 143
7.2 Test Setup . . . 145

8 Conclusions **147**
8.1 Summary . . . 147
8.2 Suggestions . . . 148

A Optimal Filter of Time-Interleaved $\Delta\Sigma$ Converter **153**

B PDF Estimation Method and VHDL-AMS Listing **155**
B.1 PDF estimation method . . . 155
B.2 VHDL-AMS Listing . . . 156

C Résumé étendu **161**
C.1 Architecture des CANs . . . 161
C.2 Modulateur $\Sigma\Delta$ passe-haut . . . 162
C.3 Convertisseurs $\Sigma\Delta$ combinant avec l'entrelacement temporel . . . 164
C.4 Méthodologie de conception avec VHDL-AMS . . . 166
C.5 Implémentation . . . 168

C.6 Conception des masques et carte de test 168

C.7 Conclusions 171

Bibliography **173**

© Van Tam Nguyen, Telecom Paris - July 2004

List of Figures

2.1 3-bit flash ADC 6

2.2 Semi-flash ADC 8

2.3 Successive approximation ADC structure 9

2.4 Pipeline ADC structure 10

2.5 Time-interleaved ADC structure. 12

2.6 Hybrid filter bank ADC architecture. 13

3.1 Conventional pulse code modulation (PCM), including analog antialiasing filter for curtaining the aliasing noise in the encoder and for smoothing the output from the decoder. 19

3.2 Oversampling pulse code modulation. The modulation and demodulation occur at sufficiently high sampling rate that digital filters can provide most for the antialiasing and smoothing functions. 20

3.3 An analog signal that has been (a) sampled at the Nyquist rate, and (b) oversampled. 20

3.4 Power spectral density of quantization noise when the input signal is oversampled. 21

3.5 General structure of a feedback modulator. 22

3.6 First-order low-pass $\Delta\Sigma$ modulator. 25

3.7 Second-order low-pass $\Delta\Sigma$ modulator with Boser's structure. 26

3.8 First-order $\Delta\Sigma$ modulator model with low frequency noise. 28

3.9 Second-order $\Delta\Sigma$ modulator model with low frequency noise. 29

3.10 Conventional $\Delta\Sigma$ modulator model in the presence of the low frequency noise. 29

3.11 Spectrum representation of different signals in $\Delta\Sigma$ modulator. (a): input signal; (b): output signal in the presence of the low frequency noise. 30

3.12 Locations of zeros of the noise transfer function in the z-plane. 31

3.13 Chopper stabilized high-pass $\Delta\Sigma$ modulator in the presence of the low frequency noise. 32

3.14 Evolution of the input signal in the frequency domain. 32

3.15 Second-order high-pass $\Delta\Sigma$ modulator. 34

3.16 Undecimated spectrum of digital output signal of second-order high-pass $\Delta\Sigma$ modulator. 36

3.17 SNR versus input signal level of the second-order high-pass $\Delta\Sigma$ modulator. 37

3.18 Output spectrum of the low-pass $\Delta\Sigma$ modulator (a) and output spectrum of the chopper stabilized $\Delta\Sigma$ modulator. 38

3.19 Parasitic-insensitive non-inverting SC integrator. 39

3.20 SC implementation of the high-pass filter 40

3.21 SC implementation of the high-pass filter with different parasitic capacitors. 40

3.22 Real quantizer model 43

3.23 Locations of poles of the noise transfer function in the z-plane. (a): stable modulator ; (b): unstable modulator. 44

3.24 Divergence of internal states when the modulator is unstable. y_1 : output of the first high-pass filter, y_2 : output of the second high-pass filter. 46

3.25 Threshold of the pole in the high-pass filter assuring the stability of the high-pass $\Delta\Sigma$ modulator. 48

3.26 Signal-to-noise ratio of the second-order high-pass $\Delta\Sigma$ modulator versus the pole of the high-pass filter. 49

4.1 Architecture of time-interleaved $\Delta\Sigma$ converter. 55

4.2 Equivalent multiplication models of the multiplexer and demultiplexer with $M-1$ delays of the demultiplexer relative to the multiplexer in the time-interleaved $\Delta\Sigma$ converter. 56

4.3 An example of the processing performed by a four channels time-interleaved $\Delta\Sigma$ converter in the absence of quantization error with three delays of the demultiplexer relative to the multiplexer. 57

4.4 Linear model of $\Delta\Sigma$ modulator. 58

4.5 The time-interleaved $\Delta\Sigma$ ADC quantization model. 58

4.6 The impulse response and frequency response of an optimal channel filter for a time-interleaved $\Delta\Sigma$ converter employing four channels of fourth-order $\Delta\Sigma$ modulators. 65

(a) 67

(b) 67

(c) 67

4.7 The ideal DR in dB of the time-interleaved $\Delta\Sigma$ converter versus m_0, with $M = 4, 8, \cdots, 30$, for (a) second-order, (b) third-order, and (c) fourth-order $\Delta\Sigma$ modulators. The length-401 channel filters are used. 67

(a) 69

(b) 69

(c) 69

4.8 The ideal DR in dB of the time-interleaved $\Delta\Sigma$ converter versus channel filter length, N, with $M = 4, 8, \cdots, 30$ for (a) second-order, (b) third-order, and (c) fourth-order $\Delta\Sigma$ modulators. 69

4.9 The ideal DR of the time-interleaved $\Delta\Sigma$ converter for optimal channel filter versus the number of channels on a log scale. 70

4.10 Output spectrum of time-interleaved fourth-order ΔΣ ADC with four channels in the presence of the channel mismatch. 72

4.11 Diagram of the time-interleaved high-pass ΔΣ ADC. Multi-cadence system presentation. 74

4.12 Frequency domain presentation of time-interleaved ΔΣ ADC. 76

4.13 Output signal spectrum of the time-interleaved fourth-order high-pass ΔΣ ADC employing four channels in the presence of the channel mismatch. 78

4.14 Interleaved high-pass ΔΣ ADC architecture with adaptive channel gain equalization. 79

4.15 Magnitude of the weights as they converge to the final value. 81

4.16 Output signal spectrum with four algorithms. 82

4.17 Output signal spectrum of the time-interleaved high-pass ΔΣ ADC with adaptive channel gain equalization 84

5.1 Design process: the entire digital design process is already fully automated, but analog and mixed-signal design is hindered by the "Gap", which reflects a lack of tool support for the design process between system-level specification and transistor-level implementation. 91

5.2 Elementary blocks building the high-pass ΔΣ modulator using SC techniques. 94

5.3 Discrete model of the sampling process when the sampling time nT is perturbed by a random process $\delta T(t)$. 95

5.4 Model of a random sampling jitter : x(t) is the input signal, e(t) is white noise with mean value, 0, and standard deviation, 1. 96

5.5 (a) MOS S/H, and (b) its equivalent noisy circuit when Φ_S is high. . 96

5.6 Thermal noise model : x(t) is the input signal, e(t) is white noise with mean value, 0, and standard deviation, 1. 97

5.7 Non-differential representation of the high-pass filter with an input, V_{in}, and an input-referred amplifier noise source, e_{amp}. 98

5.8 The estimated probability density function of our generator in VHDL-AMS (blue) and the theoretical probability density function of white noise (red) with mean value, 0, and standard deviation, 1. 100

5.9 Switch model. 103

5.10 Sinusoidal input of a S/H (blue), Its output with the model of switch in VHDL-AMS (black) and Its output with Eldo transistor-level (red). 104

5.11 Operational amplifier model. 106

5.12 Operational amplifier response 107

5.13 Circuit nonidealities of the high-pass filter building the high-pass $\Delta\Sigma$ modulator. 108

5.14 Comparator with hysteresis. 109

5.15 State diagram of comparator with hysteresis. 110

5.16 Power spectral density of chopper stabilized second-order $\Delta\Sigma$ modulator with an ideal modulator and thermal noise, jitter noise and op-amp noise models. 111

5.17 Schema block of high-pass second-order $\Delta\Sigma$ modulator in the presence of op-amp noise. 112

5.18 SNDR performance of the high-pass modulator versus the input signal amplitude resulting from simulation in consideration of all of the nonidealities. 119

6.1 Fully differential, SC implementation of the high-pass filter. 122

6.2 Filter configured during the sampling phase; S (a), and charge redistribution phase, T (b). 124

6.3 Two-stage operational amplifier 127

6.4 Bias circuit of two-stage operational amplifier 128

6.5 Frequency response of operational amplifier with a 2pF load capacitances at each output. 129

6.6 Output excursion of operational amplifier 130

6.7 CMOS Switch 131

6.8 Dynamic latch used as the comparator core (a) and simplified representation of the latch in the active phase ($clock = VDD$) (b). 133

6.9 Complete comparator. 135

6.10 Implementation of chopper block 135

6.11 Implementation of multiplexor 136

6.12 Clock generator. 138

6.13 Clock phases. 139

6.14 Clock buffer 139

7.1 Layout of the second-order high-pass $\Delta\Sigma$ modulator and a two channels time-interleaved second-order high-pass $\Delta\Sigma$ converter. 144

7.2 Diagram of test setup. 145

8.1 New implementation of second-order high-pass $\Delta\Sigma$ modulator based on Boser's structure of low-pass second-order $\Delta\Sigma$ modulator. 149

8.2 New implementation of second-order high-pass $\Delta\Sigma$ modulator based on classical second-order low-pass $\Delta\Sigma$ modulator. 150

A.1 (a) : FIR filter; (b) Symmetric FIR filter 153

C.1 Implémentation en capacités commutées du bloc de base du modulateur $\Sigma\Delta$ passe-haut. 163

C.2 Architecture du convertisseur $\Sigma\Delta$ en combinant avec l'entrelacement temporel. 164

C.3 La dynamique idéale du convertisseur $\Sigma\Delta$ en combinant avec l'entrelacement temporel avec des filtres de canal idéaux en fonction du nombre de canaux pour trois modulateurs différents. 165

C.4 Dessin de masque du modulateur $\Sigma\Delta$ passe-haut d'ordre 2 et du convertisseur $\Sigma\Delta$ passe-haut en conbinant avec l'entrelacement temporel. 169

C.5 Diagramme de la carte de test. 170

© Van Tam Nguyen, Telecom Paris - July 2004

List of Tables

2.1 Truth table for flash converter in Figure 2.1 7

4.1 The minimal filter length of the optimal channel filter allowing to attain an DR equal to the ideal DR minus 1 dB. 70

4.2 Step size value for LMS, SD-LMS, SE-LMS and SS-LMS algorithms. . 80

4.3 DR(dB) of ADC with different algorithms 83

5.1 Modelling space covered by VHDL-AMS 89

5.2 Simulation parameters. 111

5.3 Threshold of parameters representing jitter noise, switch noise and amplifier noise. 115

5.4 High-pass modulator SNDR performance versus the on-resistance of the switch. 116

5.5 Low-pass modulator SNDR performance versus the static gain and the slew-rate of the amplifier. 116

5.6 High-pass modulator SNDR performance versus the static gain and the slew-rate of the amplifier. "x" means that the modulator is unstable. 117

5.7 High-pass modulator SNDR performance versus the transition frequency to sampling frequency ratio. 117

5.8 High-pass $\Delta\Sigma$ modulator SNDR performance versus capacitor mismatch. 118

5.9 Specification summary. 119

6.1 Transistor sizes of the operational amplifier. 128

6.2 Transistor sizes of the bias circuit. 129

6.3 Operational amplifier performances. 130

6.4 Transistor sizes of the dynamic latch. 134

7.1 Expected performance of the high-pass second-order modulator. . . . 146

C.1 Spécifications des différents paramètres de nonidéalité pour obtenir une performance de moins 3 dB de la performance idéale d'un modulateur $\Sigma\Delta$ passe-haut d'ordre 2. 167

C.2 Performance du modulateur $\Sigma\Delta$ passe-haut d'ordre 2. 171

© Van Tam Nguyen, Telecom Paris - July 2004

Listings

5.1 White noise generator in VHDL-AMS. 99

5.2 Simple model of switch in VHDL-AMS where only on-resistance and off-resistance are taken into account. 102

5.3 Simple model of op-amp in VHDL-AMS where only static gain and saturation are taken into account. 105

B.1 Model of switch in VHDL-AMS where on-resistance, off-resistance, parasitic capacitances and leakage current are taken into account. . . 156

B.2 Model of comparator with hysteresis in VHDL-AMS. 157

Abbreviations

ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
DEA	Differential and Algebraic Equation
$\Delta\Sigma$	Delta Sigma
DR	Dynamic Range
DSPF	Detailed Standard Parasitics File
DUT	Device Under Test
FIR	Finite Impulse Response
HDL	Hardware Description Language
IIR	Infinite Impulse Response
LMS	Least Mean Square
LTI	Linear Time Invariant
OCEANE	Outils pour la Conception et l'Enseignement des circuits intégrés ANalogiquEs
Op-amp	Operational amplifier
OSR	Oversampling ratio
PDF	Probability Density Function
$\Pi\Delta\Sigma$	Pi Delta Sigma
SC	Switched-Capacitor
SDL	Schematic Driven Layout
SD-LMS	Sign-Data Least Mean Square
SE-LMS	Sign-Error Least Mean Square
SFDR	Spurious Free Dynamic Range
S/H	Sample-and-Hold

SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SS-LMS	Sign-Sign Least Mean Square
VHDL	Very high speed integrated circuits Hardware Description Language
VHDL-AMS	VHDL-Analog and Mixed-Signal
VLSI	Very Large Scale Integration

Chapter 1

Introduction

1.1 Motivations and Objectives

Analog-to-Digital Converters (ADC) are key components in almost all modern communication systems. High speed and high resolution ADCs are required in many applications, such as advanced radar systems, multi-beam adaptive digital beamforming array transceivers, smart radios for wireless communications, anti-jam global positioning system receivers, wide-bandwidth modems, and software radios.

Nowadays, there exist a lot of techniques that allow a very high precision conversion, such as the analog-to-digital conversion based on the delta-sigma ($\Delta\Sigma$) modulation and oversampling [1]. However, the process of converting the analog signal to a digital one often limits the overall system speed. In contrast, there are other techniques that provide a very high speed conversion but have just an average or even low resolution, such as flash converter or time-interleaved converter.

Associating the high speed and the high resolution in one ADC has been long time a tough challenge in the research of analog-to-digital conversion techniques. Conventionally, one seeks to improve one of these two properties while trying to keep the other. Recently, a number of research teams [2, 3, 4] have involved in exploiting the $\Delta\Sigma$ ADC for converters that provide both high speed and high resolution. It is not an easy task and so far the result has not been very satisfying. The converters investigated are the $\Pi\Delta\Sigma$ [3] and the time-interleaved $\Delta\Sigma$ [4]. But as in any parallel architecture, these two suffer from the channel mismatch.

In this work, we will attempt to improve the efficiency of parallel $\Delta\Sigma$ converter, especially by minimizing the effect of channel mismatch.

Theoretical study of parallel $\Delta\Sigma$ converters during the first years of this research reveals that the high-pass $\Delta\Sigma$ modulator has good potential to eliminate efficiently the channel offset, especially in time-interleaved $\Delta\Sigma$ converters. It follows that a simple digital channel equalization technique would minimize effectively the channel gain mismatch effect.

At this stage, the high-pass $\Delta\Sigma$ modulator must be deeply investigated.

The principle of $\Delta\Sigma$ modulation was discovered long time ago and during the last ten years the converters based on this principle have become very popular. However, this popularity does not concern the "high-pass $\Delta\Sigma$ modulator". The reason may lie in its difficult implementation and the uncertainty about its stability and performance in the presence of circuit nonidealities.

Persuaded by its potentials, our research is focused on the high-pass $\Delta\Sigma$ modulator. Our objectives consist of studying its principle, its performance and stability, and then comparing it to low-pass modulators to show out its superiority.

To fulfil these objectives, our task consists of implementing the high-pass $\Delta\Sigma$ modulator and analyzing the circuit nonideality effect on its performance.

1.2 Organization

This dissertation is organized into eight chapters, including this introduction. The next chapter briefly reviews some of the prominent architectures of ADC, their principle of operation, advantages and drawbacks and their field of application.

Chapter 3 presents the high-pass delta sigma ($\Delta\Sigma$) modulator. Its advantages and drawbacks compared to those of the low-pass one are made obvious. An switched-capacitor (SC) implementation of the building block of high-pass $\Delta\Sigma$ modulator, referred to as high-pass filter, is studied. The stability of the high-pass modulator is also investigated. Critical parameters ensuring the modulator stability are demonstrated.

Chapter 4 is devoted to the time-interleaved $\Delta\Sigma$ converter. The advantage of using high-pass $\Delta\Sigma$ modulators in such an architecture, is demonstrated. A dig-

ital channel equalization technique minimizing the effect of channel mismatch, is proposed.

Chapter 5 presents a top-down design methodology with VHDL-AMS, the modelling, determination of nonideality effect and simulation of $\Delta\Sigma$ modulator in VHDL-AMS.

Chapter 6 proposes an implementation example of a second-order high-pass $\Delta\Sigma$ modulator and a two channels time-interleaved second-order high-pass $\Delta\Sigma$ converter in a 0.35 μm CMOS process.

Chapter 7 presents the layout of the prototype, the test setup and the expected performance of the high-pass modulator.

Finally, Chapter 8 concludes the dissertation with a summary of results as well as suggestions for further exploration.

Chapter 2

Analog-to-Digital Converter Architectures

2.1 Introduction

A lot of research has been done on the implementation of ADCs. Many techniques for doing analog-to-digital conversion have been developed. In this chapter, some of the prominent architectural styles are presented and compared. Each architecture has its advantages and disadvantages, and each one has a set of applications for which it is the best solution.

2.2 Flash Converter

The flash converter [5, 6, 7, 8, 9, 10, 11], also known as fully parallel architecture, is fundamentally the fastest architecture. It is also conceptually the easiest to understand. An n-bit flash ADC consists of an array of $2^n - 1$ comparators and a set of $2^n - 1$ reference values. The set of reference values is generally generated from a resistor string and a reference source, V_{ref}. Each comparator samples the input signal and compares the signal to one of the reference values. It then generates an output indicating whether the input signal is larger or smaller than the reference assigned to itself. The set of $2^n - 1$ comparator outputs that results is often referred to as a thermometer code. This name is derived from the fact that if the comparator outputs are listed in a column and ordered according to the reference

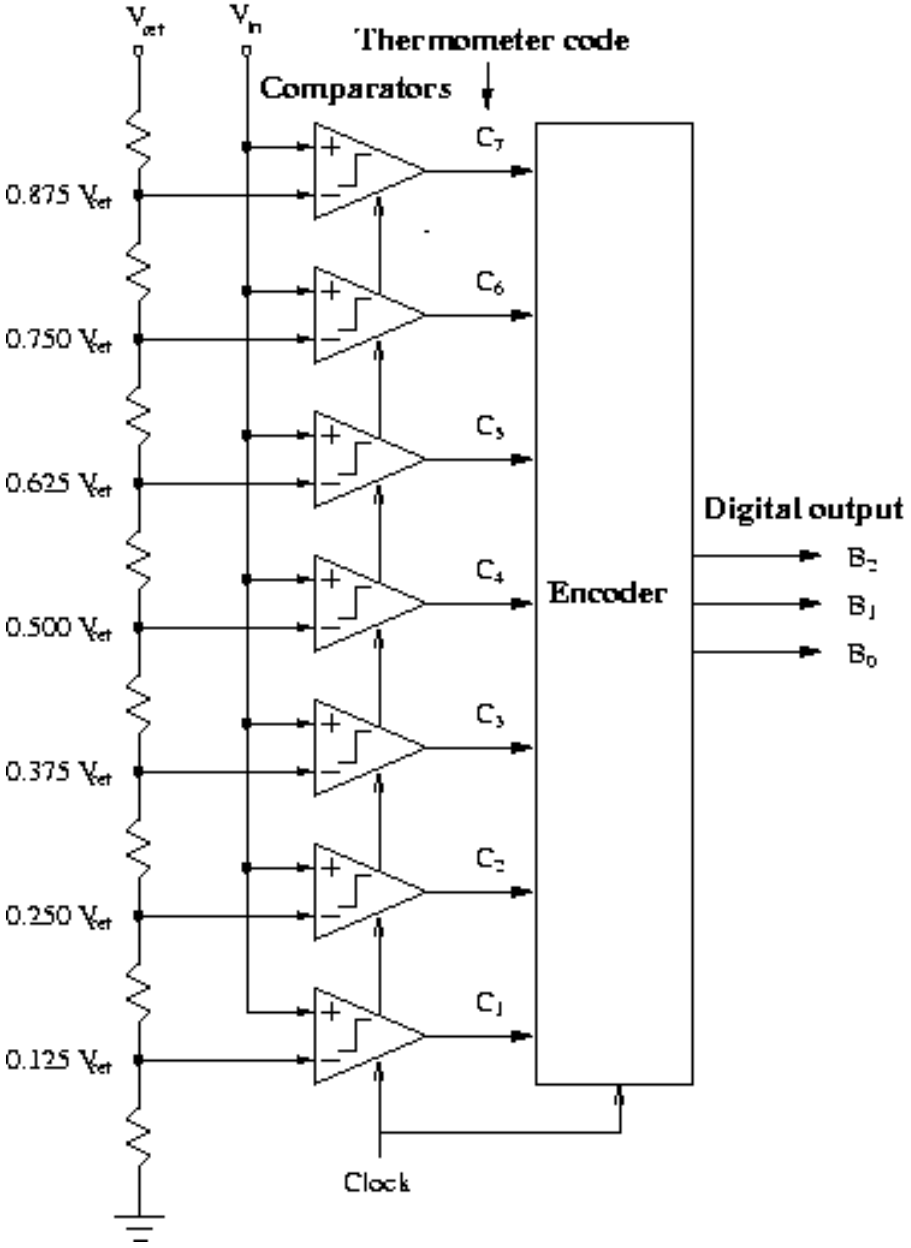


Figure 2.1: 3-bit flash ADC

values associated with the comparator that produced them, the ones would all be at the bottom, and the zeros all at the top as shown in Table 2.1. The level of the boundary between ones and zeros would indicate the value of the signal, much as the level of mercury in a mercury thermometer indicates the temperature.

A simple 3-bit flash ADC is shown in Figure 2.1. The encoder converts the thermometer code produced by the comparators to a binary code as shown in the truth table in Table 2.1. As seen from the figure, the comparators all operate in parallel. Thus, the conversion speed is limited only by the speed of the comparator or the sampler. For this reason, the flash ADC is capable of high speed.

The two primary drawbacks of the flash ADC are the large hardware requirement and the sensitivity to comparator offsets. As mentioned above, $2^n - 1$ comparators are required. For this reason, a high resolution flash ADC requires a large circuit area and dissipates high power. The required comparator offset voltage for a flash ADC with n bit resolution is less than $1/2^n$ relative to the reference voltage value. At high resolutions, this required comparator offset becomes very small. Because comparators with small offsets are difficult to design and expensive to build and because so many comparators are required, ADCs with resolutions higher than 8-bit rarely use the flash architecture.

	C_7	C_6	C_5	C_4	C_3	C_2	C_1	B_2	B_1	B_0
$V_{in} < 0,125V_{ref}$	0	0	0	0	0	0	0	0	0	0
$0.125V_{ref} < V_{in} < 0,25V_{ref}$	0	0	0	0	0	0	1	0	0	1
$0.25V_{ref} < V_{in} < 0,375V_{ref}$	0	0	0	0	0	1	1	0	1	0
$0.375V_{ref} < V_{in} < 0,50V_{ref}$	0	0	0	0	1	1	1	0	1	1
$0.50V_{ref} < V_{in} < 0,625V_{ref}$	0	0	0	1	1	1	1	1	0	0
$0.625V_{ref} < V_{in} < 0,75V_{ref}$	0	0	1	1	1	1	1	1	0	1
$0.75V_{ref} < V_{in} < 0,875V_{ref}$	0	1	1	1	1	1	1	1	1	0
$0.875V_{ref} < V_{in}$	1	1	1	1	1	1	1	1	1	1

Table 2.1: Truth table for flash converter in Figure 2.1

To decrease hardware requirement, i.e. to reduce the number of comparators, two-step flash architecture, also known as semi-flash architecture, can be used. A two-step flash ADC [12, 13, 14, 15, 16] as shown in Figure 2.2 consists of two stages, each containing a flash ADC. In this type of ADC, the conversion does not happen

all at once as in the flash ADC. Here, the conversion takes, as indicated in its name, two steps. During the first one, the most significant bits of the digital output are determined by the first stage flash ADC. Then a DAC converts this digital result back to an analog signal to be subtracted from the input signal. This residue is then sent to the second stage flash ADC which determines the least significant bits of the digital output. The conversion time for a two-step flash ADC is longer than for a simple flash, but it is still very fast. Furthermore, the two-step flash ADC requires only $2 \times 2^{n/2}$ comparators. Thus, it saves hardware. As a result, two-step flash ADCs are often used in the 10-bit resolution range.

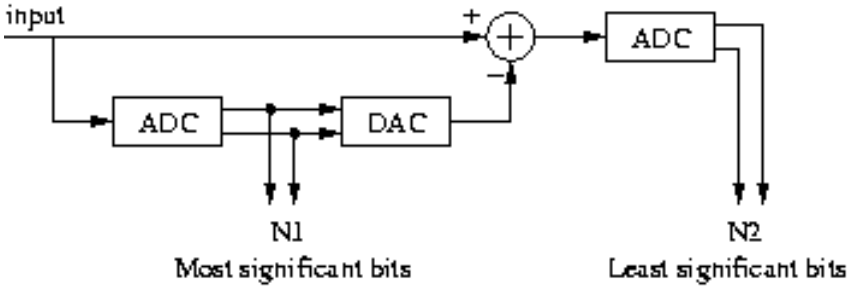


Figure 2.2: Semi-flash ADC

The folding ADC architecture [17, 18, 19, 20, 21] is a popular subset of the two-step flash architecture. In this architecture, the DAC and differencing blocks are replaced by an analog preprocessing circuit called a folding circuit. The folding circuit has a triangular input-output characteristic. The output of this block can be used as the input to a fine ADC that determines the least significant bits of the digital output.

Decreasing even more the hardware requirement is the goal of subranging architecture. A subranging ADC [22, 23, 24, 25, 26, 27, 28, 29] is a multi-step converter architecture that includes two-step flash ADCs and other ADCs that extend the concept of the two-step flash ADC to a larger number of steps. By breaking the conversion process into multiple steps, fewer comparators are required at the cost of the longer conversion time. Each stage is responsible for resolving some part of the digital output word and delivering a residue to the following stage. The conversion time required increases while the hardware required decreases with the number of stages. Thus, there is a trade-off between speed and hardware. The comparators in the front stages need not be very accurate, but the comparators in the last stage must be accurate to the full resolution of the ADC.

From their principle, the flash converters are limited to 6- or 8-bit, which is insufficient for instrumentation. This handicap is negligible in digital oscilloscopy: certain manufacturers use 6-bit converters, which are enough to describe the vertical axis of screen with a resolution higher than 2%. They are also used for DVD and hard disks readers. For the applications requiring high but not extreme speeds, we can use semi-flash or multi-step converters, which use much less comparators and preserve an interesting speed of conversion, with a resolution capable to reach 12-bit.

2.3 Successive Approximation ADC

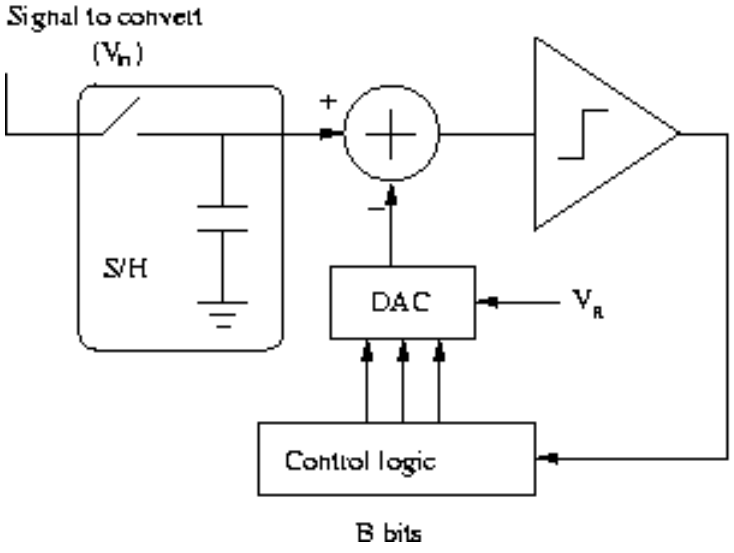


Figure 2.3: Successive approximation ADC structure

A successive approximation ADC [30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52], also known as a binary search ADC, is a special type of subranging ADC that uses a DAC to produce an analog signal that approximates the input sample. By adjusting the DAC until its output matches the input sample, a digital code representing the analog input can be generated. A successive approximation ADC consists of only one stage containing a S/H, an ADC, a DAC, and a digital processor that controls the DAC. An example of a successive approximation ADC is shown in the block diagram in Figure 2.3. In this example, the ADC consists of a single comparator. The operation of the successive approximation ADC is as follows. The control logic is initialized, and this initializes the output of the DAC. A sample of the input signal is taken by the S/H circuit,

and the initial DAC output is subtracted from the input sample. The difference is quantized by the comparator which instructs the control logic to either increase or decrease the DAC output. The new DAC output is again subtracted from the input sample, and the process repeats until the desired accuracy is obtained. This single comparator successive approximation ADC resolves one bit per cycle.

The advantage of this converter is a very little hardware requirement. Without considering the S/H, no amplifier is required, and only a single comparator is needed. By calibrating or trimming the DAC, very high resolution can be obtained. But its disadvantage is that the number of cycles required per sample is proportional to the number of bits. Therefore, this converter architecture is slower than a flash.

Concerning their applications, these components are very popular, from digital audio to data acquisition card and also in micro controllers.

2.4 Pipeline Converter

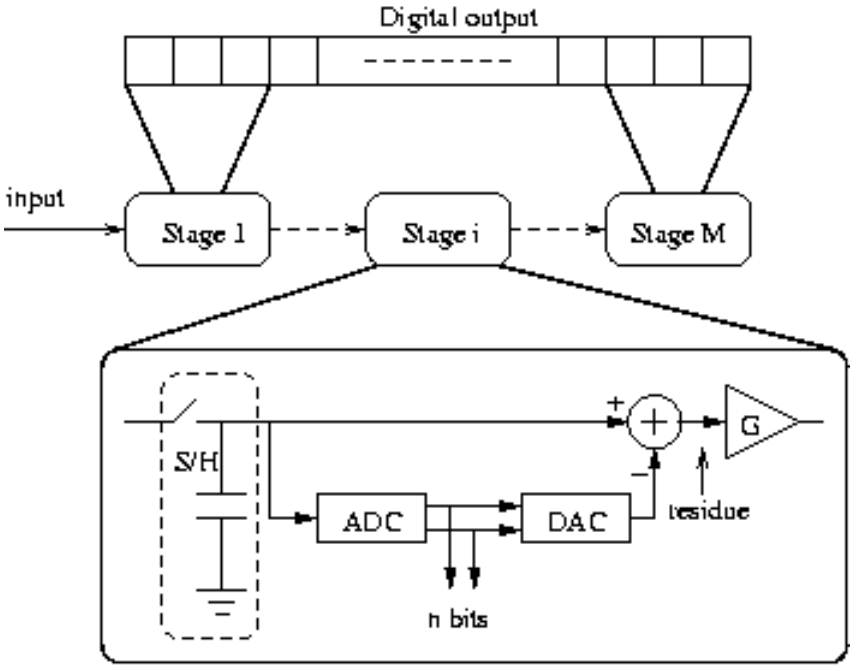


Figure 2.4: Pipeline ADC structure

A pipelined ADC [53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69] is another type of subranging ADC which improves the throughput rate and tolerance

to comparator errors. The block diagram in Figure 2.4 shows its structure. The pipelined ADC is similar to the subranging ADC with the exception that a sample-and-hold (S/H) circuit and amplifier has been added to each stage. The S/H circuit is used by the first stage to sample the input. Subsequent stages use a S/H circuit to sample the residue from the previous stage. This feature allows each stage of the pipeline to begin processing a new sample as soon as its residue is sampled by the following stage. Thus, the throughput rate is independent of the number of stages in the pipeline. Because of this feature, pipelined ADCs can generally operate at much higher sampling rates than other subranging ADCs.

Although the throughput rate is independent of the number of stages in the pipeline, conversion time for any given sample is proportional to the number of stages in the pipeline. This is because the signal must work its way through all of the stages before the complete output word is generated. This delay can be an issue if the pipelined ADC is part of a feedback system.

The amplifier is used to amplify the residue before passing it on to the next stage. By doing this, the resolution requirements for the following stages are relaxed. One significant implication of this is that the comparators in the last stages of the pipeline need not be accurate to the full ADC resolution as they are required to be in other subranging ADCs.

The disadvantage of adding the gain blocks is that they tend to be the dominant source of power dissipation in the ADC. Therefore, pipelined ADCs tend to dissipate more power than subranging ADCs. But like the other subranging ADCs, pipelined ADCs can achieve high resolutions with relatively little hardware. Furthermore, mismatches can be eliminated by self-calibration techniques.

In raison of their tolerance to comparator offsets and the ability of the pipeline stages to operate in parallel, pipelined ADCs are well suited for high resolution applications where high speed is required.

2.5 Time-Interleaved ADC

When even higher conversion speed is desired, parallelism can be applied. Figure 2.5 shows a system view of the architecture for parallel pipeline ADC. The parallelism has been initially used with Nyquist converter [70, 71, 72, 73, 74, 75, 76, 77]. This

technique consists of implementing identical ADCs in parallel and then activating ADCs one by one with some delays. If N channels are used, each channel is operated at frequency of f_s/N, where f_s is the system overall sampling frequency. A multiplexer and a demultiplexer are used at the input and the output of the system. This way, throughput of the system is increased by N times at the cost of increasing hardware. Since a DAC reference can be shared by all the channels, the hardware requirement increases less than the first order linear dependence. Sharing DAC reference is also desired to improve the matching of the channels.

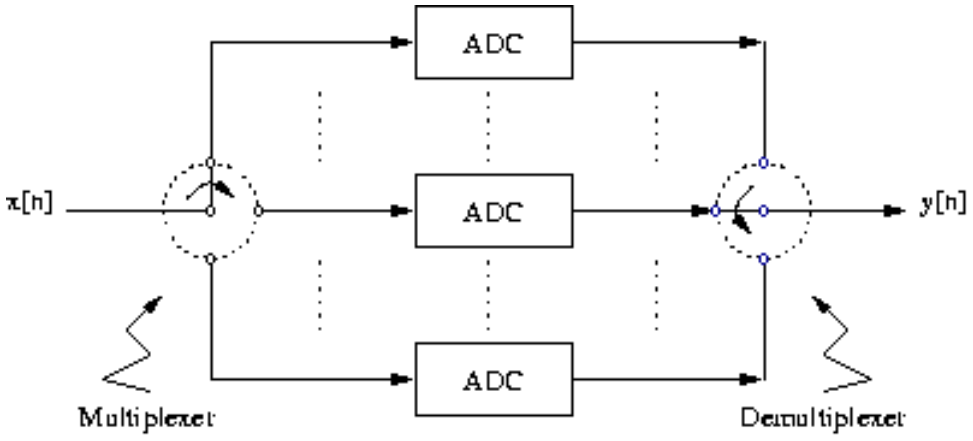


Figure 2.5: Time-interleaved ADC structure.

The most critical problem that needs to be solved in parallel structure is how to improve the matching between channels. This directly affects the highest resolution we can achieve [78, 79]. Calibration techniques have been investigated to minimize the effect of channel mismatch [71, 79, 80, 81, 82, 83]. Another problem of this kind of converter is the clock jitter which modifies both the overall quantization noise and signal. To solve this problem, an additional sampler operating at N times higher than the others, can be used as shown in [84].

The throughput rate of time-interleaved converter can reach some gigasamples per second. However, the resolution is very limited. It cannot exceed 8-bit. The time-interleaved converter is thus used in the very high speed applications, for example digital oscilloscopy.

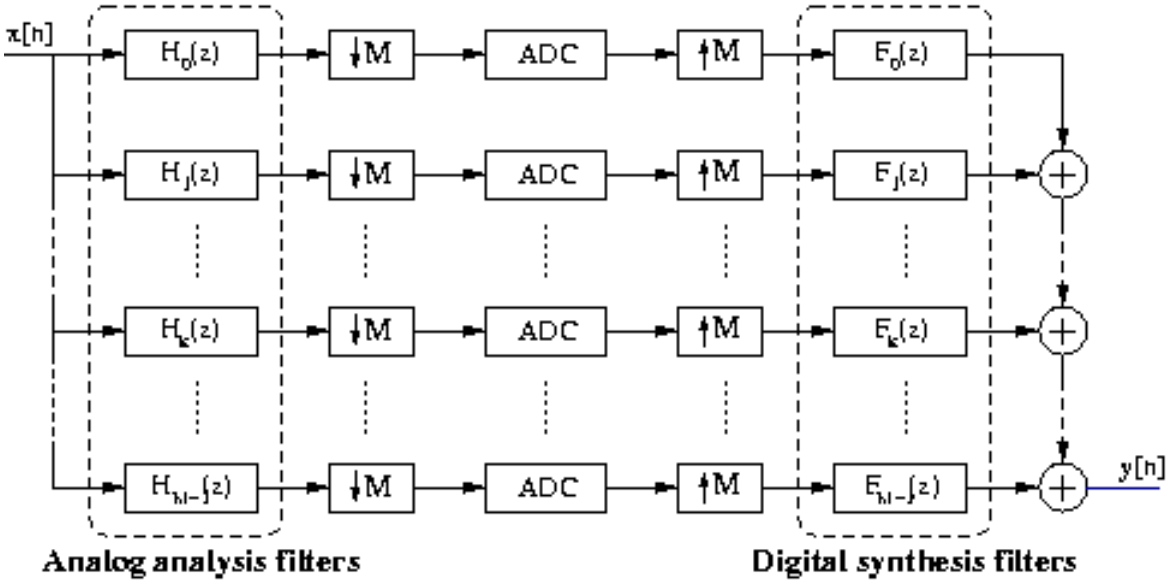


Figure 2.6: Hybrid filter bank ADC architecture.

2.6 Hybrid Filter Bank ADC

Using a hybrid filter bank for ADC is an unconventional application of the hybrid filter bank architecture that improves the speed and resolution of the conversion over the standard time-interleaved conversion technique [2, 85, 86, 87]. Hybrid filter bank ADC uses analog analysis filter to allocate a frequency band to each ADC in the array and digital synthesis filter to reconstruct the digitized signal as shown in Figure 2.6. The time-interleaved ADC architecture is just a particular case of the hybrid filter bank ADC architecture where analog analysis and digital synthesis filters are replaced with delays. The hybrid filter bank ADC significantly improves the speed and resolution of the conversion by attenuating the effect of the mismatches between the converters in array, which otherwise severely limit the resolution of the system. This advantage raises from the isolation of the converters in array from each other, what the time-interleaved system cannot do. The hybrid filter bank is expected to provide analog-to-digital conversion with resolution between 10 and 14-bit at a speed from 50 to 300 megasamples per second [86, 87].

However this kind of converter has some drawbacks. The major one is the complexity of the analog analysis filters. A particular strategy must be found to avoid high-order filter. Algorithms of iterative design to calculate successively the filter transfer function could be considered [86, 87]. The jitter problem is a delicate one

and must be investigated more deeply.

Applications of high speed, high resolution ADC include direct digital receivers for wireless communications application, radar receivers, test equipment such as oscilloscopes, spectrum analyzers, networks analyzers, digital and pattern generators, modem and medical imaging systems.

2.7 $\Delta\Sigma$ Converter

Currently, the analog-to-digital conversion using oversampling and $\Delta\Sigma$ modulation techniques [1, 88, 89, 90], provides the highest resolution ADCs. The operation of this kind of converter is based on a $\Delta\Sigma$ modulator which repeatedly samples the input and performs a few bits quantization of the error between the signal and its estimate. By sampling the signal many times, errors due to the coarse quantization and noise are averaged out. The quantized data is then digitally post filtered and decimated to attenuate the quantization noise power under the desired level. While the performance of the converters, in terms of resolution and speed, is primarily determined by the analogical modulator, the filter of decimation determines surface and consumption. A more detailed overview of conventional $\Delta\Sigma$ modulator and an investigation of high-pass $\Delta\Sigma$ modulator will be presented in Chapter 3.

In parallel with analog-to-digital conversion, other applications of the $\Delta\Sigma$ modulation have been developed. Realizing the modulator thanks to a digital stage, and filtering the resulting signal by an analog low-pass filter, carry out a DAC having performance as good as that of the best conventional DAC [91, 92]. Other operations can be realized thanks to the $\Delta\Sigma$ modulation [93]. For example, we can produce FIR [56, 94] or IIR [95] filters without multiplier, adaptive filters [96], amplitude modulator [97] or PLL [98].

A major drawback of $\Delta\Sigma$ ADC is its limited conversion bandwidth. This is because of oversampling requirement. Recently, $\Delta\Sigma$ ADC with low sampling ratio that uses conventional $\Delta\Sigma$ ADCs in parallel to extend the conversion bandwidth of the overall ADC, was introduced [3, 4]. A time-interleaved $\Delta\Sigma$ converter is a particular case of the parallel $\Delta\Sigma$ converter. As any parallel architecture, this one suffers from channel mismatch. This problem will be minimized by using high-pass $\Delta\Sigma$ modulators and channel equalization technique. This will be presented in

Chapter 4.

2.8 Conclusion

Various ADC architectures have been presented. Their principle of operation, advantages and drawbacks, and also their application field have been discussed. All the converters can be gathered into three large families: the flash, the pipeline and the $\Delta\Sigma$ converters.

The flash converters are certainly the fastest. They can currently reach a speed of some gigasamples per second. However, they have a relatively low precision which does not exceed 8-bit.

The pipeline converters are an intermediate solution between the high speed and high resolution conversion. Thanks to digital calibration techniques, this kind of converter can currently have a relatively high resolution that can reach 14-bit. An advantage of the pipeline converters is that they are able to give a precision at desired sampling frequency, provided that this desired resolution is not very high. Some authors announce that the precision of the pipeline converter can be comparable with that of the $\Delta\Sigma$ converter thanks to digital calibration.

The $\Delta\Sigma$ converters are certainly the most precise. They can have a resolution of 24-bit. Apart from high resolution, they have other attractive properties, especially high dynamics, high linearity and low sensitivity to circuit imperfections. The major drawback of these converters is the limited bandwidth because of oversampling. Because of their many interesting properties, much research has been involved in order to increase the passband of the input signal using the $\Delta\Sigma$ modulation like parallel $\Delta\Sigma$ converter. But it still remains in the field of research.

Like the parallel $\Delta\Sigma$ converters, the converters using the hybrid filter bank are promising. But again, they is still in the field of research. Only time-interleaved converter is already industrialized.

Chapter 3

High-Pass Delta Sigma Modulator

3.1 Introduction

High resolution low cost ADCs have been widely used in the application areas of instrumentation, measurement, telecommunications, digital signal processing, and consumer electronics, etc. Primarily because of advances in Very Large Scale Integration (VLSI) technologies, among different types of ADCs, that based on oversampling and $\Delta\Sigma$ modulation has become more and more attractive in applications requiring high precise analog-to-digital conversion with narrow bandwidth [1, 88, 89, 90]. Their popularity derives from their reduced analog processing and relaxed sensitivity to analog circuit errors in comparison with other analog-to-digital conversion approaches. These advantages come at the expense of a relatively large amount of digital processing and the requirement that much of the circuitry must run at clock speeds that are significantly higher than the analog-to-digital conversion rate. Although they employ complicated digital circuitry, their relatively simple analog circuitry tends to be robust with respect to nonideal circuit behavior [1, 99, 100]. They generally do not require the trimmed components necessary in conventional high precision ADCs. Consequently, high precision $\Delta\Sigma$ ADC can be implemented using high density VLSI processes optimized for digital circuitry wherein analog accuracy tends to be sacrificed in favor of increased circuit density and speed. This allows integration of the ADC with others digital signal processing components. Such integration gives rise to smaller, more reliable and less expensive system.

Typically, $\Delta\Sigma$ ADCs consist of a $\Delta\Sigma$ modulator followed by a digital decimation

filter. The $\Delta\Sigma$ modulator samples the input signal at many times the Nyquist rate (process referred to as oversampling) and performs very coarse analog-to-digital conversion at the resulting narrow-band sequence. Through the use of coarse digital-to-analog conversion and feedback, the quantization error introduced by the coarse quantizer is spectrally shaped (process referred to as quantization noise shaping) so that its power resides primarily outside the signal band. The digital decimation filter removes the out-of-band portion of the quantization error and reduces the output rate to the Nyquist rate of the input signal.

Oversampling, in conjunction with quantization noise shaping and decimation filtering, thus results in the effect of high precision ADC despite the use of coarse ADC and DAC. In particular, 1-bit ADC and 1-bit DAC are often used which have the added benefit that static errors in their analog levels only affect the gain and offset of the overall system. Moreover, other types of errors originated from nonideal circuit behavior such as analog noise are at least partially removed by the decimating filter. Oversampling also permits the use of simple, low-order analog antialiasing filters because much of the required antialiasing functionality can be included in the digital decimation filter.

Without considering the inherent internal circuit noise, the oversampling and $\Delta\Sigma$ modulation can perform extremely high resolution analog-to-digital conversion without high accuracy device matching. In practical, however, the circuit low frequency noise, such as flicker noise, offset voltage of the op-amp (offset noise) and clock feedthrough noise, always exists in the circuit and degrades seriously the performance of the $\Delta\Sigma$ modulators. Two major techniques, namely the correlated double sampling [101, 102, 103] and chopper stabilization [102, 103, 104, 105] have been proposed and applied to the operational amplifier (op-amp) to reduce the low frequency noise problem. However, the noise reduction is not very efficient and the resolution is still degraded. In this chapter, a new architecture called the high-pass $\Delta\Sigma$ modulator is proposed to solve the problem and also improve the performance of parallel architecture. In this architecture, the chopper stabilized technique is applied to the $\Delta\Sigma$ modulator, rather than to the op-amp, to efficiently reduce the circuit noise. The simulation results have verified the new design concept.

In this chapter, the high-pass $\Delta\Sigma$ modulator will be deeply investigated. Its principle, characteristics, stability, and also its basis building block and performance will be presented in the next six sections.

3.2 Conventional $\Delta\Sigma$ Modulator

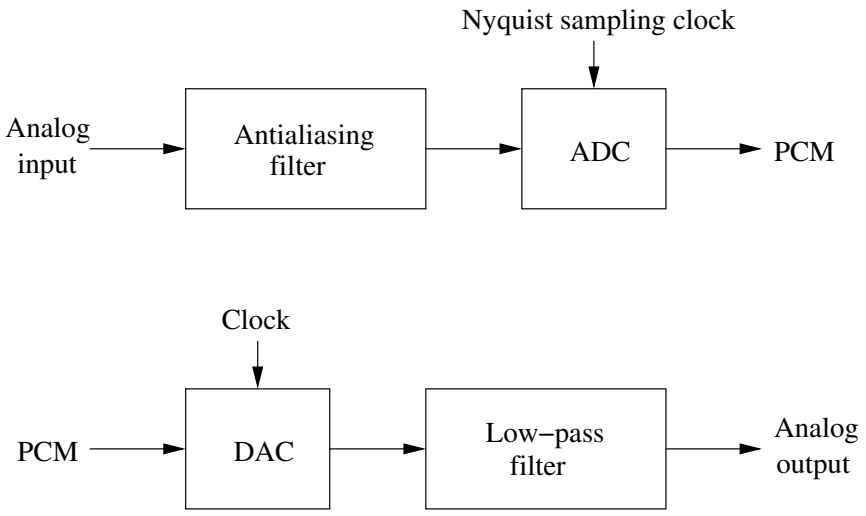


Figure 3.1: Conventional pulse code modulation (PCM), including analog antialiasing filter for curtaining the aliasing noise in the encoder and for smoothing the output from the decoder.

Conventional converters, illustrated in Figure 3.1, are often difficult to be implemented in fine-line VLSI technology. It is because conventional methods need precise analog components in their filters and conversion circuit, and also because their circuits can be very vulnerable to noise and interference. The virtue of the conventional methods is their use of a low sampling frequency, usually the Nyquist rate of the signal, i.e. twice the signal bandwidth.

Unlike the conventional converters, the oversampling or $\Delta\Sigma$ converters, illustrated in Figure 3.2, can use simple and relative high-tolerance analog components to achieve high resolution. However, they require fast and complex digital signal processing stages. These converters modulate the analog signal into a simple code, usually single-bit words, at a frequency much higher than the Nyquist rate.

By exploiting the speed of a VLSI technology, it is often possible to sample the input signal at a rate much higher than the Nyquist rate. The oversampling offers the immediate advantage of relaxing the requirement for a steep transition band on the antialiasing filter, as illustrated in Figure 3.3. However, oversampling by itself leads to only modest improvements in resolution of the converter. If the quantizer is also embedded in a feedback loop, it is possible to significantly increase the resolution

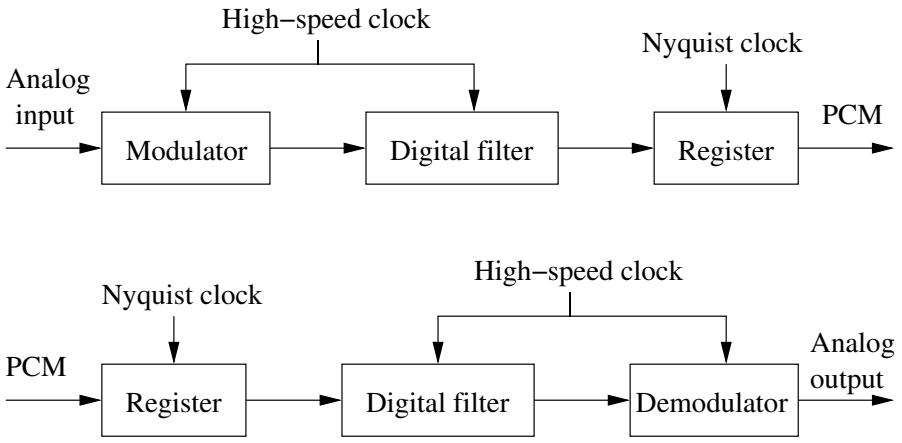


Figure 3.2: Oversampling pulse code modulation. The modulation and demodulation occur at sufficiently high sampling rate that digital filters can provide most for the antialiasing and smoothing functions.

of a converter beyond what can be achieved simply by oversampling.

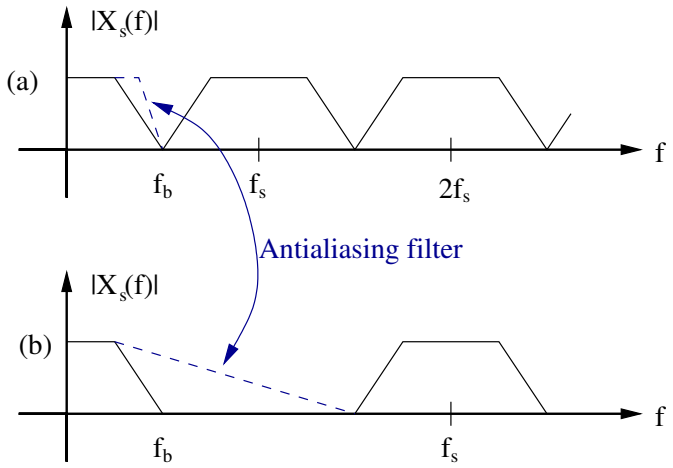


Figure 3.3: An analog signal that has been (a) sampled at the Nyquist rate, and (b) oversampled.

It is important to note that the quantization process in a $\Delta\Sigma$ converter employing feedback differs fundamentally from that in a Nyquist rate converter. Indeed, in a $\Delta\Sigma$ converter, it is not necessary to quantize the signal to the full resolution of the converter because each sample of the input signal does not correspond to only one output sample. Rather, in the digital filter that follows the $\Delta\Sigma$ modulator, many coarsely quantized samples are processed to yield a more precise estimate of the analog input signal at a lower sampling rate. Thus, each output sample depends on

a long sequence of input samples. In many cases, single-bit quantization is sufficient in a $\Delta\Sigma$ modulator.

The resolution of a Nyquist rate converter can be increased in a straightforward manner by operating the converter at a sampling rate in excess of the Nyquist rate. Under certain conditions, the quantization error is often approximated as additive white noise despite the deterministic nature of the quantizer [106, 107, 108], the total noise power, $\Delta^2/12$, where Δ is the quantization step size, is uniformly distributed across the sampling bandwidth, $-f_s/2$ to $f_s/2$. When the input is oversampled, the signal bandwidth, $-f_b$ to f_b, is only a fraction of the sampling bandwidth, as depicted in Figure 3.4. Therefore, in the presence of oversampling, the inband power of the quantization noise can be expressed as

$$\sigma_e^2 = \frac{\Delta^2}{12}\frac{1}{OSR}, \tag{3.1}$$

where OSR, which is equal to the ratio of the sampling frequency to the Nyquist frequency, $OSR = f_s/(2f_b)$, is called the oversampling ratio. Thus, the quantization noise power, σ_e^2 , is reduced by a factor of OSR, and the maximum achievable signal-to-noise ratio (SNR) increases by 3 dB, or 1/2 bit, per octave of oversampling.

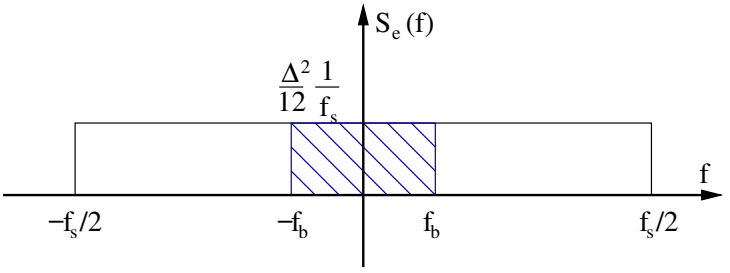


Figure 3.4: Power spectral density of quantization noise when the input signal is oversampled.

Simply increasing the sampling rate does not significantly improve the SNR of a Nyquist-rate converter. For example, in order to improve the resolution of a Nyquist-rate converter with a 22 kHz audio signal bandwidth from 8-bit to 16-bit, it is necessary to increase the sampling frequency of the converter from 44 kHz to over 2.8 GHz. Moreover, due to the correlation of the quantization error with the input signal, it is possible to place the converter in a state where no degree of oversampling will improve its resolution. An example of such a situation is when a dc input is applied to the converter. Fortunately, as will be reviewed in the following sections,

the inband quantization noise power can be suppressed dramatically by embedding the quantizer in a feedback loop. In this manner, the quantization noise is spectrally shaped such that the bulk of it is moved out of the signal passband. The structure formed by enclosing a quantizer in a feedback loop with filters in either, or both, the forward and return paths is commonly referred to as a feedback modulator.

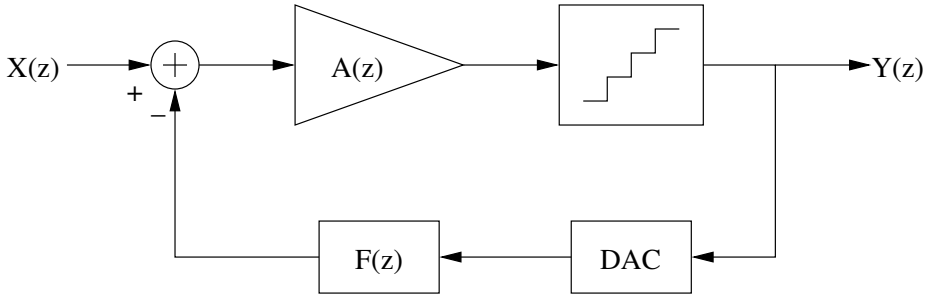


Figure 3.5: General structure of a feedback modulator.

The general structure of a feedback modulator is illustrated in Figure 3.5, which shows a quantizer embedded in a loop with a DAC in the feedback path. The transfer function of the filter in the forward path of the modulator is denoted $A(z)$, while the filter in the feedback path has the transfer function $F(z)$. The output of a feedback modulator is described in the z-domain by

$$Y(z) = \frac{A(z)}{1 + A(z)F(z)}X(z) + \frac{1}{1 + A(z)F(z)}E(z), \tag{3.2}$$

where $X(z)$ and $E(z)$ represent the transforms in z-domain of the input signal and quantization error, respectively.

Feedback modulators are commonly described in terms of two broad classes based on the characteristics of the forward-path and feedback-path transfer functions. In *predictive* modulators, the feedback filter, $F(z)$, has a large gain in the signal passband and provides an estimate of the input signal, which is then subtracted from the actual input to the modulator, $X(z)$. If the predicted value is close to the input value, the quantizer input will be small, allowing the use of a quantizer with a small input range. In fact, by encoding the rate of change of a signal rather than the signal itself, a *predictive* modulator can employ a quantizer with a small step size and a commensurately small quantization error. In contrast, *noise shaping* modulators do not reduce the magnitude of the quantization noise. Instead, a large frequency-dependent gain in the forward path, $A(z)$, is used to spectrally shape the quantization noise and suppress it in the signal passband. Most of the power in the

quantization noise is moved into the stopband where it is removed by a digital filter that follows the modulator.

In a predictive modulator, both the input signal and the quantization noise undergo spectral shaping [109, 110, 111, 112]. This fact has important implications in the practical implementation of feedback modulators. As it is shown in (3.2), the signal transfer function, $S(z)$, of a feedback modulator is

$$S(z) = \frac{A(z)}{1 + A(z)F(z)}. \tag{3.3}$$

Since the passband gain of the feedback filter, $F(z)$, is very high in a predictive modulator, the signal transfer function is approximately $1/F(z)$. Therefore, the digital filter that follows a predictive modulator must apply an inverse transfer function, $\hat{F}(z)$, which is a digital approximation of the analog feedback filter transfer function $F(z)$, to the output of the modulator in order to recover the input signal. Mismatch between $\hat{F}(z)$ and $F(z)$ presents an immediate limitation because the nonidealities in the analog circuits, that are the root cause of the mismatch, cannot be predicted *a priori*. Furthermore, mismatch-related errors are greatly amplified because the passband gain of $F(z)$ and $\hat{F}(z)$ is very high.

In noise shaping modulators, only the quantization noise is spectrally shaped [88, 113, 114, 115, 116]. The forward filter, $A(z)$, has a large passband gain and the feedback filter, $F(z)$, is independent of frequency in the passband. Therefore, the signal transfer function in (3.3) reduces to a constant in the passband, and the digital filter that follows a noise shaping modulator must only reject the large, out-of-band quantization noise without altering the frequency response in the signal passband. The performance of a noise shaping modulator is not limited by the need to match a digital decoding filter, $\hat{F}(z)$, to the analog feedback filter, $F(z)$, in the modulator. For this reason, noise shaping topologies are preferred if the feedback modulator is to be implemented with analog circuitry. Our research focuses therefore exclusively on noise shaping topologies.

At this stage, it is important to note that in the development of noise shaping techniques it was usually presumed that the signal passband was situated at baseband. However, spectral shaping of noise is not restricted to the low-pass domain. Rather, through an appropriate choice of the forward and feedback transfer functions, $A(z)$ and $F(z)$, it is possible to shape the bulk of the quantization noise power away from any region in the sampling bandwidth, $-f_s/2$ to $f_s/2$. The con-

cept of high-pass noise shaping will be developed later in this chapter after an initial discussion of low-pass noise shaping.

In noise shaping topologies, the forward path filter is designed to have a large gain in the passband in which the quantization noise is to be suppressed. As shown in Figure 3.5, if $F(z)$ is chosen to be 1, the z-domain expression for the output can be written as

$$Y(z) = \frac{A(z)}{1 + A(z)} X(z) + \frac{1}{1 + A(z)} E(z), \tag{3.4}$$

where $X(z)$ and $E(z)$ are the z-transforms of the input signal and quantization error, respectively. The quantization noise transfer function becomes

$$N(z) = \frac{1}{1 + A(z)}. \tag{3.5}$$

Therefore, if the quantization noise is to be suppressed in the baseband, $A(z)$ must have a large dc gain. There are many transfer functions that satisfy this condition and could be used to implement a noise shaping modulator. But the transfer functions comprised of integrators are specially suited for VLSI implementation, because the analog circuits required to implement the transfer function are simple and robust.

A z-domain representation of a first-order $\Delta\Sigma$ modulator is depicted in Figure 3.6. The modulator contains a subtraction node, a discrete-time integrator, and a 1-bit quantizer. The quantization noise is represented by the additive term, $E(z)$. The integrator ideally provides an infinite gain at dc, which, as seen in (3.4), is necessary to suppress the quantization noise at baseband. In a similar fashion, a simple high-pass $\Delta\Sigma$ modulator can be derived from the first-order low-pass prototype by replacing the integrator with a basis block that provides an infinite gain in the high-pass region of interest.

A multi-bit quantizer can be embedded in the feedback loop in order to improve the dynamic range of the modulator for a given oversampling ratio, or to reduce the oversampling ratio for a given dynamic range [117, 118, 119]. However, the multi-level DAC in the feedback path is then required to have a linearity equal to or exceeding the overall linearity of the modulator. Otherwise, nonlinearity in the feedback DAC will introduce harmonic distortion directly at the input to the modulator. Dynamic element matching techniques can be used to randomize and decorrelate the error from the nonideal DAC, thus causing the error to appear as an additive white noise, rather than as harmonic distortion, at the expense of increased power and

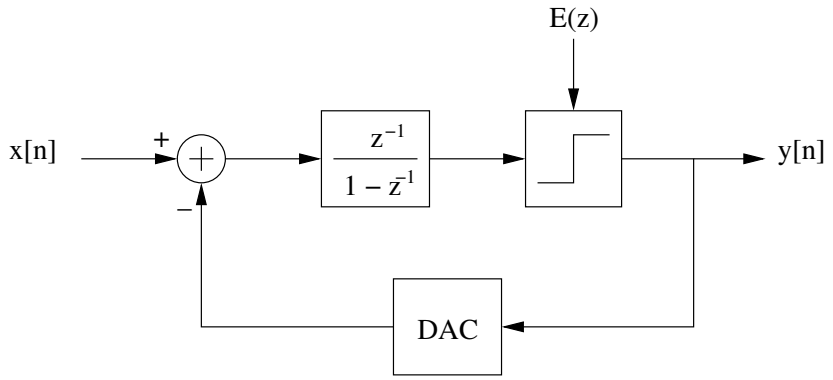


Figure 3.6: First-order low-pass $\Delta\Sigma$ modulator.

complexity in the modulator [120, 121, 122, 123]. Therefore, $\Delta\Sigma$ modulators are often implemented using inherently linear 1-bit quantizers and 1-bit DACs and are operated at oversampling ratios high enough to guarantee the suppression of the large quantization noise associated with an 1-bit quantizer. Single-bit DACs can still generate gain and offset errors in the feedback path, but $\Delta\Sigma$ modulators are relatively insensitive to these perturbations [88].

In the z-domain representation of the first-order $\Delta\Sigma$ modulator shown in Figure 3.6, the quantization noise is represented by an additive white noise source, $E(z)$. In fact, the 1-bit quantizer topology strongly violates the assumptions of the additive white noise model. In particular, the quantization noise is highly correlated with the input signal. However, it is useful to begin the analysis using this model to estimate the SNR of the modulator. The results are then confirmed through computer simulations of a behavioral model of the modulator. The 1-bit DAC is assumed to be ideal and does not introduce any additional noise. In the z-domain, the output of the first-order low-pass modulator is

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z), \tag{3.6}$$

which consists of the input, $X(z)$, delayed by one sample period, plus a first-order high-pass shaping of the additive quantization noise, $E(z)$.

Figure 3.7 shows the block diagram of second-order $\Delta\Sigma$ modulator with Boser's structure [88]. This structure is very efficient because of the two following reasons :

- Improvement of the input dynamic;
- The first-stage integrator can be used as the second-stage integrator. It implies

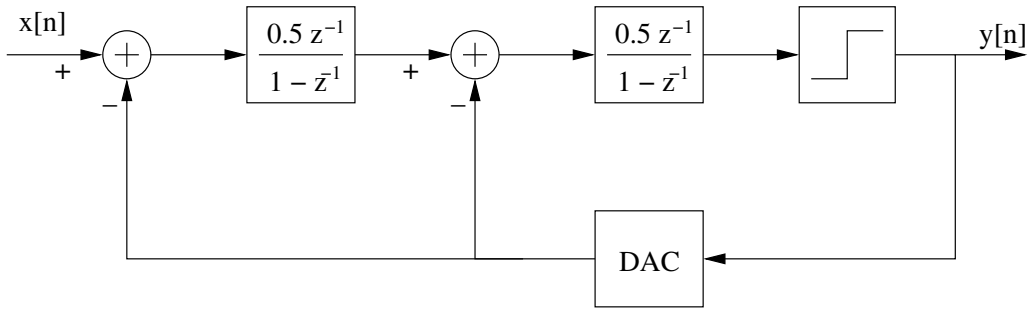


Figure 3.7: Second-order low-pass $\Delta\Sigma$ modulator with Boser's structure.

time reduction for circuit design and mask design.

The output of the second-order low-pass $\Delta\Sigma$ modulator can be qualitatively written as

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z). \tag{3.7}$$

The second-order shaping of $E(z)$ suppresses the quantization noise more effectively in the baseband than first-order shaping. In general, as the order of the noise shaping increases, the level of quantization noise present in the signal passband decreases and the out-of-band noise increases more than commensurately. Although the quantization noise is suppressed more effectively through the use of higher-order modulators, the order of a modulator cannot be increased arbitrarily because it is difficult to guarantee the stability of third- and higher-order single-bit modulators [124, 125, 126]. For certain combinations of input signals and initial conditions, the internal states of the higher-order modulator can continue to grow without bound, eventually saturate the analog circuitry. If this condition persists after the input signal to the modulator is removed, additional circuitry is needed to sense and reset the internal modulator states [127]. Special design procedures can be followed in order to guarantee that the modulator can recover when overdriven at the input or when initially placed in an overload state. Single-loop higher-order $\Delta\Sigma$ modulator can be stabilized by correct choice of filter coefficients and by restricting the region of operation [126, 128, 129]. Alternatively, higher-order modulators can be implemented by cascading first- and second-order modulators, which are known to be stable [92, 118, 130].

If the noise-differencing low-pass $\Delta\Sigma$ modulator topology is extended to the

L^{th}-order case, the noise transfer function is

$$N(z) = (1 - z^{-1})^L, \tag{3.8}$$

which in the frequency domain is

$$N(f) = N(z)|_{z=e^{j2\pi fT_s}} = \left(1 - e^{-j2\pi fT_s}\right)^L. \tag{3.9}$$

Under the additive white noise model, the power of the quantization noise, E(z), is $\Delta^2/12$, and is distributed uniformly in the sampling bandwidth, $-f_s/2$ to $f_s/2$. Therefore, the power spectral density of the quantization noise is

$$S_e(f) = \frac{P_e}{f_s} = \frac{\Delta^2}{12}\frac{1}{f_s}, \qquad -\frac{f_s}{2} < f < \frac{f_s}{2}, \tag{3.10}$$

and the spectral density of the shaped quantization noise is

$$S_Q(f) = |N(f)|^2 S_e(f) = (2sin(\pi fT_s))^{2L}\ \frac{\Delta^2}{12}\frac{1}{f_s}. \tag{3.11}$$

By integrating $S_Q(f)$ over the band of interest, the power of the quantization noise present in the signal band can be found. The out-of-band quantization noise is assumed to be rejected by a low-pass digital filter that follows the modulator. Since $f_b << f_s$, the integral can be evaluated under the approximation $sin(x) \approx x$ to yield an inband quantization noise power equal to

$$P_Q = \int_{-f_b}^{f_b} S_Q(f)df \approx \left(\frac{\pi^{2L}}{2L+1}\right)\left(\frac{1}{OSR^{2L+1}}\right)\frac{\Delta^2}{12}, \quad OSR >> 1. \tag{3.12}$$

For this 1-bit modulator, a full-scale sinusoid has a peak-to-peak amplitude equal to the quantization step size, Δ, and a power equal to $\Delta^2/8$. Hence, the dynamic range of an L^{th}-order, low-pass $\Delta\Sigma$ modulator as a function of OSR is

$$DR = \frac{3}{2}OSR^{2L+1}\frac{2L+1}{\pi^{2L}} \tag{3.13}$$

where, as defined previously, OSR is equal to the ratio of the sampling frequency to the Nyquist frequency, $OSR = f_s/(2f_b)$. This DR increases $3(2L+1)$ decibels for every doubling of sampling rate, providing $(L + \frac{1}{2})$ extra bits of resolution.

3.3 Presence of Low Frequency Noise

The presence of the low frequency noises, such as flicker noise or $1/f$ noise, and offset noise of the op-amp, degrades seriously the performance of $\Delta\Sigma$ converter. In

the SC integrator, the $1/f$ noise source are both integrated and translated by the integrator circuit, its effect can be conveniently represented by two noise sources equal in magnitude to the $1/f$ noise of the op-amp, one in series with the input of the SC integrator and one in series with the output [104]. The effect of the offset noise of the op-amp in the SC integrator can be considered as an offset noise source in series with the input of the integrator. Consequently, the effect of the low frequency noise in the SC integrator can be modelled as two additive low frequency noise sources, one at the input and one at the output of the integrator. As a result, for the first-order $\Delta\Sigma$ modulator, the effect of the low frequency noise is modelled as two low frequency noise sources, one denoted as $E^1_{lf}(z)$ in the input, and the other denoted as $E^2_{lf}(z)$ in the output of the integrator, as shown in Figure 3.8.

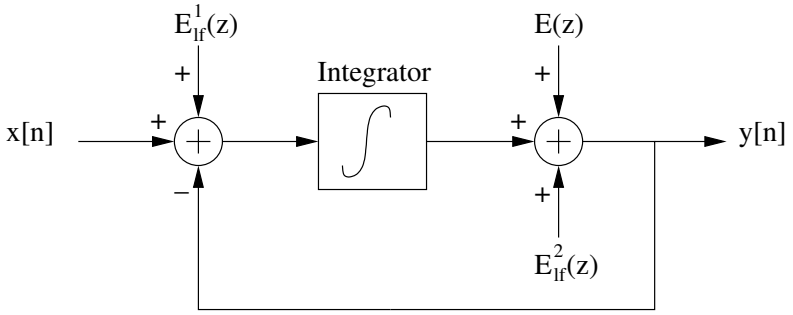


Figure 3.8: First-order $\Delta\Sigma$ modulator model with low frequency noise.

As the input signal, the first low frequency noise component $E^1_{lf}(z)$ goes through the modulator and results in a low frequency noise component at the output. The second low frequency noise component, as the quantization noise, is filtered by the quantization noise transfer function, $N(z)$, and results in $E^2_{lf}(z)\,N(z)$ at the output of the modulator. This component is still a low frequency noise component but negligible because the quantization noise transfer function, $N(z)$, has a very high attenuation at low frequency range. In other words, the overall low frequency noise effect can be modelled as a low frequency component at the output of the modulator.

In the presence of the low frequency noise, the equivalent of the second-order $\Delta\Sigma$ modulator is shown in Figure 3.9. The output signal contains another component denoted $E_{lf}(z)$ in addition to the useful signal and quantization noise. Then, the output of the second-order $\Delta\Sigma$ modulator can be written as

$$Y(z) = X(z)z^{-2} + E(z)(1 - z^{-1})^2 + E_{lf}(z), \tag{3.14}$$

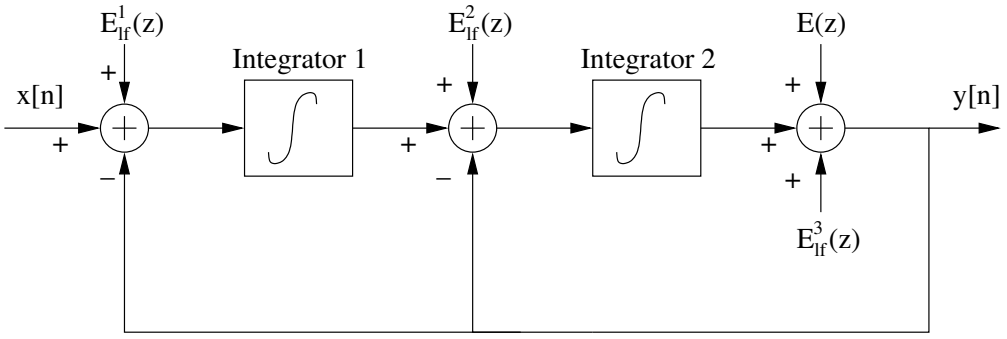


Figure 3.9: Second-order $\Delta\Sigma$ modulator model with low frequency noise.

where $E_{lf}(z)$ is

$$E_{lf}(z) = E^1_{lf}(z)z^{-2} + E^2_{lf}(z)z^{-1}(1-z^{-1}) + E^3_{lf}(z)(1-z^{-1})^2. \tag{3.15}$$

This equation reveals that the effect of $E^2_{lf}(z)$ and $E^3_{lf}(z)$ is negligible, but $E^1_{lf}(z)$ still goes through the modulator. In consequence, the effect of $1/f$ noise and offset noise can be modelled as a low frequency noise component at the output of the second-order $\Delta\Sigma$ modulator.

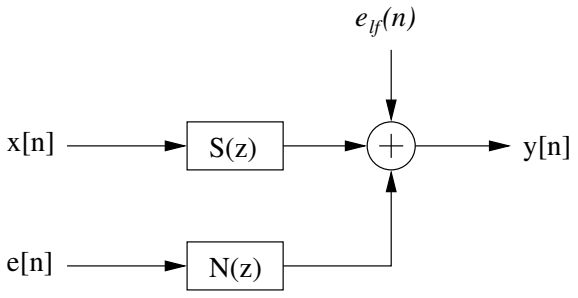


Figure 3.10: Conventional $\Delta\Sigma$ modulator model in the presence of the low frequency noise.

Continuing in the same reasoning, the same conclusion can be drawn for any low-pass $\Delta\Sigma$ modulator. The equivalent model of the conventional $\Delta\Sigma$ modulator in the presence of the low frequency noise is presented in Figure 3.10. It consists of an equivalent low frequency noise source $e_{lf}(n)$ and an additive noise source modelling the quantization noise. The function of the conventional delta sigma modulator can be characterized in the z-domain by

$$Y(z) = X(z)S(z) + E(z)N(z) + E_{lf}(z), \tag{3.16}$$

where $S(z)$ and $N(z)$ are the transfer function in z-domain of the input signal and quantization noise respectively, and $E(z)$ and $E_{lf}(z)$ represent the z-transform of the quantization noise and equivalent input low frequency noise, $e_{lf}(n)$, respectively. The last one directly contaminates the digital output signal.

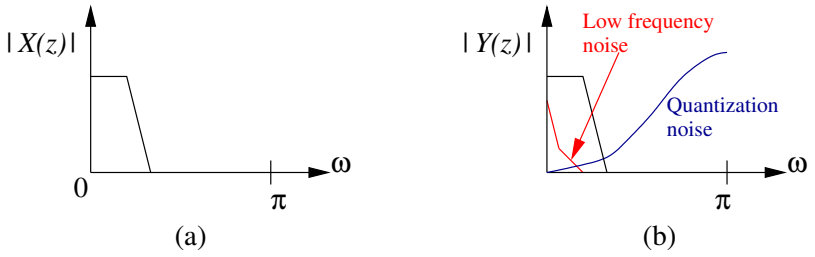


Figure 3.11: Spectrum representation of different signals in $\Delta\Sigma$ modulator. (a): input signal; (b): output signal in the presence of the low frequency noise.

Figure 3.11 presents the spectrum representation of various signals at the input and the output of the modulator. It also shows clearly the contamination of the low frequency noise to the digital output signal.

3.4 Principle of high-pass $\Delta\Sigma$ Modulator

The principles of noise shaping can be extended from the low-pass case, in which the quantization noise is suppressed around dc, to more general bandpass case where the quantization noise is attenuated in a narrow passband centered at an intermediate frequency. The quantization noise in a noise shaping modulator can be suppressed in any narrowband portion of the sampling bandwidth by designing the transfer function of the forward path filter, $A(z)$ in Figure 3.5, to have a resonant peak in the signal passband. In particular, the quantization noise can be shaped to low frequency region and suppressed in the high frequency region around one-half of the sampling frequency, $f_s/2$. The locations of zeros of the noise transfer function in the z-plan are then illustrated in Figure 3.12. They are at dc for the low-pass modulator and at $f_s/2$ for the high-pass one. The transformation of a low-pass to high-pass modulator is a low-pass to high-pass transformation for the quantization noise transfer function. It is also the low frequency to high frequency transformation for a signal. This transformation is in fact the transformation $z \rightarrow -z$ in z-domain. Therefore, the signal and quantization noise transfer functions of the high-pass modulator, denoted

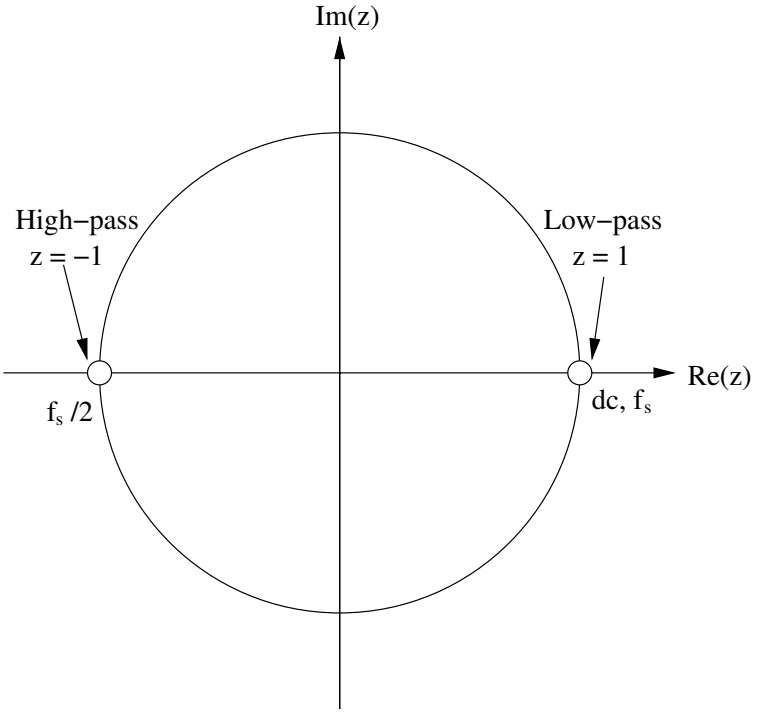


Figure 3.12: Locations of zeros of the noise transfer function in the z-plane.

as $S_{hp}(z)$ and $N_{hp}(z)$ respectively, are written as

$$S_{hp}(z) = S(-z), \tag{3.17}$$

$$N_{hp}(z) = N(-z), \tag{3.18}$$

where $S(z)$ and $N(z)$ are the signal and quantization noise transfer functions of the corresponding low-pass modulator. The signal transfer function of the high-pass $\Delta\Sigma$ modulator, $S_{hp}(z)$, has a passband around one-half of the sampling frequency so that the input signal in the frequency band around $f_s/2$ can go through the modulator. The quantization noise transfer function of the high-pass $\Delta\Sigma$ modulator $N_{hp}(z)$ have a very high attenuation around $f_s/2$ so that a large part of the quantization noise can be distributed out of the signal band around one-half of the sampling frequency.

As in the low-pass modulator, the effect of $1/f$ noise and the offset noise can be considered as an additive low frequency noise source at the output of the high-pass modulator. Figure 3.13 shows a high-pass $\Delta\Sigma$ modulator with an equivalent low frequency noise $e_{lf}(n)$, a chopper multiplication at the front-end, and a chopper multiplication at the back-end. The first chopper multiplication transforms a signal from low frequency range to high frequency one and the second chopper makes the converse operation.

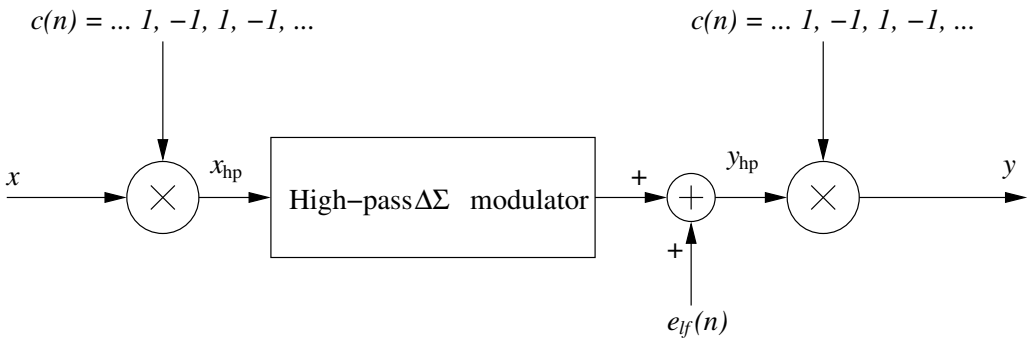


Figure 3.13: Chopper stabilized high-pass $\Delta\Sigma$ modulator in the presence of the low frequency noise.

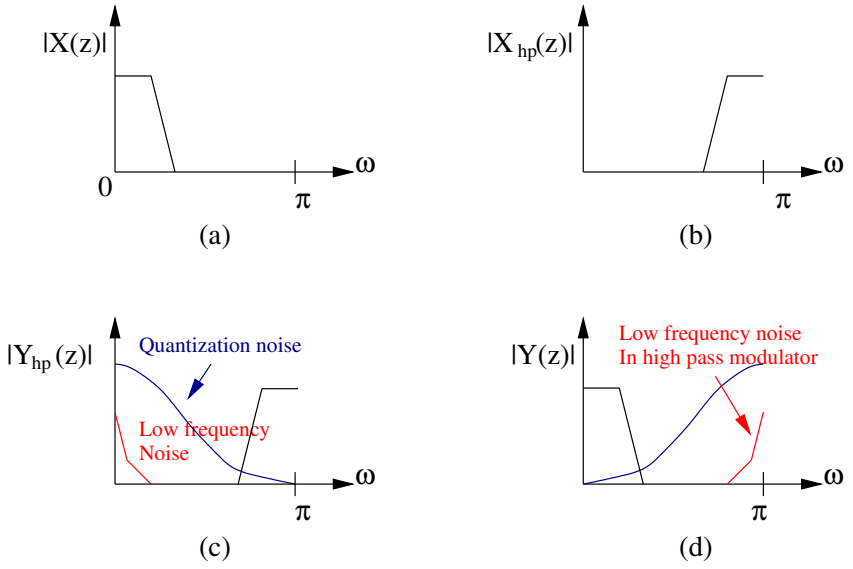


Figure 3.14: Evolution of the input signal in the frequency domain.

The operation principle of the schema block in Figure 3.13 is qualitatively described as follows. At first, the input signal x with the spectrum shown in Figure 3.14(a), is chopped into the band around one-half of the sampling frequency and then denoted as the signal x_{hp} with the spectrum shown in Figure 3.14(b). The signal x_{hp} adding with the low-frequency noise is modulated by the high-pass $\Delta\Sigma$ modulator and then becomes the signal y_{hp} as shown in Figure 3.14(c). Finally, the signal y_{hp} is chopped back to get the desired digital output signal y. At the same time, the low frequency noise is chopped out of the baseband. As shown in Figure 3.14(d), the digital output signal y is immune from the contamination of the low frequency noise.

The immunity from the low frequency noise can also be proved theoretically. Indeed, the chopper multiplication can be characterized in the z-domain as

$$X_{hp}(z) = X(-z), \tag{3.19}$$

$$Y(z) = Y_{hp}(-z), \tag{3.20}$$

The output of the high-pass $\Delta\Sigma$ modulator can be written as

$$Y_{hp}(z) = X_{hp}(z)S_{hp}(z) + E(z)N_{hp}(z) + E_{lf}(z). \tag{3.21}$$

By replacing $X_{hp}(z)$, $S_{hp}(z)$, and $N_{hp}(z)$ from the equations (3.17), (3.18), and (3.19) in the equation (3.21), it follows

$$Y_{hp}(z) = X(-z)S(-z) + E(z)N(-z) + E_{lf}(z). \tag{3.22}$$

From the equations (3.20) and (3.22), it results in

$$Y(z) = X(z)S(z) + E(z)N(z) + E_{lf}(-z). \tag{3.23}$$

The equation (3.23) is obtained this way because the quantization noise, $E(z)$, is assumed to be white noise (E(z) = E(-z)). As shown in the equation (3.23), the output circuit noise term becomes $E_{lf}(-z)$ which is a high frequency term because $E_{lf}(z)$ is a low frequency term. Therefore, it will not contaminate the digital output signal which is at low frequency range.

The signal and quantization noise transfer functions of the high-pass modulator are obtained by applying the transformation $z \rightarrow -z$ to that of the low-pass one. Therefore, the high-pass modulator can be realized by applying the transformation $z \rightarrow -z$ to a low-pass modulator. Ideally, the transformation does not affect the

dynamics of the low-pass prototype $\Delta\Sigma$ modulator; consequently the resulting high-pass modulator is stable if the provided low-pass prototype is stable. In a similar manner, the z-transform of the basis block building the high-pass modulator is realized by applying this transformation to an integrator, the basis block building the low-pass modulator whose z-transform is given by

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{3.24}$$

Consequently the transfer function of the basic block of the high-pass modulator is given by

$$H_{hp}(z) = \frac{-z^{-1}}{1 + z^{-1}}. \tag{3.25}$$

This transfer function can be described such that each output sample is the negative of the sum of the previous input plus the previous output.

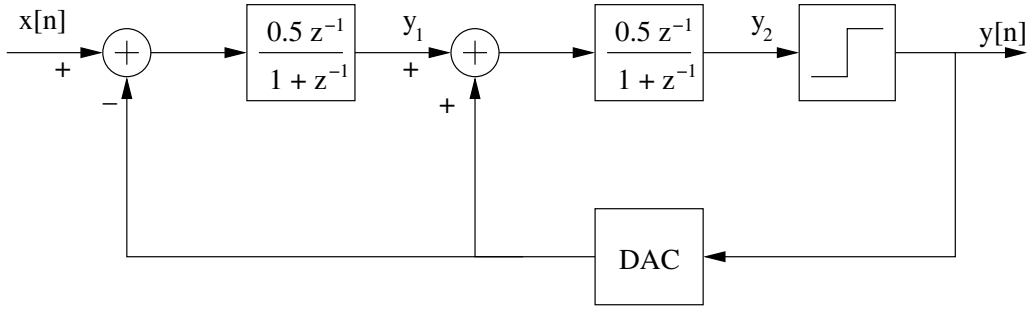


Figure 3.15: Second-order high-pass $\Delta\Sigma$ modulator.

Figure 3.7 represents typically a low-pass second-order $\Delta\Sigma$ modulator with Boser's structure. Applying the transformation $z \rightarrow -z$ results in the structure of the second-order high-pass $\Delta\Sigma$ modulator which is shown in Figure 3.15. In z-domain, the output of the second-order high-pass $\Delta\Sigma$ modulator is

$$Y(z) = z^{-2}X(z) + \left(1 + z^{-1}\right)^2 E(z). \tag{3.26}$$

The $z \rightarrow -z$ transformation has changed the zeros of low-pass noise transfer function in the z-domain from $z = 1$ to $z = -1$, the noise suppression region has been shifted from dc to $f_s/2$.

3.5 Performance of high-pass $\Delta\Sigma$ Modulator

The dynamic range of a high-pass $\Delta\Sigma$ modulator can be estimated in the same manner used to calculate the dynamic range of a low-pass modulator. If the archi-

tecture illustrated in Figure 3.15 is extended to the L^{th}-order case by applying the transformation $z \rightarrow -z$ to the L^{th}-order low-pass architecture, the resulting noise transfer function is

$$N_{hp}(z) = \left(1 + z^{-1}\right)^L, \tag{3.27}$$

which in the frequency domain can be written as

$$N_{hp}(f) = N_{hp}(z)|_{z=e^{j2\pi fT_s}} = \left(1 + e^{-j2\pi fT_s}\right)^L. \tag{3.28}$$

Assuming that the quantization noise, $E(z)$, is additive white noise, with a total power of $\Delta^2/12$ that is distributed uniformly in the sampling bandwidth, $-f_s/2$ to $f_s/2$, the power spectral density of $E(z)$ is

$$S_e(f) = \frac{\Delta^2}{12}\frac{1}{f_s}, \qquad -\frac{f_s}{2} < f < \frac{f_s}{2}. \tag{3.29}$$

The spectral density of the shaped quantization noise is given then by

$$S_Q(f) = |N_{hp}(f)|^2 S_e(f) = (2cos(\pi fT_s))^{2L}\ \frac{\Delta^2}{12}\frac{1}{f_s}. \tag{3.30}$$

The power of the quantization noise in the signal band can be found by integrating the power spectral density of the shaped quantization noise over the band of interest. The out-of-band quantization noise is assumed to be rejected by a digital filter that follows the modulator. The input signal of the high-pass ΔΣ modulator is at high frequency region. The signal band is thus $f_s/2 - f_b$ to $f_s/2$ and plus $-f_s/2$ to $f_b - f_s/2$, which is equivalent to apply the transformation $z \rightarrow -z$ to a low frequency signal of band $-f_b$ to f_b. Since the signal band, $2f_b << f_s$, the integral can be evaluated under the approximation $cos\left(\frac{\pi}{2} - x\right) = sin(x) \approx x$ to yield an inband quantization noise power equal to

$$\begin{aligned} S_Q &= \int_{\frac{f_s}{2}-f_b}^{\frac{f_s}{2}} S_Q(f)df + \int_{-\frac{f_s}{2}}^{-\frac{f_s}{2}+f_b} S_Q(f)df && (3.31)\\ &= 2\left[\int_{\frac{f_s}{2}-f_b}^{\frac{f_s}{2}} (2cos(\pi fT_s))^{2L}\ \frac{\Delta^2}{12}\frac{1}{f_s}df\right] && (3.32)\\ &\approx \frac{\Delta^2}{12}\frac{\pi^{2L}}{2L+1}\frac{1}{OSR^{2L+1}}, \qquad OSR >> 1 && (3.33) \end{aligned}$$

where OSR is the oversampling ratio defined here as $f_s/(2f_b)$. Thus, the expression for inband quantization noise power calculated in (3.33) takes on the same form as the expression derived for an L^{th}-order low-pass modulator in (3.12). For this 1-bit modulator, a full-scale sinusoid has a peak-to-peak amplitude equal to the

quantization step size, Δ, and a power equal to $\Delta^2/8$. Hence, the dynamic range of a L^{th}-order high-pass $\Delta\Sigma$ modulator as a function of OSR, is

$$DR = \frac{3}{2} OSR^{2L+1} \frac{2L+1}{\pi^{2L}} \tag{3.34}$$

The expression of the dynamic range for the L^{th}-order high-pass modulator in (3.34), also corresponds to that of an L^{th}-order low-pass modulator in (3.13).

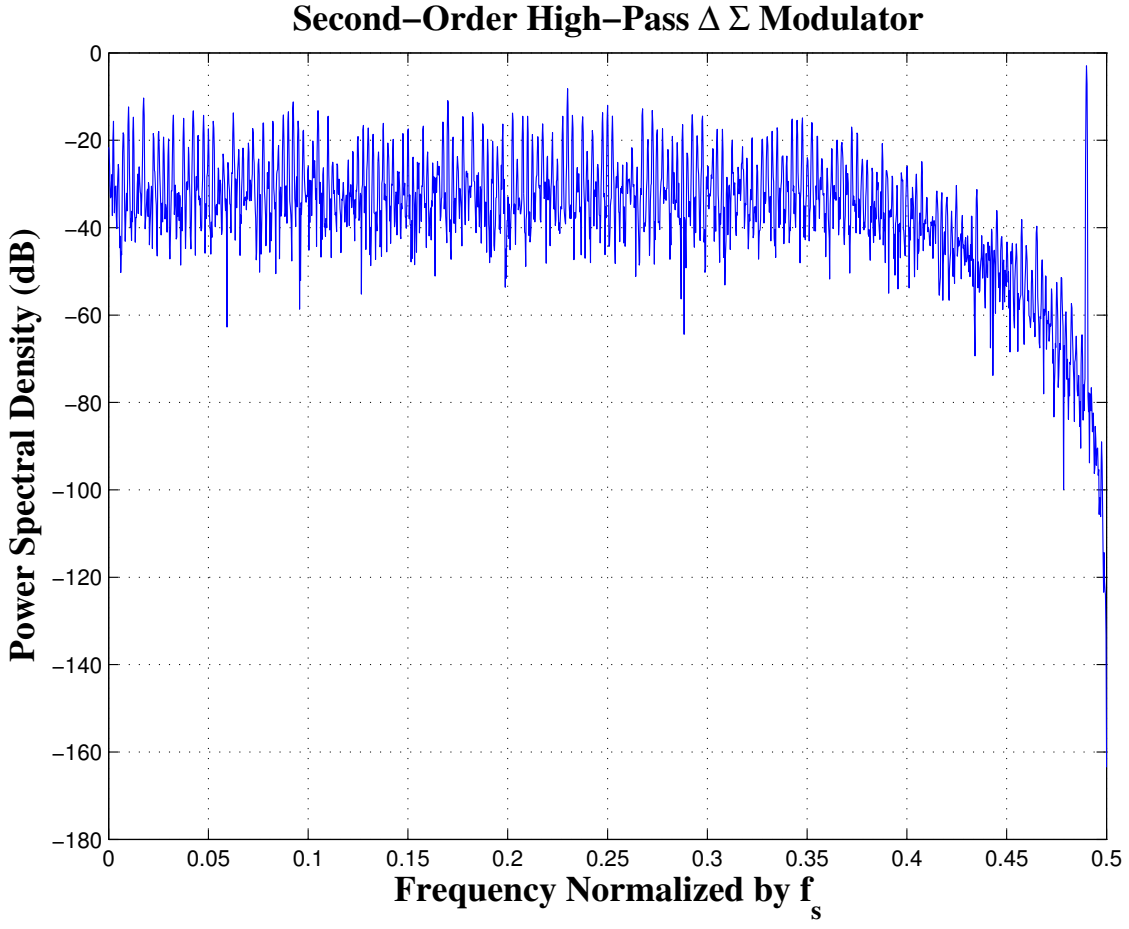


Figure 3.16: Undecimated spectrum of digital output signal of second-order high-pass $\Delta\Sigma$ modulator.

The expressions that have been derived for the inband quantization noise power, (3.33), and the dynamic range, (3.34), of the L^{th}-order high-pass modulator closely match the results of simulation of the modulator using MATLAB. The following figures show results from these simulations. In the following discussion, the modulator's full-scale analog input range is defined as the step size of its single-bit quantizer, Δ. Figure 3.16 shows the undecimated spectrum of digital output signal of second-order high-pass $\Delta\Sigma$ modulator of Figure 3.15 when a high frequency signal obtained

by transforming a sinusoid of amplitude normalized of 0.5 is applied. Figure 3.17 show that the signal-to-noise ratio with $OSR = 32$ and $f_s = 10MHz$, versus the input signal level, closely corresponds to the straight-line characteristic derived from a linearized model of the modulator in (3.34). The input signal having a frequency of 4.985 MHz is obtained by transforming a sinusoid of frequency 15kHz to high frequency region.

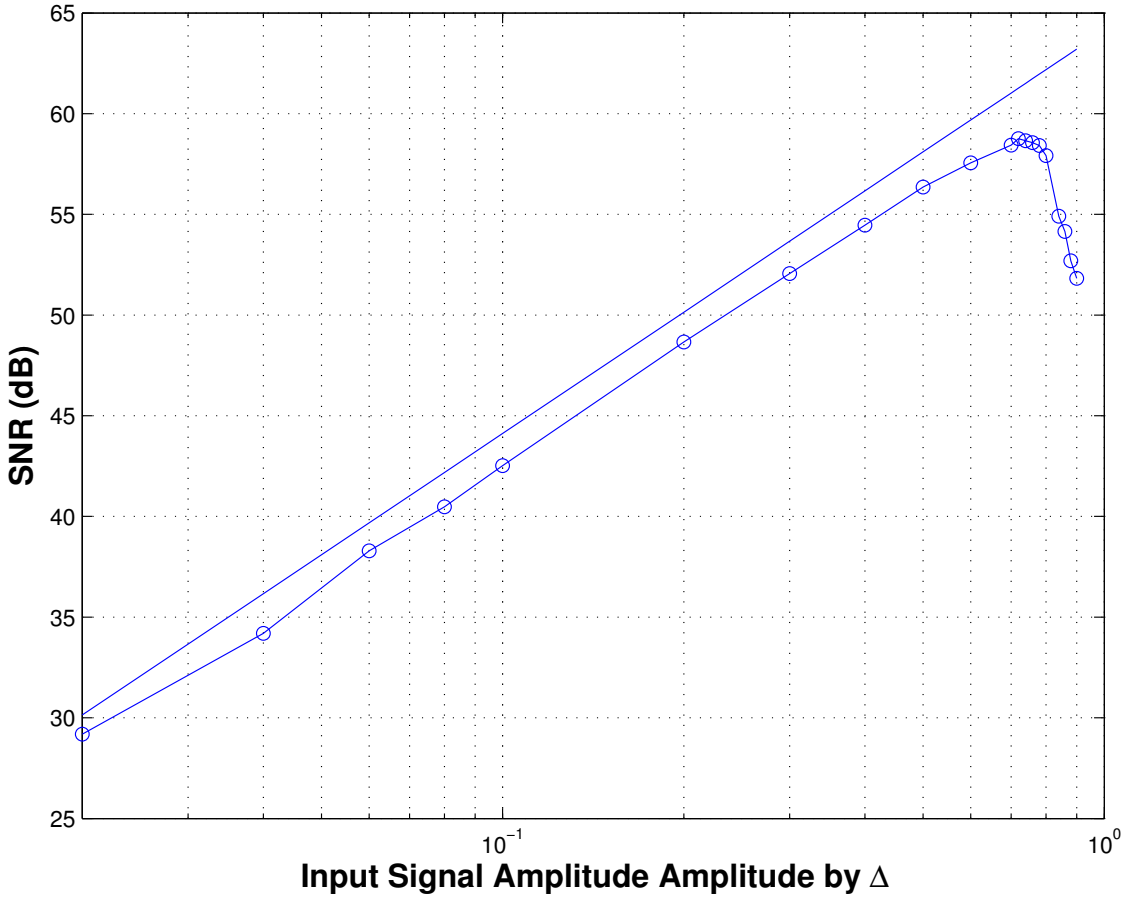


Figure 3.17: SNR versus input signal level of the second-order high-pass ΔΣ modulator.

Considering once again the schema block in Figure 3.13, the operation of the chopper stabilized modulator using the high-pass modulator is equivalent to that of the low-pass modulator. A sinusoid signal of amplitude $\Delta/2$ is applied to the input of the second-order low-pass ΔΣ modulator and the undecimated spectrum of the output is plotted in Figure 3.18(a). The same sinusoid signal is applied to the chopper to transform it to high frequency, and then goes through the high-pass ΔΣ modulator. The output of the high-pass modulator, a high frequency digital signal,

is then transformed to low frequency. The undecimated spectrum of the final signal obtained is plotted in Figure 3.18(b). The low frequency noise degrades significantly the low-pass modulator performance as shown in figure 3.18(a). But this problem disappears completely in the high-pass case as shown in Figure 3.18(b).

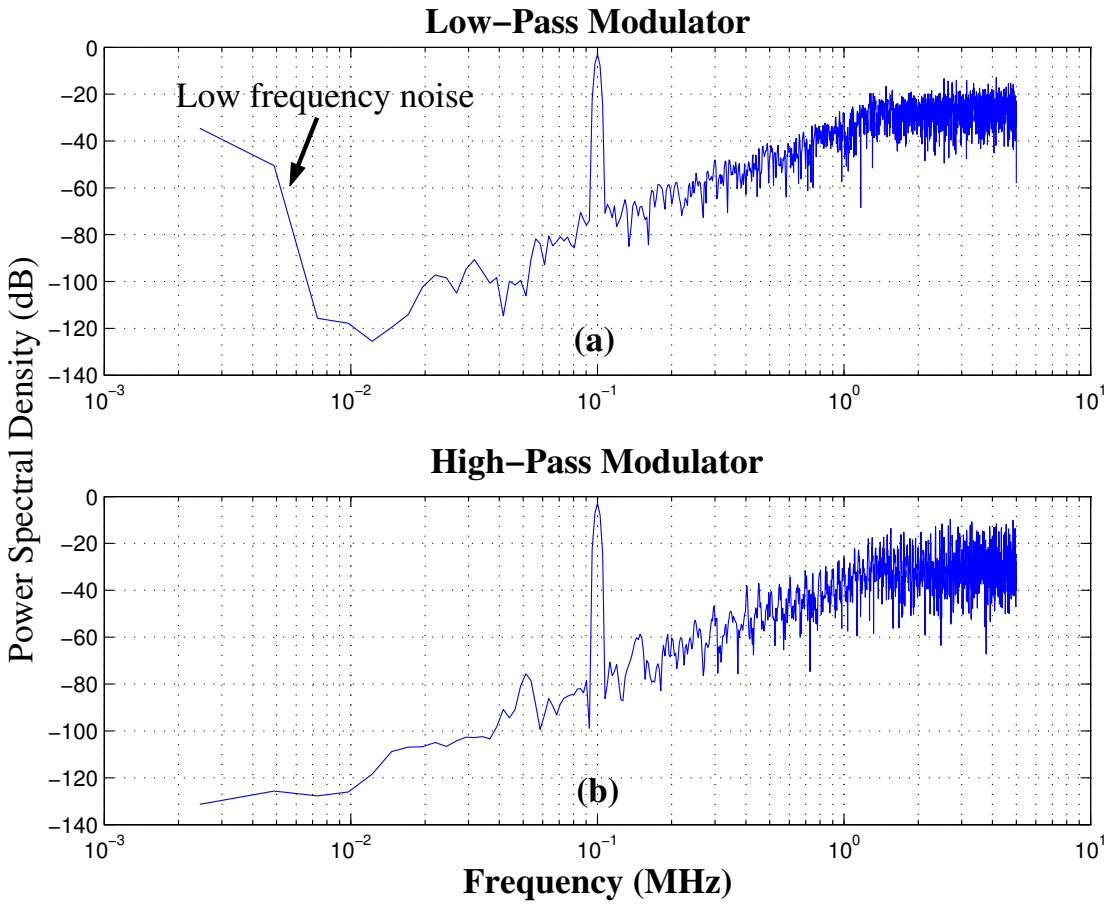


Figure 3.18: Output spectrum of the low-pass $\Delta\Sigma$ modulator (a) and output spectrum of the chopper stabilized $\Delta\Sigma$ modulator.

3.6 Switched-Capacitor Basis Block Implementation

In general, most integrated circuit implementation of $\Delta\Sigma$ converters use SC circuits because of following reasons :

- Easy to simulate;

- Compatible with VLSI CMOS process (extra poly layer desirable to make small-area linear caps);
- Insensitive to clock jitter as long as full settling occurs;
- Insensitive to exact shape of op-amp settling waveform as long as full settling occurs;
- Pole-zero locations are set by capacitor ratio, which are highly accurate.

In this section, we study an implementation in SC technique of the basis block building the high-pass modulator whose z-transfer function is given by $\frac{z^{-1}}{1+z^{-1}}$. From now on in this report, this block is called "high-pass filter".

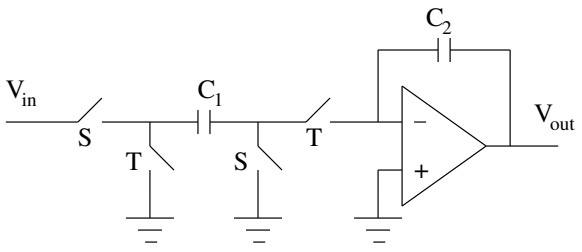


Figure 3.19: Parasitic-insensitive non-inverting SC integrator.

Figure 3.19 presents the parasitic-insensitive SC integrator whose ideal transfer function is given by

$$H(z) = \frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}. \tag{3.35}$$

The high-pass filter, the basis building component of the high-pass $\Delta\Sigma$ modulator, can be implemented as described in Figure 3.20. This implementation is based on the introduction of an extra feedback loop around the integrator, such that the desired transfer function for the high-pass filter is realized. Sign change in the extra feedback loop is obtained thanks to fully differential implementation. To simplify the analysis, only non-differential circuit is presented in Figure 3.20.

On the sampling phase, a charge proportional to V_{in} is stored on C_1 and a charge proportional to V_{out} is stored across C_3. On the subsequent charge redistribution phase, charge is transferred from C_1 to C_2 and C_3 to C_2. Because the capacitor C_3 is cross-coupled around the op-amp, the charge transferred from C_3 effectively undergoes an inversion during the charge redistribution phase. The ideal transfer

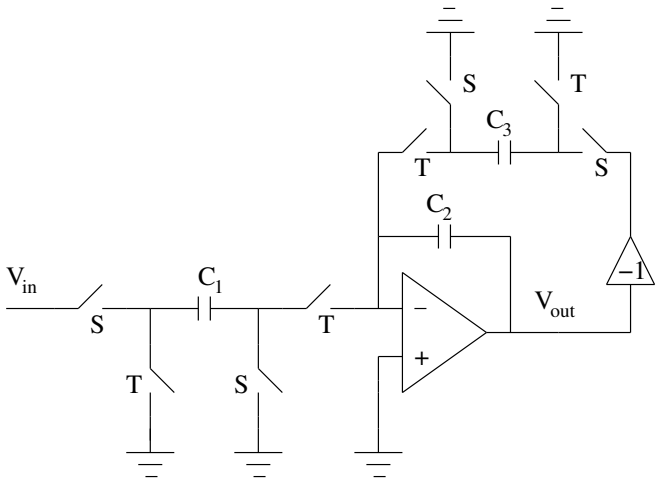


Figure 3.20: SC implementation of the high-pass filter

function of the high-pass filter described in Figure 3.20 is given by

$$H_{hp}(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 + \dfrac{C_3 - C_2}{C_2} z^{-1}}. \tag{3.36}$$

When $C_3 = 2C_2$, the filter described in Figure 3.20 realizes the desired high-pass filter transfer function, $\dfrac{z^{-1}}{1 + z^{-1}}$.

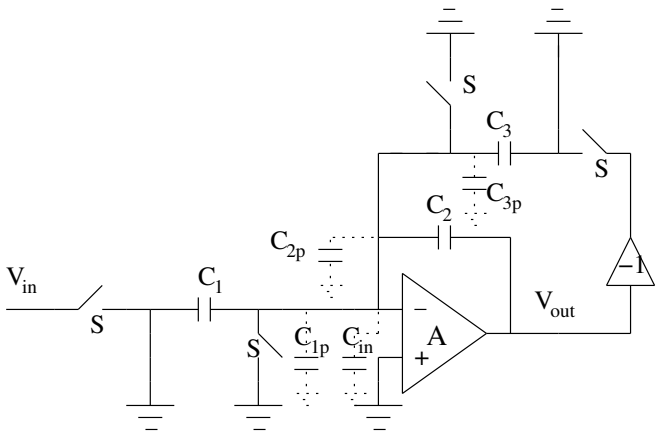


Figure 3.21: SC implementation of the high-pass filter with different parasitic capacitors.

In the presence of various parasitic capacitors and finite static gain of the op-amp as illustrated in Figure 3.21, the transfer function of the high-pass filter becomes

$$H_{hp}(z) = \frac{C_1}{C_2} \frac{(1-\alpha)z^{-1}}{1 + \beta z^{-1}}, \tag{3.37}$$

where the terms α and β, model perturbations in the gain and pole locations of the high-pass filter respectively, are given by

$$\alpha = \frac{1}{A}\frac{C_1 + C_2 + C_3 + C_{para}}{C_2 + \dfrac{C_1 + C_2 + C_3 + C_{para}}{A}} \simeq \frac{1}{A}\left(1 + \frac{C_1}{C_2} + \frac{C_3}{C_2} + \frac{C_{para}}{C_2}\right), \tag{3.38}$$

$$\beta = \frac{\dfrac{C_3 - C_2}{C_2} - \dfrac{C_2 + C_{para}}{AC_2}}{1 + \dfrac{C_1 + C_2 + C_3 + C_{para}}{AC_2}}, \tag{3.39}$$

where C_{para} represents not only parasitic capacitance at the input of the op-amp but also the various parasitic capacitors due to switches connected to the negative input of the op-amp and parasitic capacitors of C_1, C_2 and C_3.

In the presence of the limited op-amp bandwidth, the SC high-pass filter of Figure 3.20 suffers from incomplete settling. If the high-pass filter is assumed to settle linearly with a single-pole response, incomplete settling manifests itself only as an gain error [88]. In this case, the transfer function of the high-pass filter described in Figure 3.20 is

$$H_{hp}(z) = \frac{C_1}{C_2}(1 - g)\frac{(1 - \alpha)z^{-1}}{1 + \beta z^{-1}}, \tag{3.40}$$

where gain error term g is

$$g = e^{-T_s/\tau}, \tag{3.41}$$

where T_s is the sampling period and τ is the closed-loop time constant of the high-pass filter which is approximately

$$\tau \approx \frac{1}{2\pi f_u}\frac{C_1 + C_2 + C_3 + C_{para}}{C_2}, \tag{3.42}$$

where f_u is the unity-gain frequency of the op-amp. As the sampling rate is increased, the available settling time τ decreases, and gain error in (3.41) would become increasingly large. It should be noted that, in practice, settling in SC circuits is rarely governed by a strictly linear, single pole response. Rather, the settling process usually includes a signal-dependent slewing component and is influenced by non-dominant poles and slew-rate of the op-amp [130, 131], as well as finite switch resistances in the SC network. But fortunately, like integrator gain error in low-pass modulator, the high-pass filter gain error in the high-pass modulator, does not degrade much the performance of the converter.

3.7 Modulator Stability

This section introduces the notions of stability, saturation, and the maximal level of specific input signal for $\Delta\Sigma$ modulators. They are different from those usually used in the case of linear circuit, in reason of particular structure of the $\Delta\Sigma$ modulator that contains a nonlinear stage which is the quantizer. The saturation of the modulator is defined by the exceeding (overstepping) of normal operation region of a building component of the system. For example, an electronic integrator presents a maximal output voltage. We will use the definition of S. Hein [132] and O. Macchi [133, 134] about the stability of nonlinear system. In this definition, the internal signals are assumed not to be bound by saturation.

The $\Delta\Sigma$ modulator is stable for a input signal family F_λ whose amplitude is inferior or equal to λ. It concerns bounded-input bounded-output stability. The $\Delta\Sigma$ modulator is considered completely unstable if it is unstable for zero signal family (F_0). In the case of ideal modulator, not considering saturation, the maximal input signal level is the maximal input signal amplitude for which the modulator is always stable. In the other case, where internal signals are bound by saturation, the maximal input signal level is the maximal input signal amplitude for which all internal signals always stay inferior to the threshold of saturation. However, the maximal input signal level of $\Delta\Sigma$ modulator depends on the input signal form. But in the case of mono-bit modulator, the maximal input signal level is approximatively the maximal value of feedback coefficient, i.e. the unity in the relative value.

The $z \rightarrow -z$ transformation is a particularly attractive one since it does not affect the dynamics of the prototype. As a result, the high-pass $\Delta\Sigma$ modulator is stable if and only if the corresponding low-pass $\Delta\Sigma$ modulator is stable and the SNR curves of the modulators are identical. This property can be illustrated more in detail as follows :

While the quantizer is uniform and ideal, i.e. without limitation of output signal level, the error due to quantizer is called granular noise. We can demonstrate that the granular noise does not induce the instability problem. In the case of real quantizer, it can be split up into an ideal quantizer following a clipping as shown in Figure 3.22.

When the input of quantizer exceeds its saturation threshold, the error is called slope overload noise. And only the slope overload noise intervenes in the stability

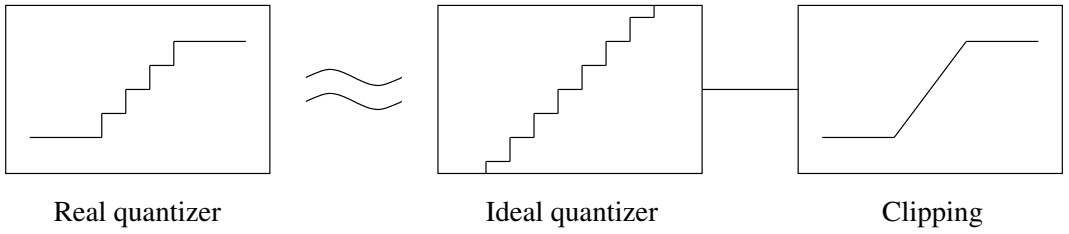


Figure 3.22: Real quantizer model

problem of the $\Delta\Sigma$ modulator. In a particular case where the quantizer is just a comparator, the classical method to study the modulator stability is the introduction of quantizer gain depending on the average signal level at its input. Then output of the comparator is given by

$$Y(z) = \eta V(z) + E(z), \tag{3.43}$$

where $V(z)$ and $E(z)$ represent the z-transforms of the input of the quantizer and quantization error. This model, utilized by R. T. Baird [135], is based on the theorem of Kalman on the nonlinear system [136]. The amplifier gain, η, is adjusted in such a way that the maximal input signal multiplied by this gain is about 2. The quantization noise transfer function, $N(z)$, becomes

$$N(\eta, z) = \frac{1}{1 + \eta A(z)}, \tag{3.44}$$

where $A(z)$ is the transfer function of the filter in the forward path of the modulator. The ideal quantizer is obtained when $\eta = 1$, $N(z)$ finds its expression indicated in (3.5).

The modulator is unstable if for every positive value of η, the module of poles of function $N(\eta, z)$ is superior or equal to 1, as shown in Figure 3.23(a). The modulator is completely stable if for every positive value of η, the module of poles of function $N(\eta, z)$ is inferior or equal to 1, as shown in Figure 3.23(b).

In the case of high-pass $\Delta\Sigma$ modulator, its noise transfer function is obtained from the noise transfer function of low-pass $\Delta\Sigma$ modulator corresponding by applying the transformation $z \rightarrow -z$. Note $N_{hp}(\eta, z)$ the noise transfer function of high-pass $\Delta\Sigma$ modulator and $N(\eta, z)$ that of low-pass $\Delta\Sigma$ modulator corresponding, we have

$$N_{hp}(\eta, z) = N(\eta, -z). \tag{3.45}$$

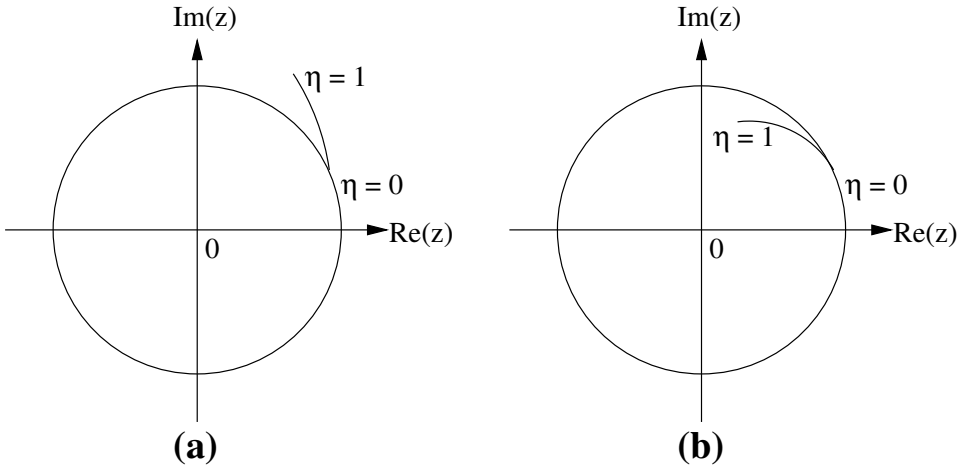


Figure 3.23: Locations of poles of the noise transfer function in the z-plane. (a): stable modulator ; (b): unstable modulator.

Therefore, if z_0 is a pole of $N(\eta, z)$, then $-z_0$ will be a pole of $N_{hp}(\eta, z)$ and vice versa. It implies that if for every positive values of η, the module of every poles of function $N(\eta, z)$ is inferior or equal to 1, then the module of every poles of function $N_{hp}(\eta, z)$ is also inferior or equal to 1, and vice versa. In other words, the high-pass modulator is stable if and only if the corresponding low-pass modulator is stable.

However, it is possible to excite the modulator into an unstable state that is characterized by large oscillations in internal states and a poor inband SNR that is not commensurate with that predicted by linear analysis. The potential for the onset of unstability is related to the initial conditions in the modulator as well as the magnitude of the error resulting from circuit nonidealities such as capacitor mismatch.

In reality, with the high-pass filter implementation as shown in Figure 3.20, there is an error on the high-pass filter pole β as shown in (3.39). Furthermore, the high-pass filter pole can be greater than 1. In this case, the high-pass filter is unstable that might drive the high-pass modulator unstable. The high-pass filter pole, β, is a critical parameter because it determines high-pass filter stability. It has to be inferior to 1 so that the high-pass filter is stable. Ideally, it is equal to 1. However in the presence of various parasitic capacitors, capacitors at the input of the op-amp and in particular capacitor mismatch, β may be greater than 1. In this case, the pole of the high-pass filter will lie outside of the unit circle, $|z| = 1$, which means that the filter is inherently unstable. Depending on the severity of the

high-pass filter pole error and the magnitude of the initial state and overload input that the modulator is subjected to, unstability may be introduced in the modulator that persists after the input to the modulator has been removed. This unstability is characterized by internal states that continues growing without bound, or that clips at internal limits, even when there is no input to the modulator. But it is important to note that the unstability of the high-pass filter does not immediately drive the high-pass modulator unstable when β is close enough to its ideal value, 1. It is then necessary to determine threshold values of β so that the high-pass $\Delta\Sigma$ modulator always stays stable. This threshold dependent on the modulator used, can be obtained by simulations or can be predicted. This is the goal of the following analysis.

From equation 3.39, we note that

$$\beta \leq \frac{C_3 - C_2}{C_2} - \frac{C_2 + C_{in}}{AC_2} \leq \frac{C_3 - C_2}{C_2} = \frac{C_3}{C_2} - 1. \tag{3.46}$$

Ideally, we have $C_3 = 2C_2$, and $\beta = 1$. However, as mentioned above, β may be lightly superior to 1. Relation (3.46) indicates that if β is superior to 1, the error committed in β is inferior to the maximal error on capacitor ratio, which is the main source implying modulator unstability.

The analysis based on a linear gain model of the quantizer [137, 138], initially established for low-pass modulator, can be used to analyze the stability and especially the internal signal bounds of the high-pass modulator. As in the low-pass case, the limitation of this analysis is only for the noiseless sinusoidal input and the internal signal bounds obtained are not precise. The analysis based on the limit cycles phenomenon [139] is capable to find out the analytical maximal internal signals levels of the second-order modulator. However, the predictions are too severe and then pessimistic. The analysis based on state space, initially analytical, are focused on noiseless constant input [140, 141, 142]. This idea is extended to noisy constant input by using convex invariant sets algorithm [143, 144, 145]. It is possible to extend this algorithm to noisy sinusoidal input to predict the modulator dynamics. Therefore, many input signal families can be studied for the modulator stability problem. The idea is to discretize the state space and seek for a convex invariant set. The drawback of this method is that the precision of the prediction depends on the discretisation level. Therefore, the execution speed of the algorithm, to have a good prediction, is lower than that of simulation.

The determination of the pole error bound ensuring the stability of the high-pass

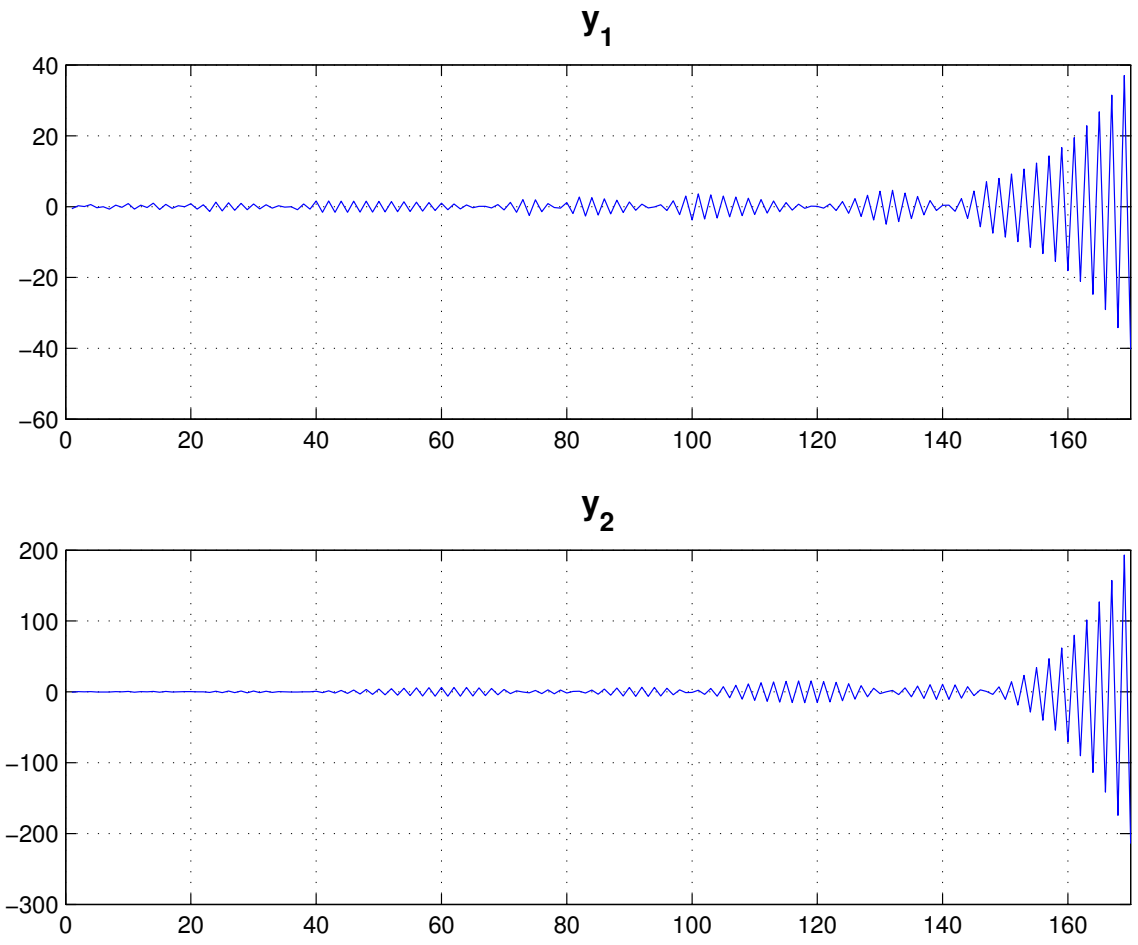


Figure 3.24: Divergence of internal states when the modulator is unstable. y_1 : output of the first high-pass filter, y_2 : output of the second high-pass filter.

modulator can be made by simulation. If the modulator is unstable, its internal states have very large oscillation and diverge very quickly. Let's note y_1 and y_2 the output of the first and second high-pass filter of the modulator in Figure 3.15. The rapid divergence of these internal states indicates the unstability of the modulator. Without considering the filter saturation, only few hundred points are enough to observe a very big divergence and rapid oscillation as shown in Figure 3.24. In the other case, the saturation is rapidly observed. Therefore, quick simulation can determine the threshold value of β ensuring the stability of the modulator. Simulations show that the stability of the high-pass modulator depends on the high-pass filter gain error, input signal and high-pass filter pole error. However, the influence of the high-pass filter gain errors on the stability of the modulator is negligible and the first high-pass filter pole is more critical than the second high-pass filter pole. Assume that the two high-pass filters building the second-order high-pass modulator are identical, their poles are naturally considered equal to each other.

Assume that the corresponding low frequency signal of the input signal, i. e. the signal that forms the high frequency signal through the transformation $z \rightarrow -z$, can be written as

$$x(t) = A\,sin(2\pi f_{in} t) + C_{dc} + C_{noise}, \tag{3.47}$$

where A, C_{dc}, and C_{noise} are the magnitude of the sinusoidal component, dc component and noise component of the signal $x(t)$, respectively. Thus, five input signal families can be considered : constant signal, noise signal, noisy constant signal, sinusoidal signal and noisy sinusoidal signal. The noise component is considered as white noise with mean value 0 and standard derivation σ. Let's denote $\hat{p}$ the threshold pole assuring the stability of the modulator for a input signal family. Figure 3.25 shows simulation results. The values of A, C_{dc} and σ are relative to the quantization step size, Δ. During the simulations, the frequency of the input signal, in the case where the input has a sinusoidal component, is 15 KHz, and the sampling frequency is 10 MHz. When noise is introduced into the input signal, a Monte Carlos analysis is made with 1024 runs per parameter. A run is called positive if the internal states of the modulator are all bounded. The threshold determining the stability of the modulator is 95% positive responses. Figure 3.25 shows the pole threshold assuring the stability of the high-pass modulator as a function of the amplitude of the sinusoidal component, the dc component and the noise standard derivation. This figure consists of six parts, each of which shows plots of the pole threshold versus dc component. For each noise standard derivation (0.01, 0.05, 0.1, 0.15 and 0.2), nine

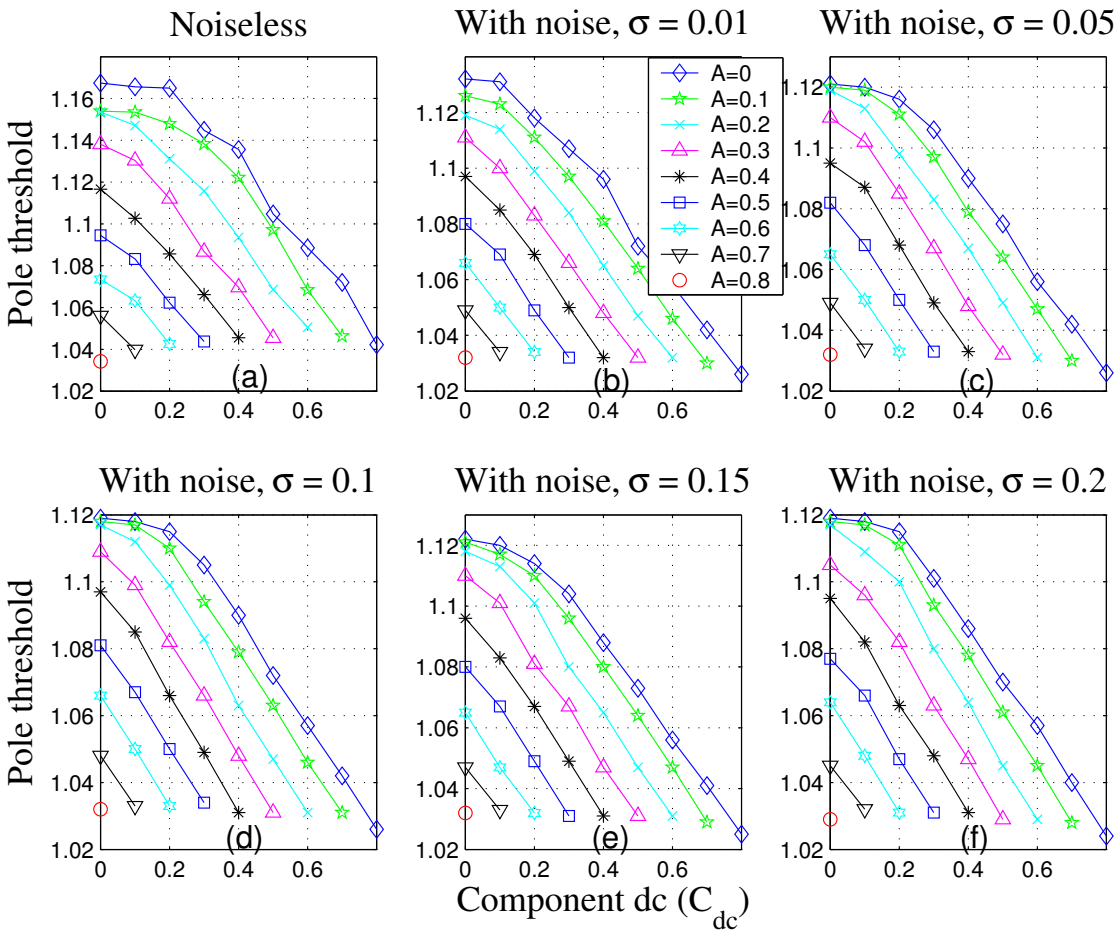


Figure 3.25: Threshold of the pole in the high-pass filter assuring the stability of the high-pass $\Delta\Sigma$ modulator.

curves are shown; from bottom to top the curves correspond to $A = 0, 0.1, \cdots, 0.8$, respectively. While nil signal is applied to the modulator, the threshold high-pass filter pole error must be smaller than 0.17, equivalently to 17% error, to assure the stability of the modulator. When a 0.8 dc constant is applied to the modulator, the threshold of the high-pass filter pole error is much more restricted, just only 0.034, or 3.4% error as shown in Figure 3.25(a). If the input signal is a noisy signal whose noise standard derivation is 0.01, the threshold goes down to 2.8% as shown in Figure 3.25(b). Increasing the noise standard derivation reduces the pole threshold. When the noise standard derivation is 0.2 which is excessively high in the oversampling system, the pole threshold is 1.024 or equivalently 2.4% error on the high-pass filter pole.

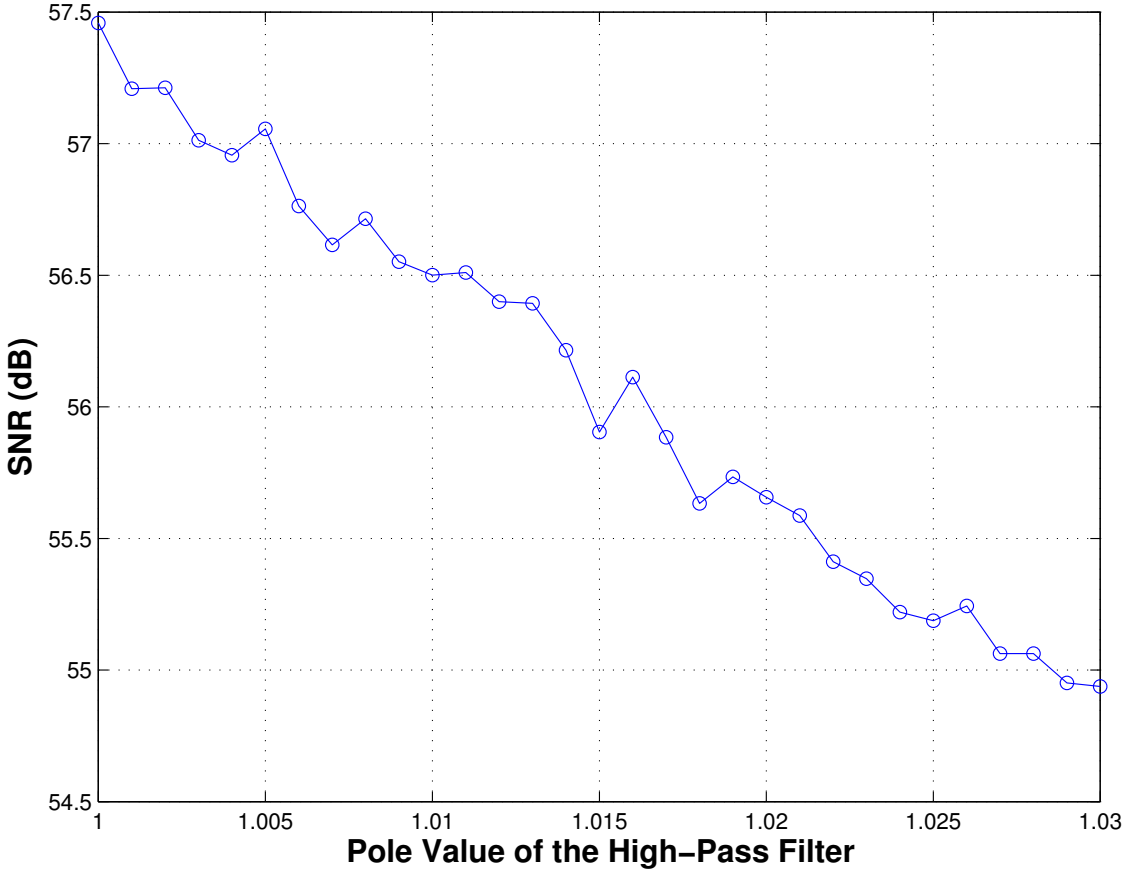


Figure 3.26: Signal-to-noise ratio of the second-order high-pass $\Delta\Sigma$ modulator versus the pole of the high-pass filter.

Figure 3.26 shows the SNR of the modulator versus the pole of high-pass filter. The sampling frequency is 10 MHz with thirty two times oversampling. The equiv-

alent low frequency signal of the input signal is a sinusoid whose amplitude is 0.7 relative to one-half of quantization full-scale and the frequency varying from 10KHz to 100KHz. The average of SNR obtained is plotted in Figure 3.26. The pole error in the high-pass filter introduces the inband noise, and degrades the modulator performance. But as shown in the Figure 3.26, when pole error is under 1%, the modulator performance degradation is about only 1 dB. Therefore, if the threshold of 1% error on the pole in the high-pass filter is satisfied, then not only the stability of the modulator is ensured, but also the degradation of the high-pass $\Delta\Sigma$ modulator perofrmance is negligible. From (3.46), this condition requires capacitor matching on the order of 1%.

3.8 Conclusion

The high-pass $\Delta\Sigma$ modulator is based exactly on the same principle as the low-pass $\Delta\Sigma$ modulator, i.e. the quantization noise is shaped away from the signal band by a loop filter. The only difference is the position of the signal band, now located at one-half of the sampling frequency, instead of a passband at dc for the low-pass modulator. The high-pass modulator is realized by applying the transformation $z \rightarrow -z$ to a low-pass modulator.

The architecture and the principle of high-pass $\Delta\Sigma$ modulator have been presented. Ideal performance of a high-pass $\Delta\Sigma$ modulator is equivalent to that of the corresponding low-pass modulator. For a L^{th}-order high-pass modulator, a $L + 1/2$-bit of resolution is gained for every doubling of OSR. An implementation in SC technique of the high-pass filter, the basis block building the high-pass modulator, has been presented based on the introduction of an extra feedback loop around the integrator. The stability of the high-pass modulator has been analyzed. Simulations indicate that the modulator remains stable for a wide range of overload conditions, provided that the pole error in the high-pass filter remains bounded by approximately 2.4%. If this pole error is smaller than 1%, then the degradation of the high-pass $\Delta\Sigma$ modulator is negligible. This condition requires capacitor matching on the order of 1%.

The theoretical analysis and simulation results show that this kind of modulator eliminates completely the low frequency noise. Therefore, it is very useful and attractive for applications requiring high resolution, high linearity and wide band-

width. However, the analysis of the nonideality effect on the performance of the high-pass modulator is necessary to establish its practical limitations.

Chapter 4

Time-Interleaved $\Delta\Sigma$ Converter

4.1 Introduction

Conventional $\Delta\Sigma$ ADCs are widely used in low bandwidth applications such as the high fidelity audio processing, because they offer high precision conversion and are amenable to implementation using VLSI processes optimized for digital circuitry. Oversampling, in conjunction with quantization noise shaping and decimation filtering, results in the effect of high precision ADC, despite the use of coarse ADC and DAC without high component matching accuracy, as explained in the Chapter 3. However, their oversampling requirement has so far prevented their widespread application to higher bandwidth application.

Typically, to achieve a given precision, the input sample rate of a $\Delta\Sigma$ ADC must be significantly higher than the conversion rate. Therefore, the maximum analog-to-digital conversion rate is usually much lower than the maximum clock rate for a given circuit technology. For conversion rates below a few MHz, the oversampling requirement has generally not been a significant problem. However, in higher bandwidth applications such as video processing and digital radio the oversampling requirement has been prohibitive [1, 88, 89, 90]. The throughput rate of digital signal processing systems operating on analog inputs is often limited by the speed of the ADC interface. Most approaches to reduce the oversampling requirement have involved either increasing the order of the $\Delta\Sigma$ modulator so as to improve its noise shaping capability, increasing the number of coarse ADC bits, or a combination thereof. Unfortunately, increasing the order of the $\Delta\Sigma$ modulator

without increasing the number of coarse ADC bits generally results in systems that are only marginally stable and have reduced stable input range [124, 126] or that are sensitive to component matching errors [118, 146, 147]. Similarly, increasing the number of coarse ADC bits generally gives rise to systems that are highly sensitive to DAC errors in the ΔΣ modulator feedback paths.

Recently, several approaches using parallelism have been studied in order to increase the bandwidth of ΔΣ ADCs [2], in particular the time-interleaved ΔΣ ADCs [4], and the ΠΔΣ ADCs [3]. It has been shown that there is only a small difference between the performance of the ΠΔΣ ADC and the time-interleaved ΔΣ ADC [148]. The time-interleaved ΔΣ ADC is more efficient in terms of area than ΠΔΣ ADC [149]. However, its performance is very sensitive to the low frequency noises, such as DC offset noise, flicker noise and clock feedthrough noise, and channel gain mismatch.

This chapter presents a new time-interleaved ΔΣ ADC architecture which is immune to low frequency noise and thus makes it easier for the channel gain equalization to minimize the effect of channel gain mismatch. The chapter is divided into sept sections including this introduction. The next section presents the conventional time-interleaved ΔΣ architecture. The third section analyzes the theoretical performance of this architecture. Section 4.4 demonstrates its sensitivity to nonideal circuit behavior. Section 4.5 introduces the new architecture, the time-interleaved high-pass ΔΣ ADC. Section 4.6 presents an adaptive channel gain equalization technique. Finally, Section 4.7 concludes this chapter.

4.2 Architecture

A simple structure of the time-interleaved ΔΣ ADC architecture is shown in Figure 4.1. It consists of M parallel channels of low-pass ΔΣ modulators and low-pass channel filters that all operate on the input signal, $x[n]$. Although the input to each modulator is sampled at $1/M$ the clock rate, each modulator still operates at the full rate. During the time when the input signal is not applied to the modulator, the input is connected to the ground. The input signal is multiplexed, low-pass ΔΣ modulated, low-pass filtered, and demultiplexed to produce the output signal, $y[n]$. As in conventional ΔΣ ADC, various ΔΣ modulators can be used in this architecture, but the choice of the modulator is generally determined by the specifics

of the application and the constraints of the circuit technology.

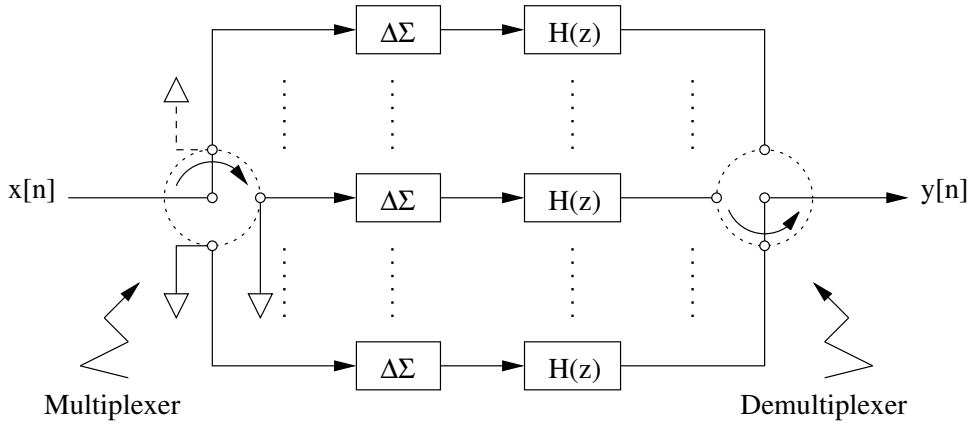


Figure 4.1: Architecture of time-interleaved $\Delta\Sigma$ converter.

The digital filters, $H(z)$, depend on the type of $\Delta\Sigma$ modulator used. The constraints on the channel filters for the perfect reconstruction of the input signal is that every M^{th} filter tap coefficient should be zero, except at the center tap. The remaining filter coefficients are chosen to minimize the quantization noise introduced by the $\Delta\Sigma$ modulators. In theory, the performance of the time-interleaved $\Delta\Sigma$ ADC is equivalent to the performance of a single channel $\Delta\Sigma$ ADC with the time oversampling rate multiplied by M.

The multiplexer and demultiplexer are considered as its equivalent multiplication schemes. They are effectively equivalent to the multiplication of their i^{th} channel input sequence by a specific periodic sequence formed from the i^{th} column vector of the unitary matrix of dimension-M, as illustrated in Figure 4.2. In this example, there is $M-1$ delays of the demultiplexer relative to the multiplexer. The delays of the demultiplexer from the multiplexer being an architecture parameter vary from zero to $M-1$.

To show how the time-interleaved $\Delta\Sigma$ converter works, we consider as an example, a four channels time-interleaved $\Delta\Sigma$ converter with FIR filters of length-7. For the sake of simplicity and without loss of generality, we suppose that the $\Delta\Sigma$ modulators have $S(z) = 1$. The overall useful signal can therefore be calculated by considering the time-interleaved $\Delta\Sigma$ converter without the $\Delta\Sigma$ modulators. Figure 4.3 shows the four channels time-interleaved $\Delta\Sigma$ converter at time $n = n_0$ with the $\Delta\Sigma$ modulators omitted. The multiplexer has three delays relative to the demultiplexer. As shown in Figure 4.3, the digital output, $y[n]$, depends on the channel

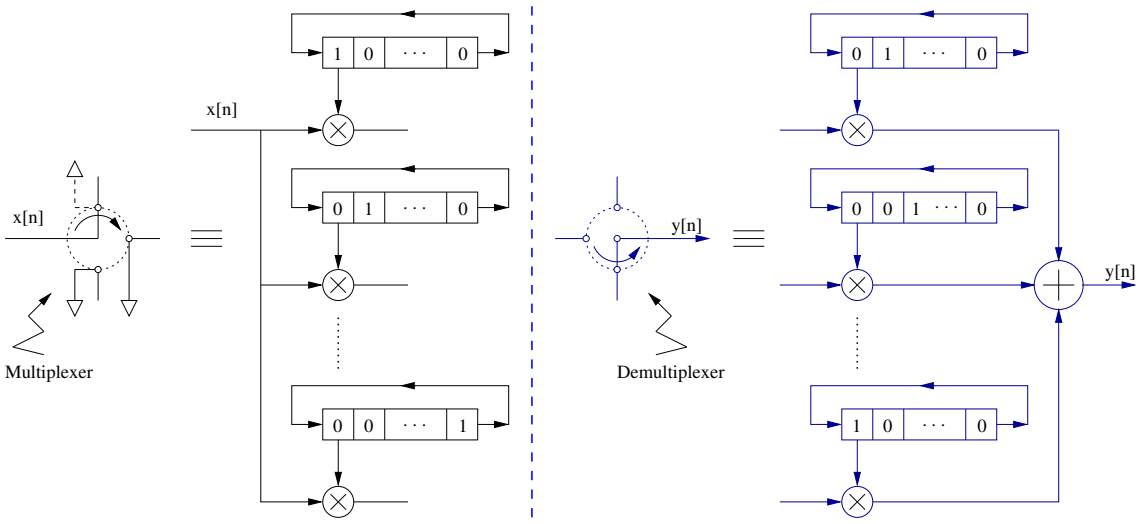


Figure 4.2: Equivalent multiplication models of the multiplexer and demultiplexer with $M-1$ delays of the demultiplexer relative to the multiplexer in the time-interleaved $\Delta\Sigma$ converter.

connected to the demultiplexer. At time $n = n_0$, the digital output is just the output of the fourth channel, so $y[n_0] = h[3]x[n_0 - 3]$.

Now consider the system of Figure 4.3 at the next time instant, $n = n_0 + 1$. The digital output is just the output of the first channel, so $y[n_0 + 1] = h[3]x[n_0 + 1 - 3]$. Continuing in this reasoning, it is evident that $y[n] = h[3]x[n - 3]$ for all n, so the digital output is just a delayed and scaled version of the input sequence. A particularly important feature of this system is that the overall output only depends on the center coefficient of the channel filter, $H(z)$, namely $h(3)$.

The overall quantization error, on the other hand, depends on all the coefficients of $H(z)$. This is because each $\Delta\Sigma$ modulator quantization error is introduced just prior to the channel filter, $H(z)$, so the overall quantization error is just one of the M $\Delta\Sigma$ modulator quantization errors after it has been filtered by $H(z)$. Since the $\Delta\Sigma$ modulator quantization errors were not multiplexed prior to filtering, the effect of the filtering has not the same property as in the case of the input signal. If the $\Delta\Sigma$ modulator quantization errors have most of their power at high frequencies, the use of low-pass filter $H(z)$ results in a significant attenuation of the quantization error contributed by each channel. And the power of the overall quantization error may be also attenuated.

An obvious limitation of the time-interleaved $\Delta\Sigma$ converter of the example pre-

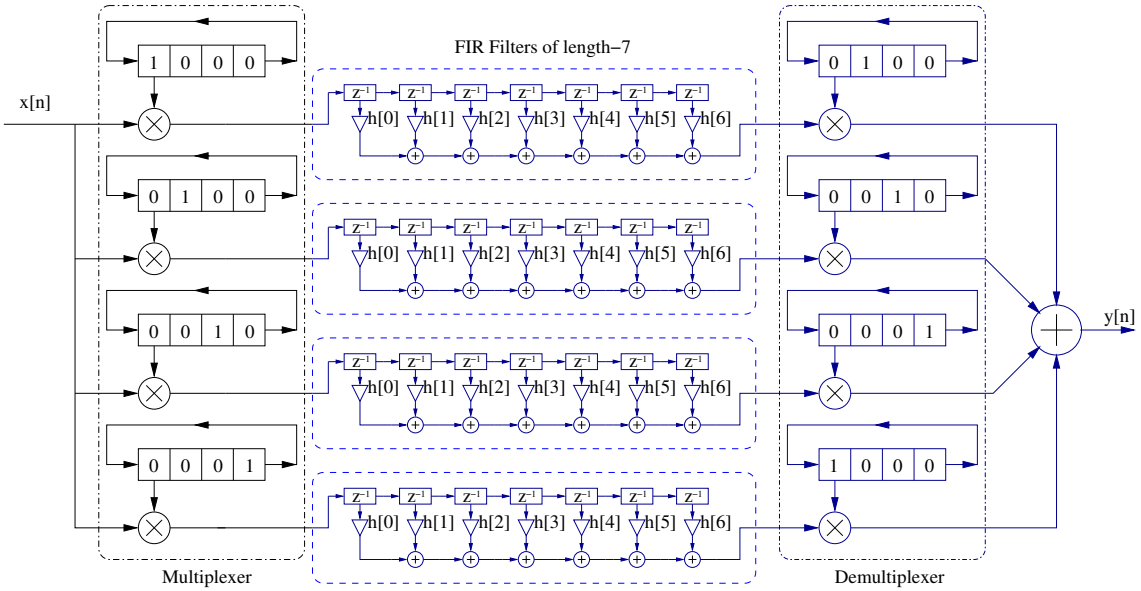


Figure 4.3: An example of the processing performed by a four channels time-interleaved $\Delta\Sigma$ converter in the absence of quantization error with three delays of the demultiplexer relative to the multiplexer.

sented in Figure 4.3 is that the filters have only length-7. Indeed, if longer filters were used, it would be possible to better attenuate the quantization error from each channel, although the overall useful signal would not be simply a delayed version of the input sequence. For instance, if length-11 filters were used, an extension of the argument above indicates that the overall useful signal would have the form $y[n] = h[3]x[n-3] + h[7]x[n-7]$. In this case, the time-interleaved $\Delta\Sigma$ converter would act as a linear time invariant (LTI) filter with transfer function $z^{-3}(h[3]+h[7]z^{-4})$ with respect to the input sequence. This filtering can be avoided, i.e. the overall useful signal is still a delayed and scaled version of the input sequence, by constraining $H(z)$ such that $h[4] \neq 0$ and $h[7] = 0$ or vice versa. The nine remaining coefficients can be chosen to minimize the power of the overall quantization error. Of course, this approach is not limited to length-11 filters. It can be generalized to filters of any length. In the next sections, we will present a method of determining the constrained filter coefficients and optimally choosing the unconstrained coefficients for any filter length. The minimum overall quantization error power obtainable as a function of filter length for various $\Delta\Sigma$ modulators will also be calculated.

4.3 Theoretical Performance

In general, the digital output signal of a low-pass ΔΣ modulator is a coarsely quantized sequence, i.e. rarely more than a few bits, that in the absence of circuit errors, can be considered as the sum of an useful signal and a quantization error. Therefore, as shown in Figure 4.4, a low-pass ΔΣ modulator is ideally equivalent to a LTI filter, shown as $S(z)$, plus an additive quantization error source, denoted as $e_{q_i}(z)$. The useful signal is given by $x_i[n] * s[n]$, where $s[n]$ is the impulse response of signal transfer function S(z).

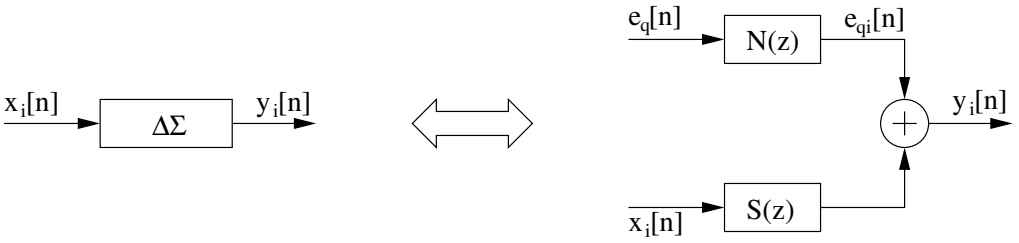


Figure 4.4: Linear model of ΔΣ modulator.

With the model presented in Figure 4.4 of low-pass ΔΣ modulator, the time-interleaved ΔΣ converter can be modelled as a linear system to which the M ΔΣ modulator quantization errors are added as shown in Figure 4.5

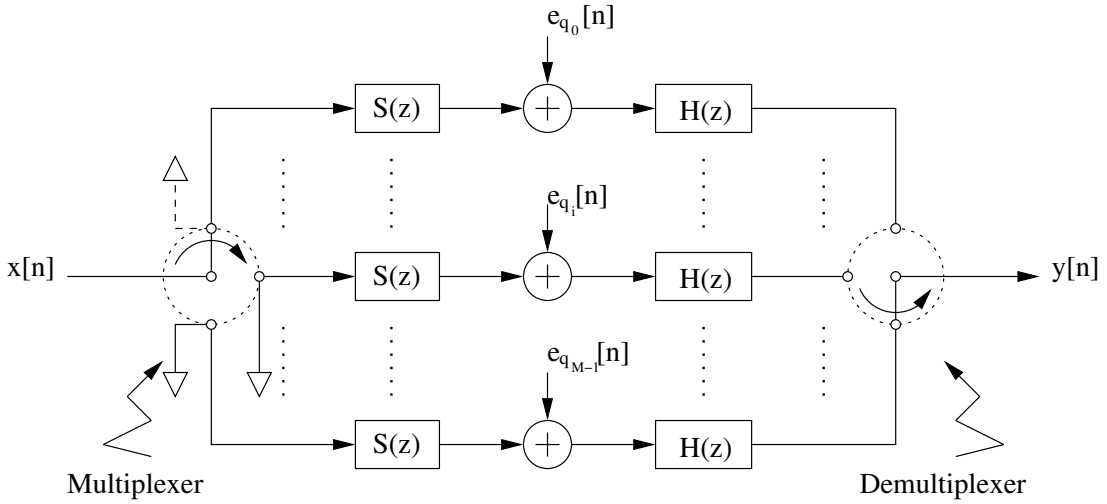


Figure 4.5: The time-interleaved ΔΣ ADC quantization model.

Consequently, the digital output signal is a digital sequence that is the sum of

an overall useful signal and an overall quantization error. That is

$$y[n] = w[n] + e[n], \tag{4.1}$$

where $w[n]$ denotes the overall useful signal and $e[n]$, the overall quantization error. By superposition, the overall useful signal can be calculated by considering the quantization error of each channel $\Delta\Sigma$ modulator to be zero. In the same reasoning, the overall quantization error can be calculated by considering the input signal to be zero.

4.3.1 Overall Useful Signal

The overall useful signal is a linear time variant filtered version of the input sequence. By considering the i^{th} channel without quantization error, and let $q[n] = s[n] * h[n]$, the output signal can be given by

$$t_i[n] = \sum_{k=0}^{\infty} q[k]x[n-k]u_i[n-k]u_i[n+k_0], \tag{4.2}$$

where k_0 represents the delays of the demultiplexer relative to the multiplexer and $u_i[n]$ is a specific sequence depending on the number of channels, M, and channel number, i. This sequence represents the multiplexer and demultiplexer in the time-interleaved $\Delta\Sigma$ ADC architecture as indicated in Figure 4.2. The sequence $u_i[n]$ is defined by

$$u_i[n] = \begin{cases} 1 & \text{if } n-i \text{ is a multiple of } M \\ 0 & \text{otherwise} \end{cases}. \tag{4.3}$$

The overall useful signal is just the sum of M $t_i[n]$ sequences :

$$w[n] = \sum_{i=0}^{M-1} t_i[n] = \sum_{k=0}^{\infty} q[k]x[n-k] \sum_{i=0}^{M-1} u_i[n-k]u_i[n+k_0]. \tag{4.4}$$

From the definition of $u_i[n]$ given in equation (4.3), it follows that

$$\sum_{i=0}^{M-1} u_i[n-k]u_i[n+k_0] = C_M[k+k_0], \tag{4.5}$$

where

$$C_M[n] = \begin{cases} 1 & \text{if } n \text{ is a multiple of } M \\ 0 & \text{otherwise} \end{cases}. \tag{4.6}$$

So the overall useful signal from (4.4) becomes

$$w[n] = \sum_{k=0}^{\infty} q[k]x[n-k]C_M[k+k_0], \tag{4.7}$$

from which we have

$$w[n] = x[n] * h'[n], \tag{4.8}$$

where

$$h'[n] = C_M[n+k_0](s[n] * h[n]), \tag{4.9}$$

or, equivalently

$$W(z) = H'(z)X(z). \tag{4.10}$$

Then, general expression for $h'[n]$ as a function of the channel filter impulse response, $h[n]$, the $\Delta\Sigma$ modulator signal impulse response, $s[n]$, and the delays, k_0, in equation (4.9) can be simplified as follows:

Assume that the channel $\Delta\Sigma$ modulator is an ideal L^{th}-order modulator and the channel filter is a causal FIR filter of length-N, then we have $s[n] = \delta[n-L]$ and $h[n] = 0$ if $n < 0$ or $n \geq N$. Therefore, the equation (4.9) becomes

$$h'[n] = C_M[n+k_0]h[n-L] \tag{4.11}$$

By the definition of z-transform, it follows

$$H'(z) = \sum_{n=L}^{L+N-1} C_M[n+k_0]h[n-L]z^{-n}. \tag{4.12}$$

Replacing $C_M[n]$ from equation (4.6) in the last equation, results in

$$H'(z) = z^{-k_0} \sum_{i=n_0}^{n_1} h[iM - k_0 - L]z^{-iM}, \tag{4.13}$$

where

$$n_0 = \left\lceil \frac{L+k_0}{M} \right\rceil \quad \text{and} \quad n_1 = \left\lceil \frac{L+k_0+N-1}{M} \right\rceil. \tag{4.14}$$

Therefore, the overall useful signal, $w[n]$, depends on every M^{th} value of the channel filter impulse response, $h[n]$. In this sense, the effect of the filtering performed by $H(z)$ is at least partially negated. If $H(z)$ is restricted such that

$$h[n] = \begin{cases} 1 & \text{when } n = i_0\, M \ - k_0 - L \\ 0 & \text{when } n = i\, M \ - k_0 - L \ \text{ with } n_0 \leq i \neq i_0 \leq n_1 \end{cases}, \tag{4.15}$$

then it follows that $H'(z) = z^{-k_0 - i_0 M}$. In other words, we have

$$w[n] = x[n - k_0 - M\, i_0]. \tag{4.16}$$

The overall useful signal is just a delayed version of the input signal. So the effect of filtering performed by $H(z)$ is completely negated. The coefficients not specified by (4.15) have no effect on the overall useful signal, so they may be chosen to minimize the power of overall quantization error. This is the subject of the next subsection.

4.3.2 Overall Quantization Error

A meaningful measure of the ADC quantization error performance is the power of the overall quantization error which can be written as

$$P_e = \frac{1}{\pi} \int_{-\pi}^{\pi} S_{ee}\left(e^{j\omega}\right) d\omega, \tag{4.17}$$

where $S_{ee}(e^{j\omega})$ is the power spectral density of the overall quantization error, $e[n]$.

To evaluate the power of the overall quantization error, P_e, it is necessary to calculate the power spectral density of the overall quantization error, $S_{ee}(e^{j\omega})$. From Figure 4.4, it follows

$$e[n] = \sum_{i=0}^{M-1} u_i[n + k_0] e_i[n], \tag{4.18}$$

where $e_i[n] = e_{qi}[n] * h[n]$ is the quantization error contributed by the $i^{th}\Delta\Sigma$ modulator as measured at the output of channel filter, $H(z)$. The autocorrelation of $e[n]$ is defined as $R_{ee}[k] = E\left(e[n]e[n+k]\right)$. Substituting (4.18) into this definition and interchanging the expectation and the summation results in

$$R_{ee}[k] = \sum_{i=0}^{M-1} \sum_{j=0}^{M-1} u_i[n + k_0] u_j[n + k_0 + k] E\left(e_i[n] e_j[n+k]\right). \tag{4.19}$$

It can be shown that for many of the known $\Delta\Sigma$ modulators and most practical input sequences that do not overload the $\Delta\Sigma$ modulators, $e_i[n]$ and $e_j[n+k]$ are uncorrelated when $i \neq j$, and $R_{e_i e_i}$, the autocorrelation of $e_i[n]$, is independent of i. It follows that (4.19) reduces to

$$R_{ee}[k] = C_M[k] R_{e_i e_i}[k]. \tag{4.20}$$

Taking the Fourier transform of 4.20 results in

$$S_{ee}\left(e^{j\omega}\right) = \frac{1}{M} \sum_{k=0}^{M-1} S_{e_i e_i}\left(e^{j(\omega - 2\pi k/M)}\right), \tag{4.21}$$

where $S_{e_i e_i}\left(e^{j\omega}\right)$ is the power spectral density of $e_i[n]$.

The most common method of analyzing ΔΣ modulators involves modelling the coarse ADCs within the ΔΣ modulators as additive uniformly distributed white noise sources [1]. This method of analysis is widely used, and is a good method in terms of calculating average quantization error power. Applying the model gives

$$S_{e_i e_i}\left(e^{j\omega}\right) = \frac{\Delta^2}{12}\left|N\left(e^{j\omega}\right)H(e^{j\omega})\right|^2, \tag{4.22}$$

where $N(z)$ is the effective filter imposed on the white quantization noise by the ΔΣ modulator, and Δ is the quantization step size. Thus, the power spectral density of the overall quantization error can be written as

$$S_{ee}\left(e^{j\omega}\right) = \frac{\Delta^2}{12M}\sum_{k=0}^{M-1}\left|N\left(e^{j(\omega-2\pi k/M)}\right)H(e^{j(\omega-2\pi k/M)})\right|^2. \tag{4.23}$$

This expression in conjunction with (4.17) is used to calculate the power of the overall quantization error, P_e, as follows

$$P_e = \frac{1}{2\pi}\int_{-\pi}^{\pi}\frac{\Delta^2}{12M}\sum_{k=0}^{M-1}\left|N\left(e^{j(\omega-2\pi k/M)}\right)H(e^{j(\omega-2\pi k/M)})\right|^2 d\omega. \tag{4.24}$$

Since discrete time Fourier transforms are periodic-2π, this can be written as

$$P_e = \frac{\Delta^2}{24\pi}\int_{-\pi}^{\pi}\left|N\left(e^{j\omega}\right)H\left(e^{j\omega}\right)\right|^2 d\omega. \tag{4.25}$$

By Parseval's Theorem, this is equivalent to

$$P_e = \frac{\Delta^2}{12}\sum_{m=-\infty}^{\infty}\left[h[m]*n[m]\right]^2, \tag{4.26}$$

where $n[m]$ is the impulse response of ΔΣ modulator quantization error transfer function, $N(z)$. With some algebra, this becomes

$$P_e = \sum_{j=-\infty}^{\infty}h(j)\sum_{k=-\infty}^{\infty}R_{j,k}h[k], \tag{4.27}$$

where

$$R_{j,k} = \frac{\Delta^2}{12}\sum_{m=-\infty}^{\infty}n[m-j]n[m-k]. \tag{4.28}$$

Let

$$\mathbf{h} = \begin{bmatrix} h[0] \\ \vdots \\ h[N-1] \end{bmatrix} \text{ and } \mathbf{R} = \begin{bmatrix} R_{0,0} & \cdots & R_{0,N-1} \\ \vdots & & \vdots \\ R_{N-1,0} & \cdots & R_{N-1,N-1} \end{bmatrix}, \tag{4.29}$$

then more compact notation of the power of the overall quantization error is given by

$$P_e = \mathbf{h^t R h}. \tag{4.30}$$

From this expression, we can calculate the optimal channel filter for which the power of the overall quantization error is minimized. This is the subject of the next subsection.

4.3.3 Optimal Channel Filter

The reduction of the power of the overall quantization error, P_e, results in the improvement of the ADC precision. In this subsection, we look for a particular channel filter, $H(z)$, that minimizes the power of overall quantization error, P_e. If such a filter could be found, it will be called the optimal channel filter.

Conditions in (4.15) indicate that there is a particular element of $\mathbf{h}$, whose index is $(i_0\,M - k_0 - L)$, that is constrained to be 1. The index of this element is hereafter denoted as m_0. It follows that $m_0 = i_0\,M - k_0 - L$. Each element with an index shifted by multiple of M from m_0 is constrained to be zero. Each of these constrained indexes is referred to as a "constraint index".

We note that the vector formed by deleting the elements of $\mathbf{h}$ with constraint indexes and conditions in (4.15) completely define the impulse response of the channel filter, $H(z)$.

Let $\mathbf{R_1}$ be the submatrix formed by deleting the columns and rows of $\mathbf{R}$ with constraint indexes, let $\mathbf{b}$ be the vector formed from the $(m_0)^{th}$ column of $\mathbf{R}$, let $\mathbf{b_1}$ be the vector formed from $\mathbf{b}$ by deleting the elements with constraint indexes, and let $\mathbf{h_1}$ be the vector formed from $\mathbf{h}$ by deleting the elements with constraint indexes.

Let

$$\mathbf{a} = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix},$$

$\mathbf{a}$ has N elements and only its $(m_0)^{th}$ element is 1, so $\mathbf{Ra} = \mathbf{b}$. Let $\mathbf{x} = \mathbf{h}$ - $\mathbf{a}$, the power of overall quantization error becomes

$$P_e = (\mathbf{x} + \mathbf{a})^{\mathbf{t}}\mathbf{R}(\mathbf{x} + \mathbf{a}). \tag{4.31}$$

Developing this expression results in

$$P_e = \mathbf{x}^{\mathbf{t}}\mathbf{R}\mathbf{x} + 2\mathbf{b}^{\mathbf{t}}\mathbf{x} + R_{m_0,m_0}. \tag{4.32}$$

The elements of $\mathbf{x}$ whose indexes are not constraint indexes are equal to those of $\mathbf{h}$ and the element of $\mathbf{x}$ with constraint indexes are zero, so

$$P_e = \mathbf{h_1^t}\mathbf{R_1}\mathbf{h_1} + 2\mathbf{b_1^t}\mathbf{h_1} + R_{m_0,m_0}. \tag{4.33}$$

Because P_e is a quadratic function of $\mathbf{h_1}$, the minimum of the power of the overall quantization error, P_e, is reached when the multivariable derivative of P_e, $\nabla P_e = 0$. The value of $\mathbf{h_1}$ that minimizes P_e, is named $\mathbf{h_1^{opt}}$. From (4.33), it follows

$$\nabla P_e = 2\mathbf{R_1}\mathbf{h_1} + 2\mathbf{b_1}. \tag{4.34}$$

Therefore, if $\mathbf{R_1}$ is nonsingular, then

$$\mathbf{h_1^{opt}} = -\mathbf{R_1^{-1}}\mathbf{b_1}. \tag{4.35}$$

From $\mathbf{h_1^{opt}}$ in conjunction with the conditions in (4.15), the optimal channel filter impulse response $\mathbf{h}$ is completely obtained. The only remaining problem is to prove the nonsingularity of the matrix $\mathbf{R_1}$.

Since P_e is the power of the overall quantization error, it must be positive for any channel filter. Equivalently $\mathbf{h^t R h} > 0$ for any $\mathbf{h}$. Therefore, $\mathbf{R}$ is a positive definite matrix.

Let $\mathbf{d}$ be a column vector of length-N whose elements with constraint indexes are zero, and let $\mathbf{d_1}$ be the matrix formed from $\mathbf{d}$ by deleting the elements with constraint indexes, (4.15). Since $\mathbf{R}$ is positive definite, then

$$\mathbf{d^t R d} = \mathbf{d_1^t R_1 d_1} > \mathbf{0} \quad \text{for any } \mathbf{d_1}. \tag{4.36}$$

Therefore, $\mathbf{R_1}$ is also positive definite, so nonsingular. The nonsingularity of the matrix $\mathbf{R_1}$ is proven.

The optimal channel filter can be demonstrated as symmetric when the filter length is odd and m_0 is the center index of the optimal channel filter, $\mathbf{h_{opt}}$. Since $\mathbf{R}$

is symmetric Hermitian matrix, $\mathbf{R_1}$ is also symmetric Hermitian. The inverse matrix, $\mathbf{R_1^{-1}}$ of $\mathbf{R_1}$ is thus symmetric. Moreover, the column vector $\mathbf{b_1}$ is a symmetric vector in relation to its center index. Consequently, the optimal filter $\mathbf{h_1^{opt}}$ is symmetric too. The symmetry of the channel filter allows to divide by 2 the number of multipliers in filter design. Figure 4.6 illustrates the impulse response and frequency response of the optimal channel filter, $H^{opt}(z)$, for a time-interleaved $\Delta\Sigma$ converter employing four channels of fourth-order $\Delta\Sigma$ modulators. We observe that the optimal filter is a low-pass filter.

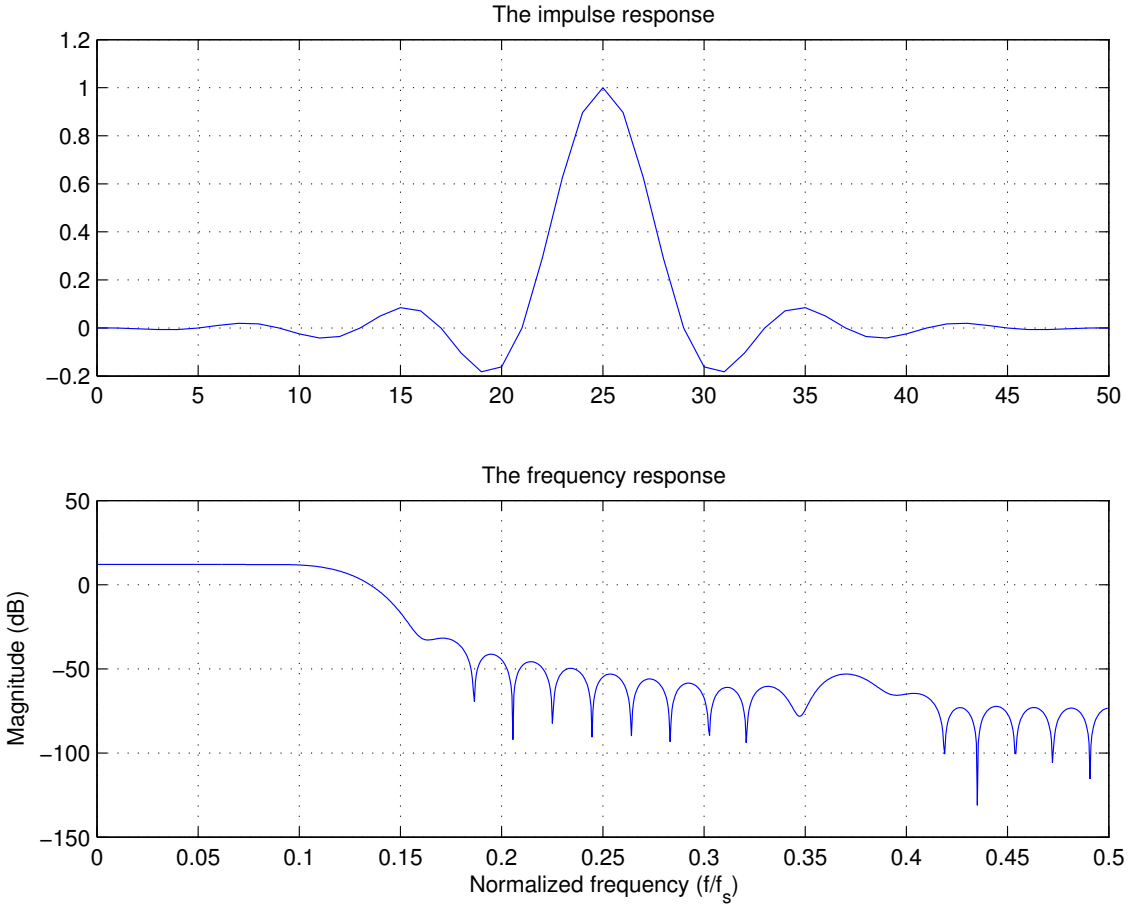


Figure 4.6: The impulse response and frequency response of an optimal channel filter for a time-interleaved $\Delta\Sigma$ converter employing four channels of fourth-order $\Delta\Sigma$ modulators.

In summary, for an ideal L^{th}-order $\Delta\Sigma$ modulator that has $S(z) = z^{-L}$ and generates quantization error, whose power spectral density is that of noise driving an LTI filter, $N(z)$, we have found a solution for the impulse response of the odd-

length-N FIR filter $H(z)$, that minimizes the power of the overall quantization error, P_e, under the constraint that the overall useful signal is just a delayed version of the input signal.

Although a large class of $\Delta\Sigma$ modulators, including most of the multi-stage $\Delta\Sigma$ modulators, have these properties [1, 126], there exist many useful $\Delta\Sigma$ modulators for which the signal transfer function, $S(z)$, is not just a delay. For example, in most of the single-loop higher-order $\Delta\Sigma$ modulators, $S(z)$ corresponds to infinite impulse response (IIR) low-pass filter [124]. Although the power spectral density of the quantization error from these $\Delta\Sigma$ modulators is often modelled as that of white noise driving an LTI filter, $N(z)$, there is not yet a rigorous theoretical basis for doing so. Nevertheless, if the quantization error is at least quasistationary sequence, and its power spectral density is known, then the problem of choosing the optimal constrained filter, $H(z)$ is well posed and in principle may be solved. However, there is no obvious general formula for choosing the optimal constrained filter $H(z)$. For $\Delta\Sigma$ modulators outside the class of $\Delta\Sigma$ modulators considered above, the optimization is much more complex and must be performed on a case by case basis.

4.3.4 Ideal Performance Obtainable

A sinusoidal signal is often used to characterize an ADC. The dynamic range is defined as the ratio between the output power at the frequency of a sinusoidal input with full-scale range amplitude and the output power when the input is a sinusoidal of the same frequency, but of a small amplitude, so that it cannot be distinguished from noise, i.e. SNR = 0. Ideally, the full-scale range of the modulator input is approximately given by that of the quantizer. In the single-bit quantization case, the full-scale sinusoid has a peak-to-peak amplitude equal to the quantization step size, Δ, and a power, P_s, equal to $\Delta^2/8$. Therefore the ideal dynamic range expressed in decibels of the time-interleaved $\Delta\Sigma$ converter with a sinusoidal input signal can be calculated as

$$DR = 10log\left(\frac{P_s}{P_e}\right) = 10log\left(\frac{\Delta^2}{8\,P_e}\right), \tag{4.37}$$

where P_e is given by the expression in (4.30) with the optimal channel filters.

As shown in the previous subsection, the longer is the channel filter length, the smaller is the power of the overall quantization error. But, as will be illustrated

hereafter, when the channel filters are sufficiently long, the power of the overall quantization noise gets almost constant. An increase in length no longer significantly decreases P_e. With a filter length-401, we observe already this phenomenon. This length is hence used to determine the influence of m_0 ($m_0 = i_0\,M - k_0 - L$ defined from (4.15) as the constraint index so that $h_{opt}[m_0] = 1$) in the system performance. Figure 4.7 shows plots of ideal DR versus the position of m_0 for various numbers of

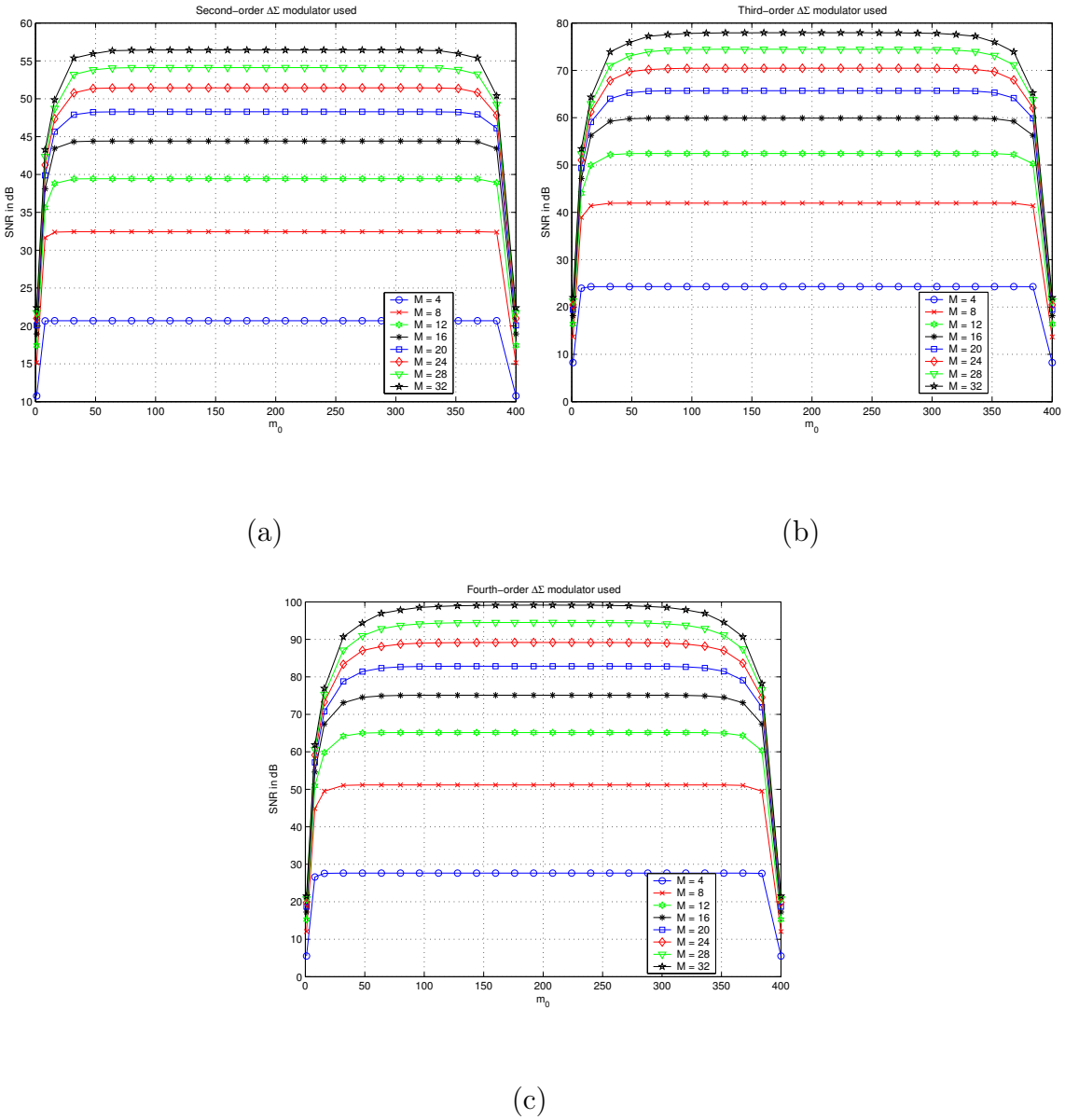


Figure 4.7: The ideal DR in dB of the time-interleaved $\Delta\Sigma$ converter versus m_0, with $M = 4, 8, \cdots, 30$, for (a) second-order, (b) third-order, and (c) fourth-order $\Delta\Sigma$ modulators. The length-401 channel filters are used.

channels and modulator orders. This figure consists of three parts, each of which

shows plots of the ideal DR of the time-interleaved $\Delta\Sigma$ converter versus the position of m_0. For each $\Delta\Sigma$ modulator, eight curves are shown; from bottom to top the curves correspond to $M = 4, 8, \cdots, 32$ respectively. It shows clearly that for each $\Delta\Sigma$ modulator and each number of channels, the maximum of DR is reached when m_0 is the center index of filter impulse response. Therefore, m_0 is taken from now on as the center index of filter impulse response.

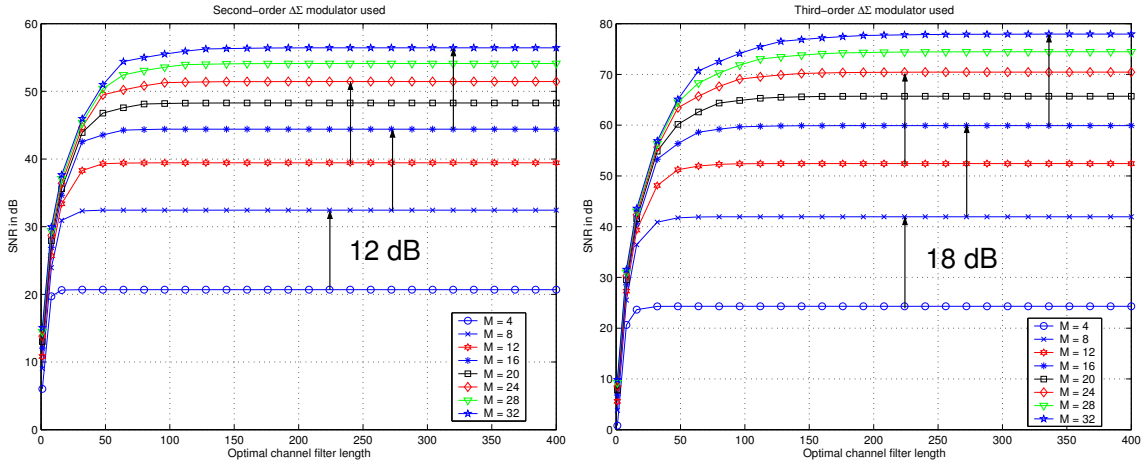
Figure 4.8 shows the ideal performance obtainable using the optimal channel filter derived from Subsection 4.3.3. It shows plots of the ideal DR of the time-interleaved $\Delta\Sigma$ converter as a function of $\Delta\Sigma$ modulator order, L, number of channels, M, and channel filter length, N. This figure consists also of three parts, each of which shows plots of the ideal DR of a time-interleaved $\Delta\Sigma$ converter versus the channel filter length. For each $\Delta\Sigma$ modulator, eight curves are shown; from bottom to top the curves correspond to $M = 4, 8, \cdots, 32$ respectively. For a given number of channels, filter length, and modulator order, the ideal DR can be determined using Figure 4.8.

Figure 4.9 shows the maximum attainable of the ideal DR as the function of the number of channels on the log scale for each $\Delta\Sigma$ modulator order. From bottom to top, the curves shown correspond to second-, third-, and fourth-order $\Delta\Sigma$ modulator, respectively. For each DR calculation, the filter length was sufficiently long that an increase in length would not significantly decrease DR. We observe that in each case the curve is straight and for every doubling of the number of channels, the ideal DR increases by approximatively $6L$ dB where L is the modulator order, as already indicated in Figure 4.8. This implies that doubling the number of channels increases the conversion accuracy of the time-interleaved $\Delta\Sigma$ converter by approximatively L-bit. Therefore, in this architecture, the number of channels, M, plays almost the same role as the OSR in the conventional $\Delta\Sigma$ converter.

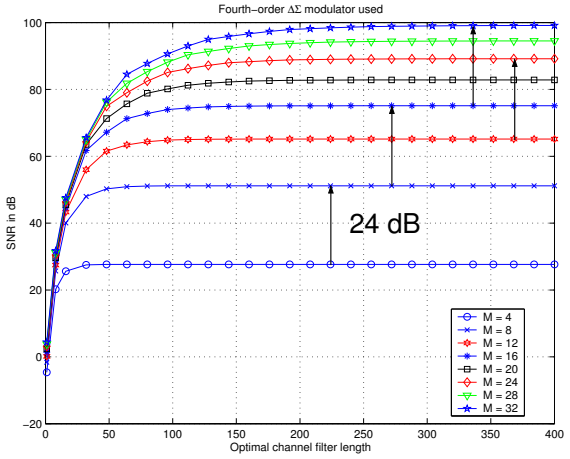
4.3.5 Minimal Filter Length of the Optimal Filter

To simplify the complexity of the channel filters, it is necessary to determine the minimal filter length allowing to attain a performance close to the ideal DR. Table 4.1 presents the minimal filter length of the optimal channel filters as a function of the modulator order and the number of channels, with which the DR obtained is only 1 dB lower than the ideal maximum DR attainable.

As we know, the minimal filter length depends on the modulator order and the



(a) (b)



(c)

Figure 4.8: The ideal DR in dB of the time-interleaved $\Delta\Sigma$ converter versus channel filter length, N, with $M = 4, 8, \cdots, 30$ for (a) second-order, (b) third-order, and (c) fourth-order $\Delta\Sigma$ modulators.

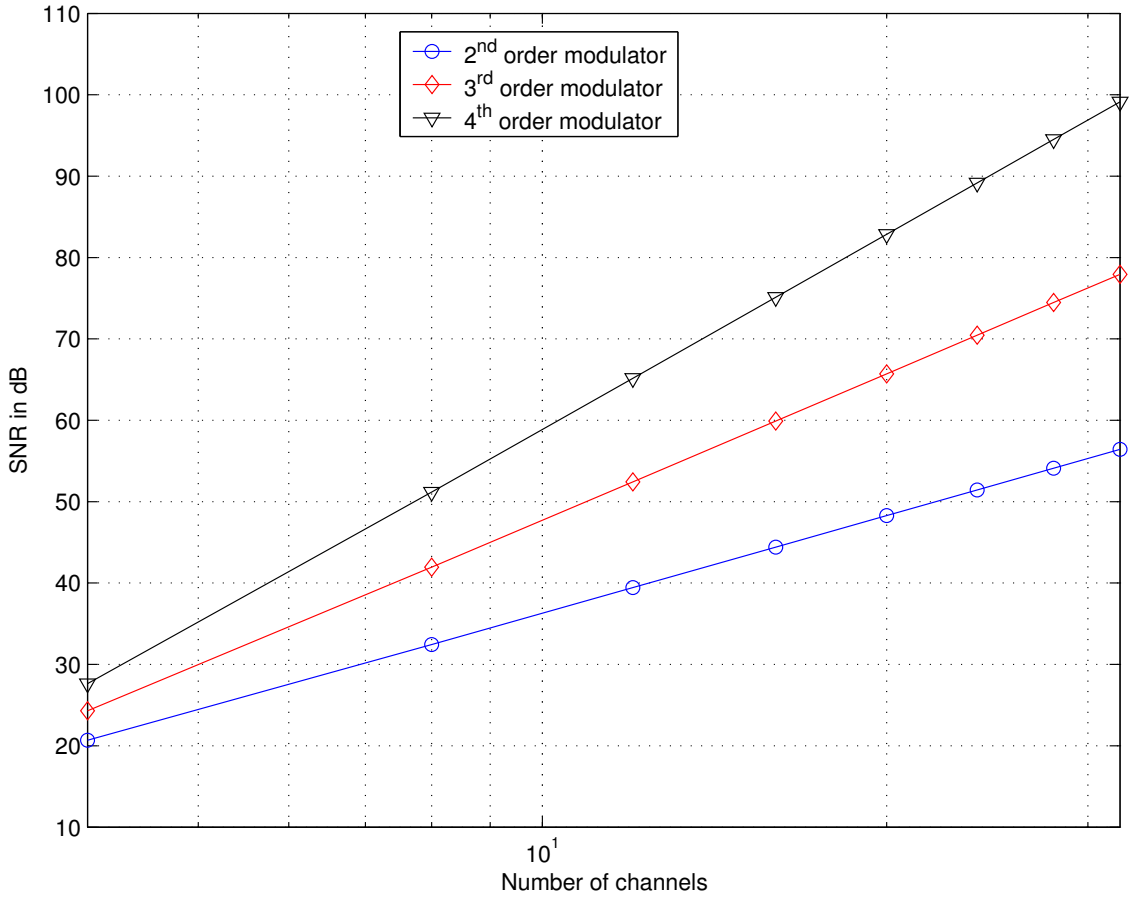


Figure 4.9: The ideal DR of the time-interleaved $\Delta\Sigma$ converter for optimal channel filter versus the number of channels on a log scale.

Number of channels : M	Modulator order : L		
	2	3	4
4	7	15	22
8	22	34	47
12	34	54	75
16	46	72	102
20	58	91	128
24	70	110	154
28	82	129	180
32	94	148	206

Table 4.1: The minimal filter length of the optimal channel filter allowing to attain an DR equal to the ideal DR minus 1 dB.

number of channels. The minimal filter length required to have a desired DR can be calculated. The study of the optimal filter complexity as a function of the filter length, presented in Appendix A, shows that the number of adders and multipliers needed are $M\left(N-1-2\left[\frac{N+1}{2M}\right]\right)$ and $M\left(\frac{N-1}{2}-2\left[\frac{N+1}{2M}\right]\right)$, respectively. The filter length, N, is odd and m_0 is the center of the filter so that the optimal filter is symmetric. In this case, the filter complexity is divided by a factor of two, approximately.

4.4 Sensitivity to Nonideal Circuit Behavior

Parallel $\Delta\Sigma$ converters such as $\Pi\Delta\Sigma$ converter and time-interleaved $\Delta\Sigma$ converter, are sensitive to nonideal circuit behavior [150, 151, 152]. Circuit nonidealities reduce the conversion accuracy of the time-interleaved $\Delta\Sigma$ converter below that predicted by the theoretical analysis. Common types of nonideal circuit behavior arise from different sources: electronic noise, errors in the nominal values of components such as capacitors and resistors, finite op-amp gain and bandwidth, non-zero op-amp settling time, comparator hysteresis and clock timing jitter. In the $\Delta\Sigma$ modulators, these nonidealities manifest themselves as analog gain mismatch, high electronic noise floor, integrator leak, integrator nonlinearity, nonuniform quantization levels in the coarse ADC, and nonuniform reference levels in the DAC. In time-interleaved $\Delta\Sigma$ converter, the nonidealities additionally manifest themselves as channel gain and offset mismatch.

The presence of the nonideal circuit behavior causes the output to contain an overall circuit error component denoted as $e_{ni}[n]$ in addition to the overall signal, w[n], and overall quantization error, $e[n]$. Therefore, the output can be written as the sum of three components as

$$y[n] = w[n] + e[n] + e_{ni}[n]. \tag{4.38}$$

The overall circuit error component can be divided into two types: one is common to conventional $\Delta\Sigma$ ADC, and the other is specific to the time-interleaved $\Delta\Sigma$ converter. This allows existing results concerning nonideal circuit behavior in conventional $\Delta\Sigma$ ADC to be applied directly to the time-interleaved $\Delta\Sigma$ converter. The overall circuit error component can be considered as the sum of the two subcomponents: the conversion error subcomponent and the reconstruction er-

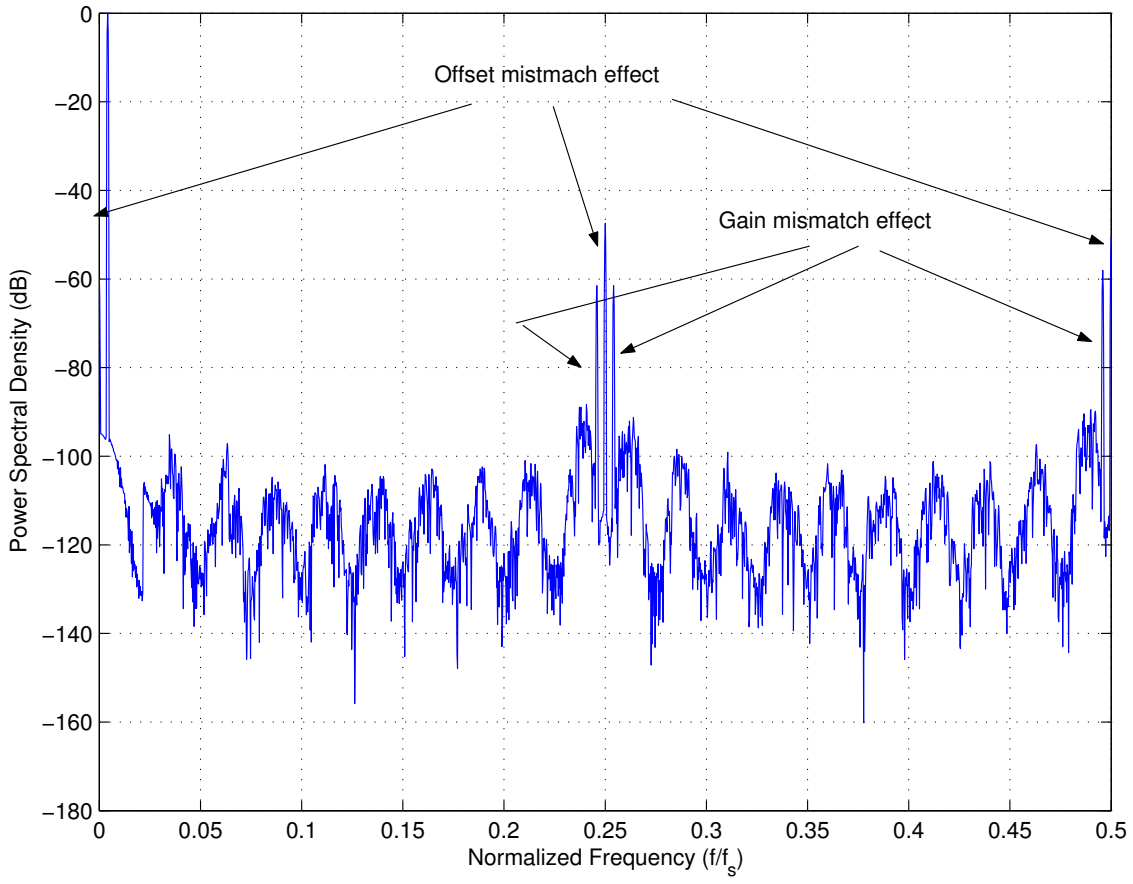


Figure 4.10: Output spectrum of time-interleaved fourth-order $\Delta\Sigma$ ADC with four channels in the presence of the channel mismatch.

ror subcomponent. The conversion error subcomponent is the result of all types of nonideal $\Delta\Sigma$ modulator performance arising from nonideal circuit behavior except for $\Delta\Sigma$ modulator signal component gain and offset error. The reconstruction error subcomponent is the aggregate of all analog-to-digital conversion errors arising from nonideal circuit behavior that are not part of the conversion error subcomponent, such as channel gain and offset errors.

The conversion error subcomponent is analogous to the error caused by nonideal circuit behavior in conventional $\Delta\Sigma$ ADC. Each channel of the time-interleaved $\Delta\Sigma$ converter contains the equivalent of a conventional $\Delta\Sigma$ ADC because each $\Delta\Sigma$ modulator is followed by a low-pass filter. Hence, on each channel the component of the sequence just prior to the demultiplexer arising from the nonideal $\Delta\Sigma$ modulator has the same characteristics as the corresponding component of the output of a conventional $\Delta\Sigma$ ADC. In general, the M such error components are correlated. However, they originate from sources located after the multiplexer in the time-interleaved $\Delta\Sigma$ converter. Consequently, they are decorrelated by the demultiplexer. As a result, they add in power, not in amplitude: the power of the conversion error subcomponent is simply the sum of the powers of the low-pass filtered errors from the M nonideal $\Delta\Sigma$ modulators. It follows that this error is about M times the corresponding error at the output of a conventional $\Delta\Sigma$ ADC.

Unlike the conversion error subcomponent, the reconstruction error subcomponent does not have a direct analogy in conventional $\Delta\Sigma$ ADC. This error arises from mismatch among the signal component gains and offsets of the $\Delta\Sigma$ modulators. To evaluate these errors and their effect on the converter performance, we proceed as follows:

Assume that α_i and β_i are respectively the gain error and the offset of the i^{th} channel. After some calculations, the overall error component, $e_{ni}[n]$, can be expressed as a function of α_i and β_i, and also $h[n]$ and $x[n]$ as follow.

$$e_{ni} = \sum_{k=0}^{N-1} h[k]x[n-L-k] \sum_{i=0}^{M-1} u_i[n+k_0](\alpha_i - 1)u[n-L-k] + \sum_{k=0}^{N-1} h[k] \sum_{i=0}^{M-1} u_i[n+k_0]\beta_i \tag{4.39}$$

This error will increase the inband noise level that degrades the SNR of the converter and introduce undesired tones that reduce the SFDR of the converter.

Figure 4.10 shows simulation data that illustrates the effect of the reconstruction error subcomponent. This figure shows precisely the power spectrum density of the

time-interleaved ΔΣ converter output in the presence of channel gain errors and channel offset. In this example, a fourth-order cascaded (2-2) ΔΣ modulator is used, and the number of channels is set to four. As shown in Figure 4.10, channel offset mismatch causes additive tones at integer multiples of F_s/M and channel gain mismatch results in amplitude modulation of the input samples, and causes scaled copies of the input spectrum to appear centered around integer multiples of the F_s/M. All these mismatches increase the noise floor of the ADC, and degrades the SNR and reduces the SFDR. When the OSR is only four, we obtain an ideal DR of 75 dB. In presence of gain error and offset, the performance is degraded by about 10 dB for 0.5% gain mismatch, and by about 20 dB for 0.5 % offset mismatch. It is therefore necessary to find a calibration technique that reduces the effect of the channel mismatch.

4.5 Time-Interleaved High-Pass ΔΣ ADC

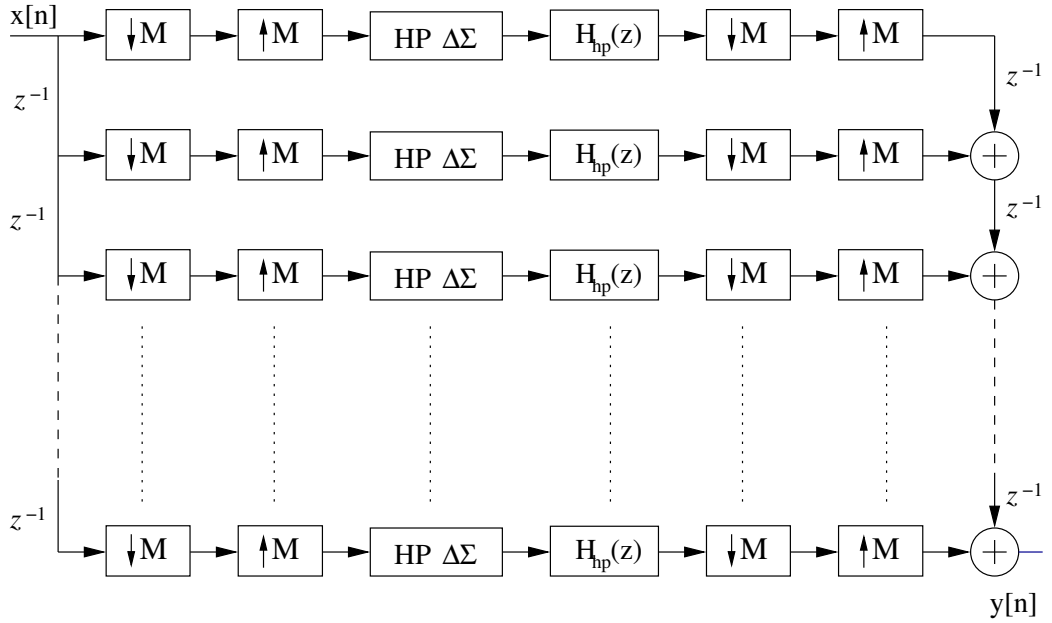


Figure 4.11: Diagram of the time-interleaved high-pass ΔΣ ADC. Multi-cadence system presentation.

As presented above, channel mismatch caused by circuit nonidealities degrades significantly the performance of the time-interleaved ΔΣ ADC. Channel offsets, for example, introduce undesired tones that degrade the SFDR of the time-interleaved

$\Delta\Sigma$ ADC. The correlated double sampling and chopper stabilization are two common techniques used to reduce the low frequency noise effect, so the offset effect. In the chopper stabilization technique, the input signal is mixed up and away from the low frequency region by a chopper mixer so that low frequency noises introduced in the subsequent signal processing will not affect the input signal [102, 103, 104, 105, 153]. This technique can be applied to the $\Delta\Sigma$ modulator as explained in Chapter 3.

In this section, we propose to adapt this technique to the time-interleaved $\Delta\Sigma$ converter by replacing the low-pass modulators with high-pass modulators and low-pass channel filters with high-pass channel filters. The obtained converter is called time-interleaved high-pass $\Delta\Sigma$ converter. The multiplexer and demultiplexer are respectively equivalent to a delay chain followed by M-fold decimators and M-fold expanders followed by a delay chain. Thus the time-interleaved high-pass $\Delta\Sigma$ ADC can be shown as in Figure 4.11. The chopper mixer is no longer needed in this architecture. Its role can be played by the multiplexer with an even number of channels. For the sake of simplicity and without loss of generality, the correctness of the proposed technique is demonstrated in Figure 4.12 which presents the frequency domain evolution of the input signal in the case where there are only two channels.

In the time-interleaved low-pass $\Delta\Sigma$ converter, the spectrum of the input signal entering in a channel is shown in Figure 4.12(a - lp). The input signal is decimated and the aliased result is shown in Figure 4.12(b - lp). The expander creates an M-fold compressed version of the signal at point X2 in the frequency domain as shown in Figure 4.12(c - lp). The low-pass $\Delta\Sigma$ modulator shapes the quantization noise to high frequency range and introduces low frequency noise as shown in Figure 4.12(d - lp). The low-pass filter allows only one image of the signal pass through and eliminates the bulk of the quantization noise as shown in Figure 4.12(e - lp). The decimator after the filter reconstructs the image of X1 at point Y2 as shown in Figure 4.12(f - lp). But the signal at point Y2 is contaminated by low frequency noise. We note that the aliasing of the signal at point X1 is still preserved at the point Y2. The aliased terms are cancelled using an M-fold expender and by summing the outputs of the channels with appropriate delay as shown in Figure 4.12(g - lp)(h - lp). The digital output of the converter is contaminated by low frequency noise.

When the high-pass $\Delta\Sigma$ modulators are used, the first four operations are not changed as shown in Figure 4.12(a - hp), (b - hp), (c - hp). But unlike the low-pass modulator, the high-pass modulators shapes the quantization noise to low frequency

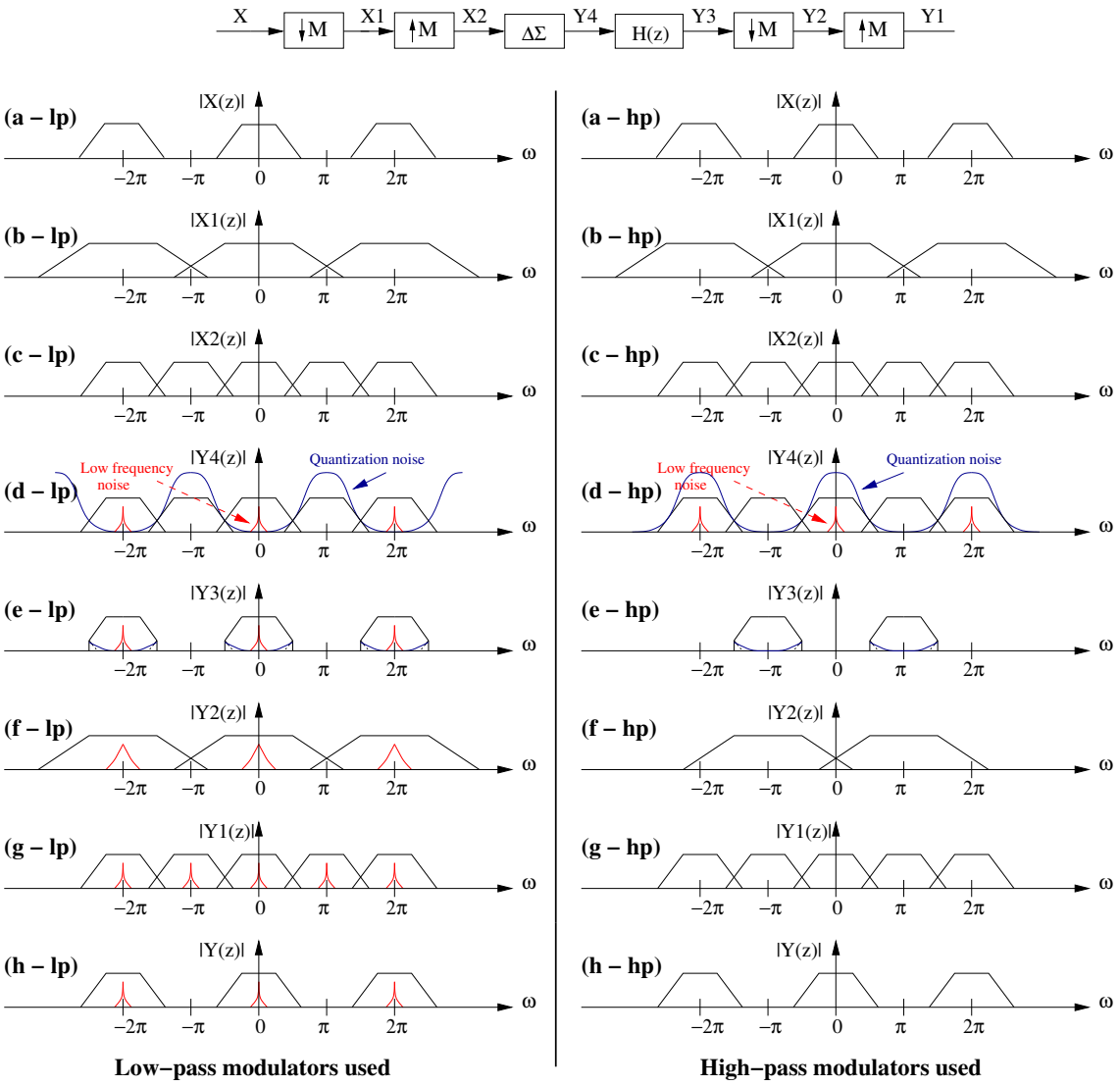


Figure 4.12: Frequency domain presentation of time-interleaved high-pass ΔΣ ADC. On the left, the low-pass modulators are used. On the right, the high-pass modulators are used.

(a): Spectrum of the input signal ;

(b): Spectrum of signal at the M-fold decimator output;

(c): Spectrum of signal at the M-fold expander output;

(d): Spectrum of signal et the ΔΣ modulator output;

(e): Spectrum of signal at the channel filter output;

(f): Spectrum of signal at the digital M-fold decimator output;

(g): Spectrum of signal at the digital M-fold expender output;

(h): Spectrum of the converter output signal.

range as shown in Figure 4.12(d - hp). The bulk of quantization noise and the low frequency noise are eliminated by the high-pass channel filter as shown in Figure 4.12(e - hp). If the number of channels, M, is even, then there is an image of the input signal centered around $f_s/2$. The high-pass filter allows therefore this image pass through. In other words, the useful signal is now at high frequency region. This phenomenon occurs if and only if the number of channels is even. We can recover the useful signal, X(z), and cancel aliased terms from Y2(z) through an M-fold expender in summing the channel outputs with appropriate delay as shown in Figure 4.12(g - hp)(h - hp). The digital output of the converter is completely immune to low frequency noise.

The ideal performance of the time-interleaved high-pass $\Delta\Sigma$ ADC is equivalent to that of the conventional $\Delta\Sigma$ ADC. The advantage of the former is its immunity from the offset mismatch effect that is a serious problem for the latter. The ideal performance of the time-interleaved high-pass $\Delta\Sigma$ ADC with fourth-order high-pass $\Delta\Sigma$ modulators have been simulated for various numbers of channels. The fourth-order high-pass $\Delta\Sigma$ modulator used for the simulations was similar to the fourth-order low-pass $\Delta\Sigma$ modulator, but consisted of cascades of two second-order high-pass $\Delta\Sigma$ modulators, that were themselves obtained from the second-order low-pass $\Delta\Sigma$ modulators by replacing z with $-z$. The output $Y(z)$ of the resulting fourth-order high-pass $\Delta\Sigma$ modulator can be qualitatively written as

$$Y(z) = X(z)z^{-4} + E(z)\left(1 + z^{-1}\right)^{-4} \tag{4.40}$$

where $X(z)$ is the input and the $E(z)$ is the quantization noise. The equation clearly indicates that the quantization noise is shaped to low frequency range. Consequently, a digital high-pass filter can be used to remove the out-of-band quantization noise. The high-pass channel filters used in simulations were obtained from low-pass channel filters by replacing z with $-z$. Figure 4.13 shows the power spectrum of the output of the time-interleaved high-pass $\Delta\Sigma$ ADC in the presence of channel gain and offset mismatch. In Figure 4.13, the advantage of using the high-pass $\Delta\Sigma$ modulators in the time-interleaved $\Delta\Sigma$ converter is clearly shown: undesired tones generated from channel offset mismatch have been completely removed.

However, undesired tones caused by the channel gain mismatch still remain in the output spectrum as shown in Figure 4.13. The channel gain mismatch reduces still the SFDR performance of the converter. Therefore, the minimization of the channel gain mismatch effect is necessary and will be studied in the next section.

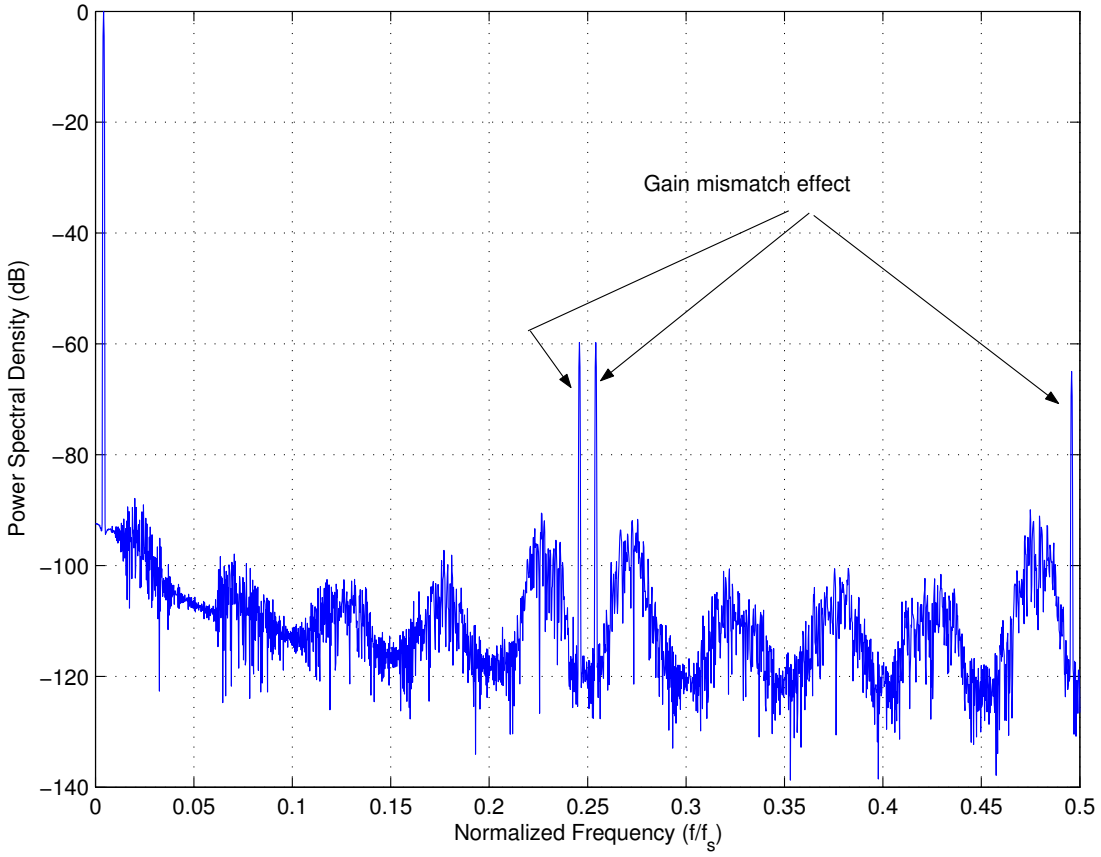


Figure 4.13: Output signal spectrum of the time-interleaved fourth-order high-pass $\Delta\Sigma$ ADC employing four channels in the presence of the channel mismatch.

4.6 Adaptive Equalization of Channel Gain Mismatch

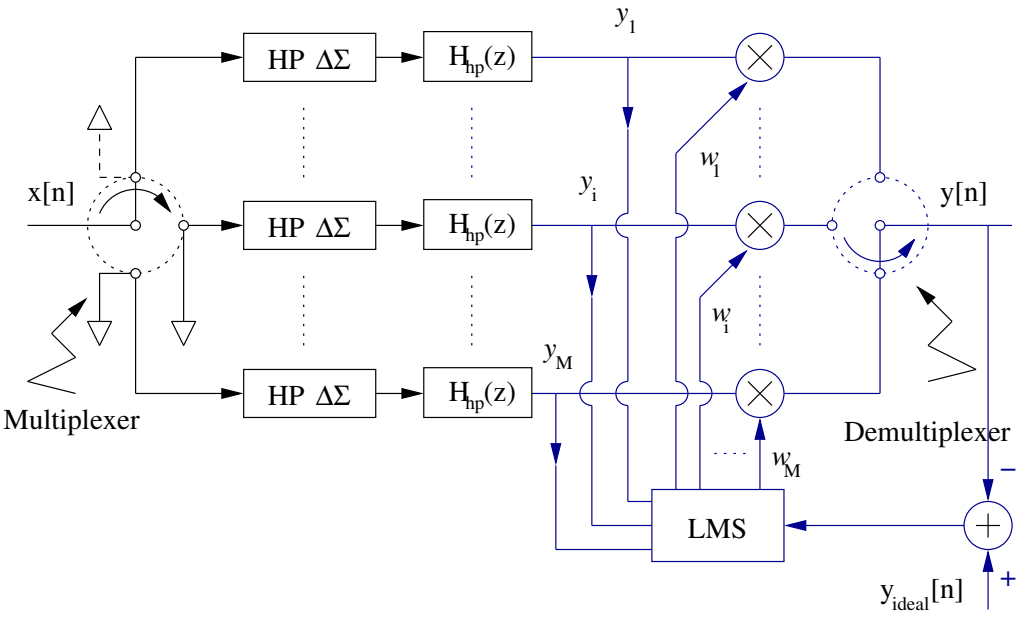


Figure 4.14: Interleaved high-pass ΔΣ ADC architecture with adaptive channel gain equalization.

The channel gain mismatch degrades the performance of the converter. If all channel gains are known, the effect of channel gain mismatch may be corrected by a digital post processing. But the actual channel gains are not known. To solve this problem, we propose a simple adaptive channel gain equalization scheme that minimizes the channel gain mismatch effect on the converter performance.

Indeed, the channel gain mismatch could be equalized simply by adding an extra multiplier after each channel output. These are shown as weights $[w_1, w_2, ...w_M]$ in Figure 4.14. The idea is that when the weights are chosen to be the inverse of the corresponding channel gain, the overall channel gain will be unity, and the effect of the channel gain mismatch will be removed.

There are different alternative approaches to obtain the desired values of the weights. Here, we propose a simple adaptive scheme as shown in Figure 4.14, based on the well known least-mean-square (LMS) algorithm, due to its implementation simplicity and robust performance. For even greater implementation simplicity, the sign-data, the sign-error and the sign-sign LMS (SD-LSM, SE-LMS and SS-LMS respectively) algorithms [154] can be used. They will also be studied. The

efficiency of all these methods will be then compared in terms of performance and implementation simplicity.

The weights can be obtained iteratively from the equations (4.41), (4.42), (4.43) and (4.44) for LMS, SD-LMS, SE-LMS and SS-LMS algorithms respectively.

$$\hat{\mathbf{W}}_{k+1} = \hat{\mathbf{W}}_k + \mu\,(y_{ideal}(n) - y(n))\hat{\mathbf{Y}}, \tag{4.41}$$

$$\hat{\mathbf{W}}_{k+1} = \hat{\mathbf{W}}_k + \mu\,(y_{ideal}(n) - y(n))\,\mathrm{sgn}(\hat{\mathbf{Y}}), \tag{4.42}$$

$$\hat{\mathbf{W}}_{k+1} = \hat{\mathbf{W}}_k + \mu\,\mathrm{sgn}(y_{ideal}(n) - y(n))\,\hat{\mathbf{Y}}, \tag{4.43}$$

$$\hat{\mathbf{W}}_{k+1} = \hat{\mathbf{W}}_k + \mu\,\mathrm{sgn}(y_{ideal}(n) - y(n))\,\mathrm{sgn}(\hat{\mathbf{Y}}), \tag{4.44}$$

where

$$\mathrm{sgn}(x) = \begin{cases} +1 & \text{when } x \geq 0 \\ -1 & \text{when } x < 0 \end{cases}. \tag{4.45}$$

$\hat{\mathbf{W}}$ is a vector formed by the weights $[w_1, w_2, ...w_M]$, and $\hat{\mathbf{Y}}$ is formed by the channel outputs $[y_1, y_2, ...y_M]$, $y_{ideal}(n)$ is the ideal output and k is time index. Step size, μ, is a parameter that control stability and convergence rate. All weights are initialized to 1.

The value of the adaptation constant, μ, depends on the algorithm used. Too small step size will make the algorithm take a lot of iterations; While too big step size will not ensure the convergence of weights. Simulations show that the chosen step size μ, indicated in Table 4.2, when the input signal is a sinusoidal signal, presents a good compromise between the convergence rate and convergence precision for each algorithm used.

Algorithm	LMS	SD-LMS	SE-LMS	SS-LMS
μ	4	1	1/256	1/4096

Table 4.2: Step size value for LMS, SD-LMS, SE-LMS and SS-LMS algorithms.

Figure 4.15 shows the magnitude of the weights as they approach the inverse of the real channel gains. We observe that in terms of algorithm convergence speed, the SD-LMS algorithm is the fastest and the SS-LMS algorithm is the slowest. When considering algorithm implementation, the LMS algorithm is the most complex while the SS-LMS algorithm is the simplest. The SD-LMS, being simpler than the LMS algorithm, requires M slicers and M trivial multipliers which is more complex than the SE-LMS algorithm requiring 1 slicer and M trivial multipliers, where M is the

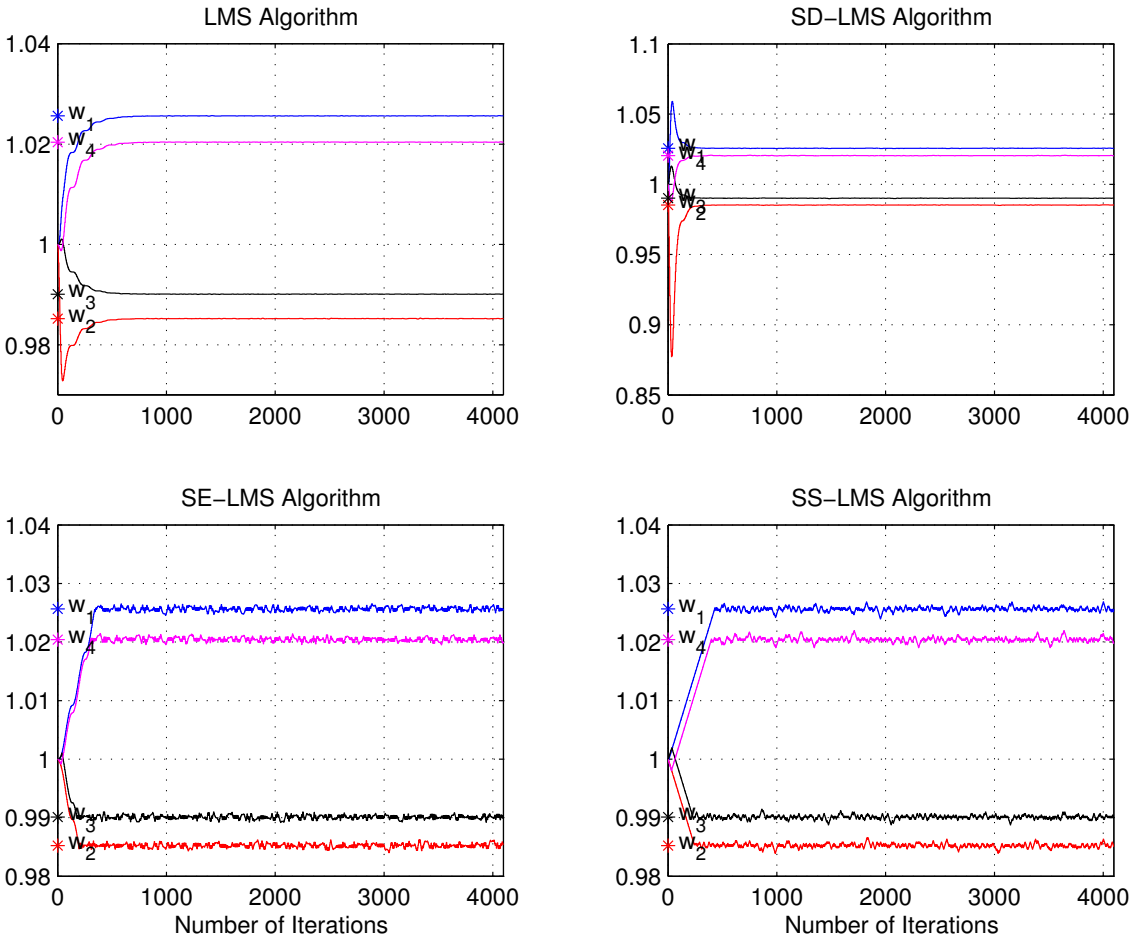


Figure 4.15: Magnitude of the weights as they converge to the final value.

number of weights being adapted [154]. In terms of performance, we observe that the LMS is the best as shown in Figure 4.15. But the result obtained from SD-LMS is really close to that from LMS. When SE-LMS or SS-LMS algorithms are used, the inband noise floor is increased as shown in Figure 4.16.

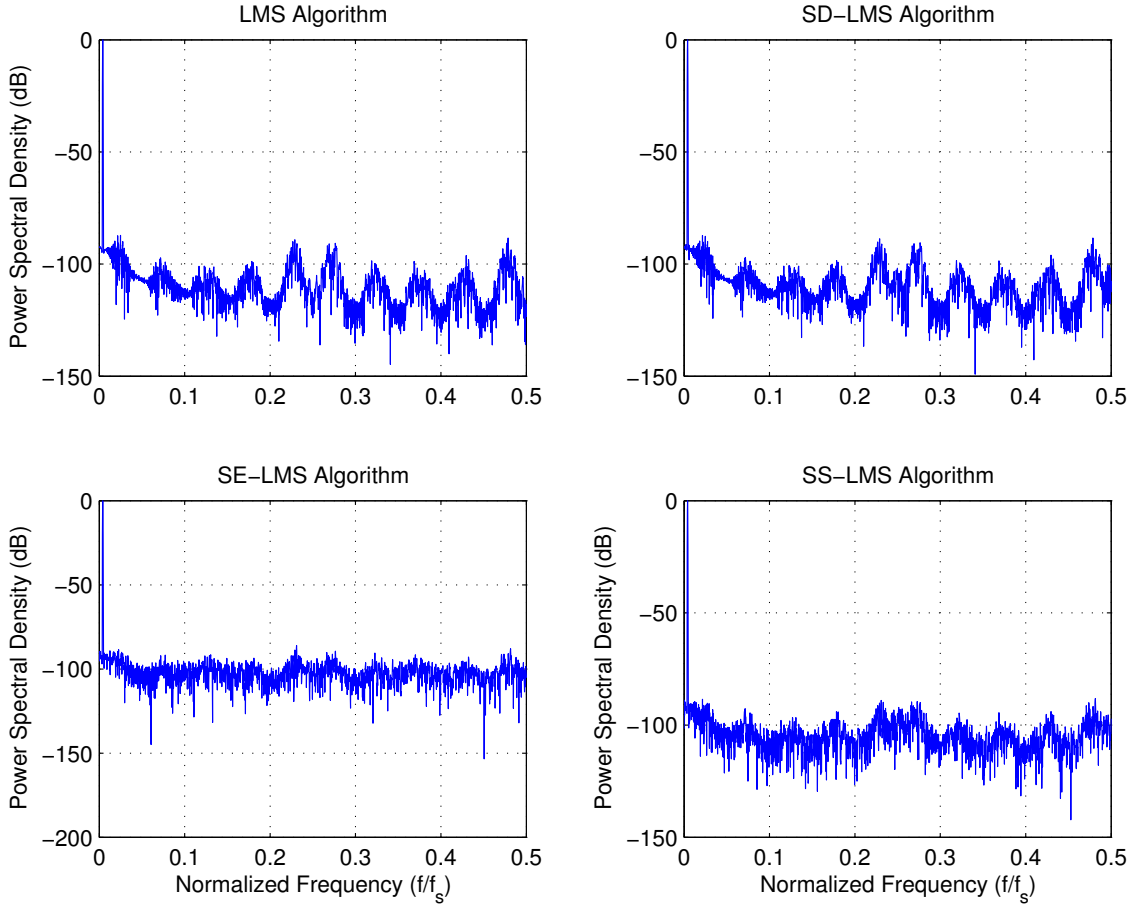


Figure 4.16: Output signal spectrum with four algorithms.

To compare more precisely the performance of the four algorithms, we resort to Monte Carlo analysis. An uniform random error which varies from -0.5 to 0.5 and whose variance is 0.01 is added to each channel, i.e. the relative standard deviation of gain error is 10%. The number of simulation runs for the Monte Carlo analysis is 2048, the result obtained is shown in Table 4.3. Concerning the DR of the converter, we achieve the highest DR with LMS algorithm that is very close to ideal performance. The SD-LMS provides a result very close to that of LMS algorithm, while SE-LMS and SS-LMS algorithms give us similar results which are about 4 dB lower than that of LMS and SD-LMS algorithms.

	Ideal	LMS	SD-LMS	SE-LMS	SS-LMS
Mean	75.10	73.1	72.9	69.2	69.7
Standard deviation		1.22	1.23	1.41	1.36

Table 4.3: DR(dB) of ADC with different algorithms

Using the LMS and SD-LMS algorithms, all the undesired tones generated by the channel gain mismatch are almost completely eliminated. But SD-LMS is better in term of implementation and arithmetic complexity. Especially, when the step size, μ, is 1, the arithmetic complexity of the SD-LMS becomes much simpler than that of LMS. SD-LMS is clearly the better choice than LMS. Between the other two algorithms, we observe that the performance provided by SS-LMS is slightly better than that of SE-LMS. Moreover, the implementation of SS-LMS is simpler than that of SE-LMS. Consequently, SS-LMS outweighs SE-LMS. Therefore, the choice must be done between SD-LMS and SS-LSM. This choice depends on the specifications of a given application. For high resolution application, the SD-LMS algorithm should be chosen. The output spectrum of the final gain equalized time-interleaved high-pass sigma-delta ADC is plotted in Figure 4.17. The figure clearly shows the absence of the undesired tones generated by the channel gain mismatch and offset mismatch.

4.7 Conclusion

The time-interleaved $\Delta\Sigma$ converter is a form of parallel $\Delta\Sigma$ converter. The use of $\Delta\Sigma$ modulators in parallel architecture may allow the $\Delta\Sigma$ conversion technique to be applied to higher bandwidth applications. The advantage of the time-interleaved $\Delta\Sigma$ converter is its reduced complexity. For a system containing M L^{th}-order $\Delta\Sigma$ modulators, about L-bit of resolution is obtained for every doubling the number of channels. The number of channels plays almost the same role as the OSR in the conventional $\Delta\Sigma$ converter.

However, this kind of converter is sensitive to nonideal circuit behavior, especially the channel mismatch. We have proposed a new time-interleaved $\Delta\Sigma$ ADC architecture using high-pass $\Delta\Sigma$ modulators instead of low-pass modulators. The ideal performance of the time-interleaved high-pas $\Delta\Sigma$ converter is identical to that

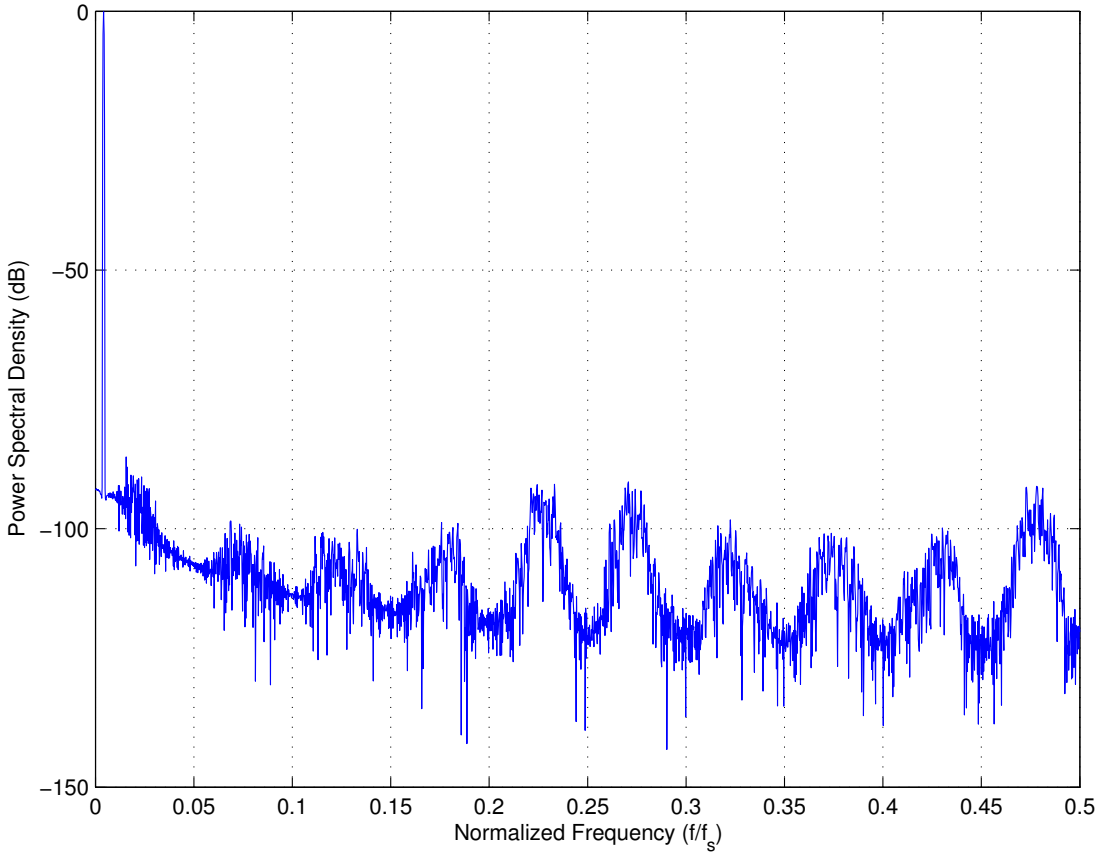


Figure 4.17: Output signal spectrum of the time-interleaved high-pass $\Delta\Sigma$ ADC with adaptive channel gain equalization

of the time-interleaved low-pass $\Delta\Sigma$ ADC, but with the additional benefit of immunity to channel offset mismatch. Unlike the time-interleaved low-pass $\Delta\Sigma$ converter, the proposed one needs an even number of channels. Regarding the channel gain mismatch, an adaptive channel gain equalization method based on LMS algorithm, has been proposed and studied in order to minimize the effect of this mismatch. Furthermore, the time-interleaved high-pass $\Delta\Sigma$ ADC is obtained from the time-interleaved $\Delta\Sigma$ ADC without extra hardware complexities. The analysis is general in that it does not place any significant restriction on the types of $\Delta\Sigma$ modulators. The ideas presented in this chapter may allow the application of $\Delta\Sigma$ modulator in high bandwidth applications such as video processing or digital radio.

Chapter 5

Design Methodology with VHDL-AMS

5.1 Introduction

A significant problem in the design of $\Delta\Sigma$ modulators in general and high-pass modulators in particular is the estimation of the nonideality effect on their performance, and their performance itself, since they are mixed-signal nonlinear circuits. Due to the inherent nonlinearity of the modulator loop, the optimization of the performance has to be carried out with behavioral time domain simulations. Naturally, circuit level simulation is the most accurate. However, the evaluation of the circuit nonidealities effect and the optimization of the building blocks embedded in the modulator are very difficult to handle because of the long simulation time. Indeed, the essence of the traditional circuit simulators is based on complicated element models. If these simulators are used to design $\Delta\Sigma$ modulators, long simulation time will make the simulator impractical to co-simulate and verify both analog and digital circuits. Moreover, in high-pass modulator, it is very important to determine the threshold value of the capacitor mismatch allowing the stability of the modulator. Such a determination is impossible with electric simulations. An intermediate stage of behavioral simulations is therefore necessary. Through multi-level abstraction models, VHDL-AMS allows to overcome the problems. Moreover, it allows a top-down design methodology. Indeed, an efficient behavioral model in VHDL-AMS reduces simulation time and reflects phenomena of circuit nonidealities. It also determines possible ranges of circuit specifications with reasonable design margins before circuit

components are implemented.

In this chapter, we present a brief overview of VHDL-AMS, and top-down design methodology. Individual blocks building the high-pass modulator are then modelled in VHDL-AMS. Various nonidealities are described and modelled. The effect of nonidealities on the modulator performance is analyzed to determine the specification for each modulator building block.

5.2 VHDL-AMS Overview

The VHDL, standardized first in 1987 and then in 1993 (VHDL 1076-1993), is a language for the description, simulation and synthesis of digital circuits for different technologies [155]. VHDL simulation model is based on a discrete-event simulation cycle. The modelling of analog systems with VHDL is possible but limited by the inherent discrete-event simulation mode. The application of discrete-event modelling mode to analog systems requires two consecutive transformations:

- The mapping of analog continuous-time systems into analog discrete-time systems based on data-sampling techniques;
- The mapping of analog discrete-time systems into VHDL syntax and semantics.

The first translation is an approximation of the continuous waveforms by a finite set of samples. If the analog waveform is frequency bandwidth limited, then the sampling inaccuracy can be eliminated, provided that the *Nyquist Criterion* is satisfied. The narrower is the bandwidth, the smaller is the number of samples.

This solution works well for relatively simple models. But complex analog models composed from several entities require more powerful modelling environment such as that provided by VHDL-AMS. This is an analog extension to VHDL providing capabilities of writing and simulating analog and mixed-signal models [156, 157].

VHDL-AMS is the IEEE-endorsed modelling language (standard IEEE 1076.1-1999) created to provide a general purpose, easily exchangeable, and open language for modern analog and mixed-signal designs [156, 157, 158]. It is a superset of VHDL that can support the description and simulation of circuits and systems that exhibit

continuous behavior over time and over amplitude. The design of analogue extension to VHDL began in 1993 and was supported by the Design Automation Standards Committee of the Computer Society of the IEEE and by Joint European Silicon Software Initiative and several industrial organizations. The IEEE Standard 1076.1-1999 has been approved on March 18, 1999 [158]. VHDL-AMS is a strict extension of VHDL, i.e. it includes the full VHDL language. The essential enhancements introduced into VHDL-AMS are:

- Support for quantities and terminals representing analogue signals and network connectivity;
- Support for simultaneous equations to model analogue behavior;
- Support for break mechanism required to model discontinuities in analogue signals.

The modelling space covered by VHDL-AMS is presented in Table 5.1.

	Continuous time	Discrete time
Continuous signal	• Differential and algebraic equation (DEA) systems • Analog components and circuits	• SC circuits • S/H
Discrete signal	• DACs	• ADCs • Sampled systems • Digital components and systems

Table 5.1: Modelling space covered by VHDL-AMS

This is a multi-domain language that is specially oriented to behavioral model and simulation of analog, digital, and mixed-signal systems. In electronics, and

especially in circuit design, behavioral modelling and simulation have become more and more frequent.

5.3 Top-Down Methodology with VHDL-AMS

Nowadays, the increasing complexity of the analog and mixed-signal circuitry makes it no longer feasible to go immediately from specification to transistor-level design. Intermediate steps become necessary. In order to address this challenge, many design teams are either looking to, or else have already implemented, top-down methodologies [159].

Top-down design methodologies have been successfully used to design digital hardware for long time [160]. These approaches follow a design from the top level, usually the specification level, down to a detailed implementation. More refinement in these methodologies works by having each level of detail used as the design specification for the level of detail immediately below. Nowadays, the methodologies of top-down design and bottom-up verification are well accepted standards in the world of digital design [160]. But this was not always the case. Prior to the availability of hardware description languages (HDLs), when designs were not as complex, there was no pressing need for top-down design techniques. It was possible to go to the detailed transistor design immediately after the release of the system specification. Today, the top-down technique enables a methodical and systematic approach to complex designs. The methodology allows system-level design flows to be exposed much earlier in the process, when they are much easier to correct.

The same raisons that forced digital design into top-down techniques are now pushing analog and mixed-signal design in the same direction [159, 161, 162]. In addition to becoming far more complex, modern analog designs frequently contain substantial mixed-signal circuitry, involving increased two-way interaction between the analog and digital portions. System-on-a-chip devices feature increasingly more analog components like ADCs, DACs, phase-locked loops, and adaptive filters, all of which are driving the demand for improved design methodologies.

The primary problem hindering the change to analog and mixed-signal top-down design and bottom-up verification has been the lack of tool support for the design process between system-level specification and transistor-level implementation, as

well as between transistor implementation and chip fabrication. The overview of

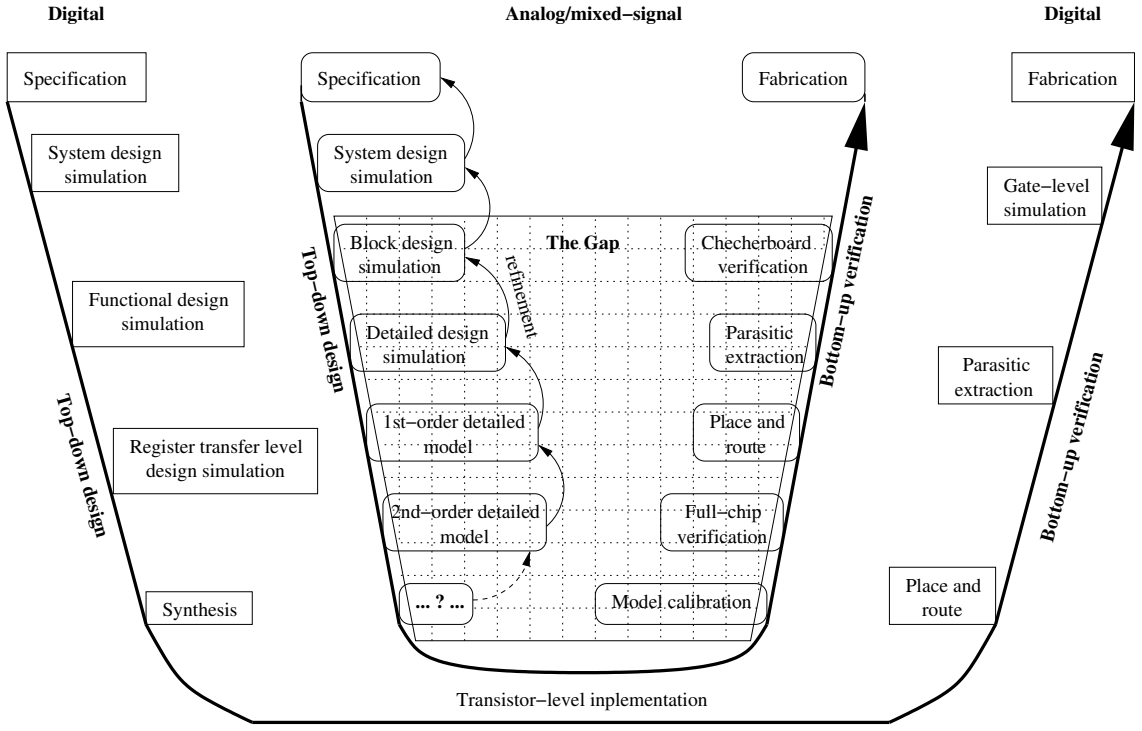


Figure 5.1: Design process: the entire digital design process is already fully automated, but analog and mixed-signal design is hindered by the "Gap", which reflects a lack of tool support for the design process between system-level specification and transistor-level implementation.

automated design for both digital and mixed-signal branches is depicted in Figure 5.1. Each branch progresses in incremental steps from specification through transistor implementation to fabrication. The digital branch, being more fully developed, flows smoothly from start to conclusion, with adequate tools in place to support each phase of development. In contrast, the analog and mixed-signal branch is subject to a number of missing tools, as highlighted by the "Gap". This gap will be filled with behavioral models in VHDL-AMS.

The architecture of the chip such as high-pass $\Delta\Sigma$ modulator and time-interleaved high-pass $\Delta\Sigma$ converter, is defined as a block diagram, simulated and optimized using VHDL-AMS. From the high-level simulation, requirements for the individual circuit blocks are derived. Circuits are then designed individually to meet these specifications. Finally, the entire chip is laid out and verified against the original requirements.

The key characteristics of these design styles are as follows.

- Separate design exploration and verification. The combination of greater simulation speed from the use of high-level behavioral models and the ability to perform parametric design make VHDL-AMS simulation appropriate for design exploration. The use of transistor-level simulation becomes more focused on verifying that the blocks match the intent of the high-level design;
- Parametric design at the system-level. VHDL-AMS provides great flexibility in modelling. However, since a fundamental objective of the block-level analysis is to develop specifications for the block implementation, good top-down practice is to write the VHDL-AMS models so that their key performance characteristics are specified using parameters and so can be easily adjusted;
- Mixed-level simulation. In general, it is much faster to verify the functionality and performance of a specific block against its specifications within a VHDL-AMS representation of the system than it is to verify the entire design at the circuit level.

In reality, a final verification of the entire design at the circuit level, in SPICE, is still desirable for verification of connectivity, proper startup, and the performance of critical paths. However, a major objective of most top-down approaches is to eliminate the need to do this more than once. These techniques require substantial attention early in the design process. This is the essential tradeoff of top-down methodologies: more analysis early in design to avoid problems later on.

A critical piece in the design flow is the simulator. It needs to accommodate the different viewpoints we have selected. We use for simulation ADVanceMS from Mentor Graphics [163]. ADVanceMS is a multilingual mixed-signal mixed-mode simulator. It simulates, simultaneously, VHDL-AMS, Verilog-A and SPICE described circuitry, in any combination. ADVanceMS uses the following solvers:

- ModelSim: VHDL, Verilog and C, optional with SDL (Schematic Driven Layout) back-annotation;
- Mach: high speed and high capacity, transistor-level timing and power analysis, including DSPF (Detailed Standard Parasitics File) parasitics;
- Eldo: analogue transistor-level simulation;

- Eldo RF: high capacity and high speed simulator, Harmonic Balance based, for analysis of RF IC circuitry like VCO's, LNA's, mixers, etc. It supports true multi-tone steady-state and noise analysis, including modulated signals;
- ADMS : above mentioned simulators grouped in one including the VHDL-AMS and Verilog-A.

With ADVanceMS, all blocks can have different parallel descriptions from high-level VHDL-AMS abstract representation, to detailed transistor-level. This flexibility of ADVanceMS is useful for the top-down design methodology.

5.4 Component models

Along with the ability to describe multi-abstraction models, the power of VHDL-AMS relies on the fact that it allows us to focus on detailling the constitutive equations of the inner submodels. VHDL-AMS takes advantage of a graph-based conceptual description to automatically compute the equations describing the conservative laws of the global model. The vertices of the graph represent effort nodes (across quantities like voltage) in the circuit, and the edges represent branches of the circuit through which information flows (through quantities like current). Thus, the assembling of complex systems is nothing more than connecting elementary objects through terminals capable of exchanging information, in such a way that the conservative semantics of the generalized Kirchoff laws are preserved. For this reason, instead of presenting complete VHDL-AMS code of complex model, we present how the model is described for each elementary block of the modulator.

Figure 3.15 in Chapter 3 shows block representation of the second-order high-pass $\Delta\Sigma$ modulator. The modulator is split up into high-pass filters, whose transfer function is $\frac{z^{-1}}{1-z^{-1}}$, a quantizer and a DAC. The high-pass filter is the critical block because its nonidealities affect highly the performance of the high-pass modulator and even its stability, as explained in detail in Chapter 3. The high-pass filter is built by switches, capacitors and op-amp as shown in Figure 3.20 of Chapter 3. Figure 5.2 summarizes the various elementary blocks that build the high-pass $\Delta\Sigma$ modulator. The nonidealities degrading the high-pass modulator performance can be implemented separately by including imperfections in the behavioral model of each building block: op-amp, switch, capacitor, quantizer and DAC.

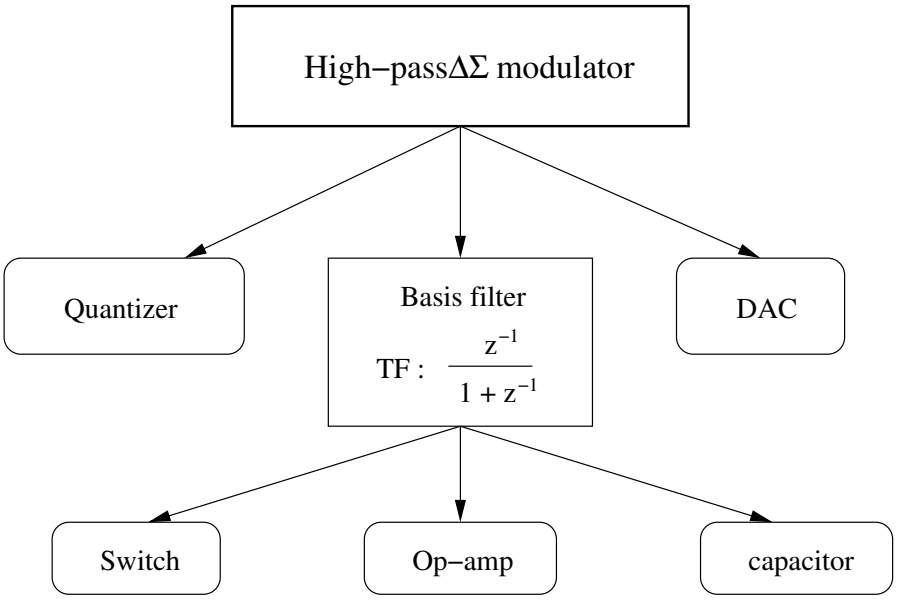


Figure 5.2: Elementary blocks building the high-pass $\Delta\Sigma$ modulator using SC techniques.

The hierarchical representation of VHDL-AMS allows us to select adequate model complexity in order to reduce simulation time. The methodology to model individual blocks is as follows : nonideality parameters of each block are introduced step by step once they have been validated through block simulation. It is obvious that the more complex is the model, the more precise behavior of the component is obtained, but the longer is the needed simulation time. There is therefore a tradeoff to do between the model accuracy and simulation time. Our modelling policy is therefore to develop various versions of each block model from the simplest to the most complex. A nonideality parameter is called "inert" if its effect on the performance of the modulator is negligible. In this case, the introduction of this nonideality parameter in the VHDL-AMS model is not necessary in order to save the simulation time.

5.4.1 Clock Jitter Noise

The operation of a SC circuit depends on complete charge transfer during each of the clock phases [164]. Once the analog signal has been sampled, the SC circuit is a sampled-data system where variations of the clock period has no direct effect on the circuit performance. Therefore, the effect of the clock jitter on a SC circuit is completely described by computing its effect on the input signal sampling.

As in any sampling system, clock jitter in high-pass $\Delta\Sigma$ modulators results in nonuniform sampling and can introduce errors into the sampled values, which increases the total error power at the quantized output. The magnitude of this error depends on both the statistical properties of the jitter and the modulator input signal.

The analysis of jitter begins with the sampling model shown in Figure 5.3. The

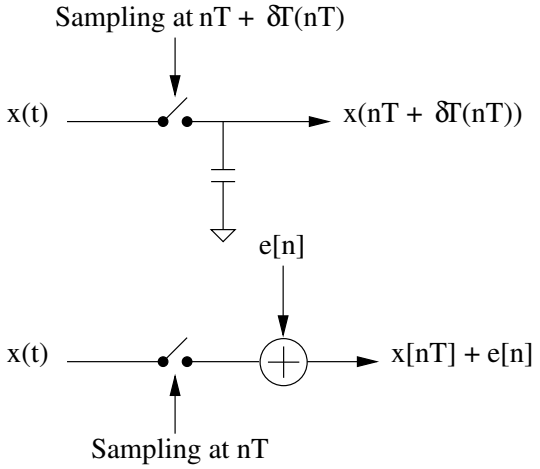


Figure 5.3: Discrete model of the sampling process when the sampling time nT is perturbed by a random process $\delta T(t)$.

input signal, $x(t)$, is assumed to be sampled at $t = nT + \delta T(nT)$, where $\delta T(t)$ is a random process that models the perturbation of the actual sampling instant from the ideal nT. The error that results from jittered sampling, $e[n]$, is defined as

$$e[n] = x(nT + \delta T(nT)) - x(nT). \tag{5.1}$$

Because $\delta T(nT) << T$, (5.1) can be approximated using a first-order Taylor expansion as

$$\begin{aligned} e[n] &\approx x(nT) + \delta T(nT)\, x'(nT) - x(nT) \\ &= \delta T(nT)\, x'(nT), \end{aligned} \tag{5.2}$$

where $x'(nT)$ is the derivative of $x(t)$ at $t = nT$.

Assuming the sampling clock jitter, δT, to be a Gaussian random process with standard deviation, ΔT, and to be white, the sampling clock jitter model is given by equation (5.2). The effect of clock jitter is then simulated at behavioral level by using the model shown in Figure 5.4. The modelling of the clock jitter effect leads to model a white noise source in VHDL-AMS that will be presented in Subsection 5.4.4.

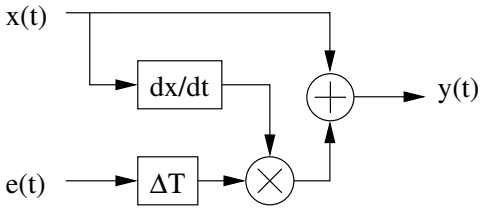


Figure 5.4: Model of a random sampling jitter : x(t) is the input signal, e(t) is white noise with mean value, 0, and standard deviation, 1.

5.4.2 Switch Noise

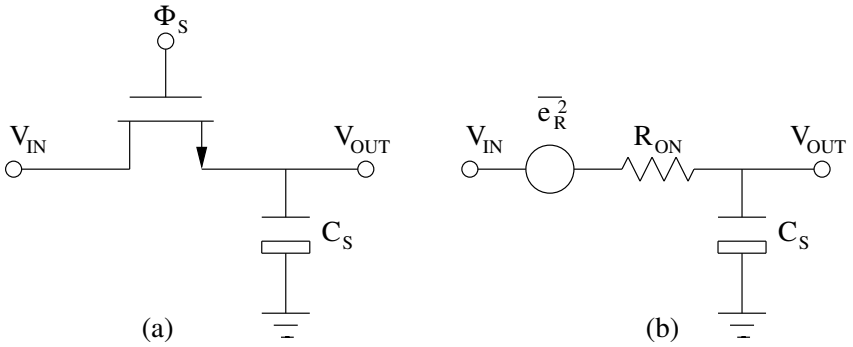


Figure 5.5: (a) MOS S/H, and (b) its equivalent noisy circuit when Φ_S is high.

Two noise sources intrinsic to the MOS switches, namely the thermal noise and flicker noise ($1/f$ noise), can potentially perturb the high-pass filter operation and increase the total error power at the output of the high-pass $\Delta\Sigma$ modulator. Thermal noise is associated with the random motion of carriers in the resistive channel, and $1/f$ noise is associated with flow of direct current in the device. In the analysis of switch noise below, $1/f$ noise is considered negligible because it is assumed that there is no static current flowing through the switched capacitors, and hence, none through the MOS device [165].

The thermal noise contributed by the MOS switches in the high-pass filter can be estimated by modelling each switch with the S/H circuit shown in Figure 5.5. When Φ_S is high and the MOS switch is on, the channel is modelled as a noiseless resistor, R_{ON}, in series with a noise source, e_R, that has a power spectral density

$$S_R(f) = 4kTR_{ON}, \qquad 0 < f < \infty \tag{5.3}$$

where k is Boltzmann's constant and T is the absolute temperature. The power of

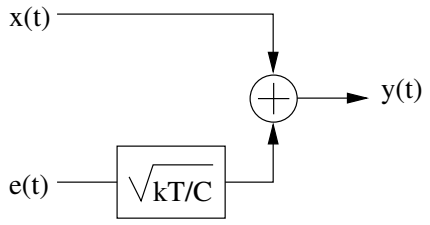


Figure 5.6: Thermal noise model : x(t) is the input signal, e(t) is white noise with mean value, 0, and standard deviation, 1.

the noise sampled onto capacitor C_S is determined by integrating the noise power spectral density, $S_R(f)$, shaped by the transfer function of the low-pass filter formed by R_{ON} and C_S.

$$P_{out} = \int_0^\infty 4kTR_{ON}\frac{df}{1+(2\pi f R_{ON}C_S)^2} = \frac{kT}{C_S}. \tag{5.4}$$

Since the sampling frequency, f_s, is much lower than the circuit bandwidth set by R_{ON} and C_S, it is shown in [102] that the process of sampling the switch noise results in the concentration of the total noise power kT/C_S into the sampling bandwidth, $-f_s/2$ to $f_s/2$. The switch thermal noise is then modelled as an additive white noise source of variance kT/C_S to the input signal as shown in Figure 5.6. Modelling of thermal noise effect, like that of jitter noise, leads therefore to model a white noise source in VHDL-AMS which will be presented in Subsection 5.4.4.

5.4.3 Operational Amplifier Noise

In addition to kT/C noise from the switches and jitter noise, noise from the op-amp also degrades the performance of the modulator. In the following analysis, it is presumed that all noise sources within the amplifier can be referred to a source at the amplifier's non-inverting input, denoted e_{amp} in Figure 5.7. The analysis is simplified by using a non-differential representation of the filter, but no error is inherent in this simplification if e_{amp} is defined to be equal to the input-referred noise of the fully differential amplifier used in the fully differential high-pass filter. Capacitor C_3 is chosen to be $2 \times C_2$ to yield the desired high-pass transfer function, as stated in Section 3.6 of Chapter 3. Capacitor C_1 is unspecified in the following analysis because it affects only the gain of the high-pass filter through the ratio C_1/C_2.

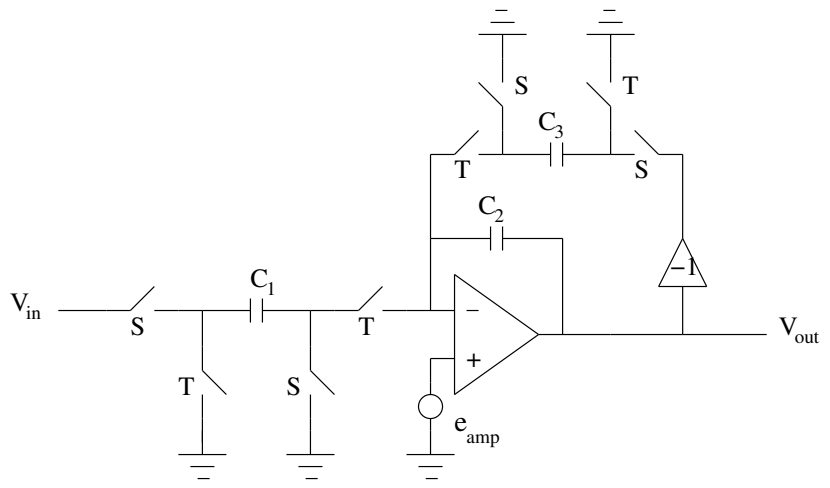


Figure 5.7: Non-differential representation of the high-pass filter with an input, V_{in}, and an input-referred amplifier noise source, e_{amp}.

The input-referred amplifier noise spectral density, $S_{amp}(f)$, typically consists of a white noise component, which is characterized by a power spectral density that is constant with frequency, and a $1/f$ noise component that is inversely proportional to frequency. The effect of $1/f$ noise is studied in detail in Subsection 5.5.1. It will be shown that $1/f$ noise can be neglected because it is concentrated in a narrow region around dc, which even in devices exhibiting high flicker noise levels, only extends into the MHz range [165], whereas the useful signal is centered at one-half of the sampling frequency, $f_s/2$. The input-referred amplifier noise power, P_{amp}, can be evaluated through a transistor-level noise simulation of the complete high-pass filter in the proper clock phase, including feedback, sampling and load capacitors. The modelling of amplifier noise, like that of jitter noise and thermal noise, leads to model a white noise source and $1/f$ noise source in VHDL-AMS, which are presented in Subsections 5.4.4 and 5.4.5.

5.4.4 White Noise Model

As explained above, modelling the thermal noise, jitter noise and op-amp noise leads to generate a white noise source in VHDL-AMS. The Box-Muller method [166, 167] is used to generate a random value chosen from a normal distribution. This method consists of two steps :

- Generating independent random values, $v1$ and $v2$, uniformly distributed over

(0, 1);

- A random value, *vnoise*, of normal distribution is derived from $v1$ and $v2$ by (5.5).

$$vnoise = \sqrt{-2\,ln(v1)}\cos(2\pi v2). \tag{5.5}$$

```
-- white noise model using MullerBox
library disciplines;
library ieee;
use disciplines.electromagnetic_system.all;
use ieee.math_real.all;

entity whitenoise is
generic (
  tau    : time;
  sd1    : integer := 47;      --- prime number
  sd2    : integer := 449          --- prime number
  );
port (terminal vout : electrical);
end entity ;

architecture behave of whitenoise is
quantity vnoise across i through vout to electrical_ground;
signal vn1,vn2 :real:=0.3;
begin
  Detection : process
  variable seed1 : integer := sd1;
  variable seed2 : integer := sd2;
  variable unf : real;
  begin
    wait for tau ;
    uniform(seed1,seed2,unf);
    vn1<= unf;
    uniform(seed1,seed2,unf);
    vn2<= unf;
  end process;
```

```
    vnoise == SQRT(-2.0*Log(vn1)) * cos(math_2_pi*vn2);
end architecture behave;
```

Listing 5.1: White noise generator in VHDL-AMS.

White noise generator in VHDL-AMS is shown in Listing 5.1. To generate a random value uniformly distributed over (0, 1), the function **uniform**, provided by the library **math_real** of ADVanceMS, is used. This function returns a pseudo-random number chosen from a uniform distribution on the interval (0, 1). This function has two parameters *seed*1 and *seed*2. They are optimized such that the generated pseudo white noise has a probability density function (PDF) close enough to the theoretical PDF of a white noise.

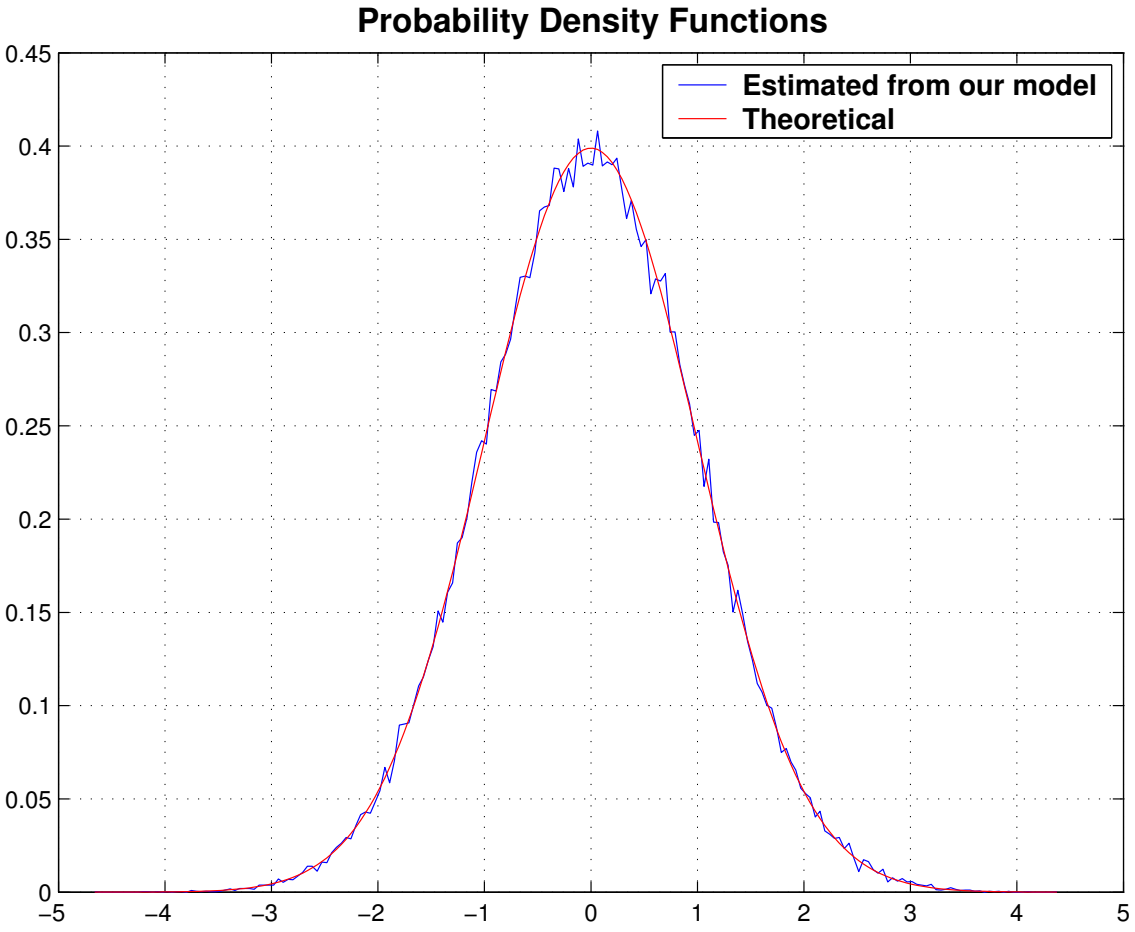


Figure 5.8: The estimated probability density function of our generator in VHDL-AMS (blue) and the theoretical probability density function of white noise (red) with mean value, 0, and standard deviation, 1.

To validate this model, we establish a very simple method to estimate the probability density function of the above mentioned generator output. This PDF estimation method is presented in Appendix B. The estimated PDF of the VHDL-AMS model output and the theoretical PDF of white noise are shown in Figure 5.8. We observe that the former matches well with the latter, it means that the model presented in Listing 5.1 generates a pseudo white noise source.

Simulations show that two parameters *seed*1 and *seed*2 of the **uniform** function must be two big prime numbers in order to have a good matching between the PDF of the generated pseudo white noise and the theoretical PDF of the white noise.

5.4.5 $1/f$ Noise Model

An effective method for generating $1/f$ noise in continuous time consists of summing a few Lorentzian spectra [168, 169]. The summation is expressed as in (5.6) for N spectra in terms of power spectral density as a function of frequency.

$$S(f) = \kappa \sum_{n=1}^{N} \frac{\varphi_n}{f^2 + \varphi_n^2} \approx \frac{\kappa}{f} \qquad \text{for } \varphi_1 < f < \varphi_n. \tag{5.6}$$

The Lorentzian spectrum can be created by filtering white noise with a single-pole low-pass filter. Equation (5.7) shows the magnitude response $H(j\omega)$ of a single-pole low-pass filter.

$$H(j\omega) = \frac{2\pi\sqrt{\varphi_i}}{j\omega + 2\pi\,\varphi_i}. \tag{5.7}$$

The power spectral density when white noise of variance κ is filtered, is then

$$S(f) = \kappa\,|H(f)|^2 = \frac{\varphi_i\,\kappa}{f^2 + \varphi_i^2}. \tag{5.8}$$

Therefore, to generate $1/f$ noise in VHDL-AMS, independent pseudo white noises with variance of κ generated by white noise model presented in Subsection 5.4.4, are filtered by parallel low-pass filters derived from 5.8. Pole placements are chosen with equal spacing in the log frequency domain, with a density of more than 1 pole per decade. A single-pole low-pass filter is implemented in VHDL-AMS through time domain equation.

$$\varphi\, v_{out} + \frac{1}{2\pi}\frac{dv_{out}}{dt} = \sqrt{\varphi} v_{in}. \tag{5.9}$$

This equation is simply implemented in VHDL-AMS as

$$\boxed{\varphi_i\,\mathrm{v_{out}} + \frac{1}{2\pi}\,\mathrm{v_{out}}\text{'dot} == \mathrm{sqrt}(\varphi_i)\ \mathrm{v_{in}}}$$

In order to generate independent white noise at the input of the parallel low-pass filters, each pair of parameters *seed*1 and *seed*2 must be different for each generated white noise source.

5.4.6 Switch Model

A switch can be simply modelled by a variable resistance depending on switch state which is equal to a small resistance, R_{on}, or a big resistance, R_{off}, representing the on-resistance or off-resistance of the switch respectively. In order to increase the convergence speed, the effective switch resistance is set to be continuous using in addition two parameters tr and tf as shown in Listing 5.2. These parameters present respectively the rising time and falling time of the effective switch resistance.

```
library disciplines;
use disciplines.electromagnetic_system.all;

entity sw is
  generic (
    ron  : real := 1.0E2;
    roff : real := 1.0E12;
    tr   : real := 1.0E-9;
    tf   : real := 1.0E-9
  );
  port (
    terminal p : electrical;
    terminal m : electrical;
    signal   h : in bit
  );
end entity sw;

architecture simple of sw is
  quantity v across i through p to m;
  signal  reff : real := roff;
begin
  P1 : process
  begin
```

```
    if h = '1' then
      reff <= ron;
    else
      reff <= roff;
    end if;
    wait on h;
  end process;
  i == v / reff'ramp(tr, tf);
end architecture simple;
```

Listing 5.2: Simple model of switch in VHDL-AMS where only on-resistance and off-resistance are taken into account.

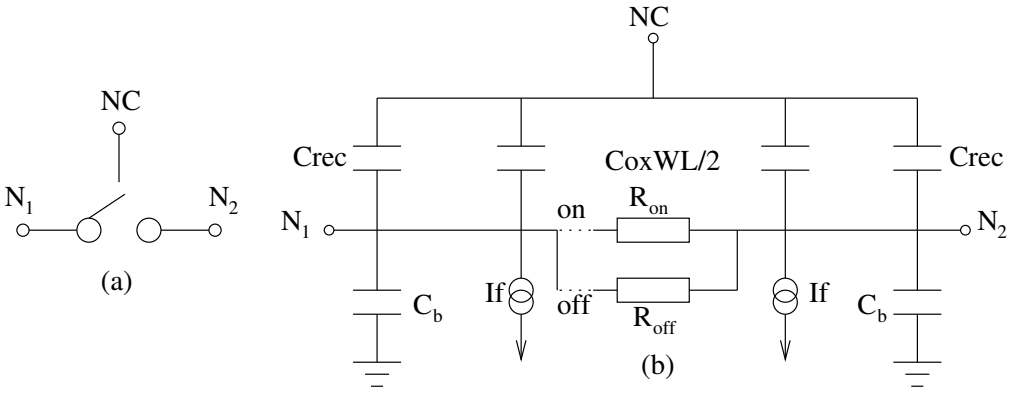


Figure 5.9: Switch model.

Nonideality parameters such as parasitic capacitances and leakage current may be added to build a very efficient behavioral model as presented in Figure 5.9. C_b can be considered as the input and output capacitor of the switch, and C_{rec} represents capacitance due to the overlap of gate poly with the source and drain area. Two current sources represent the leakage current from source-body and drain-body junctions. This model in VHDL-AMS is presented in Appendix B (Listing B.1). The exact modelling of the charge transfer is a difficult issue because it concerns load condition of drain and source in the transistor and clock waveforms. However, it is shown that this model is very efficient in transient analysis, provided that load capacitance area is 50 times greater than the product $W \times L$ of the transistors [170].

To validate this model, a S/H circuit with 1pF load capacitor is simulated in VHDL-AMS and Eldo transistor-level. The curve in black is the output of S/H using

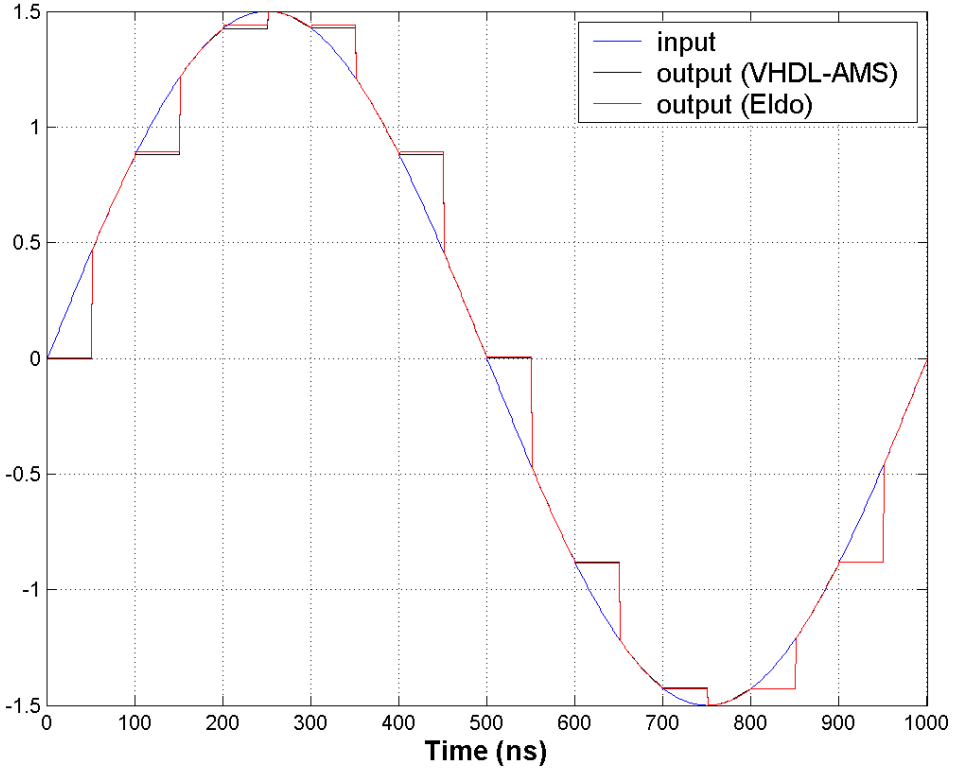


Figure 5.10: Sinusoidal input of a S/H (blue), Its output with the model of switch in VHDL-AMS (black) and Its output with Eldo transistor-level (red).

the switch and capacitor models in VHDL-AMS. The curve in red is the output of S/H using Eldo transistor-level. Two curves match almost completely each other.

5.4.7 Operational Amplifier Model

The op-amp is a major component in the high-pass filter, the key building block of high-pass modulator. The performance of the modulator depends mainly on the key op-amp parameters such as slew-rate, finite static gain, bandwidth, and saturation. These parameters are introduced one by one in the VHDL-AMS model of the op-amp in order to study their effect on the stability and the performance of the high-pass $\Delta\Sigma$ modulator.

A very simple model of amplifier is shown in Listing 5.3. In this model, the current is not taken into account, the output voltage is simply the input voltage multiplied by a gain and then limited by saturation. The amplifier gain is represented by parameter *gain* and amplifier saturations are accomplished by limiting the output voltage to two threshold values *vmax* and *vmin* as shown in Listing 5.3.

```
--- simple model of operational amplifier
library disciplines, ieee;
use disciplines.electromagnetic_system.all;
use ieee.math_real.all;

entity op_amp is
generic(
    gain : real := 100.0; -- static gain of op-amp
    vmin : real := 0.0;   -- minimal output voltage
    vmax : real := 3.3    -- maximal output voltage
  );
port (terminal vout, vp, vn: electrical);
end entity op_amp;

architecture simple of op_amp is
  quantity vs across iout through vout to electrical_ground;
  quantity vepsilon across vp to vn;
  quantity v : real;
begin
```

```
  v == gain * vepsilon;
  if v'Above(vmax) use              -- if v > vmax
    vs == vmax;
  elsif not v'Above(vmin) use       -- if v < vmin
    vs == vmin;
  else
    vs == v;
  end use;
  break on v'Above(vmax), v'Above(vmin);
end simple;
```

Listing 5.3: Simple model of op-amp in VHDL-AMS where only static gain and saturation are taken into account.

Being just the simple base of the amplifier model, the model presented in Listing 5.3 must see the finite bandwidth, or product gain-bandwidth, and especially the slew-rate to be introduced into. Coding these nonideality parameters in VHDL-AMS is not a difficult task, but the way they are described, is important.

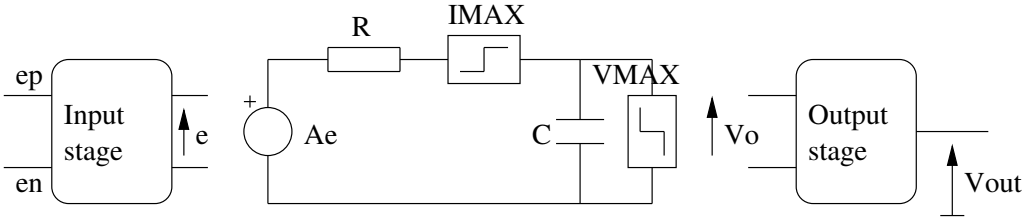


Figure 5.11: Operational amplifier model.

Figure 5.11 shows a more complete model of the op-amp. This is a one pole differential or single-stage dynamic behavioral model. The model makes it possible to specify finite input and output impedances through the input and output stages, the finite gain, finite gain-bandwidth product, slew-rate and saturation. The finite gain is defined through parameter A. The finite bandwidth is specified through an R-C network. The slew-rate and saturation are accomplished by limiting the output current to $Imax$ and the output voltage to $Vmax$, respectively. The basic equations used to transform the given specifications into internal equations in the model are given by: the -3dB cut-off frequency, f_c is defined as $1/(2\pi RC)$. If R is set to 1Ω, then we have $C = 1/(2\pi f_c)$. The output current threshold is then given by $Imax = SR/(2\pi f_c)$ where SR defines the slew-rate of the op-amp.

Figure 5.12 presents the frequency response of a modelled amplifier with 75dB gain, 165 MHz transition frequency, 10 V/μs slew-rate, and -0.1V and +0.1V positive and negative saturation potential to supply voltages .

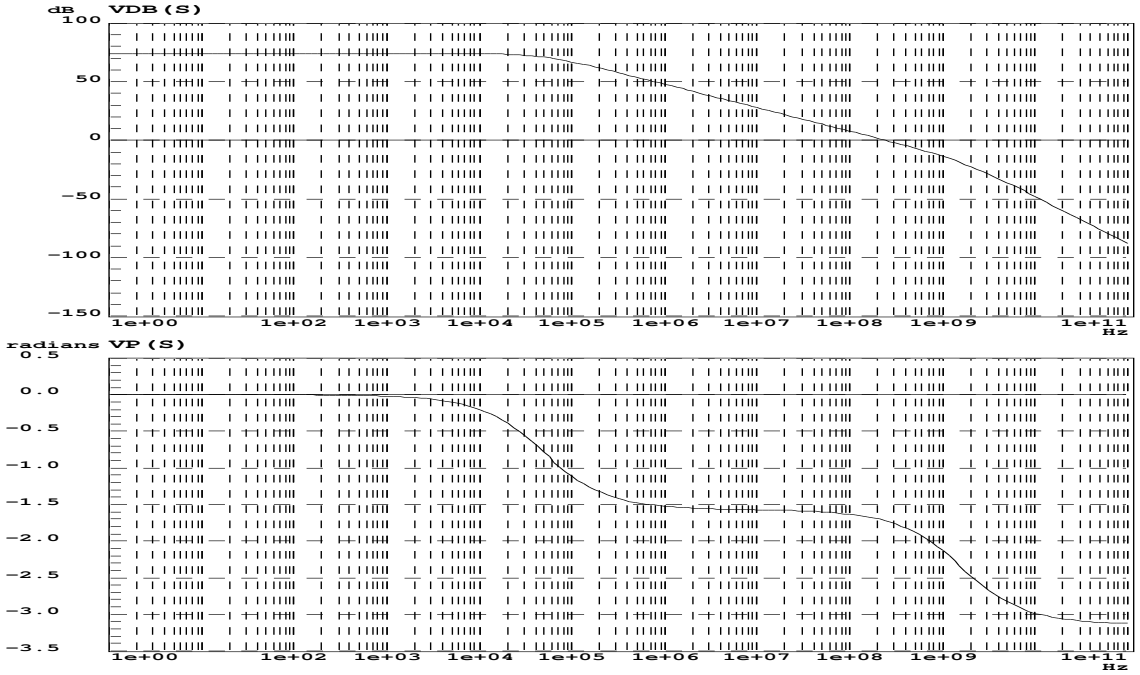


Figure 5.12: Operational amplifier response

An even more complete model is presented in [171]. This model is developed by M. Jean-Baptise KAMMERER in the Top Behave'sModel'02 contest. In this model, convergence speed is improved and the modelling of various nonideality parameters such as static gain, gain-bandwidth product, saturation and especially slew-rate, are validated [171]. This is a quite complete model which is used as our most complex model of op-amp in the simulation of $\Delta\Sigma$ modulator. The modelled parameters of the op-amp are summarized as

- Differential gain;
- -3dB cut-off frequency;
- Common-mode gain;
- Common-mode and differential input inpedances;

- Output impedances;
- Slew-rate;
- Saturation.

It is easy to insert in this model common and supply tension effect by adding the same number of source generator without modifying the other elements. To simplify analysis and reduce the simulation time, only unipolar structure is used. The dynamic behavioral model of symmetrical structure can be built easily by combining the two unipolar behavioral models corresponding in order to keep only one input stage circuit and two output stage circuits working in phase.

5.4.8 Complete Filter Model

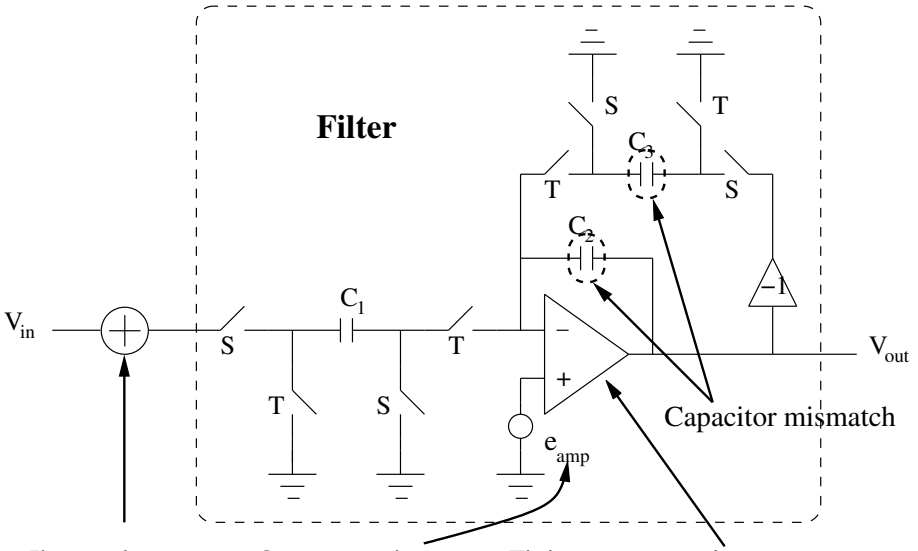


Figure 5.13: Circuit nonidealities of the high-pass filter building the high-pass $\Delta\Sigma$ modulator.

Circuit nonidealities of the high-pass filter are summarized in Figure 5.14. In the second-order high-pass $\Delta\Sigma$ modulator, as in the low-pass one, the first high-pass filter is the most sensitive component in the modulator. Therefore, all nonidealities

are included in the first high-pass filter model. Initially, all nonidealities are also applied to the second high-pass filter model. Then, some nonidealities are removed from the second high-pass filter model, if the performance of the modulator is not changed.

5.4.9 Comparator

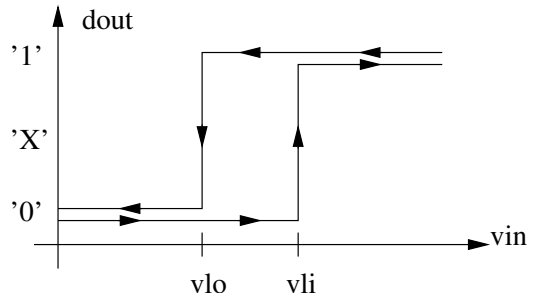


Figure 5.14: Comparator with hysteresis.

Single-bit architectures incorporate a simple comparator to perform the internal quantization. A simple DAC is then used in the feedback loop, which does not introduce any non-linearity error. An ideal behavioral model of comparator is sufficient because the impact of comparator nonlinearities is negligible compared with those of the amplifier. A more complete version of a comparator, that includes hysteresis and an unknown state of the outputs if the input remains in the transition region for more than a specified time, can be implemented using a finite state machine. It is a typical example taken for mixed-signal modelling in VHDL-AMS [156]. The finite state machine of such a comparator is shown in Figure 5.15. VHDL-AMS code of this model is illustrated in Appendix B (Listing B.2).

5.5 Simulation Results

Before studying the effect of nonidealities on the stability and performance of the high-pass $\Delta\Sigma$ modulator, it is necessary to validate the proposed set of models as a whole even if each individual block has been validated. In order to do this, we perform several simulations on the second-order low-pass modulator presented in Figure 3.7 of in Chapter 3. The obtained result is completely as expected and com-

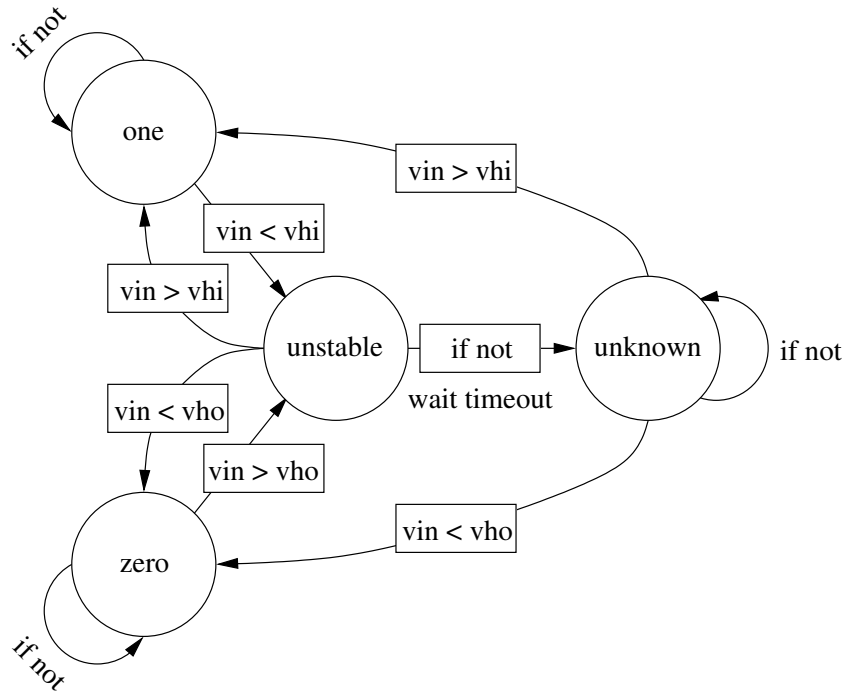


Figure 5.15: State diagram of comparator with hysteresis.

patible with result from MATLAB-SIMULINK modelling. The thermal noise, jitter noise and amplifier noise increase the inband noise floor which degrades the SNR of the low-pass modulator. The $1/f$ noise goes through the low-pass modulator, and degrades significantly the low-pass modulator performance. The finite bandwidth and slew-rate of the amplifier lead to harmonic distortion which degrades the SNDR of the low-pass modulator. The effect of the op-amp saturation depends on the saturation voltage relative to full-scale voltage, and amplitude of the input signal. For example, with a full-scale voltage of 1V, a saturation voltage of 1.5V does not degrade the modulator performance significantly, while for a saturation voltage of 1V, a significant degradation occurs for input signal amplitude larger than 0.25V. The complete simulation results, the effect of different nonidealities, specification on the elementary blocks of the high-pass second-order $\Delta\Sigma$ modulator are presented hereafter. The simulation parameters used are summarized in Table 5.2.

5.5.1 Noise Effect

As expected, thermal noise, jitter noise and amplifier noise increase the inband noise floor, as shown in Figure 5.16, which degrades the modulator performance. Unlike

Parameter	Value
Signal bandwidth	156.25 KHz
Sampling frequency	10 MHz
Oversampling ratio	32
Samples number	45000
Filter gain (C_1/C_2)	0.5
Reference voltages	$\pm$1V

Table 5.2: Simulation parameters.

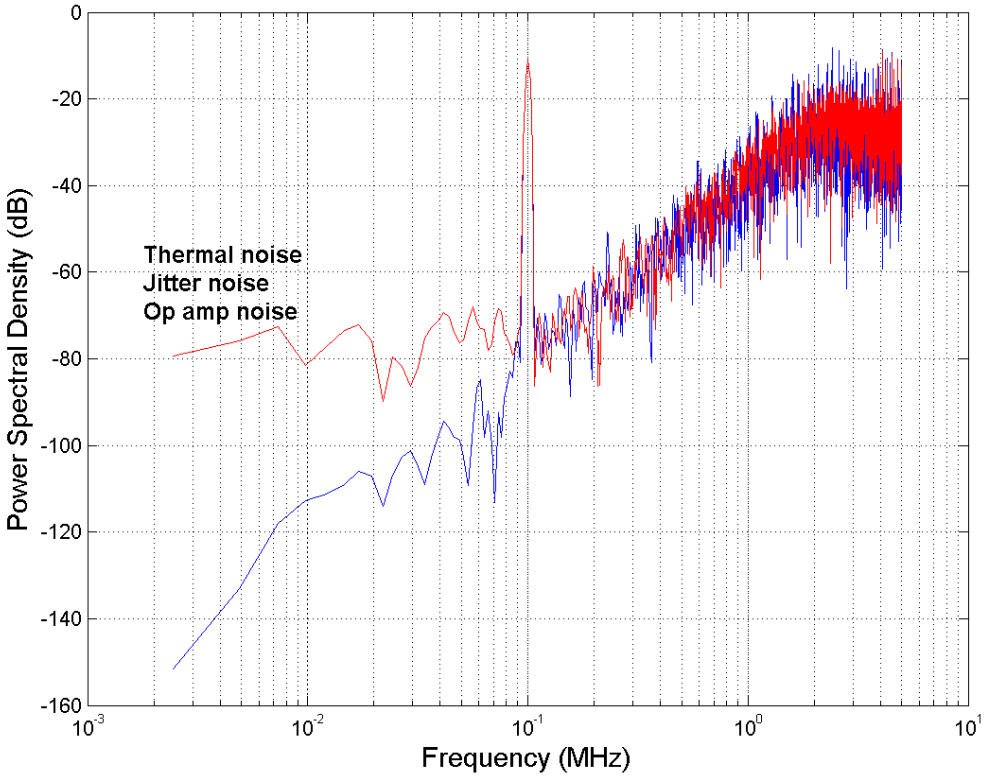


Figure 5.16: Power spectral density of chopper stabilized second-order $\Delta\Sigma$ modulator with an ideal modulator and thermal noise, jitter noise and op-amp noise models.

the effect of amplifier noise in the low-pass modulator, the amplifier noise is amplified at the high-pass modulator output. The inband noise generated by amplifier noise at the modulator output is about 15 dB higher than the input-referred amplifier noise. This increased noise at the modulator output is analyzed as follows:

The influence of the amplifier noise on the performance of the high-pass filter is gained by examining the terms involving e_{amp} in the time domain difference equation that describes the filter:

$$\begin{aligned} V_{out}[n] + V_{out}[n-1] &= \tfrac{C_1}{C_2} V_{in}[n-1] \\ &+ \left(2 + \tfrac{C_1}{C_2}\right) e_{amp}\left[n - \tfrac{1}{2}\right] + e_{amp}[n] - e_{amp}[n-1] \end{aligned} \tag{5.10}$$

Therefore, in the presence of op-amp noise and when $C_1/C_2 = 0.5$, the z-domain transfer function of the high-pass filter is given by

$$V_{out}(z) = 0.5\,\frac{z^{-1}}{1+z^{-1}} V_{in}(z) + \frac{1 + 2.5\,z^{-1/2} - z^{-1}}{1+z^{-1}} E_{amp}(z). \tag{5.11}$$

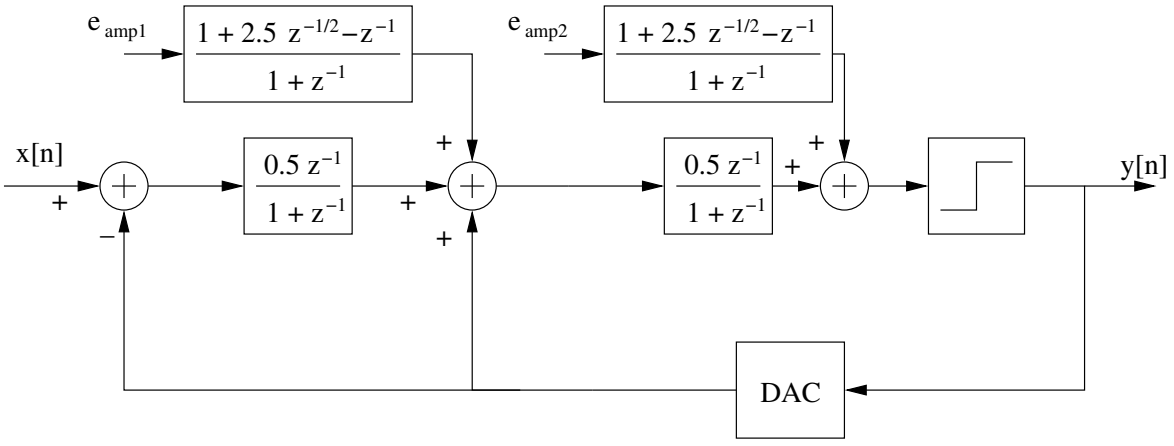


Figure 5.17: Schema block of high-pass second-order $\Delta\Sigma$ modulator in the presence of op-amp noise.

The effect of amplifier noise in the high-pass modulator is then analyzed with two independent amplifier noise sources, e_{amp1} and e_{amp2}, as shown in the block diagram of the noisy second-order high-pass $\Delta\Sigma$ modulator of Figure 5.17. If the quantizer is modelled as a gain, G, with an additive noise source, $E(z)$, the output of the high-pass modulator is described in the z-domain by

$$Y(z) = S(z)X(z) + N(z)E(z) + N_{amp1}(z)E_{amp1}(z) + N_{amp2}(z)E_{amp2}(z), \tag{5.12}$$

where signal, quantization noise transfer functions, and noise transfer functions for e_{amp1} and e_{amp2} are respectively

$$S(z) = \frac{0.25\,Gz^{-2}}{1+(2-0.5\,G)z^{-1}+(1-0.25\,G)z^{-2}}, \tag{5.13}$$

$$N(z) = \frac{(1+z^{-1})^2}{1+(2-0.5\,G)z^{-1}+(1-0.25\,G)z^{-2}}, \tag{5.14}$$

$$N_{amp1}(z) = \frac{0.5\,G\,z^{-1}\left(1+2.5\,z^{-1/2}-z^{-1}\right)}{1+(2-0.5\,G)z^{-1}+(1-0.25\,G)z^{-2}} \tag{5.15}$$

and

$$N_{amp2}(z) = \frac{G\,(1+z^{-1})\left(1+2.5\,z^{-1/2}-z^{-1}\right)}{1+(2-0.5\,G)z^{-1}+(1-0.25\,G)z^{-2}}. \tag{5.16}$$

Behavioral simulation shows that if the gain of the quantizer, G, is set to 4, then the quantization noise in the signal band is accurately estimated by (5.14), and the signal and quantization noise transfer functions find themselves the expression in (3.26) of Chapter 3, i.e. $S(z) = z^{-2}$ and $N(z) = (1+z^{-1})^2$. In this case, noise transfer functions for e_{amp1} and e_{amp2} can be simplified as

$$N_{amp1}(z) = 2\,z^{-1}\left(1+2.5\,z^{-1/2}-z^{-1}\right) \tag{5.17}$$

and

$$N_{amp2}(z) = 4\,\left(1+z^{-1}\right)\left(1+2.5\,z^{-1/2}-z^{-1}\right), \tag{5.18}$$

which, in the frequency domain, can be written as

$$\begin{aligned} N_{amp1}(f) &= N_{amp1}(z)|_{z=e^{j2\pi fT_s}} \\ &= 2e^{-j2\pi fT_s}\left(1+2.5e^{-j\pi fT_s}-e^{-j2\pi fT_s}\right) \end{aligned} \tag{5.19}$$

and

$$\begin{aligned} N_{amp2}(f) &= N_{amp1}(z)|_{z=e^{j2\pi fT_s}} \\ &= 4\left(1+e^{-j2\pi fT_s}\right)\left(1+2.5e^{-j\pi fT_s}-e^{-j2\pi fT_s}\right) \end{aligned} \tag{5.20}$$

where T_s is the sampling period. If P_{amp1} and P_{amp2} are the input-referred noise power of the first-stage amplifier and second-stage amplifier, then the spectral density of the shaped noises from e_{amp1} and e_{amp2} are respectively

$$S_{amp1,out} = |N_{amp1}(f)|^2\,\frac{P_{amp1}}{f_s}, \qquad -\frac{f_s}{2} < f < \frac{f_s}{2}., \tag{5.21}$$

and

$$S_{amp2,out} = |N_{amp2}(f)|^2\,\frac{P_{amp2}}{f_s}, \qquad -\frac{f_s}{2} < f < \frac{f_s}{2}. \tag{5.22}$$

We note that the signal passband is centered at $f_s/2$, and the passband bandwidth is assumed to be much less than f_s. Therefore, in the passband, the spectral density of the shaped noise from e_{amp1} and e_{amp2} can be approximated as

$$\begin{aligned} S_{amp1,inband}(f) &\approx S_{amp1,out}(f)|_{f=f_s/2} \\ &= |N_{amp1}(f)|^2_{f=f_s/2} \frac{P_{amp1}}{f_s} \\ &= 41 \times \frac{P_{amp1}}{f_s} \end{aligned} \tag{5.23}$$

and

$$\begin{aligned} S_{amp2,inband}(f) &\approx S_{amp2,out}(f)|_{f=f_s/2} \\ &= |N_{amp1}(f)|^2_{f=f_s/2} \frac{P_{amp2}}{f_s} \\ &= 0 \times \frac{P_{amp2}}{f_s} = 0. \end{aligned} \tag{5.24}$$

The important and disturbing implication of (5.23) is that within the passband, noise power from the first-stage amplifier is amplified by a factor of 41 at the output of the modulator. Fortunately, (5.24) indicates that the inband noise contribution from the second-stage amplifier is negligible because the noise shaping function $N_{amp2}(f)$ has a zero at $f_s/2$. The power of the amplifier noise present in the signal band, $P_{amp,inband}$, is calculated as

$$P_{amp,inband} = \int_{inband} (S_{amp1,inband}(f) + S_{amp2,inband}(f))\, df. \tag{5.25}$$

From (5.23) and (5.24), $P_{amp,inband}$ is approximately

$$\begin{aligned} P_{amp,inband} &\approx [S_{amp1,inband}(f) + S_{amp2,inband}(f)] \times B \\ &\approx 41 \times \frac{P_{amp1}}{f_s} \times B \\ &= 41 \times \frac{P_{amp1}}{OSR}, \end{aligned} \tag{5.26}$$

where B is signal bandwidth and OSR is oversampling ratio. Equation (5.26) reveals that the inband noise generated from the op-amp noise is increased by a factor of 41. This explains the increased inband noise floor generated by the op-amp noise in the simulation.

$1/f$ noise has completely no effect on the modulator performance, because the $1/f$ is drowned in the quantization noise which is shaped to low frequency region, whereas the useful signal is centered at one-half of the sampling frequency, $f_s/2$. For the same reason, the modulator performance is also insensitive to the offset of the high-pass filter generated from switches and amplifier, and comparator offset. Ideal SNR of high-pass modulator is about 57dB with 0.5V amplitude of the sinusoidal input. Table 5.3 presents the threshold of parameters representing jitter noise, switch

noise and amplifier noise so that in the presence of these noises, the modulator performance degradation is not significant: the total SNR of the modulator is set to be almost unchanged when each of these noises is introduced into the modulator model.

Type of noise	Parameter	Value
Jitter noise	ΔT	< 0.1ns
Switch noise	C	$>$10 fF
Amplifier noise	E_{amp}	$< 0.2\text{m}V_{rms}$

Table 5.3: Threshold of parameters representing jitter noise, switch noise and amplifier noise.

5.5.2 Nonideality Effect

As in low-pass modulator, the comparator nonideality effect is really negligible in the high-pass modulator. Simulation shows that the capacitor mismatch and the amplifier nonidealities, such as static gain, slew-rate and bandwidth are critical parameters of the modulator performance. Other parameters that should be considered are on-resistance, parasitic capacitance, and current leakage of the switch.

Switch Nonideality Effect

Switch nonidealities are represented by the off-resistance, R_{off}, on-resistance, R_{on}, parasitic capacitances, and leakage current. The first parameter studied is R_{off}. Simulations show that its effect is really negligible when it is higher than 10 MΩ. In fact, the off-resistance of a MOS switch is much higher than that value. This parameter is therefore considered inert. The effect of the switch on-resistance is more important. Table 5.4 shows SNDR performance of the modulator in function of the R_{on} value. We observe from simulations that a high value of the on-resistance increases the inband noise floor. Harmonic distortion becomes clearly when the on-resistance is more than 3KΩ. In order to ensure a small degradation of the modulator performance, the on-resistance is chosen to be smaller than 1kΩ.

Parasitic capacitances ($Crec$ and $WLCox$) increase also the inband noise floor,

$R_{on}(\Omega)$	100	500	1000	1500	2000	3000
SNDR	56.3	56.1	54.8	54.1	53.3	52.1

Table 5.4: High-pass modulator SNDR performance versus the on-resistance of the switch.

degrade thus the SNR performance of the modulator. Simulations show that if the overall parasitic capacitance is smaller than 30fF, this degradation is negligible. But when the parasitic capacitance of switch is superior to 50fF, the inband noise floor is completely dominated by its effect. The current leakage effect is negligible when it is weaker than 0.1μA which is much higher than the current leakage in a MOS transistor. This parameter is therefore considered inert. In the presence of the parasitic capacitances, the simulation time is about four times longer than it is when only switch on-resistance is taken into account. In order to save the simulation time, in simulations studying the amplifier nonideality effect, the simple model of switch, where only switch on-resistance is considered, is used.

Amplifier Nonideality Effect

As in low-pass modulator, the finite bandwidth and slew-rate of the amplifier lead to harmonic distortion, thus degrading the SNDR performance of the high-pass modulator. Table 5.5 presents the low-pass modulator SNDR performance versus the static gain and the slew-rate of the amplifier while the transition frequency of the amplifier is 20 times higher than the sampling frequency and a sinusoidal input signal of 15 KHz frequency and 0.5V amplitude is used.

Slew-rate (V/μs)	Gain (dB)		
	50	60	70
0.1	38.9	37.7	39.1
1	54.6	55.4	55.6
10	55.2	55.7	56

Table 5.5: Low-pass modulator SNDR performance versus the static gain and the slew-rate of the amplifier.

In the same simulation conditions, the SNDR performance of the high-pass mod-

ulator is shown in Table 5.6. The gain and slew-rate performance is more required in the high-pass modulator to remain its performance. Moreover, the slew-rate of the amplifier influences the modulator stability. Indeed, the slew-rate must be higher than 5V/μs to retain the modulator stable. This effect is specific to the high-pass modulator and due to the implementation method of the high-pass filter. In order

Slew-rate (V/μs)	Gain (dB)		
	50	60	70
1	x	x	x
5	38.6	39.2	41.4
10	43.8	45.6	47.4
50	53.1	55.3	55.5

Table 5.6: High-pass modulator SNDR performance versus the static gain and the slew-rate of the amplifier. "x" means that the modulator is unstable.

to reduce the degradation of the modulator performance due to slew-rate and finite gain of the amplifier, the slew-rate should be higher than 50V/μs and the amplifier gain should be above 60dB.

Amplifier bandwidth is also more required in the high-pass modulator in comparison with the low-pass one. While in the low-pass modulator case, the transition frequency should be just a few times higher than the sampling frequency to ensure the right operation of the low-pass modulator, in the high-pass modulator, the transition frequency of the amplifier must be much higher than the sampling frequency. Table 5.7 shows SNDR performance of the high-pass modulator versus the transition frequency of the amplifier, while the gain and especially the slew-rate of the amplifier are assumed be to high enough. In these simulations, amplifier gain and slew-rate are set to 70dB and 50V/μs, respectively.

f_t/f_s	9	10	12	14	16	18	20
SNDR	47.3	49.6	51.5	53.9	54.7	55.1	55.5

Table 5.7: High-pass modulator SNDR performance versus the transition frequency to sampling frequency ratio.

As in low-pass modulator, the effect of the op-amp saturation depends on the

saturation voltage relative to full-scale voltage, and amplitude of the input signal. When the reference voltage is set to 1V, a saturation voltage of 1.4V does not degrade the modulator performance significantly, while for a saturation voltage of 1V, a significant degradation occurs for input signal amplitude larger than 0.26V.

Capacitor mismatch

The capacitor ratio C_3/C_2 must be equal to 2 in order to ensure the right operation of the high-pass filter. Moreover, the modulator stability is sensitive to the capacitor mismatch. The simulation with VHDL-AMS confirms the result obtained in Chapter 3, that is the high-pass modulator remains stable if the capacitor mismatch is smaller than 2.4%. Table 5.8 shows SNDR performance of the high-pass modulator versus the capacitor mismatch. When the capacitor mismatch is inferior to 0.5%, the degradation of the modulator performance is really negligible. This parameter can be therefore considered inert if this requirement is satisfied.

Capacitor mismatch (%)	0.01	0.1	0.25	0.5	0.6	0.7	0.8
SNDR	55.7	55.5	55.1	54.8	54.2	53.7	53.1

Table 5.8: High-pass $\Delta\Sigma$ modulator SNDR performance versus capacitor mismatch.

5.5.3 Block Specification Summary

Elementary block specifications can be summarized in Table 5.9.

Figure 5.18 shows the SNDR performance of the high-pass modulator as a function of the input signal amplitude when all of the nonidealities are taken into account and their value is the threshold value presenting in Table 5.9.

5.6 Conclusion

In this Chapter, we have presented a top-down methodology design with VHDL-AMS. A set of models in VHDL-AMS suitable for time domain behavioral simulation of SC $\Delta\Sigma$ modulators have been developed. The proposed set of models takes

Nonideality	Parameter	Threshold value
Sampling jitter	ΔT	$<$ 0.1ns
Switch (kT/C) noise	C	$>$ 10fF
Amplifier noise	E_{amp}	$<$ 0.2mV_{rms}
Switch on-resistance	Ron	$<$ 1KΩ
Parasitic switch capacitance	Crec + WLCox	$<$ 30fF
Leakage current	Ifd	$<$ 0.1 μA
Finite gain	$Gain$	$>$ 60 dB
Transition frequency	f_t	$>$ 160 MHz
Slew-rate	SR	$>$ 50V/μs
Saturation	Vmax	$>$ 1.4V
Capacitor mismatch		$<$ 0.5%

Table 5.9: Specification summary.

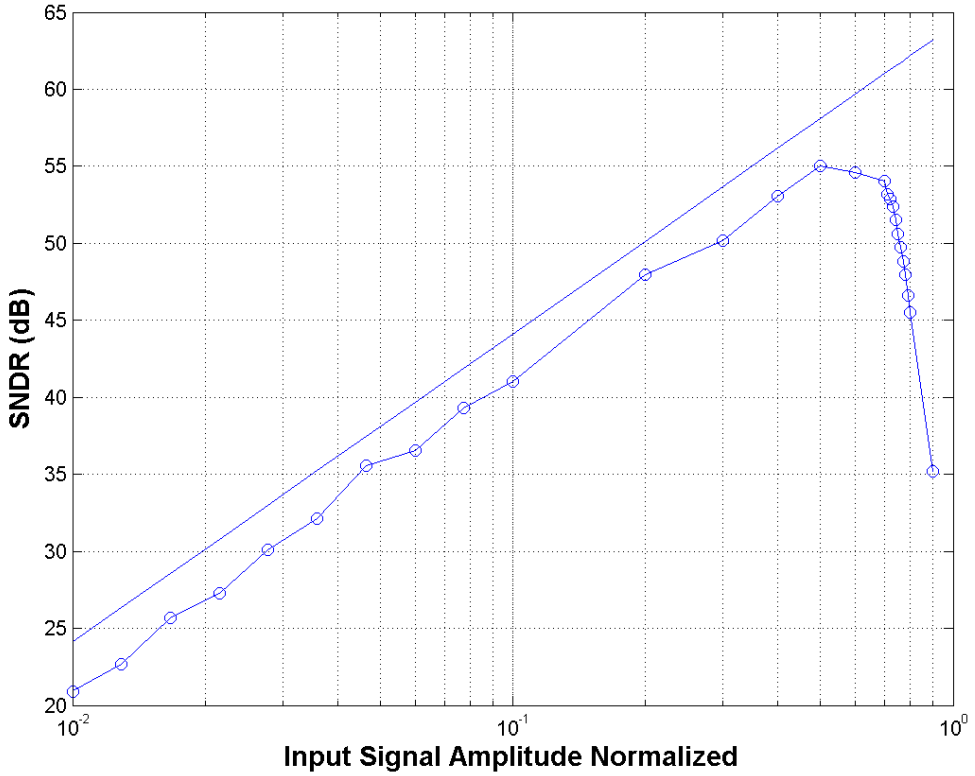


Figure 5.18: SNDR performance of the high-pass modulator versus the input signal amplitude resulting from simulation in consideration of all of the nonidealities.

into account at the behavior level most of SC $\Delta\Sigma$ modulator nonidealities, such as jitter noise, kT/C noise, $1/f$ noise, amplifier noise, switch nonidealities, amplifier nonidealities, and capacitor mismatch. This allows us to study the effect of various nonideality parameters on the high-pass $\Delta\Sigma$ modulator performance, and define the threshold set of nonideality parameters value ensuring a desired performance of the modulator. This methodology allows us not only to make a specification of each elementary device of the $\Delta\Sigma$ modulator and estimate its performance, but also to optimize various nonideality parameters to obtain a good performance of the modulator. This is really useful for high-pass $\Delta\Sigma$ modulator design, because unlike the low-pass modulator, a major problem of the high-pass modulator with the implementation of the high-pass filter we proposed, is the stability and amplified noise of the amplifier noise at the output of the modulator.

Chapter 6

Implementation

6.1 Introduction

This chapter describes the design and implementation of an high-pass second-order $\Delta\Sigma$ modulator and a time-interleaved $\Delta\Sigma$ converter using two high-pass second-order $\Delta\Sigma$ modulators. The objective of this design is to demonstrate the feasibility of implementing a high-pass $\Delta\Sigma$ modulator and the advantages of this kind of modulator. For this experience, the second-order architecture is designed to simplify the analysis and the design. Higher-order modulator using cascaded structure can be designed in the same procedure. The experimental modulator has been integrated in a 0.35μm, double-poly, quadruple-metal CMOS technology of AustriaMicroSystems (AMS)[172]. This technology includes a high-density, linear capacitor option such as double-poly or poly-diffusion capacitors and also high-density resistance which follows to design high value resistance with small area. The sampling frequency of the modulator is 10 MHz, and the passband bandwidth is more than 150KHz, equivalent to an OSR of 32. The expected SNR of the second-order high-pass $\Delta\Sigma$ modulator is 52 dB. Its power dissipation simulated is 42.44 mW, and the total power dissipation of the prototype is 127.5 mW, when the modulator is operated from a 3.3V supply.

The design of the high-pass $\Delta\Sigma$ modulator is an important part of the work knowing that the parallel converter is made by putting two high-pass $\Delta\Sigma$ modulators in parallel.

Elementary blocks of the modulator are designed by using the OCEANE software (Outils pour la Conception et l'Enseignement des circuits integres ANalogiquEs)

[173] developed by ENST to design and synthesize fundamental analog blocks, such as op-amp, clock generator, filter.

6.2 Switched-Capacitor High-Filter

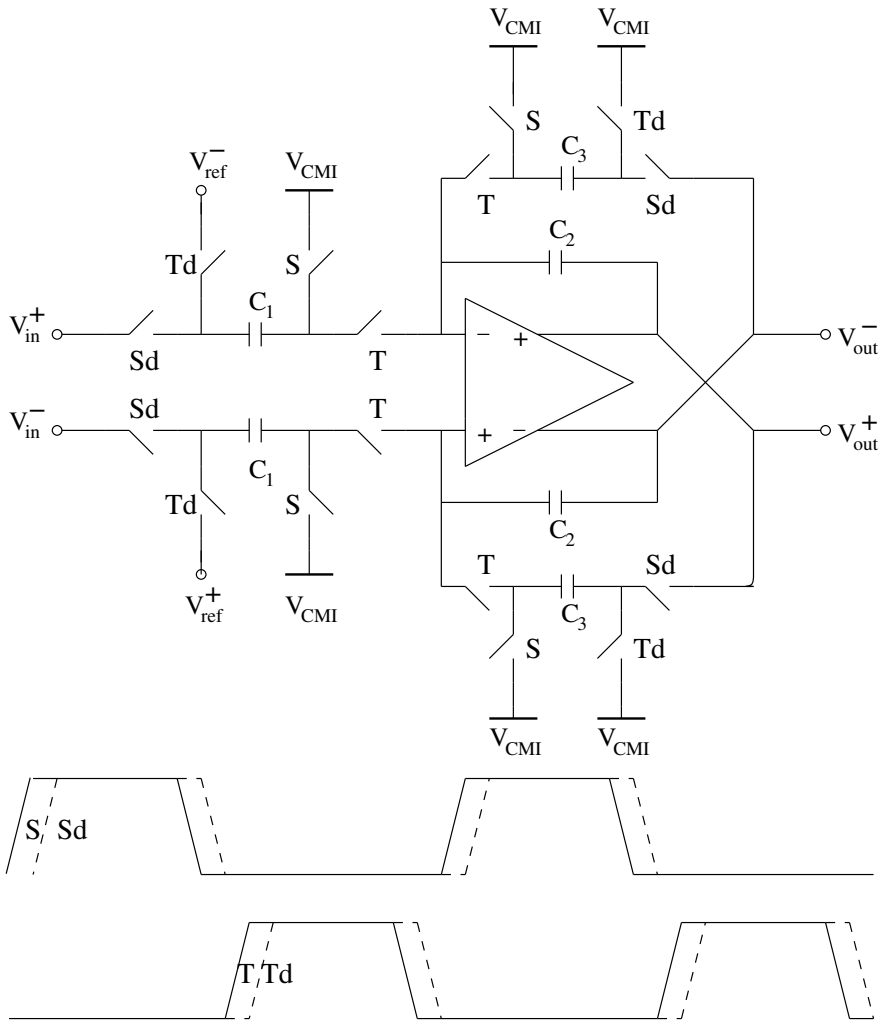


Figure 6.1: Fully differential, SC implementation of the high-pass filter.

The high-pass filters are implemented using the fully differential SC circuit shown in Figure 6.1, where $C_1 = 0.5pF, C_2 = 1pF$ and $C_3 = 2pF$. Theses values of capacitors are chosen in order to obtain the desired high-pass filter transfer function as already explained in Chapter 3. The differential topology used in the circuit of Figure 6.1 ensures that common-mode disturbances, such as noise from the power and ground rails, as well as signal-independent switch charge injection, will be cancelled

to the first order [103, 104, 174]. Furthermore, the signal voltage swings are effectively doubled, which increases the maximum signal power by a factor of four, while the kT/C noise power is only increased by a factor of two. Thus, a net improvement of 3 dB in the peak SNR is obtained if the noise floor of the circuit is dominated by kT/C noise. If op-amp noise dominates the noise performance of the fully differential circuit, the result is a 6 dB improvement in SNR [104, 174]. However, these advantages are at the expense of additional complexity imposed by the need for common-mode feedback circuitry in the amplifier and greater area required to implement a fully differential topology.

The switches are controlled by two non-overlapping clock phases, S and T, and delayed phases, Sd, Td. The use of both primary and delayed clock phases to control the switch network guarantees that the switches tied to dc common-mode voltages are turned off before those connected to nodes that have large signal-dependent swings [175].

The operation during the sampling and charge redistribution phases is depicted in Figure 6.2. On the sampling phase, S, a charge proportional to V_{in} is stored on C_1, and a charge proportional to V_{out} is stored across C_3. On the charge redistribution phase, T, $-V_{ref}$ is sampled onto C_1, and charge is transferred from C_1 to C_2, and C_3 to C_2. Because the capacitor C_3 are cross-coupled around the op-amp, the charge transferred from C_3 effectively undergoes an inversion during the charge redistribution phase. In the z-domain, the output of the filter is given by (6.1), as already presented in Chapter 3.

$$V_{out}(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 + (C_3/C_2 - 1)z^{-1}} (V_{in}(z) + V_{ref}(z)). \tag{6.1}$$

6.3 Circuit Design

6.3.1 Operational Amplifier

The op-amp is a critical device in the high-pass modulator. Its nonlinear parameters such as finite gain, finite bandwidth, slew-rate and saturation, degrade the modulator performance and can make the modulator unstable as analyzed in Chapter 6. Amplifier noise is amplified in the output of the modulator and increases the overall noise floor.

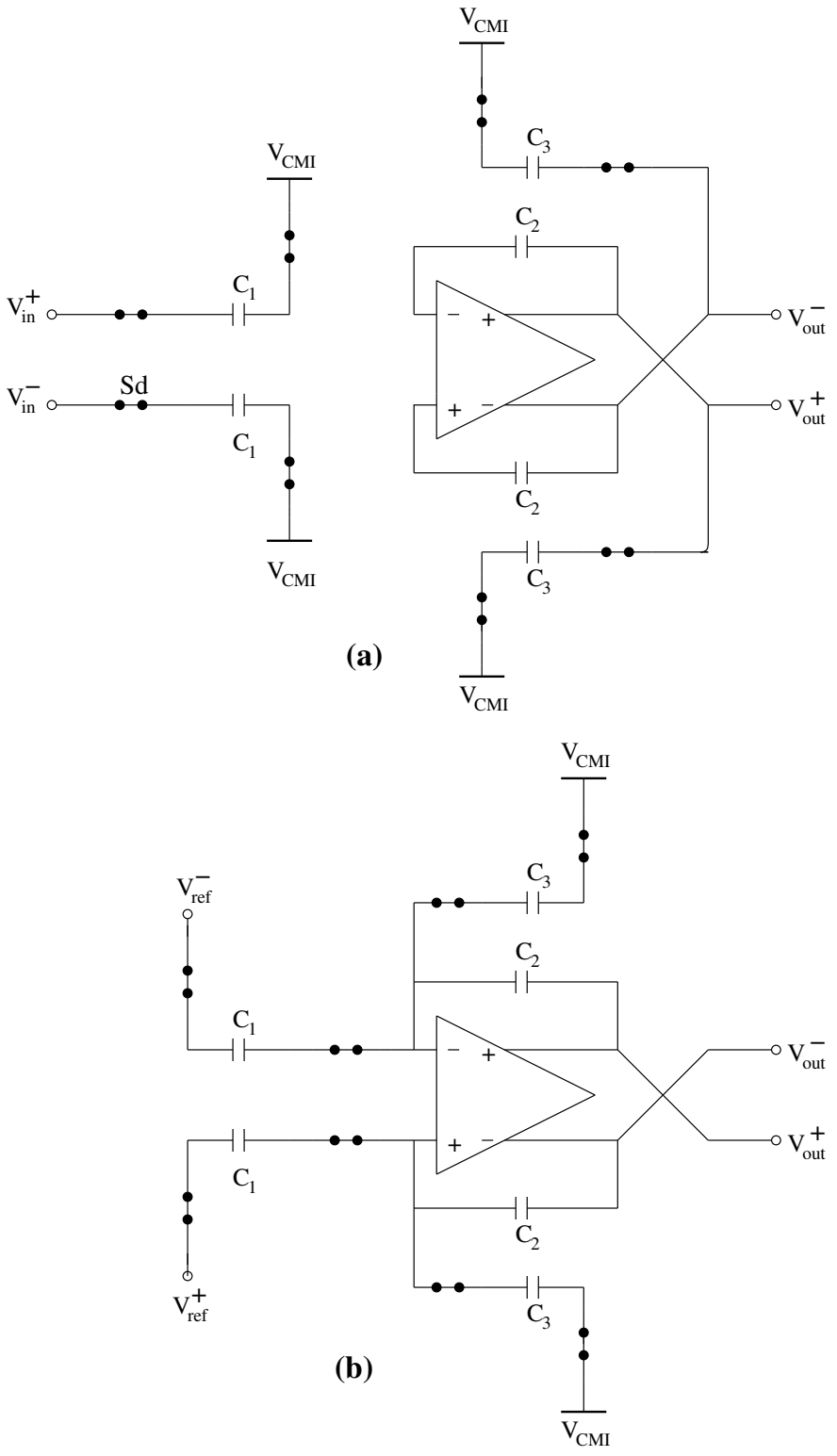


Figure 6.2: Filter configured during the sampling phase; S (a), and charge redistribution phase, T (b).

At this stage, it is useful to remind the required specification obtained from behavior simulations with VHDL-AMS. The static gain must be superior to 60 dB, the slew-rate must be stronger than 50 V/μs, and the transition frequency must be sixteen times higher than the sampling frequency, f_s. These three parameters are the most influent on the modulator performance.

Various topologies of amplifiers can be exploited to match the requirements above. Nevertheless, none of them helps achieve these objectives with a maximum gain, speed, output signal excursion and minimum consumption, surface and noise. We must do a compromise between these parameters. Initially, a choice of class operation must be done since the op-amp also differs in function of the type of bias. This can be of class A, B or AB. The two last classes work well with the systems where the processed signals are fast with important amplitudes [176]. Theoretically, there is no limit of current in these types of circuit. In practice, we talk rather about very high performances in terms of slew-rate. However, the important distortion created by these types of circuit limits their application. Consequently, our choice was directed towards class A. However, when the linearity is not a dominating criterion for the application, a comparative study, beyond the framework of this report, must be undertaken between class A and AB, since several recent works have showed the possibilities offered by the latter for switched op-amp applications [177, 178, 179].

The amplifiers are also characterized by the number of stages. We distinguish one-stage and two-stage amplifiers. In the first category, we can name the telescopic amplifier and the folded cascode amplifier. The telescopic amplifier uses a cascode topology in order to obtain higher gain than those obtained by simple topologies of amplifier. The cascoding increases considerably the output resistance and proportionally the gain of the circuit. The slew-rate of the amplifier is in fact the ratio of the output current by the load capacitance at the output of the amplifier. Consequently, to have a high performance in term of slew-rate, it is necessary to have strong output current or a low load capacitance. The amplifier noise is also an important parameter in the choice of the amplifier. In the case of the telescopic amplifier and if we consider only the thermal noise, we can calculate the significant contributions to the sources of noise. This topology also helps reach a very high products gain-bandwidth with a low consumption and a reduced silicon surface. These advantages are added to the quite simplicity of design. Nevertheless, this topology has a major disadvantage: the excursion of the output signal is very limited by the stacking of the transistors. The weaker is the supply voltage, the more

significant is the output excursion limitation. Meanwhile, the evolution of CMOS technologies leads to a fall of the supply voltage, which would result certainly in compromising the use of such a topology for the supply lower than 5V. The second disadvantage related to the telescopic amplifier is the strong dissymmetry between the positive and negative output dynamics. This results in imposing a constraint on the common-mode input of the circuit.

In order to improve the output voltage excursion of the amplifier, we can use a folded cascode amplifier. The gain of the folded cascode amplifier is weaker than that of the telescopic amplifier. In other words, to have the same gain, it is necessary to provide more current in the case of folded cascode. The folded cascode offers a better output excursion and especially a degree of freedom which is at least the same on the common-mode input. These two advantages of the folded cascode amplifier are of course at the price of increased consumption, weaker gain, reduced speed and higher noise.

We observed that obtaining a high gain is compromised by a weak excursion of the output signal and vice versa. The two-stage amplifier dissociates these two parameters to allot them on two different amplifiers or two stages. The first stage ensures the gain whereas the second ensures a maximum of excursion of output signal. The resulting gain is the gain of the two stages. In order to increase the gain considerably, the first stage can be built around the telescopic or folded cascode amplifier. The second stage is generally built around a simple common source stage. By doing this, it is possible to get a very high excursion of the output signal. Concerning the slew-rate, we can optimize this parameter according to the bias current of the two stages, but also according to compensation and load capacitances. The performance in thermal noise of the two-stage amplifier are that of the first stage plus that of the second stage. The contribution of the latter is considered negligible since its noise is divided by the gain of the first stage. The two-stage amplifier could present a potential solution since it makes it possible to obtain, with a rather simple topology, a strong gain, a high excursion of the output signal and a weak noise. The use of telescopic at the first stage could increase the gain if it proves that this one is not sufficient. Nevertheless, the problem of the common-mode persists since it is inherent with the telescopic amplifier. The use of a folded cascode makes it possible to be freed from this problem and conduit with an amplifier performance. However, the noise remains considerable. A major disadvantage of the two-stage amplifiers is their sensitivity to the load capacitance at the output. Another drawback of the

two-stage amplifier is its speed. This is due to the additional non-dominant pole added by cascading the two stages. However, the two-stage amplifier is more flexible than that of a single-stage amplifier. This suggests that the slowness of the two-stage design can be compensated without having to do a tradeoff between the gain and output signal excursion.

By comparing the single-stage with the two-stage topologies, we found that the advantages of the two-stage topology outweighed its disadvantages. Consequently, we opted for a two-stage design.

The preceding comparison does not take into account the possibilities to improve or to neutralize the disadvantages of each topology [175, 180, 181, 182]. This would require a more thorough comparative study and goes beyond a first-order comparison between the principal parameters of an amplifier. Such a study would also take into account parameters of comparison like the rejection of the common-mode, the rejection of the supply noise and consider probably other topologies such as gain-boosting amplifiers. This also asks for the availability of tools for automatic synthesis which make it possible to take into account and to compare all the parameters of various topologies of amplifiers in a fast time.

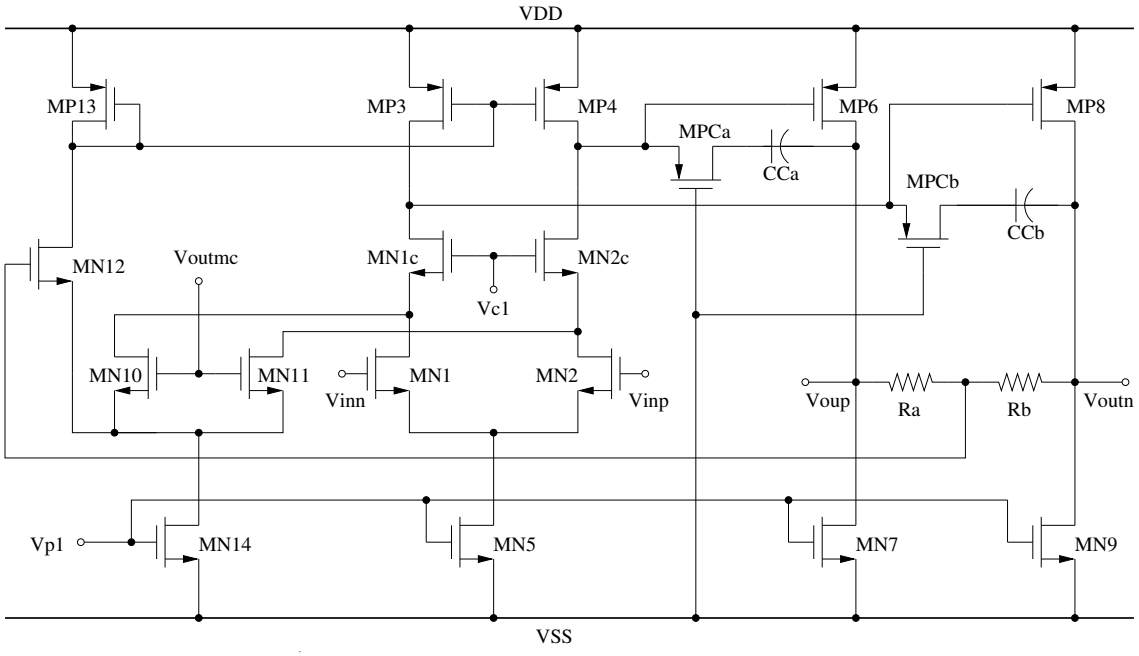


Figure 6.3: Two-stage operational amplifier

In this implementation, two-stage op-amp presented in Figure 6.3, is used. We

use the OCEANE software to design the thorough amplifier. In this design, both input and output common-mode levels are set to 1.65V. Table 6.1 presents transistor

Transistor	W/L (μm)	Transistor	W/L (μm)
MN1, MN2	10.5/0.6	MN1c, MN2c	13.8/0.6
MP3, MP4	47.2/0.6	MP6, MP8	129/0.6
MN7, MN9	43/0.6	MN5	21.5/0.6
MN10, MN11	5.25/0.6	MPCa, MPcb	4.5/0.35
MN12	10.5/0.6	MP13	35.4/0.6
MN14	35.4/0.6		

Table 6.1: Transistor sizes of the operational amplifier.

sizes of the designed amplifier.

The bias circuit providing two bias voltages $Vc1 = 1.824V$ and $Vp1 = 0.733V$ is shown in Figure 6.4. The transistor sizes of the bias circuit are presented in Table 6.2

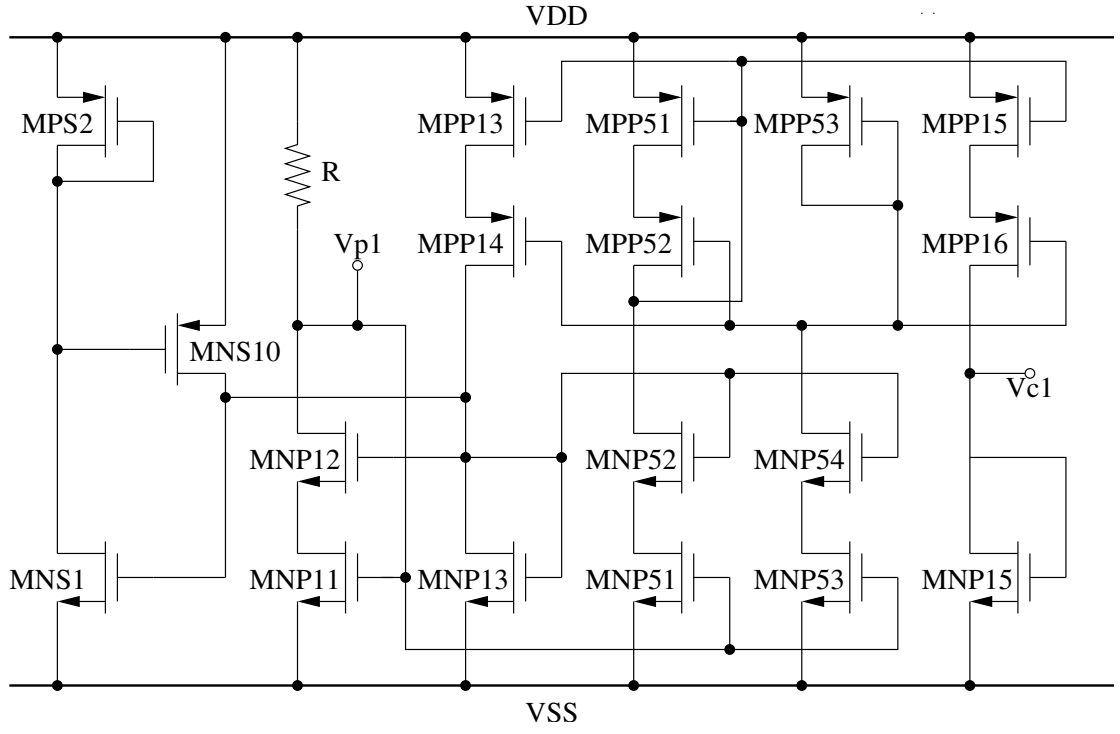


Figure 6.4: Bias circuit of two-stage operational amplifier

Transistor	W/L (μm)	Transistor	W/L (μm)
MNP11, MNP51	21.5/0.6	MNP12, MNP52	738/0.6
MNP53	21.5/0.6	MNP54	738/0.6
MPP13, MPP51, MPP15	35/0.6	MPP14, MPP52, MPP16	16.8/0.6
MNP13	1.45/0.6	MPP53	5.35/0.6
MNP15	0.7/0.6	MNS10	220.25/0.35
MPS1	0.7/0.35	MNS2	1.45/0.6

Table 6.2: Transistor sizes of the bias circuit.

Figure 6.5 shows gain and phase of the amplifier. Figure 6.6 shows output excursion of the amplifier.

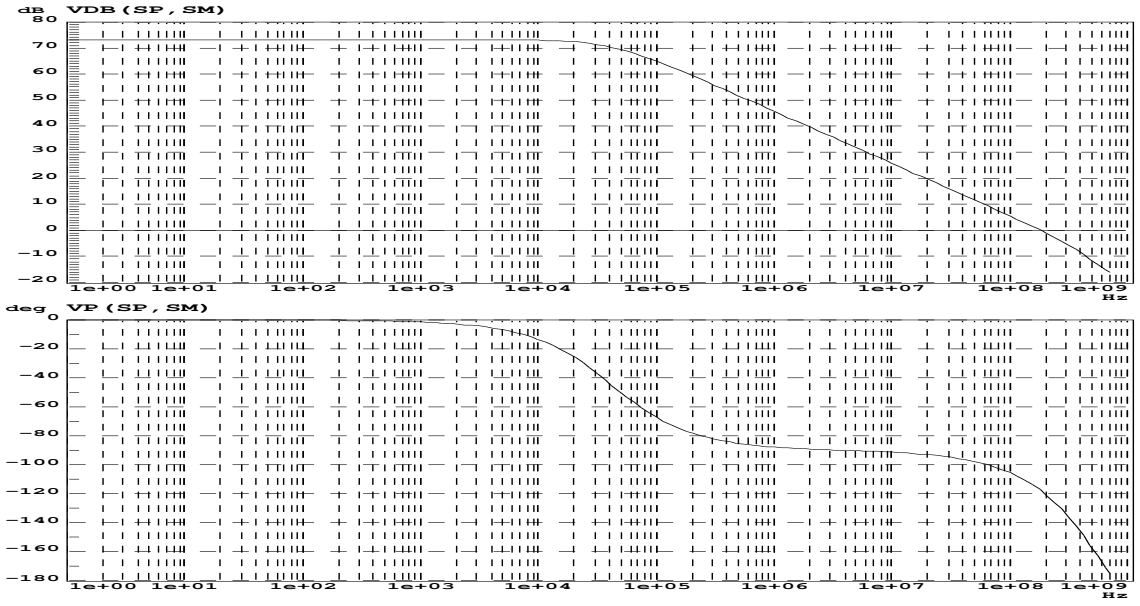


Figure 6.5: Frequency response of operational amplifier with a 2pF load capacitances at each output.

Table 6.3 presents the summary of the amplifier performance. It is completely satisfied to the specifications derived from Chapter 5.

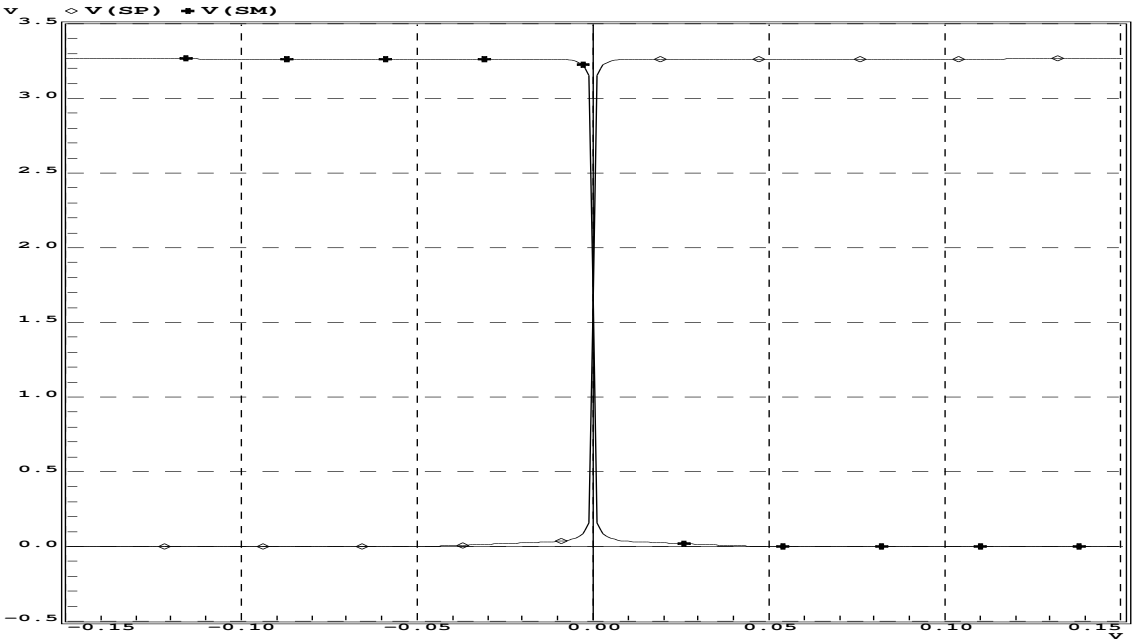


Figure 6.6: Output excursion of operational amplifier

VDD (V)	3.3
VSS (V)	0
Transition frequency : F_T(MHz)	175
Gain (dB)	74
Phase margin (degree)	61
Slew-rate (V/μs)	83
Maximal output voltage (V)	3.1
Minimal output voltage (V)	0.2
Output resistance (kΩ)	14.9
Total current (mA)	5.58
Total power consumption (mW)	16.8

Table 6.3: Operational amplifier performances.

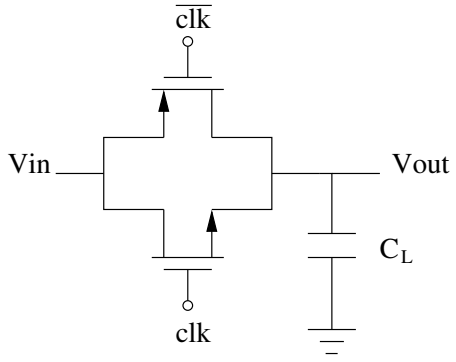


Figure 6.7: CMOS Switch

6.3.2 Switch

In general, the switch is one of the devices which generates a lot of imperfections in the SC circuit, such as gain error, offset and nonlinearity. The last type of error is very critical especially for the switches at the input of the circuit. Contrary to the NMOS and PMOS switches, CMOS switch allows the largest excursion of input signal. For this reason, our choice is directed towards this type of switch. For the switch given in Figure 6.7, if the clock phases are complementary, and the transistor is in the ohmic mode, then the equivalent on-resistance of the switch is given by (6.3).

$$R_{on} = R_{NMOS} || R_{PMOS} \tag{6.2}$$

$$R_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N (V_{DD} - V_{THN}) - \mu_p C_{ox} \left(\frac{W}{L}\right)_P (V_{SS} + |V_{THP}|) - f(Vin)} \tag{6.3}$$

where

$$f(vin) = \left[\mu_n C_{ox} \left(\frac{W}{L}\right)_N - \mu_p C_{ox} \left(\frac{W}{L}\right)_P\right] Vin. \tag{6.4}$$

The first sizing results in choosing $f(Vin) = 0$ in order to make the switch on-resistance independent of input voltage as it follows:

$$\mu_n C_{ox} \left(\frac{W}{L}\right)_N = \mu_p C_{ox} \left(\frac{W}{L}\right)_P. \tag{6.5}$$

The first criterion to be satisfied after this preliminary choice is load speed of the capacitor C_L. The time constant being equal to $\tau = R_{on} C_L$, it would be enough to choose the lowest possible resistance value to have the fastest settling of Vin, since the error in this case is proportional to $exp(-t/\tau)$. An accuracy of 0.2% of

capacitor C_L, leads to the value of R. The latter allows to determine the value of W. In other words, to have a fast settling, it would be enough that the value of W is very high. However, this conclusion is very hasty. Indeed, a second criterion must also be satisfied: the error generated by the charge injection and introduced to the output voltage, $Vout$, which is given by

$$\Delta V = \frac{WLC_{ox}(V_{DD} - Vin - V_{THN})}{C}, \tag{6.6}$$

must be minimized. This error is proportional to W. There is therefore a tradeoff between precision and settling speed. Another criterion is the linearity. Several studies were undertaken to determine the nonlinearity in the SC circuits due to the nonlinearity of the capacitors, or the various parameters of the amplifier, even the nonlinearity due to the charge injection and the coupling with the clock signal [175]. Some works are even interested in different topologies of switch [183]. The analytical study of the nonlinearity of a switch is very complex and goes beyond the framework of this report.

CMOS switch makes it possible to minimize the charge injection in assuming that the charge quantity injected by NMOS transistor is equal to that of PMOS transistor, if sizes are identical. This solution seems judicious to reducing the charge injection as well as to input dynamic improvement. The design method adopted during this study consists of improving the settling precision by fixing the length of the two transistors at the minimal value of technology (0.35μm). Then the parameter W is adjusted to satisfy the settling time requirement. The R_{on} value chosen is about 400Ω.

6.3.3 Capacitors

The design of capacitors have to take care of design rules of AMS so that the capacitor mismatch is smaller than 0.5%. The value $C_2 = 1$pF and $C_3 = 2$pF, satisfy this requirement, because capacitor matching is described by

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{AC}{\sqrt{W.L}}. \tag{6.7}$$

Parameter AC is given by AMS as $2.7\%.\mu m$ for double-poly capacitor. We use a 0.5pF capacitor as elementary capacitor in our design. For this value, capacitor sizes $W = L = 23.9\mu m$ are chosen. Thus, the capacitor mismatch is inferior to 0.2%, what satisfy completely the requirement mentioned above.

6.3.4 Comparator

The object of the comparator is to determine the sign of the output of the previous high-pass filter. Being placed in the loop of negative feedback of the system, the requirements on the performance of this circuit are relatively weak. In particular, the influence of its offset voltage on performance of the monobit high-pass modulator as well as on that of low-pass one, is negligible. Thus, the structures including a differential pair at input, which helps improve the precision, are not necessary. However, the time of comparison must be optimized to avoid introducing an important additional time into the feedback of the modulator. As in the low-pass modulator,

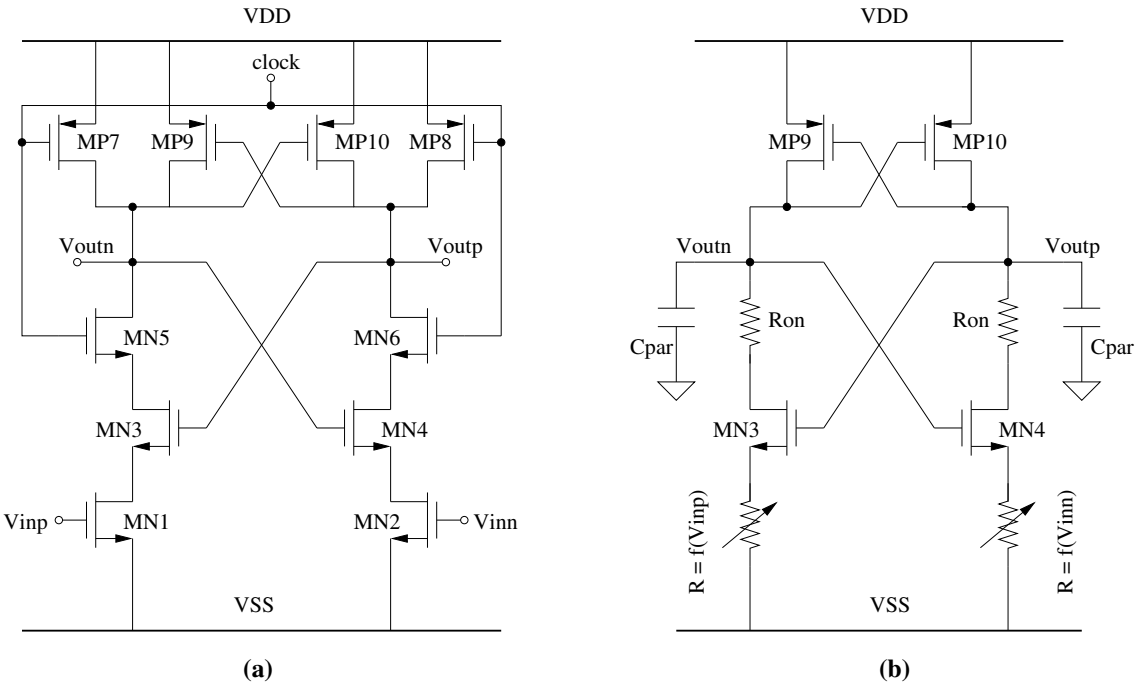


Figure 6.8: Dynamic latch used as the comparator core (a) and simplified representation of the latch in the active phase ($clock = VDD$) (b).

the structures based on the principle of positive feedback adapt perfectly to these requirements [184]. The circuit in Figure 6.8(a) corresponds to the selected comparator [65, 176, 185]. It is based on the principle of a dynamic latch initialized by *clock*. The operation is as follows:

- When *clock* is low, the outputs are initialized to VDD through $MP7, MP9$ and $MP8, MP10$. This forces the comparator to remain in an unstable state.

The input voltages are applied to the grid of $MN1$ and $MN2$ but does not have any influence on the output voltages;

- At the time when *clock* goes high, the circuit in active phase can be schematized by Figure 6.8(b). *Ron* corresponds to the resistance of the switches related to *clock*, whereas R depends on $MN1$ and $MN2$. The other components constitute two inverters configured in positive feedback. The output voltages $Voutp$ and $Voutn$ being initialized in VDD, a discharge of the $Cpar$ capacitor in transistors $MN1$, $MN3$, and $MN5$ takes place. Its speed depends on resistances *Ron* and R. Thus, a variation of the latter through an imbalance of the input voltages ineluctably induces a different exponential response between the two branches from the circuit. This effect is amplified considerably by the unstability of the feedback inverter and two outputs commutate frankly towards the stable state VDD or VSS. Of course, this phenomenon is extremely fast and this type of circuit is capable to reach a few nanosecond switching time.

In the interest of reducing the input-referred offset of the comparator, nonminimum channel length transistors are used in the dynamic latch. Table 6.4 presents the transistor sizes of the dynamic latch used as the comparator core.

Transistor	W/L (μm)	Transistor	W/L (μm)
MN1, MN2	8.4/0.7	MN3, MN4	4.2/0.7
MN5, MN6	168/0.7	MP7, MP8	4.2/0.7
MP9, MP10	672/0.7		

Table 6.4: Transistor sizes of the dynamic latch.

Because of the absence of information at the output of the circuit in the phase of initialization, a RS latch is added in the output as shown Figure 6.9. It holds the data for a full clock cycle and isolates at the same time the output of the modulator from the parasitic variations of $Voutp$ and $Voutn$. Simulations of the netlist and extraction of the layout show that the response of the comparator is of 8ns between the beginning of the active phase and the establishment with 90% of the final output value. At the end, the offset of the comparator should approach 10mV.

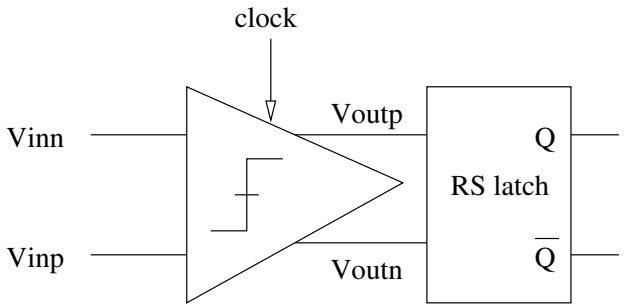


Figure 6.9: Complete comparator.

6.3.5 Chopper

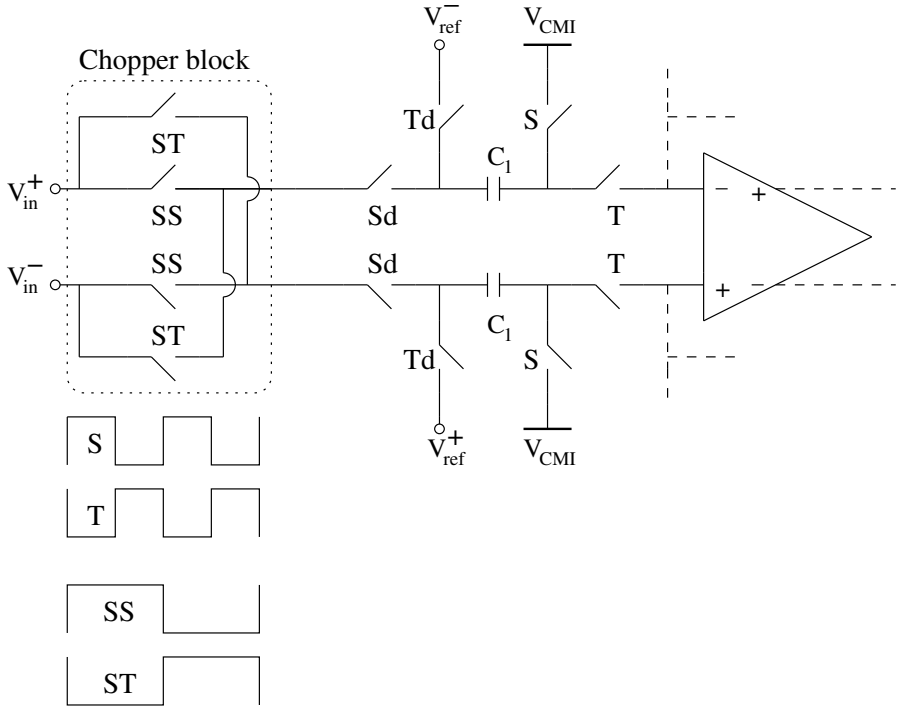


Figure 6.10: Implementation of chopper block

The chopper is implemented as shown in Figure 6.10. The design of the chopper leads therefore to design a frequency divider of frequency $f_s/2$. The frequency divider is included in the clock generator of the circuit.

The multiplexor is implemented in the same manner. Indeed, if we replace the V_{in}^+ and V_{in}^- with V_{CMI} as shown in Figure 6.11 the multiplexor for two channels is obtained. The design of a multiplexor for M channels leads to design a frequency divider of frequency f_s/M.

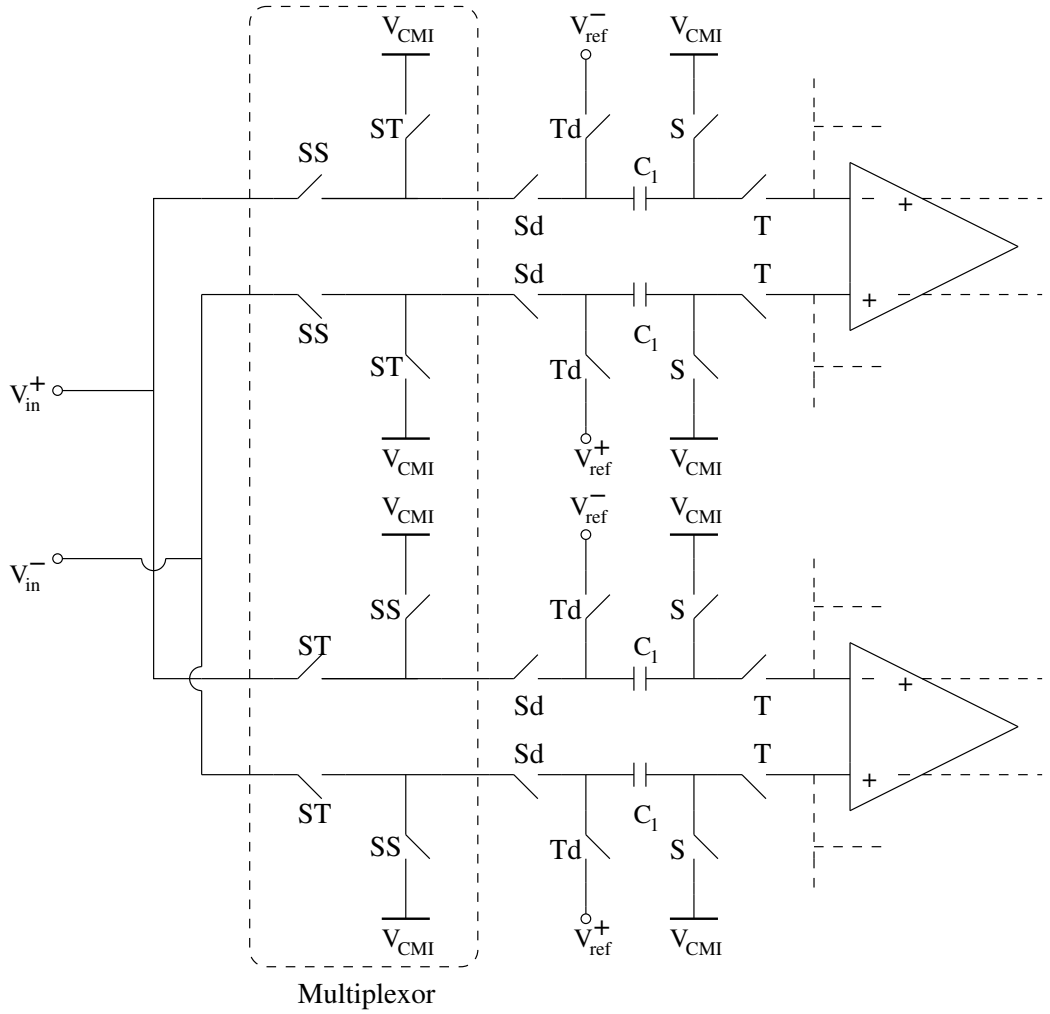


Figure 6.11: Implementation of multiplexor

6.3.6 Clock Generator

A generator of complementary and delayed phases is necessary not only for the correct operation of the SC circuit, but also to minimize the charge injection. The clock generator of phases, S, T, Sd, Ts, SS and ST is implemented as shown in Figure 6.12. The simplicity of this circuit should not dissimulate a certain number of precautions to be taken in order to ensure the correct operation of the circuit. This circuit generates, starting from a clock signal, various phases. These phases are obtained with a judicious sizing of the transistors in each logical port. This circuit attacks a great number of switches. Consequently, the load capacitance at each phase is important and not necessarily identical. A careful design must thus take into account total charges of the switches and ensure, if necessary, a charge balance by adding an additional capacitor at the output of the various phases. The phases S and SS, T and ST should be synchronized in rising edges to ensure the right operation of chopper block.

6.3.7 Clock Buffer

Clock signals must arrive at the same time at the level of the switches. There exist for that two solutions: to use a buffer for the whole of the switches connected to the clock in question, or to locally allot (to each one of them) a buffer of smaller size. The latter is more effective, at the cost of complex layout. The buffer shown in Figure 6.14, consists of two chains of inverters in parallel which generate the signal and its complement at the output without difference in time. Indeed, the sum of time-constants in each of the two branches is equalized by sizing the inverters in adequate manners. Finally, a capacitor could be connected to the output to control the slope of the clocks by desensitizing it of the parasitic capacitors of the switches

6.3.8 Real Inband Noise Effect

In the proposed implementation of the filter, it can be seen in Figure 6.2(a) that during the sampling phase, switch noise is sampled onto capacitors C_1, and C_3. During the charge redistribution phase (Figure 6.2(b)), additional noise is sampled when the charge from capacitors C_1, and C_3 is transferred to the capacitor, C_2. Since the noise sources are uncorrelated, their powers add. Therefore, using the capacitor

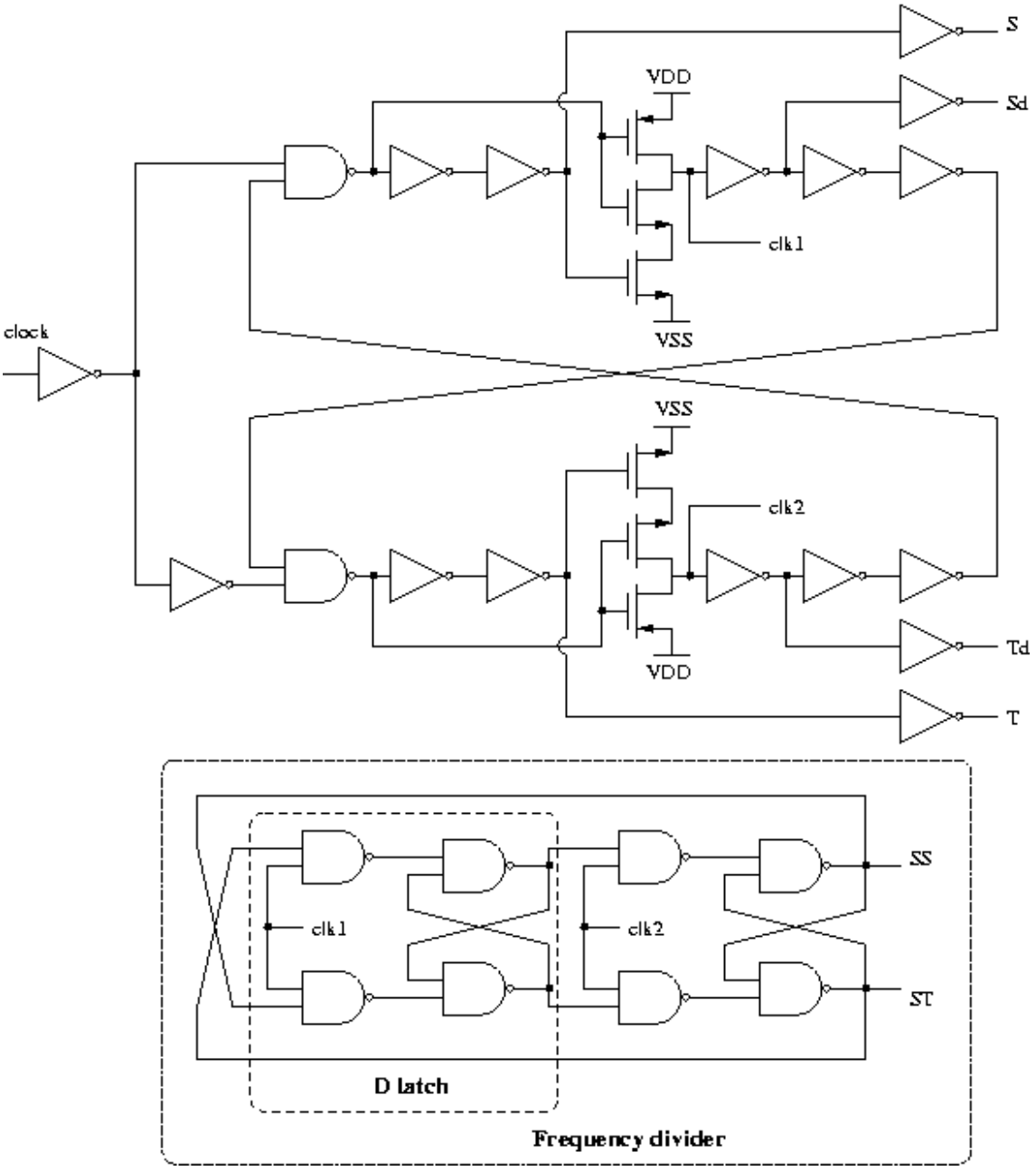


Figure 6.12: Clock generator.

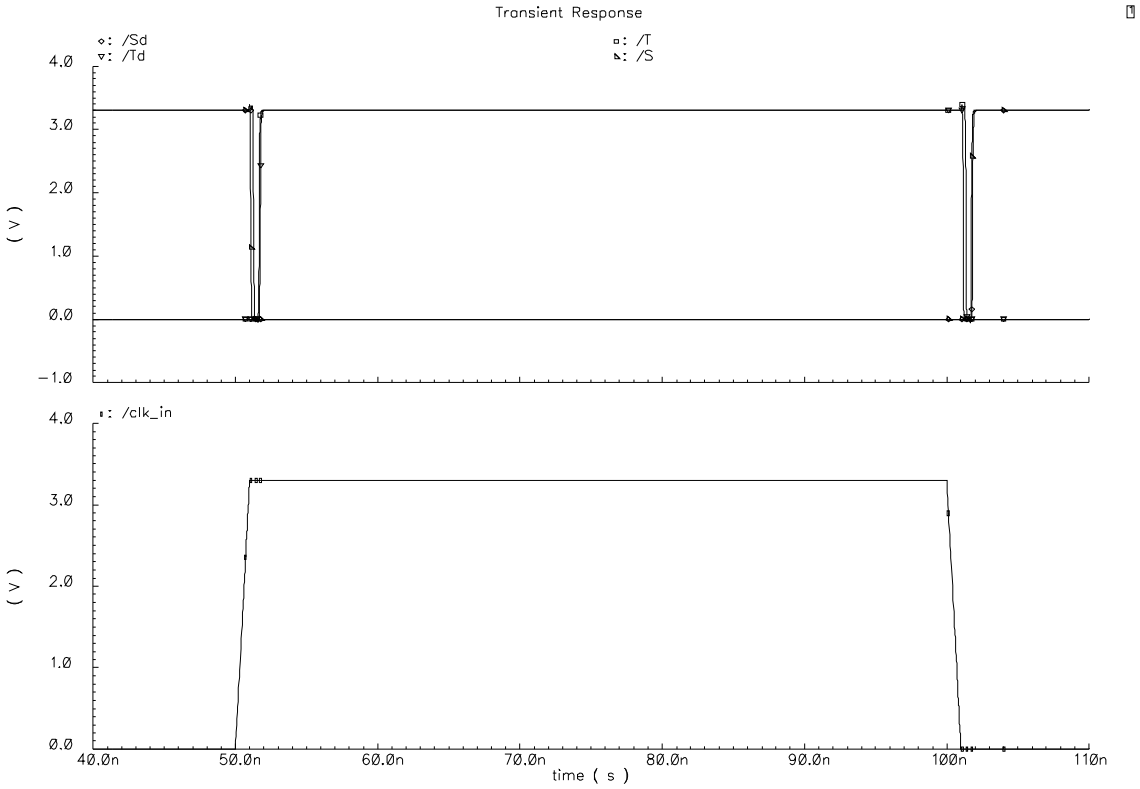


Figure 6.13: Clock phases.

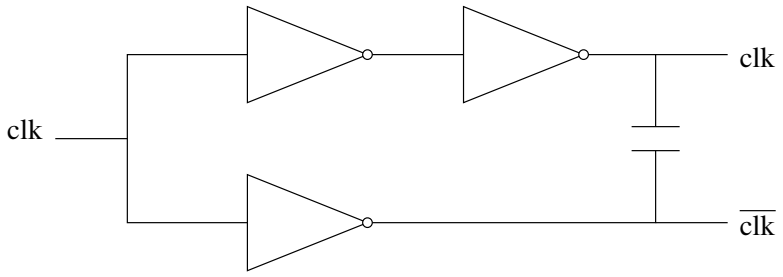


Figure 6.14: Clock buffer

values for the filter, the total power of the switch noise referred to the filter input is

$$P_{switch} = kT \times 2 \times \left(\frac{2}{C_1} + \frac{2}{C_3} \right). \tag{6.8}$$

In this expression, the factors of 2 outside and inside of parentheses account for the fact that noise is sampled during both the sampling and charge redistribution phases, and fully differential structure is used, respectively and it has been assumed that the noise sampled during both phases is bandlimited by the switch resistance and the sampling capacitor. This assumption results in an overestimate of the noise contribution during the charge redistribution phase, because the charge redistribution process is actually bandlimited by the op-amp, not by the switch network [186, 187].

Thermal noise from the switches can be referred to the inputs of each SC filter as discussed above, and then referred to the input of the modulator. However, the calculation can be simplified by neglecting switch noise from the second high-pass filter because it is attenuated by noise shaping. The total power of the switch noise referred to the input of the first filter was calculated in (6.8). Since the input of the first high-pass filter constitutes the front-end of the high-pass modulator, the total switch noise referred to the modulator's input is also given by (6.8). It is assumed that the switch bandwidth is much larger than the sampling frequency in the modulator, so P_{switch} is uniformly distributed throughout the sampling bandwidth. Because the passband bandwidth is only a fraction of the sampling bandwidth, the contribution to the inband noise power is equal to (6.8) divided by the oversampling ratio, OSR. This leads to

$$P_{switch,inband} = \frac{P_{switch}}{OSR} = \frac{4kT}{OSR} \left(\frac{1}{C_1} + \frac{1}{C_3} \right). \tag{6.9}$$

Capacitors values are chosen as $C_1 = 0.5pF$, $C_3 = 2pF$, and $OSR = 32$, then we have

$$P_{switch,inband} = \frac{1.38\,10^{-23}\,JK^{-1}\,300K}{32} \left(\frac{1}{0.5pF} + \frac{1}{2pF} \right) = 1.29\,10^{-9}\,V^2. \tag{6.10}$$

The op-amp noise is analyzed in Subsection 5.5.1 of chapter 5. The inband noise generated from op-amp noise at the modulator output is given by

$$P_{amp,inband} = 41 \times \frac{P_{amp1}}{OSR}. \tag{6.11}$$

Simulation shows that the amplifier's input-referred noise power is $P_{amp} = 1.47 \times 10^{-8}\,V^2$. From 6.11, it follows

$$P_{amp,inband} = 41 \times \frac{1.47\,10^{-8}}{32}\,V^2 = 1.8810^{-8}\,V^2. \tag{6.12}$$

In the experimental prototype, Δ is equal to 1.0 V. If switch noise and amplifier noise are the dominant noise source in the circuit, then the estimated dynamic range of the modulator is

$$\begin{aligned} DR &= \frac{\frac{1}{2}(\frac{\Delta^2}{2})^2}{P_{switch,inband} + P_{amp,inband}} \\ &= 68dB. \end{aligned} \tag{6.13}$$

6.4 Conclusion

The objective of this chapter is to realize the second-order high-pass $\Delta\Sigma$ modulator to validate the feasibility of this kind of modulator and demonstrate its advantages compared to the low-pass modulator. In order to illustrate the advantages of the high-pass modulator in time-interleaved $\Delta\Sigma$ converter, two high-pass $\Delta\Sigma$ modulators are put in parallel.

The implementation of the second-order high-pass $\Delta\Sigma$ modulator has been described in this chapter. A fully differential SC high-pass filter that implements the desired transfer function has been designed, and its limitations due to switch and amplifier noise have been analyzed. A two-stage amplifier with 75dB of gain, 83 V/μs of slew-rate, and 175 MHz of transition frequency, is designed to ensure specification derived from VHDL-AMS simulations when the high-pass filter is clocked at 10 MHz.

Additional circuits in the prototype described in this chapter include bias circuit, dynamic comparator and clock generator. The comparator is a simple dynamic latch followed by a SR latch. A noise analysis of the modulator reveals that the amplifier noise in the first high-pass filter is shaped to have a maximum spectral density in the signal band centered at $f_s/2$. This hazardous noise amplification can degrade the dynamic range of the modulator by a substantial margin, unless an op-amp is designed with a low enough input-referred noise power, such that at the output of the modulator, the level of shaped amplifier noise in the passband remains comparable to the level of inband kT/C noise.

Chapter 7

Layout and Test Setup

7.1 Layout

The prototype of a second-order high-pass $\Delta\Sigma$ modulator and a two channels time-interleaved second-order high-pass $\Delta\Sigma$ converter without channel filters is shown in Figure 7.1. The first third of the prototype is the second-order high-pass $\Delta\Sigma$ modulator. Symmetry is observed in the layout to enhance the rejection of the common-mode disturbances in the fully differential circuit. The front-end, differential inputs applied at first to chopper and then the high-pass modulator are at the left of the die. The digital circuit, seen at the right, is physically separated from the analog circuits and is powered from a separate supply. The use of different analog and digital supplies decouples the analog circuitry from the switching noise caused by large dynamic currents drawn from the digital supply. The last two thirds of the prototype consists of two identical second-order high-pass $\Delta\Sigma$ modulators without chopper in interleaving. The total area of the prototype is 1.33mm x 2.05mm, but the active area measures only 0.6mm x 1.37mm.

As discussed in Section 3.8 of Chapter 3, and Subsection 5.5.2 of Chapter 5, the stability of the modulator is affected by the mismatch between capacitors in the high-pass filter. Capacitor mismatch can cause the pole of the high-pass filter to lie outside of the unit circle. In keeping with standard practice, the capacitors are formed by connecting unit cells arranged in an array. The unit cell has a nominal capacitance of 500 fF. The 1 pF, and 2 pF necessary for the modulator are formed by interconnecting two, and four unit cells respectively. According to AMS design

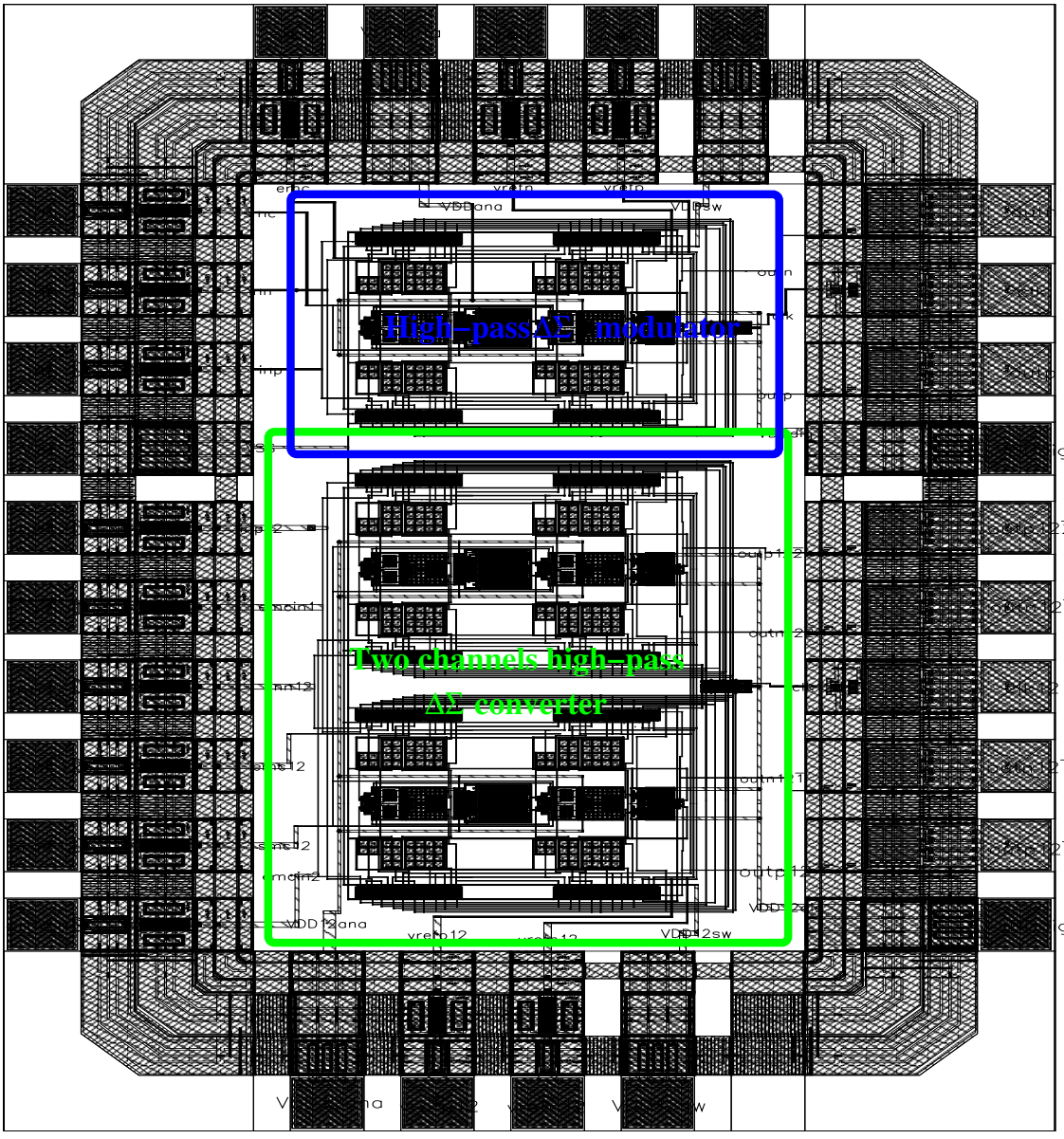


Figure 7.1: Layout of the second-order high-pass $\Delta\Sigma$ modulator and a two channels time-interleaved second-order high-pass $\Delta\Sigma$ converter.

rules, the capacitor mismatch is less than 0.2%.

7.2 Test Setup

The device under test (DUT) is packaged in a 44-pin, J-leaded chip carriers. The di-

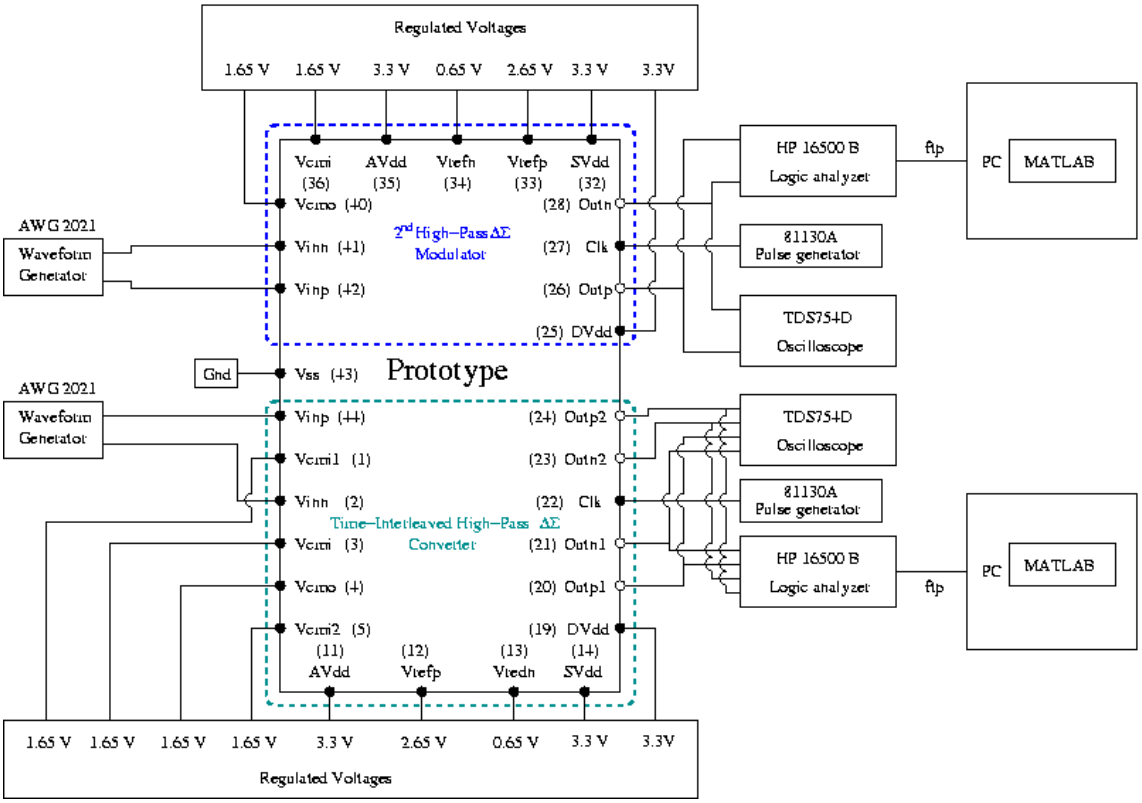


Figure 7.2: Diagram of test setup.

agram of the desired test setup is presented in Figure 7.2. The most important test is the test of functionality of the high-pass modulator before measuring its performance and its advantages in the time-interleaved $\Delta\Sigma$ converter. The supply voltages are generated from the voltage regulator MC33275. Various regulated voltages shown in Figure 7.2 are generated through terminal adjustable regulators LM317L. The impulse generator makes it possible to have a clock signal for the circuit. The differential input is generated from waveform generator AWG 2021 by granting its two outputs in opposition of phase.

The test of a $\Delta\Sigma$ modulator has to be proceeded in two steps: the static test and the dynamic test. The first test consists of verifying the right operation of bias

circuit in assuring the transistors operating in the saturation mode. The expected consumption of a high-pass second-order $\Delta\Sigma$ modulator is 42.44 mW. The total power consumption of the chip is 127.5 mW. The second test is to measure the dynamic performances of the modulator. The output is measured through the logic analyzer HP 16500 B. The resulting data from the logic analyzer is transferred to PC and processed through MATLAB tool. These treatments will allow to obtain the spectrum of the output signal. A MATLAB program calculates the SNDR and SNR of the modulator. The measurement is taken while varying the amplitude of the input signal. This enables us to plot SNDR curves with the presence of the noise and harmonic distortion. Then, with a program developed in MATLAB, we can remove the harmonics and we have the curve of the SNR as a function of the input signal amplitude. To verify the immunity of the high-pass modulator from low frequency noise, an offset or a low frequency noise source is added to one of the two reference voltages V_{ref}^{+} or V_{ref}^{-}, which are the output value of the DAC in the feedback of the modulator. The expected performance of the high-pass second-order modulator is presented in Table 7.1.

Specifications	Expected result
Supply voltage	3.3 V
Consumption	42.44 mW
Sampling frequency	10 MHz
Input signal frequency	15 KHz
OSR	32
Harmonic distortion	-65 dB
SNR	54.5 dB
SNDR	53.6 dB

Table 7.1: Expected performance of the high-pass second-order modulator.

The output of the time-interleaved high-pass $\Delta\Sigma$ converter is measured in the same manner. The output of each modulator is measured through the logic analyzer HP 16500 B. The resulting data is transferred to PC. It will be filtered by an optimal channel filter through a programme in MATLAB and demultiplexed to produce the final output signal. By this way, the performance of the converter is studied. The most important test is the immunity from channel offset. Undesired tones due to channel offset are completely drowned in the quantization noise.

Chapter 8

Conclusions

8.1 Summary

The high-pass $\Delta\Sigma$ modulator has been studied and analyzed. The high-pass $\Delta\Sigma$ modulator shapes the quantization noise to low frequency range. The signal band is located around one-half of the sampling frequency. Therefore the high-pass modulator is completely immune to low frequency noise. For a L^{th}-order high-pass modulator, a $L+1/2$-bit of resolution is gained for every doubling of OSR. The high-pass filter, the basis block building the high-pass modulator, can be implemented in SC technique based on the introduction of an extra feedback loop around the integrator, the basis block building the conventional $\Delta\Sigma$ modulator. High-pass $\Delta\Sigma$ modulators can be used as stand-alone modulators. Using a chopper at the front-end and back-end of the high-pass modulator makes it equivalent to a low-pass modulator. This chopper-stabilized high-pass modulator is immune to low frequency noise and is well suited to low frequency small signal applications.

They are also very beneficial in the time-interleaved $\Delta\Sigma$ converter, provided that the number of channels is even. The use of the high-pass $\Delta\Sigma$ modulators instead of low-pass modulators in this kind of converter preserves the converter performance with additional benefit of immunity from channel offset mismatch effect. A simple adaptive channel gain equalization using LMS algorithm has been proposed to minimize the channel gain mismatch effect.

A set of models in VHDL-AMS suitable for time domain behavioral simulation of SC $\Delta\Sigma$ modulators has been developed in order to analyze the nonideality effect

of the high-pass $\Delta\Sigma$ modulator and improve the modulator design. The proposed set of models takes into account at the behavior level most of SC $\Delta\Sigma$ modulator nonidealities, such as jitter noise, kT/C noise, $1/f$ noise, amplifier noise, switch nonidealities, amplifier nonidealities, and capacitor mismatch. This allows us to study the effect of various nonideality parameters on the high-pass $\Delta\Sigma$ modulator and define a threshold set of nonideality parameter value to ensure a desired performance of the modulator. This methodology allows us not only to make a specification of each elementary device of the $\Delta\Sigma$ modulator and estimate the modulator performance, but also to optimize various nonideality parameters to obtain a good performance of the modulator.

A prototype of a second-order high-pass $\Delta\Sigma$ modulator and a two channels time-interleaved $\Delta\Sigma$ converter, has been designed and fabricated in a 0.35μm, double-poly, quadruple-metal CMOS technology of AustriaMicroSystems. The total area of the prototype is 1.33mm x 2.05mm, but the active area measures only 0.6mm x 1.37mm. The expected power consumption of the chip is 127.5 mW. The expected performance of the high-pass modulator is 54.5 dB SNR with 10MHz sampling frequency and 32 times oversampling.

8.2 Suggestions

Although the high-pass $\Delta\Sigma$ modulator can be obtained from the corresponding low-pass $\Delta\Sigma$ modulator through the simple transformation $z \rightarrow -z$, its implementation is not an easy task. The high-pass filter, the basis block building the high-pass modulator, can be implemented in SC technique based on the introduction of an extra feedback loop around the integrator, the basis block building the conventional $\Delta\Sigma$ modulator. But analysis and behavioral simulations show that high-pass $\Delta\Sigma$ modulator with the proposed implementation has some drawbacks. It needs better op-amp performance than the low-pass modulator, especially a wider op-amp bandwidth, higher slew-rate and lower noise. The problem of stability in the high-pass modulator is more complex than it is in the low-pass modulator. Other implementations of the high-pass modulator should be studied. The implementation proposed in this thesis is based on the implementation of the high-pass filter. A more judicious idea may be to seek for a direct implementation of the high-pass modulator itself, basing on its quantization noise transfer function that must have high-pass noise

shaping, i.e. the zeros must be located at one-half of the sampling frequency. In order to do this, we might as well introduce feedback loops into the low-pass modulator, as indicated in two examples in Figure 8.1 and 8.2. The introduction of two gains c_1 and c_2 could allow us to obtain the desired quantization transfer function.

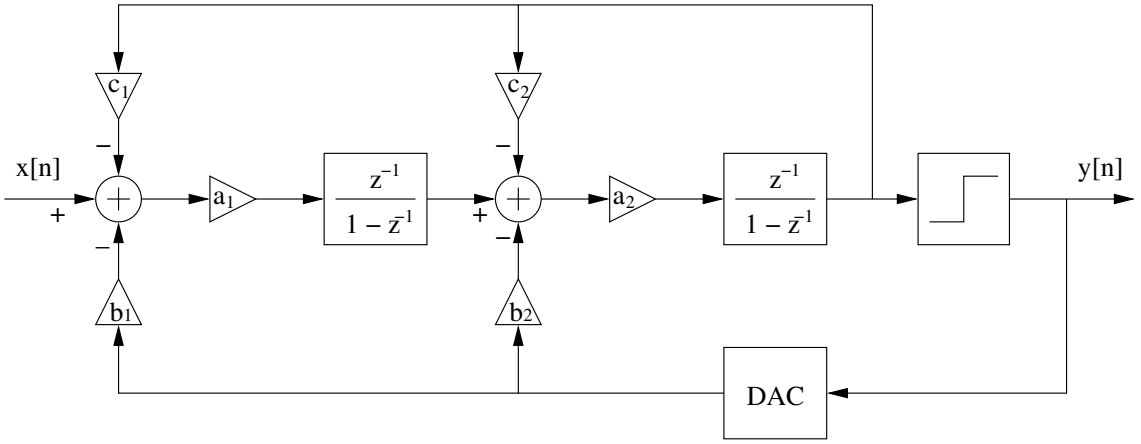


Figure 8.1: New implementation of second-order high-pass $\Delta\Sigma$ modulator based on Boser's structure of low-pass second-order $\Delta\Sigma$ modulator.

The output of the modulator in Figure 8.1 is described in z-domain by

$$Y(z) = S(z)\,X(z) + N(z)\,E(z). \tag{8.1}$$

The signal transfer function, $S(z)$, and the quantization noise transfer function, $N(z)$, are respectively

$$S(z) = \frac{a_1\,a_2\,G\,z^{-2}}{1 + (a_2(b_2\,G + c_2) - 2)z^{-1} + (1 + a_2(a_1(b_1\,G + c_1) - a_2\,G - c_2))z^{-2}}, \tag{8.2}$$

$$N(z) = \frac{1 + (a_2\,c_2 - 2)z^{-1} + (1 + a_2(a_1\,c_1 - c_2))z^{-2}}{1 + (a_2(b_2\,G + c_2) - 2)z^{-1} + (1 + a_2(a_1(b_1\,G + c_1) - a_2\,G - c_2))z^{-2}}, \tag{8.3}$$

where G is the gain of the quantizer.

If

$$\begin{aligned} a_1\,a_2\,G &= 1 \\ a_2\,c_2 &= 4 \\ a_1\,c_1 &= c_2 \\ 3\,a_1\,b_1 &= 2\,b_2 \\ a_2\,b_2 G &= -2 \end{aligned} \tag{8.4}$$

then the signal and quantization noise transfer functions are derived as $S(z) = z^{-2}$ and $N(z) = (1+z^{-1})^2$. Therefore, the modulator has a second-order high-pass noise

shaping. However, in this modulator, the introduction of two feedback loops would make the modulator unstable. But (8.4) indicates that there are six parameters under four conditions. Therefore, we have two free parameters to optimize in function of the modulator stability and performance.

The same idea can be applied to the classical second-order high-pass modulator. The signal transfer function, $S(z)$, and the quantization noise transfer function,

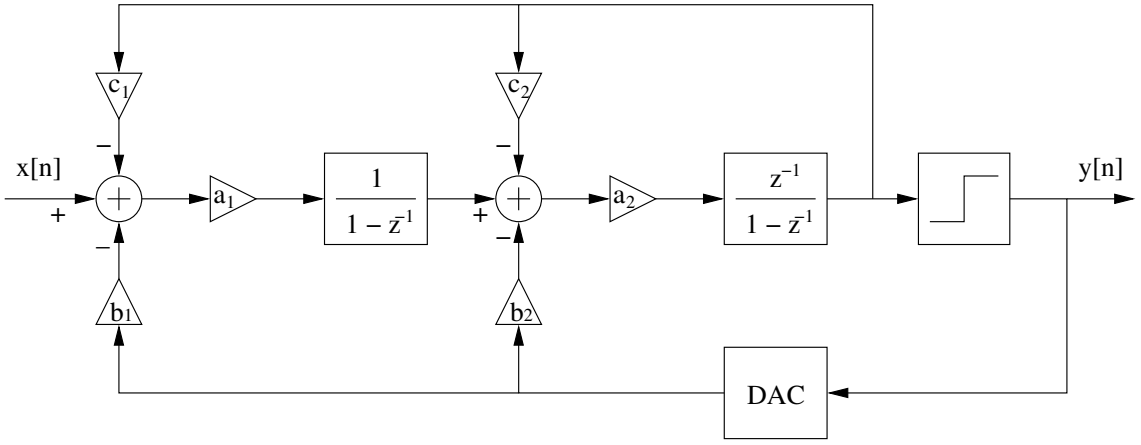


Figure 8.2: New implementation of second-order high-pass $\Delta\Sigma$ modulator based on classical second-order low-pass $\Delta\Sigma$ modulator.

$N(z)$, are given respectively by

$$S(z) = \frac{a_1\, a_2\, G\, z^{-1}}{1 + ((a_2(a_1(b_1\, G + c_1)) + b_2\, G + c_2) - 2)z^{-1} + (1 - a_2(b_2\, G + c_2))z^{-2}}, \tag{8.5}$$

$$N(z) = \frac{1 + (a_2\, c_2 - 2)z^{-1} + (1 + a_2(a_1\, c_1 - c_2))z^{-2}}{1 + ((a_2(a_1(b_1\, G + c_1)) + b_2\, G + c_2) - 2)z^{-1} + (1 - a_2(b_2\, G + c_2))z^{-2}}. \tag{8.6}$$

The conditions imposed to have a high-pass noise shaping is therefore

$$\begin{aligned} a_1\, a_2\, G &= 1 \\ a_2\, c_2 &= 4 \\ a_1\, c_1 &= c_2 \\ a_1\, b_1 &= b_2 \\ a_2\, b_2 G &= -3 \end{aligned} \tag{8.7}$$

In the same reasoning, we can introduce not only a simple gain in the extra feedback loops, but also a simple transfer function, such as a delay. An optimization

method in function of the stability, performance and complexity must be established. It would be an new idea to implement the high-pass modulator.

The set of proposed models in VHDL-AMS can be used for conventional $\Delta\Sigma$ modulators, but some improvements in terms of simulation speed would be welcome, since the simulation time is quite long at the moment. However, the time domain behavioral simulation in VHDL-AMS is promising because it can provide a very high accuracy.

Appendix A

Optimal Filter of Time-Interleaved $\Delta\Sigma$ Converter

In general, for a digital FIR filter of length-N we need $N-1$ cells of delay, $N-1$ adders and N multipliers, as shown in Figure A.1(a). It should be noted that Figure A.1(a) is not the single way to implement the digital FIR filters, but the number of basic cells remains the same when another techniques are employed. When the filter is symmetric, we can decrease by two the number of multipliers by grouping the equal coefficients, as shown in Figure A.1(b).

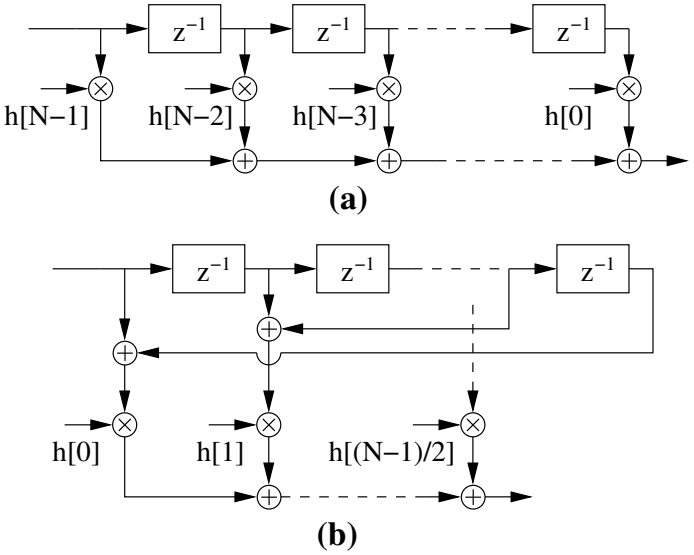


Figure A.1: (a) : FIR filter; (b) Symmetric FIR filter .

For a symmetric FIR filter of length-N (N is an odd number), theoretically we need $N-1$ cells of delay, $N-1$ adders and $(N-1)/2$ multipliers. In the case of the optimal filter, certain coefficients are zeros, this simplifies a little the hardware. Indeed, a zero coefficient involves the suppression of a couple of adder and multiplier. The optimal filter has $2 \times \left[\frac{N+1}{2M}\right]$ zero coefficients. This implies that $N-1-2 \times \left[\frac{N+1}{2M}\right]$ adders and $\frac{N-1}{2} - 2 \times \left[\frac{N+1}{2M}\right]$ multipliers are required for the optimal filter. Consequently, in the M optimal filters, there are $M\left(N-1-2 \times \left[\frac{N+1}{2M}\right]\right)$ adders and $M\left(\frac{N-1}{2} - 2 \times \left[\frac{N+1}{2M}\right]\right)$ multipliers.

Appendix B

PDF Estimation Method and VHDL-AMS Listing

B.1 PDF estimation method

If the generator output is denoted as $Vnoise$, then the PDF estimation consists of four steps as follows:

- Calculating the maximal and minimal values of V_{noise}, denoted as V_{noise}^{max} and V_{noise}^{min}, respectively;
- Dividing the interval $[V_{noise}^{min}, V_{noise}^{max}]$ in N equal segments;
- Calculating the probability in every N segments;
- If each segment is small enough, the probability density in itself is considered constant.

For 100000 values, $N = 200$, the same estimation method is applied to our model and data generated from MATLAB's function **randn**. The result from the model in VHDL-AMS is as good as the result from MATLAB. The least mean square error between estimated PDF and the theoretical PDF of $2.4\,10^{-5}$ for the model in VHDL-AMS and $1.8\,10^{-4}$ for MATLAB's function **randn**.

B.2 VHDL-AMS Listing

```
library disciplines;
use disciplines.electromagnetic_system.all;

entity sw_v0 is
  generic (
    ---- on off-resistance and transistion times
    ron  : real := 1.0E2;
    roff : real := 1.0E12;
    tr   : real := 1.0E-9;
    tf   : real := 1.0E-9;
    ----------------------
    ----recouvrement, body capacitors, leakage current
    Crec : real := 1.0e-15;
    Cox  : real := 0.0;
    Cb   : real := 1.0e-14;
    Ifsd : real := 1.0e-15
  );
  port (
    terminal S :    electrical;
    terminal D :    electrical;
    signal   h : in bit
  );
end entity sw_v0;

architecture simple of sw_v0 is
  terminal G : electrical;
  quantity v across i through S to D;
  quantity ip through S;
  quantity im through D;
  signal   reff : real := roff;
begin
  P1 : process
  begin
    if h = '1' then
```

```
      reff <= ron;
    else
      reff <= roff;
    end if;
    wait on h;
  end process;
  i == v / reff'ramp(tr, tf);
  Crec1 : entity work.capa(bhv)
        generic map( Crec )
        port map (G, S);
  Crec2 : entity work.capa(bhv)
        generic map( Crec )
        port map (G, D);
  Cox1 : entity work.capa(bhv)
        generic map( Cox )
        port map (G, S);
  Cox2 : entity work.capa(bhv)
        generic map( Cox )
        port map (G, D);
  Cb1 : entity work.capa(bhv)
        generic map( Cb )
        port map (S, electrical_ground);
  Cb2 : entity work.capa(bhv)
        generic map( Cb )
        port map (D, electrical_ground);
  ip == Ifsd;
  im == Ifsd;
end architecture simple;
```

Listing B.1: Model of switch in VHDL-AMS where on-resistance, off-resistance, parasitic capacitances and leakage current are taken into account.

```
library ieee, disciplines;
use ieee.std_logic_1164.all;
use disciplines.electromagnetic_system.all;

entity Comparator is
```

```
  generic (
    vlo, vhi: REAL :=0.0; -- thresholds
    timeout: DELAY_LENGTH
  );
  port (
    terminal ain, ref: electrical;
    signal h : in bit;
    signal dout: out std_logic
  );
end entity Comparator;

architecture Hysteresis of Comparator is
  type states is (unknown, zero, one, unstable);
  quantity vin across ain to ref;
  function level( vin, vlo, vhi: REAL) return states is
    begin
      if vin < vlo then return zero;
      elsif vin > vhi then return one;
      else return unknown;
      end if;
  end function level;
  begin
    process
      variable state: states := level( vin, vlo, vhi);
      begin
      if (h = '1') then
        case state is
          when one =>
            dout <= '1';
            wait on vin'Above(vhi); -- wait for change
                    state := unstable;
          when zero =>
            dout <= '0';
            wait on vin'Above(vlo); -- wait for change
            state := unstable;
```

```
            when unknown =>
               dout <= 'X';
               wait on vin'Above(vhi), vin'Above(vlo);
               state := level( vin, vlo, vhi);
            when unstable =>
                wait on vin'Above(vhi), vin'Above(vlo) for timeout;
                state := level(vin, vlo, vhi);
         end case;
       end if;
       wait on h;
    end process;
end architecture Hysteresis;
```

Listing B.2: Model of comparator with hysteresis in VHDL-AMS.

Appendix C

Résumé étendu

Ce travail de recherche est focalisé exclusivement sur l'extension de modulateur $\Sigma\Delta$ sur les applications de large bande. Nous proposons dans ce travail un nouveau modulateur $\Sigma\Delta$ qui n'est jamais étudié auparavant. Il s'agit du modulateur $\Sigma\Delta$ passe-haut. Ensuite, ces nouveaux modulateurs sont combinés avec l'entrelacement temporel pour améliorer la performance du modulateur $\Sigma\Delta$ parallèle, qui est une extension très prometteuse du modulateur $\Sigma\Delta$ conventionnel pour les applications de très large bande. Ce manuscrit est décomposé de huit chapitres, y compris un chapitre d'introduction, et écrit en anglais, car ce travail est effectué dans le cadre d'un projet européen.

C.1 Architecture des CANs

Il y a beaucoup de recherches sur la conception de convertisseur analogique-numérique, et pas mal de techniques et méthodes pour la conversion analogique-numérique ont été développées. Dans ce chapitre, quelques architectures importantes et essentielles est introduites et comparées. Différentes architectures d'un convertisseur analogique-numérique sont présentées. Leur principe de fonctionnement, leurs avantages et inconvénients, et leur domaine d'applications sont évoqués. Chaque architecture a ses avantages et ses inconvénients, et chacune a son ensemble d'applications pour lequel elle est la meilleure solution.

En résumé, on peut les regrouper en trois grandes famille de convertisseurs: la famille flash, la famille pipeline et la famille $\Sigma\Delta$. Les convertisseurs flash sont sans

doute les plus rapides. Ils peuvent actuellement atteindre une vitesse de quelques giga-échantillons par second. Cependant ils ont une précision relativement faible. La résolution maximale obtenue par ce type de convertisseur ne dépasse pas 8 bits.

Les convertisseurs pipeline sont une solution intermédiaire entre la conversion de grande vitesse et de grande précision. Grâce à des méthodes de calibration numérique, ce type de convertisseur peut avoir actuellement une résolution relativement élevée (de l'ordre de 14 bits). Un avantage des convertisseurs pipeline est qu'ils sont capables de donner une précision désirée avec une fréquence d'échantillonnage voulue à condition que la première ne soit pas trop élevée. Certains annoncent que la précision du convertisseur pipeline peut être comparable à celle du convertisseur $\Sigma\Delta$ grâce au développement des méthodes de calibration numérique.

Les convertisseurs $\Sigma\Delta$ sont sans doute les plus précis. Ils peuvent avoir une résolution de 24 bits. En dehors de haute résolution, ils ont beaucoup d'autres propriétés attractives, notamment la grande dynamique et grande linéarité. L'inconvénient majeur de ce type de convertisseur est la bande passante limitée à cause du suréchantillonnage. Vu de leurs nombreuses propriétés intéressantes, beaucoup de recherches sont faites pour augmenter la bande du signal d'entrée en basant sur le principe de la modulation $\Sigma\Delta$ comme convertisseur $\Sigma\Delta$ parallèle. Mais ce type de convertisseur reste encore dans le domaine de recherche. Il reste pas mal de choses à faire avant de l'industrialiser peut-être un jour.

Comme le convertisseur $\Sigma\Delta$ parallèle, les convertisseurs utilisant les bancs de filtres hybrides sont prometteurs. Mais ils restent encore dans le domaine de la recherche. Seulement l'architecture à entrelacement temporel a vu le jour dans l'industrie.

C.2 Modulateur $\Sigma\Delta$ passe-haut

Le modulateur $\Sigma\Delta$ passe-haut est basé exactement sur le même principe que le modulateur $\Sigma\Delta$ passe-bas, à savoir le bruit de quantification est mis en forme et dégagé hors de la bande du signal d'entrée par le boucle de retour. La seule différence est la position de la bande du signal, qui est maintenant située au tour de la moitié de la fréquence d'échantillonnage, au lieu de la bande de base pour le modulateur $\Sigma\Delta$ conventionnel. Le bloc de base du modulateur passe-haut a une fonction de

transfert qui est la suivante :

$$H_{hp}(z) = \frac{z^{-1}}{1 + z^{-1}}. \tag{C.1}$$

Par conséquent, le modulateur ΣΔ passe-haut peut être réalisé en appliquant la transformation $z \rightarrow -z$ au modulateur ΣΔ passe-bas.

L'architecture et le principe du modulateur ΣΔ passe-haut sont présentés et étudiés dans ce chapitre. La performance idéale d'un modulateur ΣΔ passe-haut est équivalente à celle du modulateur passe-bas correspondant. Pour un modulateur passe-haut d'ordre L, un $L + 1/2$ bits de résolution est gagné pour chaque doublement d'OSR. Une implémentation en technique des capacités commutées du filtre passe-haut, le bloc de base du modulateur passe-haut, est proposée en basant sur l'introduction d'une boucle de retour supplémentaire autour de l'intégrateur comme montrée dans Figure C.1. De ce fait, le problème d'instabilité du modulateur ΣΔ

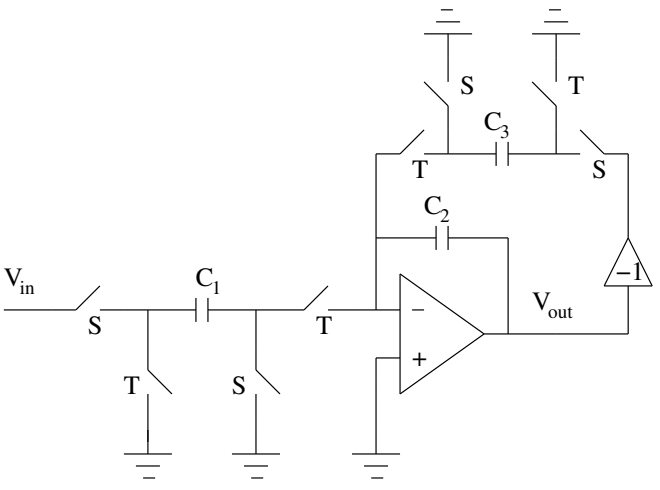


Figure C.1: Implémentation en capacités commutées du bloc de base du modulateur ΣΔ passe-haut.

passe-haut est plus compliqué que celui du modulateur ΣΔ conventionnel. Ce problème est étudié et analysé par les algorithmes d'optimisation et par des méthodes de simulations rapides. Les simulations indiquent que le modulateur reste stable à condition que l'erreur de pole du filtre passe-haut est approximativement inférieur à 2,4%. Si cette erreur de pole est plus petite que 1%, alors la dégradation de la performance du modulateur ΣΔ passe-haut est négligeable. Cette condition exige que l'erreur sur le rapport capacitif soit de l'ordre de 1%.

L'analyse théorique et résultat de simulation prouvent que ce genre de modulateur élimine complètement le bruit de basse fréquence. Par conséquent, il est très utile et attrayant pour des applications exigeant haute résolution et large bande. Cependant, l'analyse de l'effet de nonidealités sur le performance du modulateur passe-haut est nécessaire pour établir ses limitations pratiques.

C.3 Convertisseurs ΣΔ combinant avec l'entrelacement temporel

Le convertisseur ΣΔ en combinant avec l'entrelacement temporel est une forme de convertisseur ΣΔ parallèle. L'avantage du convertisseur ΣΔ en combinant avec l'entrelacement temporel est sa complexité réduite. L'utilisation des modulateurs ΣΔ dans l'architecture parallèle peut permettre à la technique de conversion basant sur la modulation ΣΔ d'être appliquée aux applications de large bande.

Une structure simple de l'architecture du convertisseur ΣΔ en combinant avec l'entrelacement temporel est montrée dans la figure C.2. Elle se compose de M canaux parallèles contenant un modulateur ΣΔ passe-bas et un filtres de canal passe-bas. Pendant que le signal d'entrée n'est pas appliqué au modulateur, l'entrée est connectée à la masse.

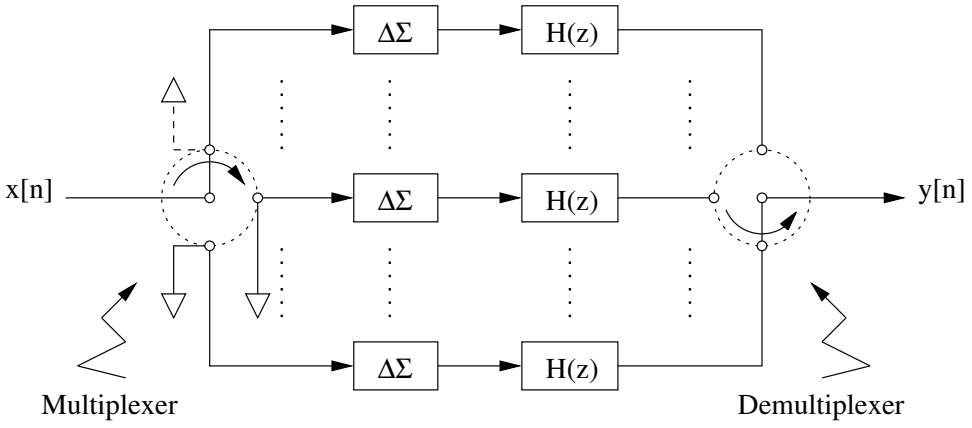


Figure C.2: Architecture du convertisseur ΣΔ en combinant avec l'entrelacement temporel.

Le filtre de canal joue un rôle particulièrement important dans cette architecture,

car il doit non seulement éliminer le bruit de quantification hors de bande, mais également respecter le principe de reconstruction parfaite du signal d'entrée. Un problème d'optimisation sous contraints est donc posé. Pour trouver le filtre de canal optimal et estimer la performance idéale de ce type d'architecture, nous avons utilisé la méthode d'analyse temporelle de l'évolution du signal d'entrée. La performance idéale du système peut être calculée en fonction de l'ordre des modulateurs utilisés et du nombre de canaux.

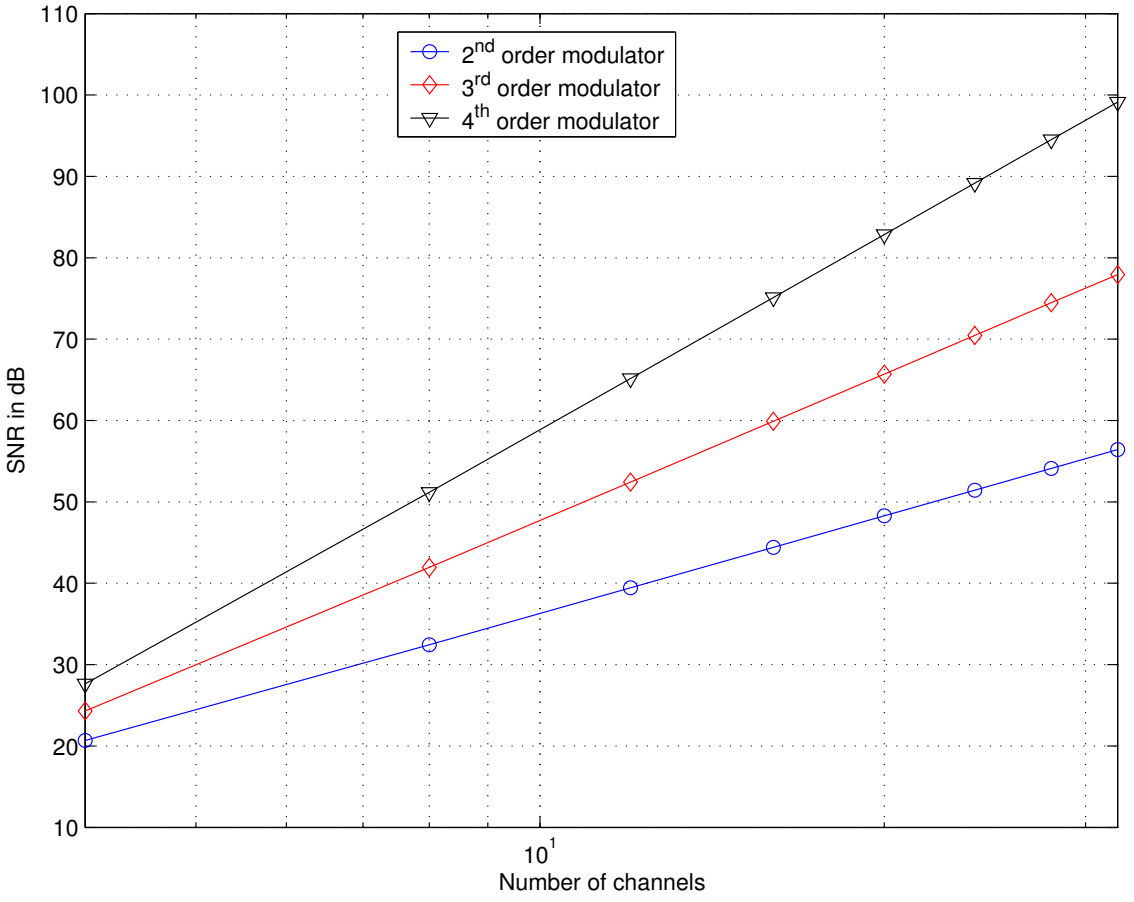


Figure C.3: La dynamique idéale du convertisseur ΣΔ en combinant avec l'entrelacement temporel avec des filtres de canal idéaux en fonction du nombre de canaux pour trois modulateurs différents.

Comme montré dans Figure C.3, pour un système contenant de M modulateurs ΣΔ d'ordre L, approximativement L-bit de résolution est obtenu pour chaque doublement du nombre de canaux. Par conséquent, le nombre de canaux joue presque le même rôle que l'OSR dans le convertisseur ΣΔ conventionnel.

Cependant, ce genre de convertisseur est sensible au comportement nonideal de circuit, en particulier à la disparité entre les canaux. Pour minimiser ce problème, nous proposons une nouvelle architecture en utilisant les modulateurs ΣΔ passe-haut au lieu des modulateurs passe-bas. La performance idéale du convertisseur ΣΔ passe-haut en combinant avec l'entrelacement temporel est identique à celle du convertisseur utilisant des modulateurs ΣΔ passe-bas, mais avec l'avantage de l'immunité à la disparité entre les canaux. En revanche, celui proposé a besoin d'un nombre paire de canaux. Concernant la disparité de gain de canal, une méthode adaptative d'égalisation de gain de canal basée sur l'algorithme de LMS, est proposée et étudiée afin de réduire au minimum l'effet de cette disparité. En outre, le convertisseur ΣΔ passe-haut en combinant avec l'entrelacement temporel est obtenu à partir du convertisseur ΣΔ passe-bas en combinant avec l'entrelacement temporel sans ajouter aucune complexité supplémentaire au niveau du matériel. L'analyse est générale parce qu'elle ne place aucune restriction significative sur les types de modulateurs ΣΔ. Les idées ont présenté en ce chapitre peuvent permettre l'application du modulateur ΣΔ dans des applications de très large bande telles que le traitement de vidéo ou la radio numérique.

C.4 Méthodologie de conception avec VHDL-AMS

Un problème significatif dans la conception des modulateurs ΣΔ en général et les modulateurs ΣΔ passe-haut en particulier, est l'évaluation de l'effet de nonidéalités sur leur performance, et leur performance elle-même, puisqu'ils sont les circuits mixtes et non-linéaires. En raison de la non-linéarité inhérente de la boucle de retour du modulateur, l'optimisation de la performance doit être effectuée avec des simulations comportementales dans le domaine temporel. Naturellement, la simulation de niveau de circuit est la plus précise. Cependant, l'évaluation des nonidealities de circuit et l'optimisation des blocs constituant le modulateur sont très difficile en raison du long temps de simulation. D'ailleurs, pour le modulateur passe-haut, il est très important de déterminer la valeur de seuil du rapport capacitif permettant la stabilité du modulateur. Une telle détermination est impossible avec des simulations électriques. Une étape intermédiaire des simulations comportementales est donc nécessaire. Par les modèles à multiniveaux d'abstraction, VHDL-AMS permet de surmonter ces problèmes.

Dans ce chapitre, nous présentons une méthodologie de conception descendante avec VHDL-AMS. Un ensemble de modèles en VHDL-AMS approprié à la simulation comportementale des modulateurs ΣΔ en technique des capacités commutés est développé et présenté. L'ensemble de modèles proposé tient compte au niveau comportemental la plupart des nonidealities du modulateur ΣΔ en technique des capacités commutés, telles que le bruit jitter, le bruit kT/C, le bruit $1/f$, le bruit de l'amplificateur, des nonidealities du commutateur, des nonidealities de l'amplificateur, et l'erreur sur le rapport capacitif. Ceci nous permet d'étudier l'effet de divers paramètres de nonidealité sur la performance du modulateur ΣΔ passe-haut et définir l'ensemble de valeur de seuil des paramètres de nonidealité assurant une performance désirée du modulateur comme montré dans Table C.1.

Nonidealité	Paramètre	Valeur de seuil
Jitter	ΔT	$<$ 0.1ns
Bruit kT/C)	C	$>$ 10fF
Bruit d'amplificateur	E_{amp}	$<$ 0.2mV_{rms}
R_{on} de l'interrupteur	Ron	$<$ 1KΩ
Capacité parasite de l'interrupteur	Crec + WLCox	$<$ 30fF
Courant de fuite	Ifd	$<$ 0.1 μA
Gain fini	$Gain$	$>$ 60 dB
Fréquence de transition	f_t	$>$ 160 MHz
Slew-rate	SR	$>$ 50V/μs
Saturation	Vmax	$>$ 1.4V
Erreur sur le rapport capacitif		$<$ 0.5%

Table C.1: Spécifications des différents paramètres de nonidéalité pour obtenir une performance de moins 3 dB de la performance idéale d'un modulateur ΣΔ passe-haut d'ordre 2.

Cette méthodologie nous permet non seulement d'obtenir la spécification de chaque composant élémentaire du modulateur ΣΔ et d'estimer sa performance, mais également d'optimiser de divers paramètres de nonidealité pour obtenir une bonne performance du modulateur. Ceci est vraiment utile pour la conception du modulateur ΣΔ passe-haut, parce qu'à la différence du modulateur passe-bas, un problème important du modulateur passe-haut avec l'implémentation proposée du filtre passe-haut, est la stabilité du modulateur et l'amplification du bruit d'amplificateur à la

sortie du modulateur.

C.5 Implémentation

L'objectif de ce chapitre est de réaliser le modulateur ΣΔ passe-haut d'ordre 2 pour valider le concept de ce genre de modulateur et démontrer ses avantages comparés au modulateur passe-bas. Afin d'illustrer les avantages du modulateur passe-haut dans le convertisseur ΣΔ combinant avec l'entrelacement temporel, deux modulateurs ΣΔ passe-haut sont mis en entrelacement temporel. L'implémentation du modulateur ΣΔ passe-haut d'ordre 2 est décrite dans ce chapitre. L'implémentation complètement différentielle en technique des capacités commutées du filtre passe-haut qui produit la fonction de transfert désirée est réalisée, et ses limitations dues au bruit du commutateur et de l'amplificateur sont analysées. Un amplificateur à deux étages avec 75 dB de gain, 83 v/μs de slew-rate, et 175 MHz de fréquence de transition, est conçu pour assurer des spécifications dérivées des simulations de VHDL-AMS quand le filtre passe-haut fonctionne à 10 MHz.

Les circuits additionnels dans le prototype incluent le circuit polarisé, le comparateur et le générateur d'horloge. Le comparateur est un simple comparateur dynamique suivi d'une bascule RS. Une analyse de bruit du modulateur indique que le bruit d'amplificateur dans le premier filtre passe-haut est mis en forme pour avoir une densité spectrale maximale dans la bande de signal centrée à la moitié de la fréquence d'échantillonnage. Cet amplification dangereuse du bruit dégrade la dynamique du modulateur par une marge substantielle, à moins qu'un amplificateur soit conçu avec une assez faible bruit, tels qu'à la sortie du modulateur, le niveau du bruit d'amplificateur mis en forme dans la bande passante reste comparables au niveau du bruit de kT/C.

C.6 Conception des masques et carte de test

Le prototype d'un modulateur ΣΔ passe-haut d'ordre 2 et un convertisseur ΣΔ passe-haut en combinant avec l'entrelacement temporel est montré dans Figure C.4. Le premier tiers du prototype est le modulateur ΣΔ passe-haut d'ordre 2. Les signaux d'entrée différentiels sont appliqués d'abord au chopper et puis le modu-

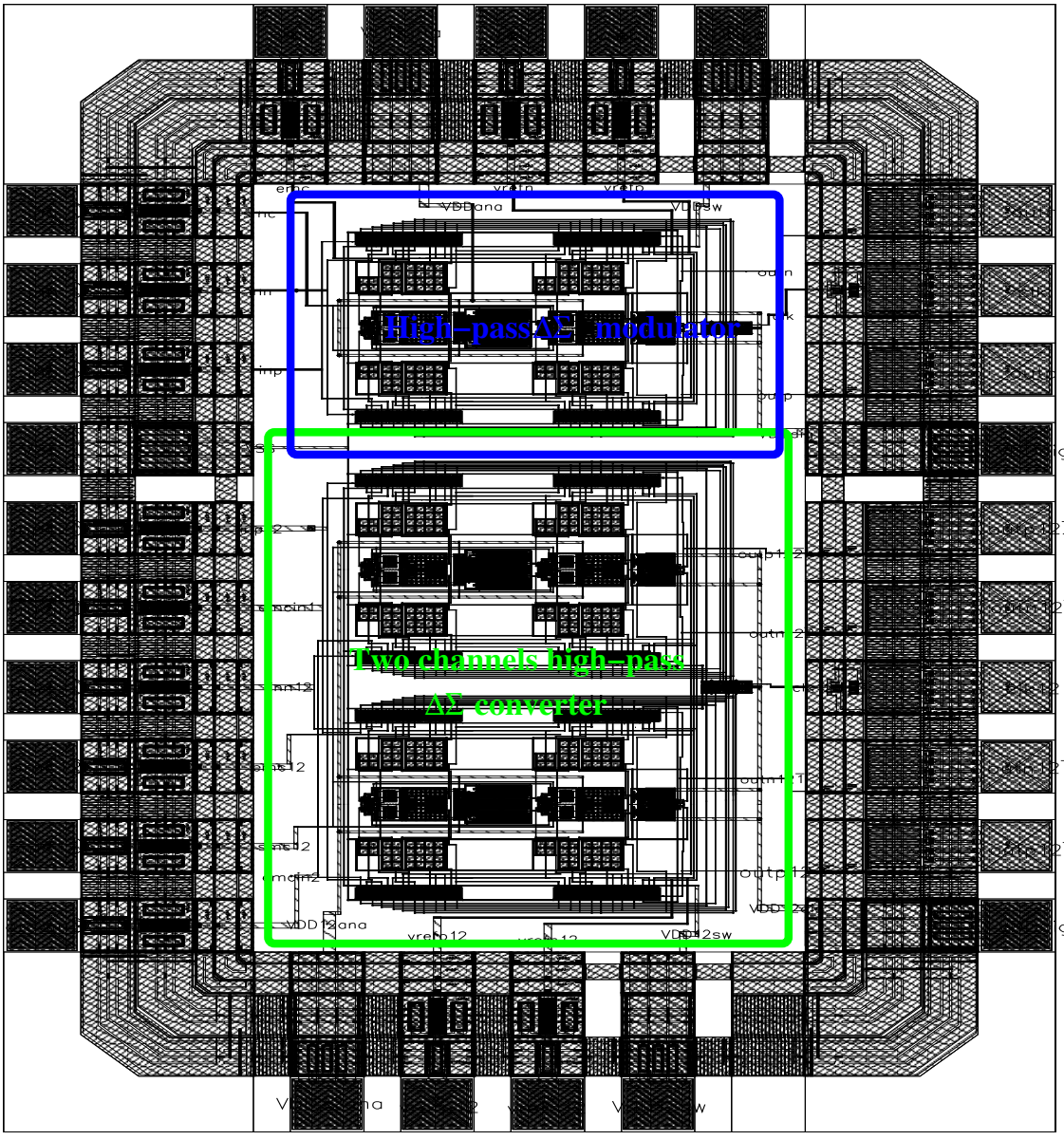


Figure C.4: Dessin de masque du modulateur ΣΔ passe-haut d'ordre 2 et du convertisseur ΣΔ passe-haut en conbinant avec l'entrelacement temporel.

lateur passe-haut qui est à la gauche. Le circuit numérique, vu à la droite, est physiquement séparé des circuits analogues et est alimenté à partir d'une alimentation séparée. L'utilisation de différentes alimentations analogique et numérique découple les circuits analogues du bruit de commutation provoqué par de grands courants dynamiques tirés de l'alimentation numérique. Les deux derniers tiers du prototype se composent de deux modulateurs $\Sigma\Delta$ passe-haut d'ordre 2 identiques sans chopper en entrelacement temporel. La surface totale du prototype est 1,33 mm x 2,05 mm, mais la surface active mesure seulement 0,6mm x 1,37mm.

La stabilité du modulateur $\Sigma\Delta$ passe-haut est affectée par l'erreur sur le rapport capacitif du filtre passe-haut. Cette erreur peut causer le pole du filtre passe-haut en dehors du cercle d'unité. Les capacités sont constitués en reliant des cellules d'unité de 500 fF. Selon des règles de conception d'AMS, l'erreur sur le rapport capacitif est moins de 0,2%, qui est largement supérieur à 1%, la condition nécessaire pour la stabilité du modulateur.

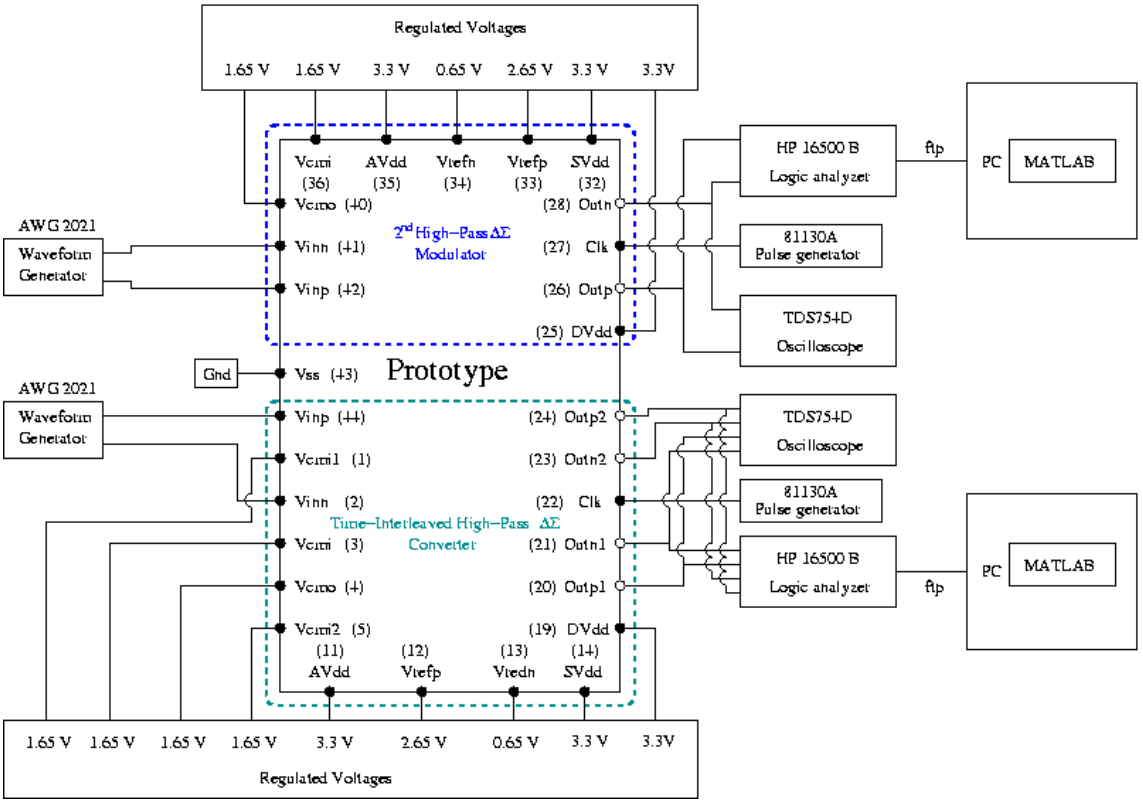


Figure C.5: Diagramme de la carte de test.

Le diagramme de la carte de test est présenté dans Figure C.5. Le test le plus important est le test de la fonctionnalité du modulateur passe-haut avant de mesurer

sa performance et ses avantages dans le convertisseur ΣΔ parallèle. Les tensions d'alimentation sont générées du régulateur de tension MC33275. De diverses tensions de référence représentées sur Figure C.5 sont générées par les régulateurs réglables M317L. Le générateur d'impulsion permet pour avoir un signal d'horloge pour le circuit complet. La performance prévue du modulateur ΣΔ passe-haut d'ordre 2 est présentée dans Table C.2.

Spécifications	Résultat prévu
Alimentation	3.3 V
Consommation	42.44 mW
Fréquence d'échantillonnage	10 MHz
Fréquence du signal d'entrée	15 KHz
OSR	32
Distorsion harmonique	-65 dB
SNR	54.5 dB
SNDR	53.6 dB

Table C.2: Performance du modulateur ΣΔ passe-haut d'ordre 2.

C.7 Conclusions

Le modulateur ΣΔ passe-haut est étudié et analysé. Ce type de modulateur met en forme le bruit de quantification et le dégage à la basse fréquence. La bande de signal à l'entrée du modulateur passe-haut est située autour de la moitié de la fréquence d'échantillonnage. Par conséquent le modulateur passe-haut est complètement immunisé au bruit de basse fréquence. Pour un modulateur passe-haut d'ordre L r, $L + 1/2$ bits de résolution est gagné pour chaque doublement d'OSR. Le filtre passe-haut, le bloc de base construisant le modulateur passe-haut, peut être implémenté en technique des capacitées commutées en basant sur l'introduction d'une boucle de retour supplémentaire autour de l'intégrateur, le bloc de base du modulateur conventionnel. Les modulateurs ΣΔ passe-haut peuvent être utilisés en tant que modulateurs autonomes en ajoutant un chopper à l'entrée du modulateur. Ce

modulateur passe-haut chopper-stabilisé qui est équivalent au modulateur conventionnel Avec l'avantage d'immunité au bruit de basse fréquence, est bien convenu à des applications de basse fréquence dont l'amplitude du signal est faible.

Elles sont également très intéressant pour les convertisseurs $\Sigma\Delta$ parallèle, notamment celui combinant avec l'entrelacement temporel, à condition que le nombre de canaux soit paire. L'utilisation des modulateurs $\Sigma\Delta$ passe-haut au lieu des modulateurs passe-bas dans ce genre de convertisseur préserve la performance du convertisseur, mais avec l'avantage additionnel de l'immunité contre la disparité de l'offset entre les canaux. On a proposé aussi une méthode adaptative simple mais efficace en utilisant l'algorithme LMS pour réduire l'effet de disparité de gain des canaux. Cette méthode simple est efficace, car les offsets des canaux sont complètement éliminés par les modulateurs passe-haut. Ces techniques permettent de réduire sensiblement l'effet de disparité entre les canaux dans une architecture parallèle.

Un ensemble de modèles en VHDL-AMS pour la simulation comportementale des modulateurs $\Sigma\Delta$ en capacités commutées dans le domaine temporel est développé afin d'analyser l'effet de nonidealité dans le modulateur $\Sigma\Delta$ passe-haut et améliorer la conception de modulateur. L'ensemble de modèles proposé tient compte au niveau comportemental des nonidealities de modulateur $\Sigma\Delta$ en capacités commutées, telles que le bruit jitter, le bruit $kT/$, le bruit $1/f$, le bruit d'amplificateur, des nonidealities du commutateur, des nonidealities d'amplificateur, et l'erreur du rapport capacitif. Ceci nous permet d'étudier l'effet de divers paramètres de nonidealité sur le modulateur $\Sigma\Delta$ passe-haut et de définir un ensemble de valeur de seuil des paramètres de nonidealité pour assurer une performance désirée du modulateur. Cette méthodologie nous permet non seulement de faire des spécifications de chaque dispositif élémentaire du modulateur et d'estimer sa performance, mais également d'optimiser de divers paramètres de nonidealité pour obtenir une bonne performance du modulateur $\Sigma\Delta$.

Un prototype d'un modulateur $\Sigma\Delta$ passe-haut d'ordre 2 et d'un convertisseur $\Sigma\Delta$ en combinant avec l'entrelacement temporel, a été conçu et fabriqué en technologie CMOS 0,35μm d'AustriaMicroSystems. La surface totale du prototype est 1,33mm x 2,05mm, mais la surface active mesure seulement 0,6mm x 1,37mm. La puissance de consommation prévue est de 127,5 mW. La performance prévue du modulateur passe-haut est de 54,5 le dB de SNR avec la fréquence d'échantillonnage de 10 MHz pour un taux de suréchantillonnage de 32.

Bibliography

[1] J. C. Candy and G. C. Termes. *"Oversampling methods for A/D and D/A Conversion", in* Oversampling Delta-Sigma Data Converter Theory, Design and Simulation. New York: IEEE Press, 1992. 1, 14, 17, 53, 62, 66

[2] O. Oliaei. *"Technique des courants commutés pour les convertisseurs a sur-échantillonnage ou sous-échantillonnage"*. PhD dissertation, Ecole nationale supérieur des télécommunications, 1997. 1, 13, 54

[3] I. Galton and H. T. Jensen. "Delta-Sigma Modulator Based A/D Conversion without Oversampling". *IEEE Trans. on Circuits and Systems-II*, 43(12):773–784, Dec. 1995. 1, 14, 54

[4] A. Esgraghi. *"High-Speed Parallel Delta-Sigma Analog-to-Digital Converters"*. PhD thesis, Wanshinton State University, 1999. Ph.D Dissertation. 1, 14, 54

[5] A. G. F. Dingwall. "Monolithic expandable 6 bit 20 MHz CMOS/SOS A/D converters". *IEEE J. Solid-State Circuits*, vol.SC-14(no.6):pp.926–932, Dec. 1979. 5

[6] D. H. Sheingold. *"Analog-Digital Conversion Handbook"*. pp.218-219. Englewood Cliffs, New Jersey: Prentice-Hall, 1986. 5

[7] A. K. Joy, R. J. Killips, and P. H. Saul. "An Inherently mnotonic 7-Bit CMOS ADC for video applications". *IEEE J. Solid-State Circuits*, SC-21(3):436–440, Jun. 1986. 5

[8] T. Kumamoto, M. Nakaya, H. Honda, S. Asai, Y. Akasaka, and Y. Horiba. "An 8-bit High Speed CMOS ADC". *IEEE J. Solid-State Circuits*, SC-21(6):976–982, Dec. 1986. 5

[9] C. W. Mangelsdorf. "A 400-MHz Input Flash Converter with Error Correction". *IEEE J. Solid-State Circuits*, 25(1):184–191, Feb. 1990. 5

[10] K. J. McCall, M. J. Demler, and M. W. Plante. "A 6-bit 125 MHz CMOS A/D Converter". *in Proc. CICC*, pages 16.8.1–16.8.4, May 1992. 5

[11] C. Donovan and M. P. Flynn. "A "Digital" 6-bit ADC in 0.25-μm CMOS". *IEEE J. Solid-State Circuits*, 37(3):432 – 437, March 2002. 5

[12] R. J. van de Plassche and R. E. J. van der Grift. "A High Speed 7 Bit A/D Converter". *IEEE J. Solid-State Circuits*, SC-14(6):938–943, Dec. 1979. 7

[13] T. Shimizu, M. Hotto, K. Maoi, and S. Ueda. "A 10-bit 20-MHz Two-Step Paralllel A/D Converter with Internal S/H". *IEEE J. Solid-State Circuits*, 24(1):13–20, Feb. 1989. 7

[14] M. K. Mayes and S. W. Chin. "A Mutistep A/D Converter Famlily with Efficient Architecture". *IEEE J. Solid-State Circuits*, 24(6):1492–1497, Dec. 1989. 7

[15] J. Doernberg, P. R. Gray, and D. A. Hodges. "A 10-bit 5-MSample/s CMOS Two-Step Flash ADC". *IEEE J. Solid-State Circuits*, 24(2):241–249, Avril 1989. 7

[16] B. Razavi and B. A. Wooley. "A 12-b 5-MSample/s Two-Step CMOS A/D Converter". *IEEE J. Solid-State Circuits*, 27(12):1667–1678, Dec. 1992. 7

[17] R. E. J. van de Grift, I. W. J. M. Rutten, and M. van der Veen. "An 8-bit Video ADC Incorporating Folding and Interpolation Techniques". *IEEE J. Solid-State Circuits*, SC-22(6):944–953, Dec. 1987. 8

[18] R. J. van de Plassche and P. Baltus. "AAn 8-bit 100-MHz Full-Nyquist Analog-to-Digital Converter". *IEEE J. Solid-State Circuits*, 23(6):1334–1344, Dec. 1988. 8

[19] J. van Valburg and R. J. van de Plassche. "An 8-bit 650-MHz Folding ADC". *IEEE J. Solid-State Circuits*, 27(12):1662–1666, Dec. 1992. 8

[20] M. P. Flynn and D. J. Allstot. "CMOS Folding ADCs with Current-Mode Interpolation". *ISSCC Dig. Tech. Papers*, pages 274–278, Feb. 1995. 8

[21] B. Nauta and A. G. W. Venes. "A 70 MSample/s 110 mW 8 b CMOS Folding Interpolation A/D Conveter". *ISSCC Dig. Tech. Papers*, pages 276–279, Feb. 1995. 8

[22] A. G. F. Dingwall and V. Zazzu. "An 8-bit 8-MHz CMOS Subraging 8-Bit A/D Converter". *IEEE J. Solid-State Circuits*, SC-20(6):1138–1143, Dec. 1985. 8

[23] J. Fermandes, S. R. Lewis, A. M. Mallinson, and Gerald A. Miller. "An 14-bit μs Subranging A/D Converter with S/H". *IEEE J. Solid-State Circuits*, 23(6):1309–1315, Dec. 1988. 8

[24] M. Ishikawa and T. Tsukahara. "An 8-bit 50-MHz CMOS Subranging A/D Converter with Pipelined Wide-Band S/D". *IEEE J. Solid-State Circuits*, 24(6):1485–1491, Dec. 1989. 8

[25] M. P. V. Kolluri. "A 12-bit 500-ns Subranging ADC". *IEEE J. Solid-State Circuits*, 24(6):1498–1506, Dec. 1989. 8

[26] R. Petschacher, B. Zojer, B. Astegher, H. Jessner, and A. Lechner. "A 10-b 75-MSPS Cubranging A/D Converter with Integrated Sample and Hold". *IEEE J. Solid-State Circuits*, 25(6):1339–1346, Dec. 1990. 8

[27] D. A. Mercer. "A 14-b 750-ns Subranging ADC with Slf-Correcting S/H". *IEEE J. Solid-State Circuits*, 26(12):1790–1799, Dec. 1991. 8

[28] B. P. Brandt and J. Lutsky. "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist". *IEEE J. Solid-State Circuits*, 34(2):1788 – 1795, Dec. 1999. 8

[29] R. C. Taft and M. R. Tursi. "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V". *IEEE J. Solid-State Circuits*, 36(3):331 – 338, March 2001. 8

[30] J. L. McCreay and P. R. Gray. "ALL-MOS Charge Redistribution Analog-to-Digital Conversion Tecniques-Part I". *IEEE J. Solid-State Circuits*, SC-10:371–379, Dec. 1975. 9

[31] R. E. Suarez, P. R. Gray, and D. A. Hodges. "ALL-MOS Charge Redistribution Analog-to-Digital Conversion Tecniques-Part II". *IEEE J. Solid-State Circuits*, SC-10:379–385, Dec. 1975. 9

[32] A. R. Hamade. "A Single Chip ALL-MOS 8-Bit A/D Converter". *IEEE J. Solid-State Circuits*, SC-13(6):785–791, Dec. 1978. 9

[33] T. P. Redfern, J. J. Connolly, S. W. Chin, and T. M. Frederiksen. "A Monolithic Charge-Balancing Successive Approximation A/D Technique". *IEEE J. Solid-State Circuits*, SC-14(6):912–920, Dec. 1979. 9

[34] B. Fotouhi and D. A. Hodges. "High-Resolution A/D Converter in MOS/LSI". *IEEE J. Solid-State Circuits*, SC-14(6):920–926, Dec. 1979. 9

[35] J. J. Connolly, T. P. Redfern, S. W. Chin, and T. M. Frederiksen. "A Monolithic 12b+Sign Successive Approximation A/D Converter". *ISSCC Dig. Tech. Papers*, pages 12–13, Feb. 1980. 9

[36] M. P. Timko and P. R. Holloway. "Techniques for Achieving High Speed-High Resolution A/D Conversion". *IEEE J. Solid-State Circuits*, SC-15(6):1040–1051, Dec. 1980. 9

[37] Z. G. Boyacigiller, B. Weir, and P. D. Bradshaw. "An Error-Correcting 14b/20ms CMOS A/D Converter". *IISSCC Dig. Tech. Papers*, pages 62–63, Feb. 1981. 9

[38] P. H. Saul. "Successive Approximation Analog-to-Digital Conversion at Video Rates". *IEEE J. Solid-State Circuits*, SC-16(3):147–151, June 1981. 9

[39] P. A. Crolla. "A Fast Latching Current Comparator for 12-Bit A/D Applications". *IEEE J. Solid-State Circuits*, SC-17(6):1088–1094, Dec. 1982. 9

[40] R. J. van de Plassche and H. J. Schouwenaars. "A Monolithic 14 Bit A/D Converter". *IEEE J. Solid-State Circuits*, SC-17(6):1112–1117, Dec. 1982. 9

[41] P. Wai Li, M. J. Chin, P. R. Gray, and R. Castello. "Ratio-Independent Algorithmic Analog-to-Digital Conversion Technique ". *IEEE J. Solid-State Circuits*, SC-19(6):828–836, Dec. 1984. 9

[42] J. Croteau, D. Kerth, and D. Welland. "Autocalibration cements 16-bit performance". *Solid-State Circuits*, SC-14(6):101–106, Sept. 1986. 9

[43] K. Bacrania. "A 12-Bit Successive-Approximation-Type ADC with Digital Error Correction". *IEEE J. Solid-State Circuits*, SC-21(6):1016–1025, Dec. 1986. 9

[44] Y. Manoli. "A Self-Calibration Metho for Fast High-Resolution A/D and D/A converters". *IEEE J. Solid-State Circuits*, 24(3):603–608, Dec. 19789. 9

[45] R. K. Hester, K. S. Tan, M. de Wit, J. W. Fattaruso, S. Kiriaki, and J. R. Hellums. "Fully Differential ADC with Rail-to-Rail Common-Mode Range and Nonlinear Capacitor Compensation". *IEEE J. Solid-State Circuits*, 25(1):173–183, Dec. 1990. 9

[46] K. Hadidi, V. S. Tso, and G. C. Temes. "An 8-b 1.3-MHz Successive-Approximation A/D Converter". *IEEE J. Solid-State Circuits*, SC-14(6):880–885, June 1990. 9

[47] K. S. Tan, S. Kiriaki, M. de Wit, J. W. Fattaruso, C. Y. Tsay, W. E. Matthews, and R. K. Hester. "Error Correction Techniques for High-Performance Differential A/D Converters". *IEEE J. Solid-State Circuits*, 25(6):1318–1327, Dec. 1990. 9

[48] J. W. Fattaruso, M. de Wit, G. Warwar, K. S. Tan, and R. K. Hester. "The Effect of Dielectric Relaxation on Charge-Redistribution A/D Converters". *IEEE J. Solid-State Circuits*, 23(6):1550–1561, Dec. 1990. 9

[49] K. Satou, K. Tsuji, M. Sahoda, H. Otsuka, K. Mori, and T. Iida. "A 12 bit 1 MHz ADC with 1mW Power Consumption". *Proc. Custom Integrated Circuits Conf*, SC-14(6):23.6.1–23.6.4, May 1994. 9

[50] S. Mortezapour and E. K. F. Lee. "A 1-V, 8-Bit Successive Approximation ADC in Standard CMOS Process". *IEEE J. Solid-State Circuits*, 35(4):642 – 646, April 2000. 9

[51] G. Promitzer. "12-bit Low-Power Fully Differential Switched Capacitor Non-calibrating Successive Approximation ADC with 1 MS/s". *IEEE J. Solid-State Circuits*, 36(7):1138 – 1143, 2001. 9

[52] C. S. Lin and B. D. Liu. "A New Successive Approximation Architecture for Low-Power Low-Cost CMOS A/D Converter". *IEEE J. Solid-State Circuits*, 38(1):54 – 62, Jan. 2003. 9

[53] C. K. Kyung and C. K. Kim. "Pipeline Analog-to-Digital Conversion with Charge-Coupled Devices". *IEEE J. Solid-State Circuits*, SC-15(2):255–257, April. 1980. 10

[54] S. H. Lewis and P. R. Gray. "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter". *IEEE J. Solid-State Circuits*, SC-22(6):954–961, Dec. 1987. 10

[55] S. Sutarja and P. R. Gray. "A Pipelined 13-bit, 250-ks/s, 5-V Analog-to-Digital Converter". *IEEE J. Solid-State Circuits*, 23(6):1316–1323, Dec. 1988. 10

[56] Y. M. Lin, B. Kim, and P. R. Gray. "A 13-b 2.5-MHz Self-Calibrated Pipelined A/D Converter in 3-mm CMOS". *IEEE J. Solid-State Circuits*, 26(4):628–636, Dec. 1991. 10, 14

[57] P. Real, D. H. Roberson, C. W. Mangelsdorf, and T. L. Tewksbury. "A Wide-Band 10-b 20-Ms/s Pipelined ADC Using Current- Mode Signals". *IEEE J. Solid-State Circuits*, 26(8):1103–1109, Aug. 1991. 10

[58] S. H. Lewis, H. S. Fetterman, G. F. Gross, Jr. Ramachandran, R. Ramachandran, and T. R. Viswanathan. "A 10-b 20-Msample/s Analog-to-Digital Converter". *IEEE J. Solid-State Circuits*, 27(3):351–358, March 1992. 10

[59] S. H. Lewis. "Optimizing the Stage Resolution in Pipelined, Multistage, Analog-to-Digital Converters for Video-Rate Applications". *IEEE Trans. Syst. II*, 39(8):516–523, Aug. 1992. 10

[60] K. Sone, Y. Nishida, and N. Nakadai. "A 10-b 100-Msample/s Pipelined Subranging BiCMOS ADC". *IEEE J. Solid-State Circuits*, 28(12):1180–1186, Dec. 1993. 10

[61] W. T. Colleran and A. A. Abidi. "A 10-h, 75-MHz Two-Stage Pipelined Bipolar A/D Converter". *IEEE J. Solid-State Circuits*, 28(12):1187–1199, Dec. 1993. 10

[62] K. Kusumoto, A. Matsuzawa, and K. Murata. "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC". *IEEE J. Solid-State Circuits*, 28(12):1200–1206, Dec. 1993. 10

[63] A. N. Karanicolas, H. S. Lee, and K. L. Bacrania. "A 15-b 1-Msample/s Digitally Self-Calibrated Pipeline ADC". *IEEE J. Solid-State Circuits*, 28(12):1207–1215, Dec. 1993. 10

[64] D. A. Mercer. "A 14-b 2.5 MSPS Pipelined ADC With On Chip EPROM". *Proc. 1994 Bipolar/BiCMOS Circuits and Technology Meeting*, pages 15–18, Sept. 1994. 10

[65] T. B. Cho and P. R. Gray. "A 10 b, 20 Msample/s, 35mW Pipeline A/D Converter". *IEEE J. Solid-State Circuits*, 30(3):166–172, March 1995. 10, 133

[66] K. K. Onodera and P. R. Gray. "A 75-mW 128-MHz DS-CDMA Baseband Demodulator for High-Speed Wireless Applications". *IEEE J. Solid-State Circuits*, 33(5):753 – 761, May 1998. 10

[67] S. Y. Chuang and T. L. Sculley. "A Digitally Self-Calibrating 14-bit 10-MHz CMOS Pipelined A/D Converter". *IEEE J. Solid-State Circuits*, 37(6):674 – 683, Aug. 2002. 10

[68] B. Murmann and B.E Boser. "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification". *IEEE J. Solid-State Circuits*, 38(12):2040 – 2050, Dec. 2003. 10

[69] D. Y. Chang and U. K. Moon. "A 1.4-V 10-bit 25-MS/s Pipelined ADC Using Opamp-Reset Switching Technique". *IEEE J. Solid-State Circuits*, 38(8):1401 – 1404, Aug. 2003. 10

[70] W. C. Black and D. A. Hodges. "Time Interleaved Converter Arrays". *IEEE J. Solid-State Circuits*, SC-15:1022–1029, Dec. 1980. 11

[71] A. Petraglia and S. K. Mitra. "Analysis of Mismatch Effects among A/D Converters in a Time-Interleaved Waveform Digitizer ". *IEEE Trans. on Instrumentation and Measurement*, 40(5):831–835, Oct. 1991. 11, 12

[72] M. Yotsuyanagi, T. Etoh, and K. Hirata. "A 10-b 50-MHz Pipelined CMOS A/D Converter with S/H". *IEEE J. Solid-State Circuits*, 28(3):292–300, March 1993. 11

[73] C. S. G. Conroy, D. W. Cline, and P. R. Gray. "An 8-b 85-MS/s Parallel Pipeline A/D Converter in 1-mm CMOS". *IEEE J. Solid-State Circuits*, 28(4):447–454, April 1993. 11

[74] K. Nakamura, M. Hotta, L. R. Carley, and D. J. Allstot. "An 85 mW, 10 b, 40 Msample/s CMOS Parallel-Pipelined ADC". *IEEE J. Solid-State Circuits*, 30(3):173 –183, March 1995. 11

[75] D. W. Cline and P. R. Gray. "A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS". *IEEE J. Solid-State Circuits*, 31:294303, March 1996. 11

[76] K. Y. Kim, N. Kusayanagi, and A. A. Abidi. "A 10-b, 100-MS/s CMOS A/D converter". *IEEE J. Solid-State Circuits*, 32:302311, March 1997. 11

[77] D. Fu, K. C. Dyer, S. H. Lewis, and P. J. Hurst. "A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters". *IEEE J. Solid-State Circuits*, 33(12):1904 – 1911, Dec. 1998. 11

[78] G. Leger, E. J. Peralias, and A. Rueda. "SFDR probability in time-interleaved ADCs with random channel mismatches". *Proceedings of IBERCHIP 2003*, 2:380–383, May 2002. 12

[79] G. Leger, E. J. Peralias, A. Rueda, and J. L. Huertas. "Impact of Random Channel Mismatch on the SNR and SFDR of Time-Interleaved ADCs". *IEEE J. Solid-State Circuits*, 51(1):140 – 150, Jan. 2004. 12

[80] Y. C. Jenq. "Digital Spectrum of Nonuniformly Sampled Signals: Theorie and Application-Measuring Clock/Aperture Jitter of an A/D System". *IEEE Trans. on Instrumentation and Measurement*, 39(6):145 –147, Dec. 1990. 12

[81] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi. "Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems". *IEEE J. Solid-State Circuits*, 48(3):261 – 271, March 2001. 12

[82] S. M. Jamal, D. Fu, N. C. J. Chang, P.J. Hurst, and S.H. Lewis. "A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter With Digital Background Calibration". *IEEE J. Solid-State Circuits*, 37(12):1904 – 1911, Dec. 2002. 12

[83] J. Elbornsson, F. Gustafsson, and J. E. Eklund. "Blind Adaptive Equalization of Mismatch Errors in a Time-Interleaved A/D Converter System". *IEEE J. Solid-State Circuits*, 51(1):151 – 158, Jan. 2004. 12

[84] K. Poulton, J. Corcoran, and T. Hormank. "A 1-GHZ 6-bits ADC System". *IEEE J. Solid-State Circuits*, SC-22(6):962–969, Dec. 1987. 12

[85] A. Petraglia and S. K. Mitra. "High-Speed A/D Conversion incorporating a QMF Bank ". *IEEE Trans. on Instrumentation and Measurement*, 41(3):427–431, Oct. 1991. 13

[86] S. R. Velazquez. *"Hybrid Filter Banks for Analog/Digital Conversion"*. PhD thesis, MIT, 1997. Ph.D Dissertation. 13

[87] S. R. Velazquez, T. Q. Nguyen, and S. R. Broadstone. "Design of Hybrid Filter Banks for Analog/Digital Conversion". *IEEE Trans. on Signal Processing*, 46(4):956–967, April. 1998. 13

[88] B. E. Boser and B. A. Wooley. "The design of sigma-delta modulation analog-to-digital converters". *IEEE J. Solid-State Circuits*, 23(6):1298–1308, Dec. 1988. 14, 17, 23, 25, 41, 53

[89] S. R. Norsworthy, R. Schreier, and G. C. Termes, editors. *Top-Down Design of High-Performance Sigma-Delta Modulators*. IEEE Press, 1997. 14, 17, 53

[90] F. Medeiro, A. Perez-Verdu, and A. Rodriguez-Vazquez, editors. *Top-down Design of High-performance Sigma-Delta Modulators*. Kluwer, 1999. 14, 17, 53

[91] L. R. Carley and J. Kenney. "A 16 bit 4th Order Noise Shaping D/A Converter". *IEEE Proc. CICC*, pages 21.7.1–21.7.4–1880, Jan. 1988. 14

[92] Y. Matsuya, K. Uchimura, A. Iwata, and T. Kaneko. "A 17 bit Oversampling D/A Conversion Technology Using Multistage Noise Shaping". *IEEE J. Solid-State Circuits*, SC-24:969–975, Aug. 1989. 14, 26

[93] F. Maloberti. "Non Conventional Signal Processing by the Use of Sigma Delta Technique: a tutorial introduction". *IEEE ISCAS*, pages 2645–2648, Avril 1992. 14

[94] H. Qiuting and G. S. Moschytz. "Analog FIR Filters with an Oversampled $\Delta\Sigma$ Modulator". *IEEE Trans. on Circuits and Systems-II : Analog and Digital Processing*, 39(9). 14

[95] B. R. Owen and D. A. John. "A Single Columm Structure for Delta-Sigma Based IIR Filters ". *IEEE ISCAS*, pages 2413–2416, Avril 1992. 14

[96] T. Ritionemi, T. Karema, and H. Tenhunen. "A Sigma-Delta Modulation based Analog Adaptive Filter". *IEEE ISCAS*, pages 2657–2660, Avril 1992. 14

[97] P. O'Leary, F. Malobert, and G. Torelli. "Oversampling Applied to Amplitude Modulation". *IEEE ISCAS*, pages 1641–1644, Avril 1991. 14

[98] C. Fiocchi, F. Malobert, and G. Torelli. "A Sigma-Delta Based PLL for Non-Sinusoidal Waweforms". *IEEE ISCAS*, pages 2661–2664, Avril 1992. 14

[99] J. C. Candy. "An Use of Limit Cycle Oscillation to Obtain Robust Analog-to-Digital converters". *IEEE communications*, Com-22:298–205, March 1974. 17

[100] J. C. Candy, W. H. Ninke, and B. A. Wooley. "A Per Channel A/D Converter having 15 Segments μ255 Companing ". *IEEE communications*, Com-24:33–42, Jan. 1976. 17

[101] R. W. Broderson and S. P. Emmons. "Noise Analysis of Switched Capacitor Network". *IEEE J. Solide-State Circuits*, SC-11, Feb. 1976. 18

[102] R. Gregorian and G. C. Termes. *"Analog MOS Intergrated Circuits for Signal Processing"*. John Wiley and Sons edition, 1986. 18, 75, 97

[103] C. C. Enz and G. C. Termes. "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections : Autozeroing, Correlated Double Sampling, and Chopper Stabilization". *Proceesing of the IEEE*, 84(11), Nov. 1996. 18, 75, 123

[104] K. C. Hsieh, P. R. Gray, D. Senderowicz, and D. G. Messerschmitt. "A Low-Noise Chopper-Stabilized Differential Switched-Capacitor Filtering Technique". *IEEE J. Solid-State Circuits*, SC-16(6):708–715, Dec. 1981. 18, 28, 75, 123

[105] L. Toth and Y. P. Tsividis. "Generalization of the Principle of Chopper Stabilization". *IEEE Trans. on Circuit and Systems-I: Fubdamental Theory and Applications*, 50(8), Aug. 2003. 18, 75

[106] W. Bennett. "Spectra of quantized signals". *Bell System Tech. Journal*, BSTJ-27:446–472, 1948. 21

[107] B. Widrow. "A study of rough amplitude quantization by means of Nyquist sampling theory". *IRE Trans. Circuit Theory*, CT-3:266–276, Dec. 1956. 21

[108] A. B. Sripad. "A neccessary and sufficient condition for quantization errors to be uniform and white". *IEEE Trans. Acoust. Speech Signal Proc.*, ASSP-25:442–448, Oct. 1977. 21

[109] F. de Jager. "Delta modulation, a method of PCM transmission using the 1-unit code". *Philips Res. Rep.*, 7:442–466, 1952. 23

[110] A. Tomozawa and H. Kaneko. "Companded delta modulation for telephone transmission". *IEEE Trans. Comm. Tech.*, COM-16, Feb. 1968. 23

[111] J. Greefkes and F. de Jager. "Continuous delta modulation". *IPhilips Res. Rep.*, 23, 1968. 23

[112] D. J. Goodman. "Companded delta modulation for telephone transmission". *IEEE Trans. Comm. Tech.*, COM-16, February 1968. 23

[113] J. C. Candy. "A use of double integration in sigma delta modulation". *IEEE Trans. on Comm.*, Com-33:249–258, 1985. 23

[114] M. W. Hauser. "Principles of oversampling A/D conversion". *J. Audio Eng. Soc.*, 39:3–26, Jan. - Feb. 1991. 23

[115] B. Leung. "Theory of SD analog to digital converter". *IEEE ISCAS 94 Tutorials*, pages 196–223, 1994. 23

[116] P. Aziz, H. Sorensen, and J. van der Spiegel. "An Overview of Sigma-Delta Converters". *IEEE Signal Proccesing Magazine*, pages 61–86, Jan. 1996. 23

[117] J. J. Paulos, G. T. Brauns, M. B. Steer, and S. H. Ardalan. "Improved signal-to-noise ratio using trilevel delta-sigma modulation". *Proc. 1987 IEEE Int. Symp. Circuits Syst.*, pages 463–466, May 1987. 24

[118] B. P. Brandt and B. A. Wooley. "A 50 MHz Multibit $\Delta\Sigma$ Modulator for 12b 2MHz A/D Conversion". *IEEE Solid-State Circuits*, SC-26:1746–1756, Dec. 1991. 24, 26, 54

[119] P. Ju, K. Suyama, P. F. Ferguson Jr., and W. Lee. "A 1.8-V digital-audio sigma-delta modulator in 0.8-mm CMOS". *IEEE Solid-State Circuits*, 32:783796, June 1997. 24

[120] L. R. Carley. "A noise-shaping coder topology for 15+ bit converters". *IEEE Solid-State Circuits*, 24(2):267–273, April 1989. 25

[121] F. Chen and B. H. Leung. "A high resolution multibit sigma-delta modulator with individual level averaging". *IEEE Solid-State Circuits*, 30(4):453–460, April 1995. 25

[122] I. Galton and P. Carbone. "A rigorous error analysis of D/A conversion with dynamic element matching". *IEEE Trans. Circuits Syst. II: Analog Dig. Sig. Proc.*, 42(2):763–772, Dec. 1995. 25

[123] F. T. Braz. *"Convertisseur analogique-numérique de type ΣΔ pour applications en radiocommunication"*. PhD dissertation, Ecole nationale supérieur des télécommunications, 2000. 25

[124] J. C. Chao, S. NAdeem, W. L. Lee, and C. G. Sodini. "A Higher Order Topology for Interpolative Modulators for OverSampling A/D Converters". *IEEE Trans. Circuits and Systems*, 37:309–318, March 1990. 26, 54, 66

[125] R. W. Adams, P. F. Ferguson Jr., A. Ganesan, S. Vincelette, A. Volpe, and R. Libert. "Theory and practical implementation of a fifth-order sigma-delta A/D converter". *J. Audio Eng. Soc.*, 39:515–528, July-August 1991. 26

[126] R. Schreier. "An Emplirical Study of High-Oder Single-Bit Delta-Sigma Modulators". *IEEE Trans. on Circuits and Systems-II : Analog and Digital Processing*, 40(8):461–466, Aug. 1993. 26, 54, 66

[127] S. M. Moussavi and B. H. Leung. "High-Order Single-Stage Single-Bit Oversampling A/D Converter Stabilized with Local Feeback Loops". *IEEE Trans. on Circuits and Systems-II : Analog and Digital Processing*, 41(1):19–25, Jan. 1994. 26

[128] W. L. Lee. "A Novel higher order interpolative modulator topology for high resolution oversampling A/D converters". Master's thesis, MIT, Cambridge, MA, 1987. 26

[129] W. L. Lee and C. S. Sodini. "A topology for higher order interpolative coders". *Proc. 1987 IEEE Int. Sysp. Circuits Sys.*, 4(8):461–466, Aug. 1987. 26

[130] L. A. Williams III and B. A. Wooley. "A third-order sigma-delta modulator with extended dynamic range". *IEEE Solid-State Circuits*, 29(3):193–202, March 1994. 26, 41

[131] S. Rabii and B. A. Wooley. "A third-order sigma-delta modulator with extended dynamic range". *IEEE Solid-State Circuits*, 29(3):193–202, March 1997. 41

[132] S. Hein and A. Zakhor. *"Sigma-Delta Modulators"*. Kluwer Academic Publishers, 1992. 42

[133] O. Macchi and C. Uhl. "Stability of a DPCM Transmission Systems". *IEEE Trans. on Circuits and Systems*, CASII-39:705–722, Oct. 1992. 42

[134] C. Uhl and O. Macchi. "Stability of a DPCM Transmission systems with an Order t predictor". *IEEE Trans. on Circuits and Systems*, CASI-40:50–54, Jan. 1993. 42

[135] R. T. Balaird and T. S. Fiez. "Stability Analysis of High-Order Modulators for Delta-Sigma ADCs". *IEEE ISCAS*, pages 1361–1364, 1993. 43

[136] G. Thaler and M. Pastel. *"Analysis and Design of Nonlinear Feedback Control System"*. Mc Grow-Hill, NT, 1962. 43

[137] R. T. Ardalam and J. J. Paulos. "An Analysis of Nonlinear Behavior in Delta-Sigma Modulators". *IEEE Trans. on Circuits ans Systems*, 34(6):593–603, June 1987. 45

[138] R. T. Balaird and T. S. Fiez. "Stability Analysis of High-Order Delta-Sigma Modulation for ADCs". *IEEE Trans. on Circuits ans Systems*, 41(1):59–62, Jan. 1994. 45

[139] S. Hein and A. Zakhor. "On the Stability of Sigma-Delta Modulators". *IEEE Trans. on Signal Processing*, 41(7):2322–2348, July 1993. 45

[140] H. Wang. "$\Sigma\Delta$ Modulation from the Perspertive of Nonlinear Dynamics ". *IEEE Int. Sym. on Cir. and Sys.*, 3:1296–1299, 1992. 45

[141] H. Wang. "A Geometrc View of $\Sigma\Delta$ Modulations". *IEEE Trans. on Cir. and Sys. II*, 39(6):402–405, 1992. 45

[142] P. Steiner and W. Yang. "Stability Analysis of the Second Order $\Sigma - \Delta Modulator$ ". *IEEE Int. Symp. on Cir. and Sys.*, 5:365–368, 1994. 45

[143] M. Goodson, B. Zang, and R. Schreiner. "Invariant Sets for general second order low-pass delta sigma modulators with dc inputs". *IEEE Int. Symp. on Cir. and Sys.*, 6:1–4, June 1994. 45

[144] M. Goodson, B. Zang, and R. Schreiner. "Proving Stability of Selta-Sigma Modulators Using Invariant Sets". *IEEE Int. Symp. on Cir. and Sys.*, 1:633–636, May 1995. 45

[145] M. Goodson, B. Zang, and R. Schreiner. "An Algorithm for Convex Positively Invariant Sets for Selta-Sigma Modulators". *IEEE Trans. on Cir. and Sys. I: Fundamental Theory and Application*, 44(1):38–44, Jan. 1997. 45

[146] M. A. Alexander, H. Mohajeri, and J. O. Prayogo. "A 192 ks/s Sigma Delta ADC with Integrated Decimation Filters Providing- 97.4 dB THD". *IEEE ISSCC Dig. Tech. Papers*, 37:190–191, 1994. 54

[147] I. Dedic. "A Sixth-order triple-loop sigma delta CMOS ADC with 90 dB SNR and 100 KHz band-width". *IEEE ISSCC Dig. Tech. Papers*, 37:188–189, 1994. 54

[148] A. Eshraghi and T. Fiez. "A Comparison of Three Parallel DS A/D Converters". *IEEE International Symposium on Circuits and Systems*, pages 517–520, May 1996. 54

[149] A. Eshraghi and T. Fiez. "An Area Efficient Time-Interleaved Parallel Delta-Sigma A/D Converter". *IEEE ISCAS*, 2:386–389, 1998. 54

[150] G. Leger and A. Rueda. "Analyse spectrale des convertisseurs $\Sigma\Delta$ a modulation de Hadamard". *Proceedings of TAISA 2003*, pages 49–52, Sep. 2003. 71

[151] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "A Tme-Interleaved Chopper-Stabilized Delta-Sigma Analog to Digital Converter with Adaptive Equalization of Channel Gain Mismatch". *IEEE Proceeding of Mixdes 2002*, 2002. 71

[152] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "A Time-Interleaved Chopper-Stabilized Delta-Sigma Analog to Digital Converter". *IEEE Proceeding of ICECS 2002*, 2002. 71

[153] Y. W. Chang, C. Y. Wu, and T. C. Yu. "Chopper-Stabilised Sigma-Delta Modulator". *IEEE ISCAS*, pages 1286–1289, Avril 1993. 75

[154] A. Shoval, D. Johns, and W. M. Snelgrove. "Comparison of DC Offset Effects in Four LMS Adaptive Algorithms". *IEEE Trans. Circuits and Systems*, 42(3):176–185, March 1995. 79, 82

[155] *IEEE Standard VHDL Language Reference Model.* IEEE Std 1076-1993. 88

[156] E. Christen and K. Bakalar. "VHDL-AMS–A Hardware Description Language for Analog and Mixed-Signal Applications". *IEEE Trans. on Cirucits and SystemsII: Analog and Digital Signal Processing*, 46(10):1263–1272, Oct. 1999. 88, 109

[157] H. Yannick and A. Vachoux. *"VHDL-AMS : applications et enjeux industriels cours et exercices corrigés".* Dunod, 2002. 88

[158] *IEEE Standard VHDL Analog and Mixed-Signal Extensions.* IEEE Std 1076.1-1999. 88, 89

[159] H. Chang, E. Charbon, U. Choudhury, A. Demir, E. Felt, E. Liu, E. Malavasi, A. Sangiovanni-Vincentelli, and I. Vassiliou. *A Top-Down Constraint-Driven Design Methodology for Analog Integrated Circuits.* Kluwer Academic edition, 1997. 90

[160] C. Rose. *The What and How of Top-Down System Design.* TD Technologies Int., 1993. 90

[161] R. McGraw, J. H. Aylor, and R. H. Klenke. "A Top-Down Design Environment for Developing Pipelined Datapaths". *Proceedings of the 35th annual IEEE DAC conference*, pages 236–241, Dec. 1998. 90

[162] K. Kundert, H. Chang, D. Jefferies, G. Lamant, and E. Malavasi. "Design of Mixed-Signal Systems-on-a-Chip". *IEEE Trans. On Computer-Aides Design of Integrated Circuits And Systems*, 19(12):1561–1571, Dec. 2000. 90

[163] Mentor Graphics. *"ADVanceMS Reference Manual™ "*. http://www.mentor.com. 92

[164] H. Hai Tao, L. Toth, and J. M. Khoury. "Analysis of timing jitter in bandpass sigma delta modulators". *IEEE Trans. on Circuit and Systems II*, 46(991-1001), Aug. 1999. 94

[165] P. R. Gray and R.G. Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley and Sons, New York, second edition, 1993. 96, 98

[166] D. E. Knuth. *"The Art of Computer Programming"*. Addition-Wesley, 1998. 98

[167] J. L. Danger, A. Ghazel, E. Boutillon, and H. Laamari. "Efficient FPGA Implementation of Gaussian Noise Generator for Communication Channel Emulation". *Proceedings. ICECS 2000*, 1(366 - 369), Dec. 1999. 98

[168] B. Pelligrini, R. Saletti, B. Neri, and P. Terreni. *"$1/f^v$ Noise Generators"*. El Sevier, 1985. 101

[169] M. F. Mar and R. W. Brodersen. "Simulation Techniques for Systems with Oversampling A/D Converters". *Proceedings of IEEE ASIC Conference and Exhibit*, pages 523 – 526, 1993. 101

[170] F. Baillieu and Y. Blanchard. *Signal Analogique Capacité Cummutée*. Dunod, 1994. 103

[171] http://www.beams.asso.fr/. 107

[172] http://www.austriamicrosystems.com. 121

[173] http://www.comelec.enst.fr/oceane. 122

[174] K. C. Hsieh and P. Gray. "A Low-Noise Chopper-Stabilized Differential Switched-Capacitor Filtering Technique". *Proceedings of IEEE Solid-State Circuits Conference*, XXIV:128 – 129, Feb. 1981. 123

[175] K. L. Lee and R. G. Meyer. "Low-Distortion Switched-Capacitor Filter Design Techniques". *IEEE J. Solid-State Circuits*, SC-20(6):1103–1113, Dec. 1985. 123, 127, 132

[176] H. Recoules. *"Modélisation du transistor MOS submicronique: application à la conception de circuit intégrés analoques et mixtes en technologies CMOS et BICMOS"*. PhD thesis, Ecole Nationale Superieure des Telecommunications, Paris, France, 1999. 125, 133

[177] V. Peluso, P. Vancorenaland, M. Steyaert, and W. Sansen. "900mV differential class AB OTA for switched opamp appliations". *Electronic Letter*, 33(17):1455–1456, 1997. 125

[178] V. Peluso, M. Steyaert, and W. Sansen. "A 1.5V-100μW $\Delta\Sigma$ Modulator with 12-b Dynamic Range Using the Switched-Opamp Technique". *IEEE J. Solid-State Circuits*, 32(7):943–952, July 1997. 125

[179] V. Peluso, P. Vancorenaland, A. Marques, M. Steyaert, and W. Sansen. "A 900mV Low-Power $\Delta\Sigma$ Converter with 77dB Dynamic Range". *IEEE J. Solid-State Circuits*, 33(12):1887 – 1897, Dec. 1998. 125

[180] A. E. Stevens and G. A. Miller. "A High-Slew Integrator For Switched-Capacitor Circuits". *IEEE Pro. Cir. and Sys. Conf.*, 29(9):1146–1149, 1994. 127

[181] J. K. Kenney, G. Rangan, K. Ramamurthy, and G. Terms. "An Enhanced Slew Rate Source Follower". *IEEE Pro. Cir. and Sys. Conf.*, 30(2):144–146, 1995. 127

[182] K. C. Kuo and A. Leuciuc. "A Linear MOS Transconductance Using Source Degeneration and Adaptive Biasing". *IEEE Trans. on Cir. and Sys. II, Analog and Digital Processing*, 48(10):937–943, Oct. 2001. 127

[183] M. Dessouky. *"Conception en vue de la réutilisation de circuits analogiques. Application : Modulateur Delta-Sigma à très faible tension"*. PhD thesis, Universite Paris VI, Paris, France, 2001. 132

[184] J. T. Wu and B. A. Wooley. "A 100-MHz pipelined CMOS Comparator". *IEEE J. Solid-State Circuits*, 23(6):1379–1385, Dec. 1988. 133

[185] A. R. Feldman. *"High-Speed Low-Power Sigma-Delta Modulation for RF Baseband Channel Applications"*. PhD thesis, Berkeley University, California, USA, 1997. 133

[186] J. H. Fischer. "Noise sources and calculation techniques for switched capacitor filters". *IEEE J. Solid State Circuits*, SC-17:742–752, Aug. 1982. 140

[187] C. A. Gobet and A. Knob. "Noise analysis of switched capacitor networks". *IEEE Trans. on Cir. Sys.*, CAS-30:37–43, Jan. 1983. 140

[188] V. T. Nguyen, P. Loumeau, J. F. Naviner, and G. Picard. "Performances theoriques et filtre optimal d'une architecture parallèle d'un CAN$\Sigma\Delta$". *Proceeding of JNDRM 2001*, 2001.

[189] V. T. Nguyen, P. Loumeau, J. F. Naviner, and G. Picard. "Convertisseur analogique numérique basé sur la modulation sigma delta en combinaison avec l'entrelacement temporel". *Proceeding of JNDRM 2002*, 2002.

[190] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "An Interleaved Delta-Sigma Analog to Digital Converter with Digital Correction". *IEEE Proceeding of ICASSP 2002*, pages IV–4193, 2002.

[191] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "Analysis of Time-Interleaved Delta-Sigma Analog to Digital Convergter". *IEEE Proceeding of VTC 2002*, 2002.

[192] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "Advatages of High-Pass $\Delta\Sigma$ Modulators in Time-Interleaved $\Delta\Sigma$ Analog to Digital Converter". *IEEE Proceeding of MWSCAS 2002*, 2002.

[193] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "Avantages des modulateurs delta-sigma passe haut pour le convertisseur sigma-delta combiné avec l'entrelacement temporel". *Proceeding of TAISA 2002*, 2002.

[194] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "Temporal and Spectral Analysis of Time-Interleaved High-pass Sigma Delta Converter". *IEEE Proceeding of ICECS 2003*, 2003.

[195] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "Analysis of High Pass filter in High Pass Sigma Delta Modulator". *IEEE Proceeding of Mixdes 2003*, 2003.

[196] V. T. Nguyen, P. Loumeau, and J. F. Naviner. "Modelisation et simulation d'un modulateur sigma delta passe haut avec VHDL-AMS". *Proceeding of TAISA 2003*, 2003.