

Wideband bandpass sigma-delta analog-to-digital conversion for nonlinearly distorted signals of power amplifiers

Dang Kien Germain Pham

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Conversion Analogique-Numérique Sigma-Delta Large-Bande Appliquée à la Mesure des Non-Linéarités des Amplificateurs de Puissance

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THÈSE

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Wideband Bandpass $\Sigma\Delta$ Analog-to-Digital Conversion for Nonlinearly Distorted Signals of Power Amplifiers

PHAM Dang-Kièn Germain

À ma mère et à mon père.

To my mother and my father.

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Résumé

Les amplificateurs de puissance, éléments constitutifs essentiels de tout système de télécommunication, vont jouer un rôle capital dans le développement des futurs systèmes de communication. En effet, il ont un impact sur l'autonomie du téléphone portable ou sur les coûts d'exploitation d'une station de base en terme de refroidissement et d'électricité, mais aussi sur la qualité du signal et la coexistence des systèmes de communication.

Aujourd'hui l'amélioration des amplificateurs de puissance nécessite un progrès technologique au niveau du composant lui même mais doit aussi tenir compte d'une approche plus globale. En particulier, le progrès dans les traitements numériques permet aujourd'hui de corriger en amont certaines distorsions qui seront générées en aval de la chaîne de communication (par l'amplificateur de puissance).

La prédistorsion numérique est une technique de correction des amplificateurs de puissance qui connaît un intérêt grandissant de par son intégration complètement numérique et par les gains en linéarité et en consommation. Cette technique nécessite une voie de retour dont un élément critique est le convertisseur analogique-numérique. Ce composant doit répondre à des contraintes de résolution, de bande passante et de linéarité élevées.

Dans cette thèse , nous proposons une nouvelle architecture de convertisseur analogique-numérique à base de modulateurs $\Sigma\Delta$ passe-bande. Cette architecture tire partie du fonctionnement passe bande des modulateurs que nous faisons travailler en parallèle, chacun centré sur différentes fréquences, mais aussi d'un agencement en cascade particulier pour éliminer le signal utile , qui est de forte puissance, dans le but de diminuer les contraintes de dynamique.

La conception haut niveau et les simulations ont été menées pour des systèmes à temps discret et aussi à temps continu et a nécessité le développement d'outils adaptés de simulation se basant sur la boîte à outils Delta Sigma Toolbox de Richard Schreier.

Abstract

Power amplifiers, which are essential elements of any communication system, will play a crucial role in the development of future communication systems. Today improving power amplifiers requires technological advances at the circuit device level, but one also must consider a more global approach. In particular, advances in digital processing can now correct in the early stage of the communication chain some distortions that are generated downstream in the chain.

Digital predistortion is a correction technique for power amplifiers that has a growing interest because of its completely digital implementation and of its gains in linearity and energy consumption. This technique requires a feedback path where the analog-to-digital converter is a critical element. This component must satisfy the constraints of high resolution , wide bandwidth, and high linearity.

In this thesis, we propose a new architecture of analog-to-digital converter based on bandpass Delta-Sigma modulators. This architecture takes advantage of operating bandpass modulators that are designed to work in parallel, each focusing on different frequencies, but also of a particular cascading arrangement to eliminate the useful signal, which has a high power, in order to reduce dynamics constraints. High-level design and simulations were carried out for discrete time and continuous time systems and also required the development of appropriate simulation tools.

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List of Abbreviations

3GPP 3rd Generation Partnership Project

ACLR Adjacent Channel Leakage power Ratio

ACPR Adjacent Channel Power Ratio

ADC Analog-to-Digital Converter

BP Band-Pass

BTS Base Transceiver Station

BW Bandwidth

CDMA Code Division Multiple Access

CIFB Cascade-of-Integrators Feedback form

CIFF Cascade-of-Integrators Feedforward form

CMOS Complementary Metal Oxide Semiconductor

CRFB Cascade-of-Resonators Feedback form

CRFF Cascade-of-Resonators Feedforward form

CT Continuous-Time

DAC Digital-to-Analog Converter

DFT Discrete Fourier Transform

DL Downlink transmission, from the BTS to the mobile equipment

DOR Digital Output Rate

DPD Digital Predistortion

DT Discrete-Time

ENOB Effective Number Of Bits

EVM Error Vector Magnitude

FBD Frequency Band Decomposition

FDMA Frequency Division Multiple Access

FoM Figure of Merit

GMSCL Generalized MSCL

HRZ Half-delay Return-to-Zero

HSDPA High-Speed Downlink Packet Access

IM Intermodulation (products)

ISI Inter-Symbol Interferences

LNA Low Noise Amplifier

LUT Look-Up Table

MASH Multi-stAge noise SHaping architecture

MSCL Multi-Stage Closed Loop

MSNBC Multi-Stage Noise Band Cancellation architecture

NCF noise cancellation filter

NRZ Non-Return-to-Zero

NTF Noise Transfer Function

OFDMA Orthogonal Frequency-Division Multiple-Access

OOBG Out-Of-Band Gain

OSR Oversampling Ratio

OTA Operational Transconductance Amplifier

PA Power Amplifier

PAE Power Added Efficiency

PAPR Peak-to-Average Power Ratio

PSD Power Spectral Density

QAM Quadrature Amplitude Modulation

QPSK Quaternary Phase-Shift Keying

RC Raised-Cosine (filter)

RRC Root-Raised-Cosine (filter)

RSTF Residual Signal Transfer Function

RZ Return-to-Zero

SAR Successive-Approximation-Registers architecture

SL Single Loop architecture

SNDR Signal to Noise and Distortion Ratio

SNR Signal to Noise Ratio

STF Signal Transfer Function

TDMA Time Division Multiple Access

UMTS Universal Mobile Telecommunications System

VLSI Very-Large-Scale Integration

WCDMA Wideband Code Division Multiple Access

Résumé étendu

Introduction

À l'heure du développement du haut débit sans fil, les besoins en communication nécessitent des systèmes de communication de haute capacité. En outre, l'évolution des télécommunications se traduit par une multiplication et une complexification des standards. Ainsi, la coexistence de ces systèmes exigera des terminaux qu'ils soient multi-mode, multi-bande et multi-standard. Par ailleurs, le domaine des télécommunications devra aussi faire face à une nouvelle difficulté majeure : le partage du spectre, dont l'usage est régulé.
Pour répondre à cette limitation, une solution de base est d'utiliser les récentes techniques de modulations numériques qui offrent un meilleur rendement spectral. Cependant, ces modulations présentent le désavantage d'avoir une enveloppe non-constante. En même temps, la tendance actuelle est d'utiliser dans les stations de base un seul amplificateur de puissance (PA) pour des transmissions multi-porteuses. Dans les deux cas, une quelconque distorsion dans la chaîne de transmission dégradera la qualité du signal émis et se traduira par un enrichissement indésirable du spectre. Or, les amplificateurs de puissance sont réputés être non linéaires.
À cela s'ajoute le problème de la consommation d'énergie, qui est devenu un enjeu politique, économique et social essentiel. Cependant, la nécessité de réduire les dégradations dues aux enveloppes variables pousse à faire fonctionner l'amplificateur de puissance dans un mode à faible rendement. Il est donc primordial de développer des systèmes plus efficaces en terme de consommation grâce à l'utilisation de nouvelles techniques et à l'intégration de composants intelligents.

Ainsi, la contrainte en capacité (au sens de Shannon) et en consommation permettent d'identifier l'amplificateur de puissance comme l'élément critique de la chaîne de transmission à améliorer.

Le projet CATRENE PANAMA [78] vise à répondre à ce besoin avec les systèmes intégrés, les systèmes discrets et les systèmes distribués. Ce projet cible un ensemble d'applications comme la 3G/4G et les ondes millimétriques pour les téléphones mobiles, les stations de base d'émission-réception, l'avionique, les communications mobiles par satellite et les réseaux domestiques. Ce projet rassemble des partenaires majeurs européens des semi-conducteurs, du test, de l'automatisation en conception électronique et du monde académique pour se concentrer sur les amplificateurs de puissance et les systèmes de transmission du futur. Notre participation à ce projet nous a permis de travailler en collaboration avec des partenaires industriels et en particulier avec NXP.

Il existe un certain nombre de techniques de linéarisation permettant d'améliorer la linéarité des amplificateurs de puissance et qui permettent, par la même occasion d'améliorer le rendement. L'une d'elles, la prédistorsion numérique, suscite un intérêt particulier du fait qu'elle bénéficie des avancées techniques de l'électronique numérique et que les systèmes de communications utilisent de plus en plus des modulations numériques.

Son implantation dans les chaînes d'émissions actuelles et futures ne représente qu'un surcoût relativement faible dans la partie numérique, mais elle nécessite une mesure des distorsions générées par l'amplificateur et donc d'une voie de retour, éventuellement dédiée, pour convertir en numérique le signal analogique radio-fréquence (RF) distordu. En outre, la mesure périodique des distorsions permet de rendre le système adaptatif et plus robuste aux variations inhérentes aux conditions de fonctionnement.

Dans ce système, le convertisseur analogique numérique qui a en charge la mesure du signal distordu doit répondre aux besoins de résolution sur le signal et aux besoins en bande passante. Or ces besoins sont assez difficiles à satisfaire dans le cadre de la prédistorsion numérique. De plus, ici aussi, sa consommation se doit d'être minimum.

Objet de l'étude

Le premier point prend en considération que les systèmes de communication récents utilisent des bandes passantes relativement larges. Le signal distordu comporte des signaux indésirables que l'on appelle produits d'intermodulation et il se caractérise par un spectre P fois plus large qu'à l'origine, P étant l'ordre de non-linéarité considéré. En pratique, on vise à numériser au moins les produits d'intermodulation d'ordre 5. En outre, ces signaux sont transposés à une fréquence centrale d'émission haute. On se rend compte que dans ce type d'application qu'est la prédistorsion numérique, le respect du théorème d'échantillonnage peut fixer la fréquence du convertisseur à des valeurs très élevées si l'on ne ramène pas le signal en basse fréquence.
Le second point implique que la résolution de conversion de ces signaux distordus doit aussi être très élevée, d'une part, parce qu'un signal multi-porteuse se caractérise par une dynamique très grande, d'autre part, parce que les distorsions ne représentent, en principe, que de faibles modifications du signal original.
Diverses techniques permettent d'augmenter les performances des convertisseurs analogiques numériques (CAN) telle que la parallélisation comme l'entrelacement temporel très utilisé avec des CAN de type pipeline, ou les traitements par décomposition fréquentielle. Une autre méthode consiste à utiliser des circuits temps continu dont les fréquences de travail sont très élevées et les consommations d'énergie réduites. Parmi les différentes architectures de convertisseurs, les modulateurs sigma-delta ($\Sigma\Delta$) présentent un intérêt particulier : une grande précision peut être atteinte pour des signaux passe-bande à fréquence centrale élevée avec peu de composants. Toutefois, malgré une limitation forte des bandes passantes de ces convertisseurs à cause de leur principe de fonctionnement par sur-échantillonnage, la littérature récente fait état de convertisseurs $\Sigma\Delta$ dont les bandes passantes permettent d'en envisager l'usage pour des applications de télécommunication large bande.

Sujet

Ce travail de thèse vise à concevoir un convertisseur analogique-numérique permettant de mesurer le signal de la voie de retour dans ce contexte de prédistorsion numérique dans les stations de base. En particulier, nous nous intéressons à développer une nouvelle architecture à base de convertisseur $\Sigma\Delta$ qui permette de numériser ce signal composé en bandes, centré en une fréquence élevée et de très grande dynamique. Nous proposons une structure innovante exploitant les propriétés de filtrage du $\Sigma\Delta$ et la mise en cascade de modulateurs et leur utilisation en parallèle sur différentes bandes pour convertir le signal.

Ce résumé présente les points essentiels de chaque chapitre de ce manuscrit. Ainsi, la partie I présentera l'application cible du CAN : la prédistorsion numérique. Nous y déve-

lopperons le cahier des charges du CAN. La partie II traitera de la conversion analogique-numérique par modulateur $\Sigma\Delta$ et détaillera les techniques de conception haut-niveau de ces convertisseurs. La partie III est consacrée à la nouvelle architecture de convertisseur que nous proposons.

Partie I : Linéarisation des amplificateurs de puissance

Les systèmes de communication actuels sont constitués de différentes parties que nous pouvons regrouper en deux grandes catégories : les éléments pour le traitement numérique et les circuits pour le traitement analogique du signal. Aujourd'hui toute l'information transmise lors d'une communication est codée numériquement et les chaînes de transmission et de réception des systèmes ont pour fonction de transformer la forme de l'information pour l'adapter au médium de transmission.

Une partie de la chaîne d'émission est représentée à la Figure 1 où sont représentés trois éléments : le bloc de modulation numérique qui transcrit l'information binaire en impulsions d'amplitude et de phase ; ce bloc est suivi des filtres numériques de mise en forme du signal puis des convertisseurs numériques analogiques générant le signal électrique qui va moduler les porteuses radio fréquence en quadrature. Dans de nombreux cas, ces signaux ont une

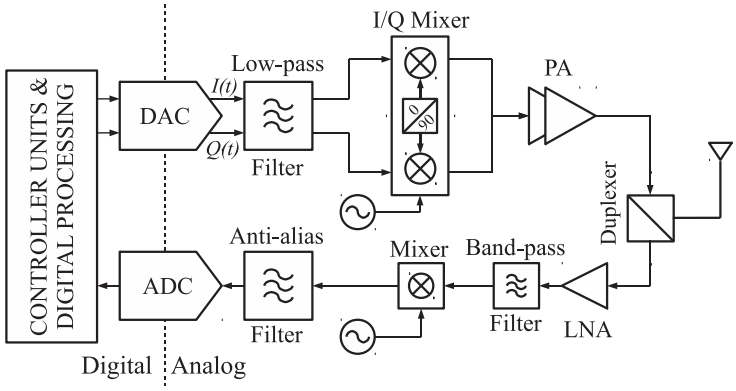


FIGURE 1 – Schéma de bloc d'un émetteur-récepteur numérique général

enveloppe non constante ce qui est problématique lorsqu'on sait que les amplificateurs de puissance sont des composants non linéaires. En effet, toute non linéarité sur un tel signal génère une détérioration du signal de même que des signaux hors bande indésirables.

Le problème s'aggrave dans le cas de stations de base qui doivent gérer des signaux multi-porteuses donc large bande. Le niveau de ses distorsions est régi par le standard de communication et dans le cadre de cette thèse nous fixons les contraintes à partir des spécifications données par le 3GPP pour le WCDMA résumé par la Table 1.

Standard	3GPP WCDMA
Bande de fréquence - Liaison descendante	2110 - 2170 MHz
Nombre de porteuses - Liaison descendante	3
Espacement des canaux et Bande passante par canal	5MHz
Filtre de mise en forme	RRC avec roll-off β=0.22 and temps symbole (chip) 1/3.84 μs
Modulation	QPSK

TABLE 1 – Spécifications considérées du 3GPP WCDMA

Le dernier élément actif de la chaîne de transmission est l'amplificateur de puissance. Son rôle est de fournir suffisamment de puissance au signal pour assurer sa transmission

correctement.

Les amplificateurs de puissance sont caractérisés par leur rendement énergétique $\eta = P_{OUT}/P_{DC}$. Ce rendement dépend des conditions de fonctionnement du PA notamment du point de polarisation et de l'excursion des signaux. Les PA sont aussi caractérisés par leur gain en puissance $G = P_{OUT}/P_{IN}$ et ce gain varie aussi avec l'excursion des signaux. La Figure 2 montre un extrait d'une documentation constructeur qui illustre les variations du gain et du rendement en fonction de la puissance délivrée dans la charge.

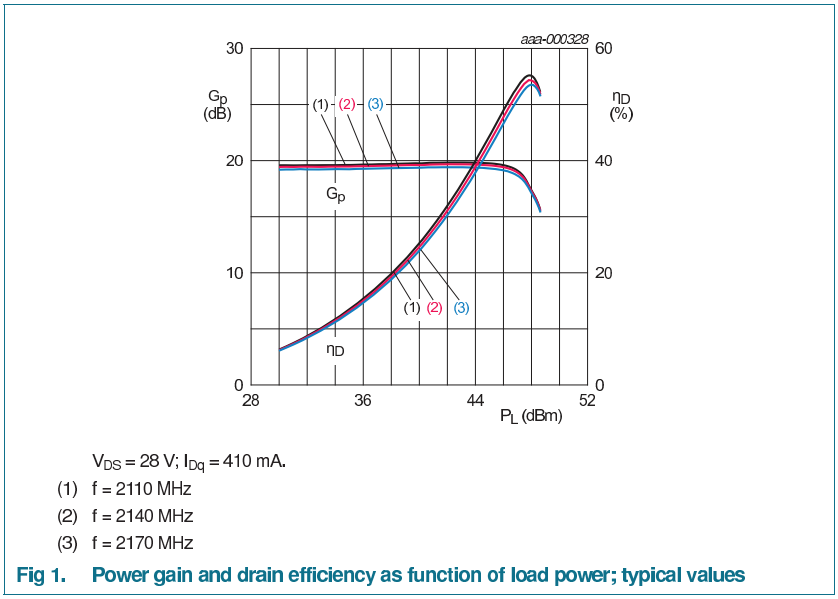


FIGURE 2 – Extrait de la fiche de constructeur du transistor de puissance BLF6G22L-40P

D'autres critères permettent de caractériser les amplificateurs de puissance comme l'EVM et les ACPR (ou ACLR). Les courbes de la Figure 2 illustrent le problème du compromis linéarité rendement : lorsque le gain est linéaire en fonction de la puissance délivrée le rendement du PA est faible, et la puissance délivrée aussi. Au contraire le rendement est élevé pour les valeurs de puissance où le gain est non linéaire et la puissance délivrée est maximum.

Pour corriger le problème de linéarité nous avons supposé durant ce travail de thèse d'utiliser la prédistorsion numérique qui consiste à faire précéder le PA d'un bloc de traitement dont la fonction est de distordre le signal d'une manière inverse à celles du PA comme schématisé par la Figure 3.

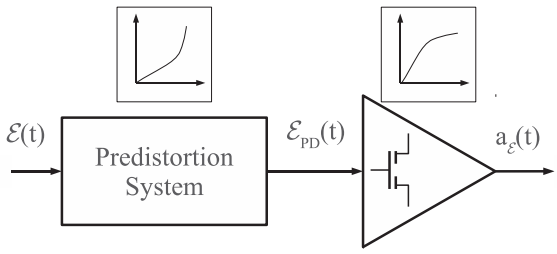


FIGURE 3 – Schéma simplifié de la prédistorsion numérique

La prédistorsion numérique est implémentée dans la partie numérique ; elle bénéficie

ainsi des avancées technologiques de l'électronique numérique et la technique reste flexible. En outre, elle peut être facilement implémentée de manière adaptative rendant le système plus robuste aux variations des caractéristiques du PA dans le temps comme le vieillissement, les variations de température et du point de fonctionnement. La Figure 4 présente le diagramme en bloc détaillé d'une chaîne d'émission avec prédistorsion numérique.

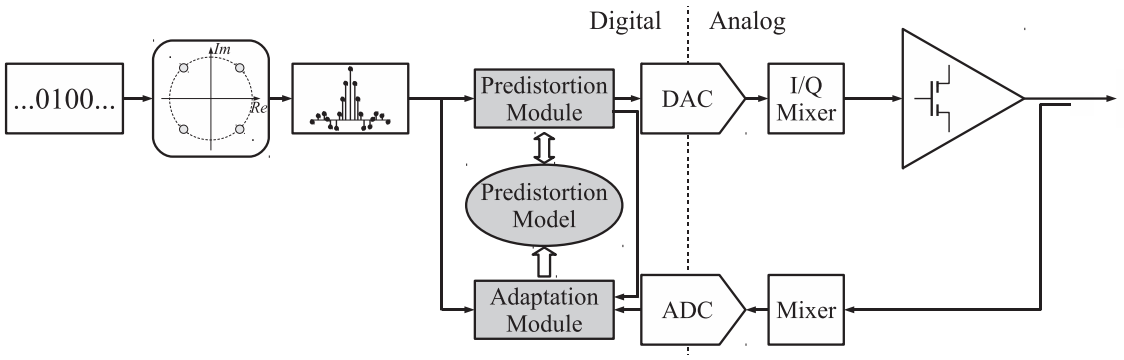


FIGURE 4 – Schéma détaillé de la prédistorsion numérique

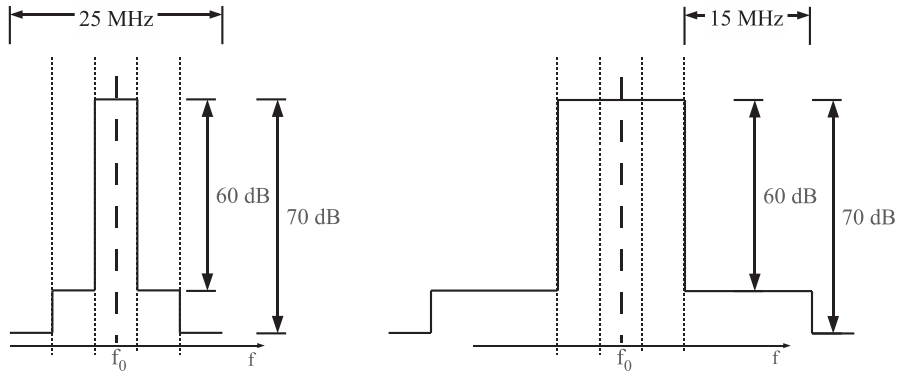
Les implémentations de prédistorsion numérique sont variées. Elles diffèrent selon le type d'apprentissage et les modèles de calcul choisis pour la fonction inverse.

Afin de caractériser avec précision le comportement du PA, la voie de mesure doit répondre à plusieurs exigences. Plus précisément, la plage de dynamique et la linéarité de la voie de mesure de retour devraient dépasser les performances de linéarité ciblée. En outre, en raison de l'accroissement spectral généré par les troisième, cinquième, et ordres supérieurs de non-linéarité, le signal déformé s'étend sur au moins trois fois la largeur de la bande initiale. Actuellement, la bande passante est généralement considérée comme mesurant au moins cinq fois l'initiale, de sorte que les composantes non linéaires d'ordre 5 peuvent être corrigées.

En observant la voie de retour de la Figure 4 nous identifions le CAN comme le composant critique de cette voie de retour. Il paraît évident que la précision de prédistorsion dépendra de la précision de le CAN. Une grande plage de dynamique et de linéarité est équivalente à une haute résolution pour le CAN et l'enrichissement spectral implique de traiter des signaux large bande. En se basant sur les spécifications de la norme pour le WCDMA, nous définissons un profil de spectre attendu pour le signal à numériser, représenté à la Figure 5.

Nous effectuons alors une revue des CAN publiés aux conférences ISSCC de 1997 à 2012 en étudiant la Figure 6 et montrons que les convertisseurs à base de modulateurs $\Sigma\Delta$ passe bande sont un choix adapté à notre application.

Enfin, nous montrons par des simulations réalisées sur le logiciel System Vue, l'effet de la quantification sur les performances de correction. La Figure 7 illustre que les performances de correction diminuent lorsque la résolution est trop faible mais aussi qu'à partir d'une certaine résolution, les performances ne s'améliorent pas même si la résolution est augmentée. Cinq bits de quantification suffisent dans ce cas de simulation pour respecter le standard. Nous avons vérifié les performances de correction pour un modulateur $\Sigma\Delta$ de résolution équivalente comme le résume la Table 2.



(a) Signal mono-porteuse (b) Signal multi-porteuse

FIGURE 5 – Schéma des spectres montrant les ACLR attendus pour les spécifications du CAN

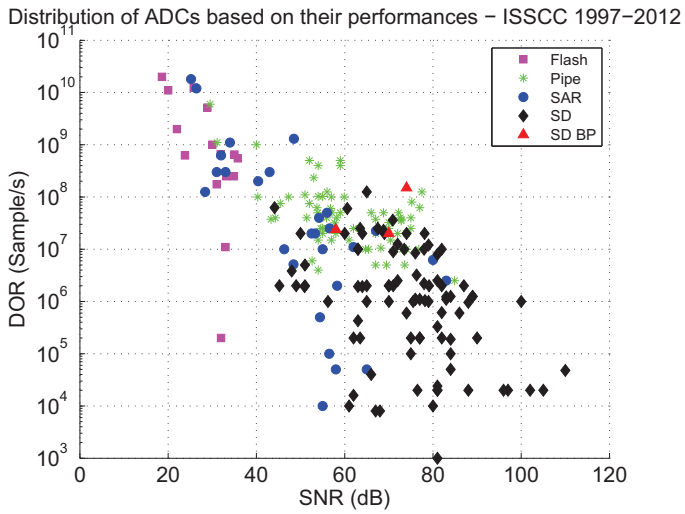


FIGURE 6 – Vue d'ensemble des CAN publiés - Répartition en fonction de leurs performances

	ACLR5	ACLR10
Idéal – Sans Quant.	59.4 dB	63.5 dB
Quantif. Flash	49,3 dB	51,4 dB
ΣΔ	51,4 dB	55,6 dB

TABLE 2 – Performances en ACLR obtenues par simulation

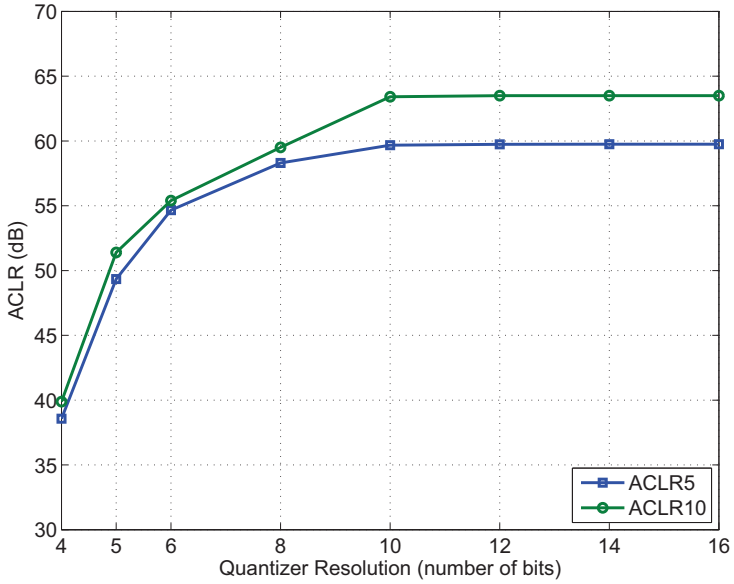


FIGURE 7 – ACLR en fonction de la résolution des données de la voie de retour

Partie II : Conception et simulation niveau système des convertisseurs ΣΔ

L'architecture générale d'un convertisseur ΣΔ est représentée à la Figure 8.

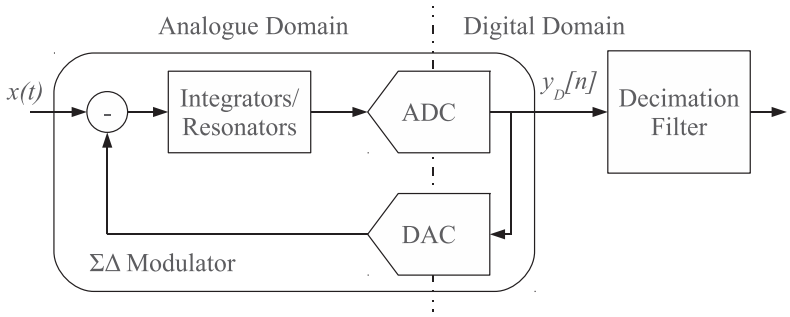


FIGURE 8 – Schéma de la structure générale d'un convertisseur ΣΔ

Bien que ces convertisseurs utilisent des CAN de faible résolution, ils ont la capacité de fournir des signaux de haute résolution. Ceci est possible grâce à l'utilisation de trois techniques : le sur-échantillonnage, la mise en forme du bruit de quantification, et le filtrage décimation. L'effet de la quantification, du sur-échantillonnage et de la mise en forme du bruit sont rappelés pour en déduire les équations de base pour le calcul du RSB. On montre que la sortie du modulateur a pour transformée en Z :

$$Y_D(z) = STF(z)\,X(z) + NTF(z)\,N(z) \tag{1}$$

La $STF(z)$ a une caractéristique passante dans la bande utile et affecte peu le signal utile $X(z)$. La $NTF(z)$ a une caractéristique coupe-bande qui permet d'atténuer le bruit de quantification dans la bande utile.

Nous rappelons aussi le problème inhérent à la structure bouclée de ces systèmes : les modulateurs ΣΔ peuvent être instables.

Enfin nous passons en revue les choix de conception haut niveau des modulateurs comme le type passe-bas ou passe-bande. La Figure 9 illustre le spectre du signal en sortie

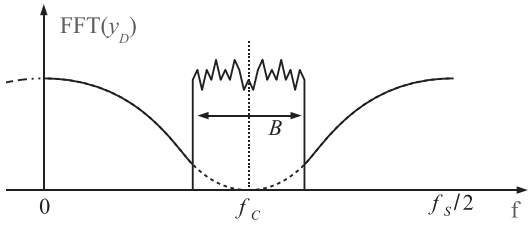
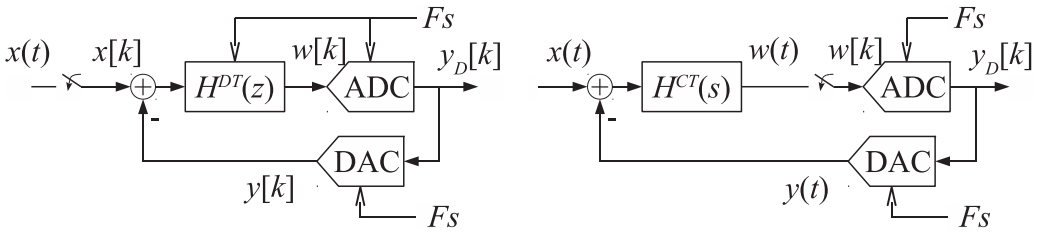


FIGURE 9 – Schéma du spectre dans le cas passe-bande

d'un modulateur passe-bande où le signal est centré autour d'une fréquence Fc et occupe une bande de largeur B. Les modulateurs peuvent aussi être à base de circuits temps-discret (TD) ou bien à temps-continu (TC). La Figure 10 illustre la différence structurelle de ces deux types de modulateurs.

Enfin, pour pallier les problèmes de stabilité et de largeur de bande, différentes architectures ont été développées comme les architectures en cascade, les architectures parallèles à entrelacement temporel et à décomposition fréquentielle. Nous concluons cette revue par une présentation d'un état de l'art des convertisseurs ΣΔ publiés dans plusieurs conférences



(a) Modulateur à temps discret (b) Modulateur à temps continu

FIGURE 10 – Schéma des implémentations des modulateurs ΣΔ

entre 2006 et 2012. La Figure 11a et la Figure 11b montrent le positionnement de chaque type de convertisseurs dans les plans de performance résolution (ENOB) en fonction de la bande passante (BW) et facteur de mérite (FOM) en fonction de la bande passante (BW).

Outre la difficulté de réalisation des circuits à haute performance, la conception des modulateurs ΣΔ peut être délicate et comporte des choix de conception influençant les performances attendues des sous-circuits dès le haut niveau de conception (architecture, valeur des coefficients). La multitude des paramètres haut niveau des modulateurs nécessite à eux seuls une méthodologie de conception. Nous abordons cette méthodologie dans le cas des modulateurs d'ordre élevé et traitons le cas des circuits TD et TC.

La boîte à outils Delta-Sigma pour MATLAB fournit des fonctions pour calculer automatiquement des expressions de NTF optimisées et les coefficients d'architecture permettant d'implémenter ces NTF. Nous rappelons la méthode de transformation pour obtenir l'expression du filtre de boucle d'un modulateur TC à partir de celle d'un modulateur TD en utilisant l'invariance de la réponse impulsionnelle. La Figure 12 détaille la structure de chaque modulateur à rendre équivalent en terme de NTF.

On montre alors que dans le cas d'un CNA NRZ, si le filtre de boucle TC s'exprime comme :

$$H^{CT}(s) = \sum_{m=1}^{N} \frac{a_m^{CT}}{s - p_m^{CT}} \tag{2}$$

Alors le filtre équivalent TD s'exprime comme :

$$H^{DT}(z) = \sum_{m=1}^{N} \frac{a_m^{DT} z^{-1}}{1 - p_m^{DT} z^{-1}} \tag{3}$$

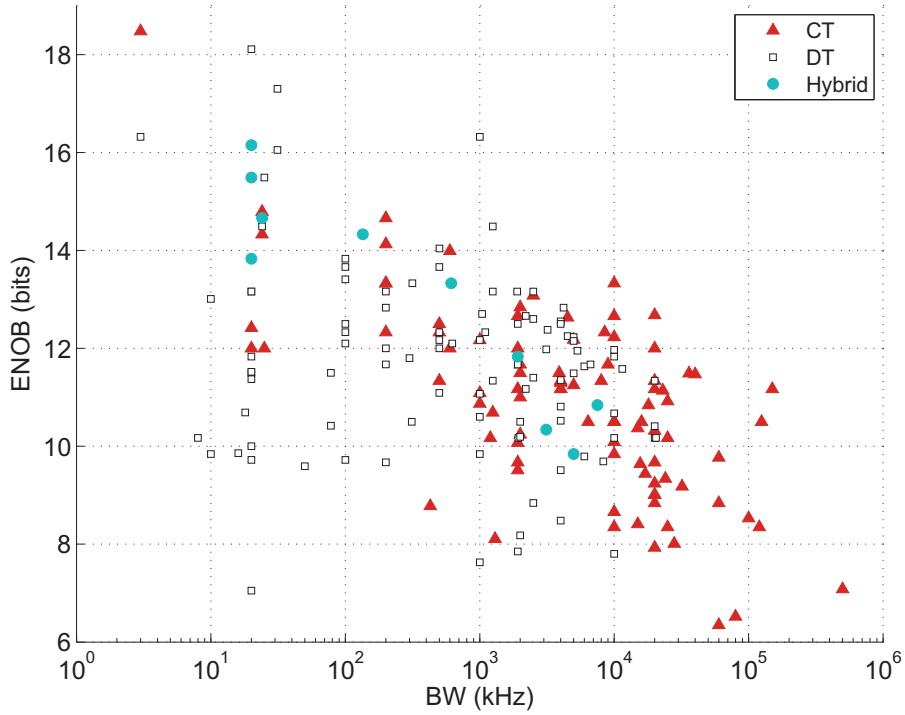
avec :

$$a_m^{DT} = \frac{a_m^{CT}}{p_m^{CT}} \left(\mathrm{e}^{p_m^{CT} T_s} - 1 \right) \tag{4}$$

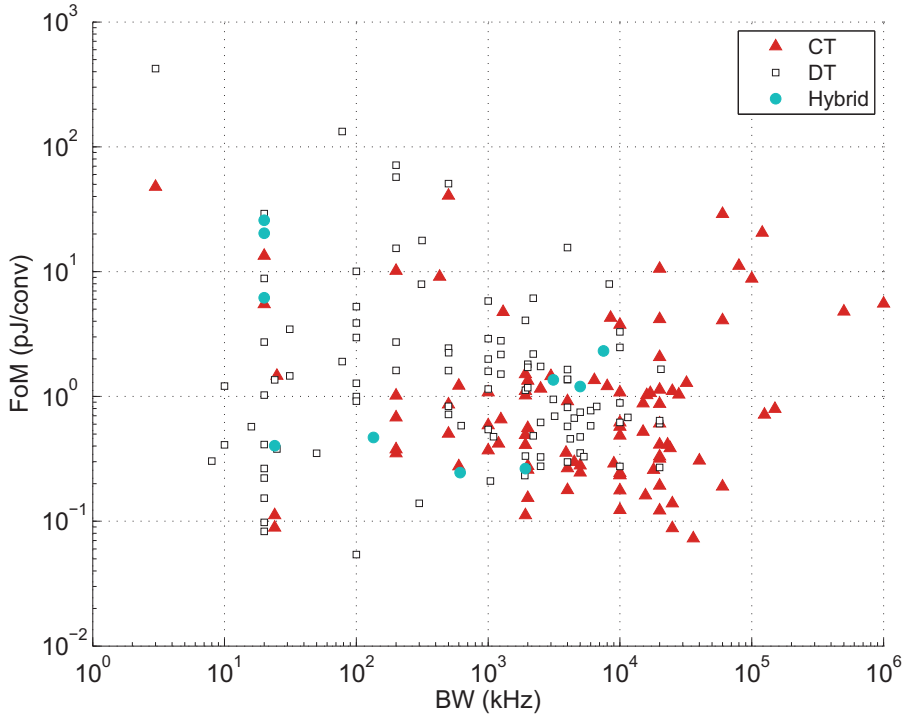
$$p_m^{DT} = \mathrm{e}^{p_m^{CT} T_s} \tag{5}$$

Le calcul des coefficients de l'architecture TC se fait de manière similaire au cas des modulateurs TD.

Une étape primordiale dans la conception des circuits est la phase de simulation. À tout niveau, la réalisation des simulations doit être rapide et conserver le maximum de précision du système. Aux hauts niveaux de conception, ces simulations se basent sur des équations

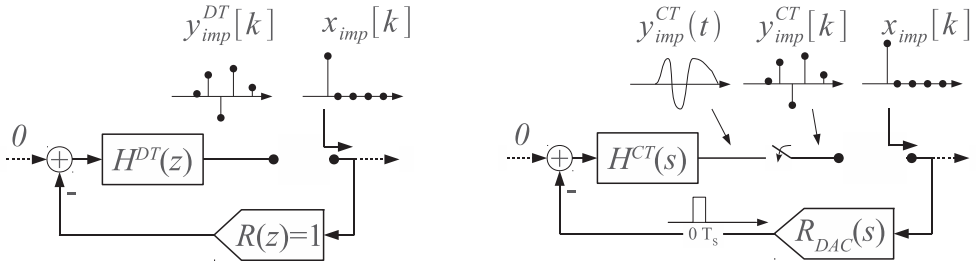


(a) Résolution en fonction de la bande passante



(b) Facteur de Mérite en fonction de la bande passante

FIGURE 11 – État de l'art des circuits de modulateurs ΣΔ — Vue générale



(a) Modulateur à temps discret (b) Modulateur à temps continu

FIGURE 12 – Schémas de la réponse impulsionnelle en boucle ouverte

temporelles assez simples qui décrivent le comportement des blocs du circuit. Comme pour tout système de simulation nous sommes confrontés à deux problèmes : le temps d'écriture et de développement du système de simulation, puis le temps d'exécution de la simulation. Souvent, plus le temps de développement est long, plus le temps de simulation est court. Durant ce travail de thèse nous avons expérimenté différentes techniques de simulation que nous regroupons en trois méthodes : la description noeud par noeud, la description matricielle via les espaces d'état et enfin, la simulation par blocs fonctionnels graphiques. Nous montrons que la méthode matricielle par espaces d'état est la plus appropriée et nous développons la technique pour l'appliquer au cas des systèmes TC comme illustré sur la Figure 13. Cette méthode nous permet de simuler précisément et très rapidement

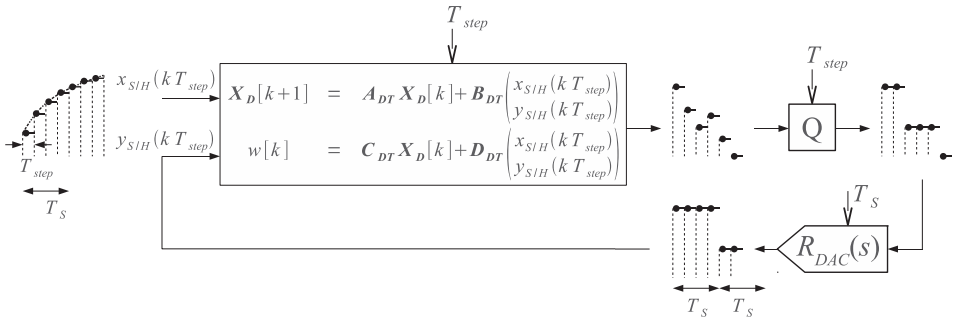


FIGURE 13 – Schéma de mise en œuvre du modèle à espace d'état discrétisé d'un modulateur TC

n'importe quel modulateur TC à CNA NRZ et de type CIFB.

Partie III : L'architecture Multi étage à suppression de bruit (MSNBC)

Dans ce travail de thèse, nous proposons une nouvelle architecture de modulateur ΣΔ adaptée à la numérisation des signaux pour la prédistorsion numérique. En se basant sur le spectre des signaux distordus et prédistordus, nous montrons qu'une structure parallèle à décomposition fréquentielle est un choix intéressant. Mais les contraintes de dynamiques sur les modulateurs traitant les bandes de puissance faible sont telles que les structures classiques ne peuvent être utilisées directement. Nous détaillons les caractéristiques du signal considéré durant ce travail ainsi que le cahier des charges associé du convertisseur.

L'idée originelle de la nouvelle architecture est illustrée à la Figure 14. Le signal est supposé être composé d'une bande de forte puissance et de bandes adjacentes de faible puissance (1). On suppose aussi que la STF est telle que, en sortie du modulateur, seule la bande principale de forte puissance est conservée, les bandes adjacentes ayant été filtrées. Alors, la sortie du modulateur est composée de cette partie du signal et du bruit de quantification mis en forme (2). En considérant le signal U qui est construit par la soustraction X - Y, on pressent que le signal X sera atténué sur sa bande principale (3). Et si le niveau du bruit est suffisamment faible, nous aurions alors réussi à filtrer le signal de la bande principale et à ne conserver que les bandes adjacentes. Il suffirait alors d'utiliser d'autres modulateurs ΣΔ passe bande centrés sur chaque bande adjacente pour les numériser avec précision (4).

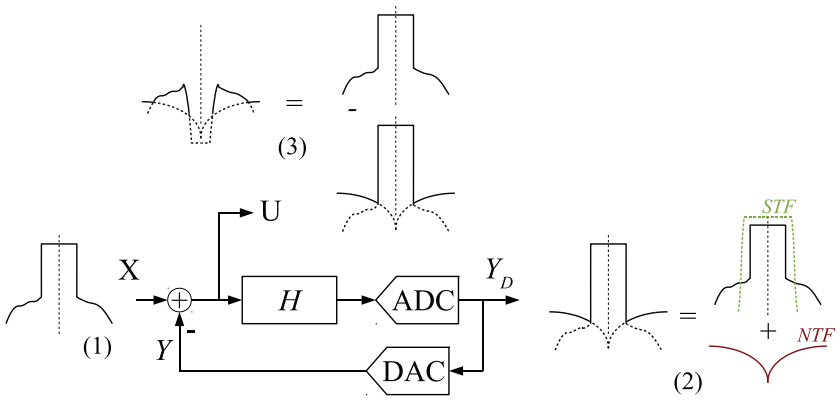


FIGURE 14 – Schéma d'une nouvelle architecture où le signal est filtré

L'étude en détail montrera que l'hypothèse faite sur la STF n'est pas tout à fait juste et que le filtrage ne peut être aussi sélectif que tel qu'on l'imaginait. En outre, le niveau du bruit de quantification mis en forme jouera aussi un rôle prépondérant dans l'évolution de cette proposition d'architecture. Cependant le principe de la soustraction du signal est valide.

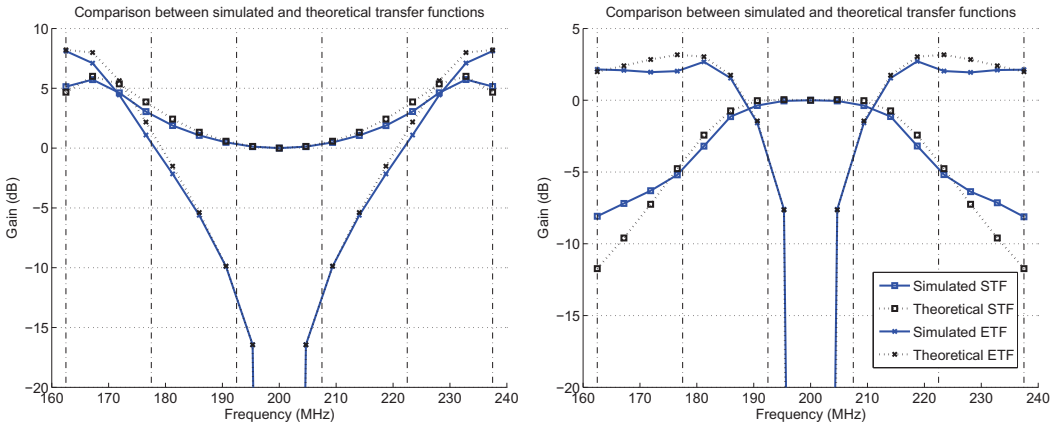
Nous appelons RSTF (Residual Signal Transfer Function) la fonction de transfert modélisant l'atténuation subie par le signal lors de cette soustraction. Nous montrons que son expression générale est :

$$\boxed{RSTF(z) \stackrel{\text{def}}{=} 1 - STF_0(z)} \tag{6}$$

Ce filtre est du même ordre que la STF et la NTF dans les architectures étudiées. Par conséquent, ses propriétés de sélectivité combinées à l'atténuation sont faibles, sauf dans le cas où la STF est strictement unitaire. Dans ce dernier cas, nous obtenons en théorie,

une suppression complète du signal d'entrée et le signal restant de la soustraction est le bruit de quantification mis en forme.

Nous montrons la validité du modèle de la RSTF par une étude théorique confirmée par simulations. Ce résultat est illustré à la Figure 15 où les courbes théoriques et obtenues par simulation sont quasiment identiques.



(a) $\{a_1 = 0.5, a_2 = 0.5\}$ (b) $\{a_1 = 0.18, a_2 = 0.4\}$

FIGURE 15 – Comparaison entre les fonctions de transfert simulées et théoriques

Nous réalisons alors une analyse de performance théorique en utilisant les fonctions de transfert et le profil du signal attendu. Nous montrons que le filtrage réalisé par la RSTF de l'exemple n'est pas suffisamment filtrante.

Nous étudions alors la situation d'un modulateur où la RSTF est conçue à partir d'un gabarit de filtre (Figure 16) et nous montrons qu'il faut un filtre d'ordre supérieur à 12 pour réaliser une atténuation suffisante mais aussi qu'il faut des quantificateurs de haute résolution pour disposer des RSB suffisants sur les bandes adjacentes. C'est pourquoi nous avons proposé de numériser le bruit de quantification directement et de le soustraire par traitement numérique.

L'architecture du convertisseur est la même, alors que le concept de base est différent comme cela est représenté à la Figure 17 et à la Figure 18. Le signal (1) est identique à celui de la Figure 14. La sortie du premier modulateur a été corrigée (2) car la STF des modulateurs est habituellement à peu près plate sur une large bande autour de la bande de travail. En regard des conclusions du paragraphe précédent, nous avons également mis à jour la représentation du signal en (3). En effet, si la STF du primaire ne distord pas trop le signal, alors la partie du signal initial est atténuée en entier et il ne reste que le bruit de quantification mis en forme (affecté d'un coefficient négatif). Ce bruit de quantification est à son tour numérisé sur une bande adjacente par le modulateur secondaire. Sa sortie en (4) est alors composée du bruit à numériser additionné au bruit propre mis en forme du modulateur secondaire. En additionnant les deux signaux, si la STF du secondaire ne distord pas trop le signal, nous supprimons les parties communes de (4) et (5), c'est à dire, le bruit de quantification du modulateur primaire dans la bande adjacente, car (4) en contient une version négative. Ce mécanisme est illustré à la Figure 18. Pour finir, on sélectionne la bande adjacente avec un filtre numérique pour ne récupérer que la bande adjacente avec résolution améliorée.

En analysant théoriquement le système représenté Figure 19, nous montrons que la

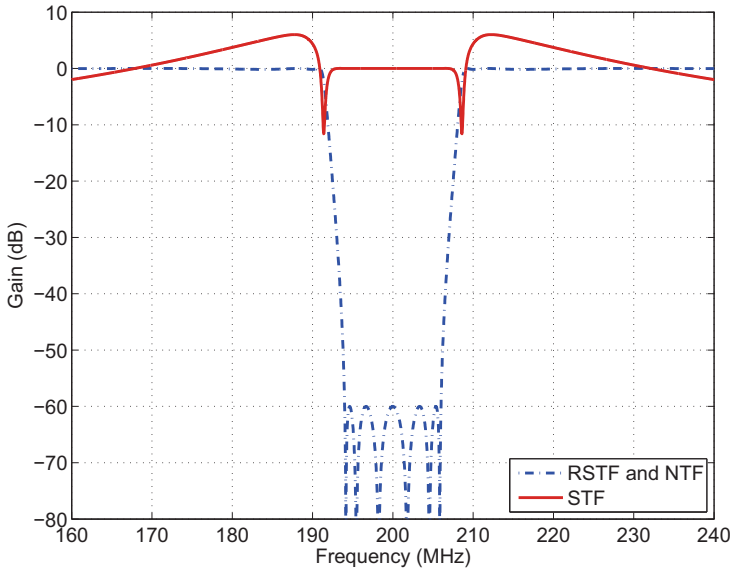


FIGURE 16 – Réponses en fréquence de la STF et la NTF dans le cas d'une RSTF conçu par gabarit

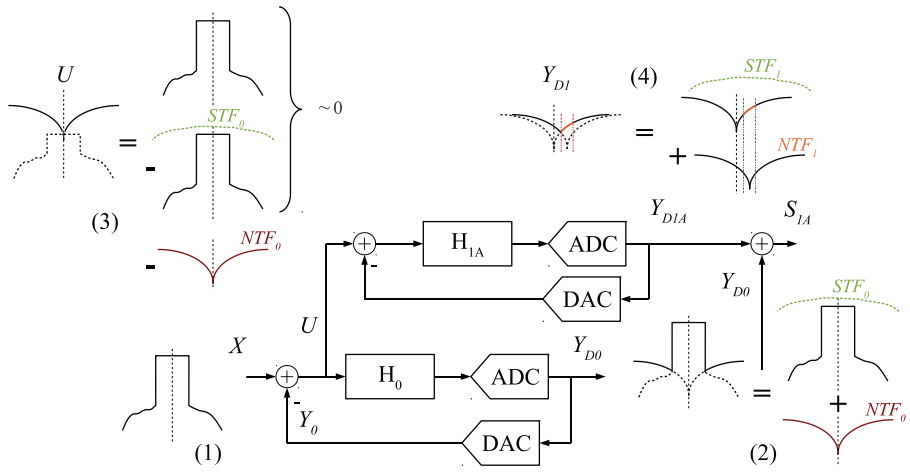


FIGURE 17 – Schéma d'explication de la nouvelle architecture à numérisation bruit

sortie après addition numérique du signal du primaire et du signal du secondaire s'écrit :

$$S_{1A}(z) = X(z) + N_{1A}(z)\, NTF_{1A}(z) \tag{7}$$

Ce qui signifie que ce signal n'est constitué que du signal d'entrée du convertisseur et du bruit de quantification du modulateur secondaire. Nous démontrons la validité de l'analyse théorique par simulation. Les spectres de la Figure 20 montrent la composition de chaque signal à différents points du convertisseur multi-étage.

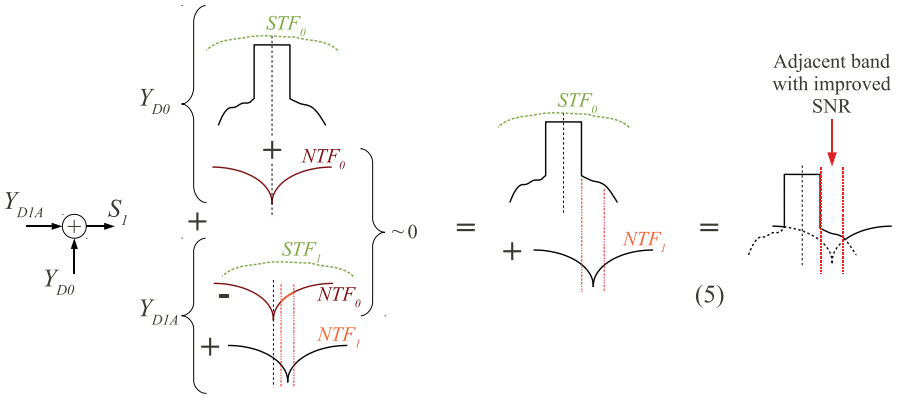


FIGURE 18 – Explication intuitive de l'annulation de bruit dans la partie numérique

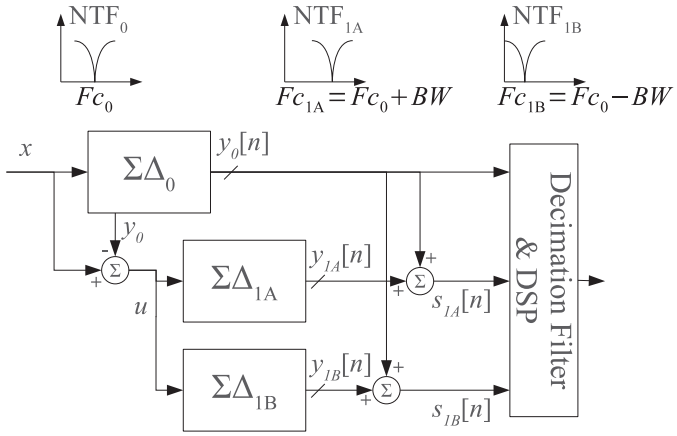


FIGURE 19 – L'architecture ΣΔ MSNBC

Enfin, nous généralisons l'analyse au cas des systèmes où les STF ne sont pas unitaires, ce qui est notamment le cas pour les modulateurs TC. Dans ces cas, il est nécessaire d'ajouter, avant l'addition numérique des signaux, des filtres numériques dits *filtres de suppression de bruit* (Noise Cancellation Filters) comme illustré à la Figure 21.

Nous montrons que, dans le cas des modulateurs à TD (Figure 22), ces filtres doivent inverser la STF du modulateur secondaire :

$$\frac{NCF_{1A}^{N}(z)}{NCF_{1A}^{D}(z)} = \frac{1}{STF_{1A}(z)} \tag{8}$$

Et ce résultat est confirmé par des simulations.

Nous montrons que dans le cas TC (Figure 23), l'expression est différente :

$$\frac{NCF_{1A}^{\tilde{N}}(z)}{NCF_{1A}^{\tilde{D}}(z)} = \frac{1 + \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)G_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} \tag{9}$$

Ce résultat est aussi validé par simulation.

En dernière partie, nous traitons de la méthodologie de conception de tels convertisseurs. Nous traitons d'un problème constaté lors de nos simulations avec la boîte à outils

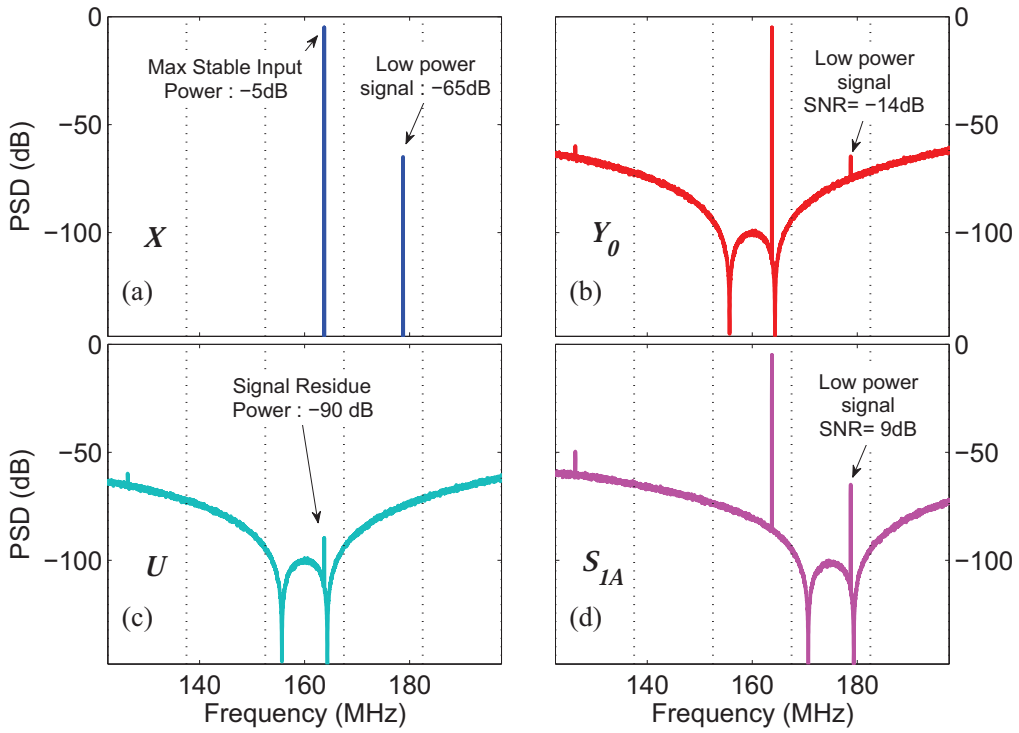


FIGURE 20 – Spectres des signaux de l'architecture obtenus par simulation

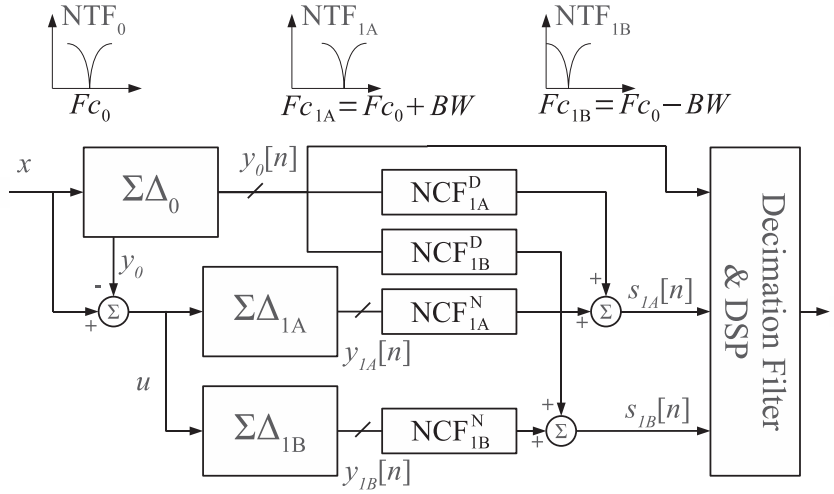


FIGURE 21 – L'architecture générale MSNBC

Delta-Sigma MATLAB. Ce problème nous a poussé à réaliser nos simulations sur des modulateurs centrés autour de $F_s/5$ et non $F_s/4$ pour éviter l'apparition de distorsions dont l'origine n'a pu encore être clairement déterminée comme illustré par les spectres à la Figure 24.

Nous proposons une méthode d'optimisation de chaque voie du convertisseur pour stabiliser et simultanément maximiser le RSB maximum de chaque modulateur. Cette optimisation est opérée en modifiant le gain hors bande de la NTF, car le RSB et la stabilité dépendent de ce paramètre, comme le montrent les courbes à la figure III.34. L'algorithme

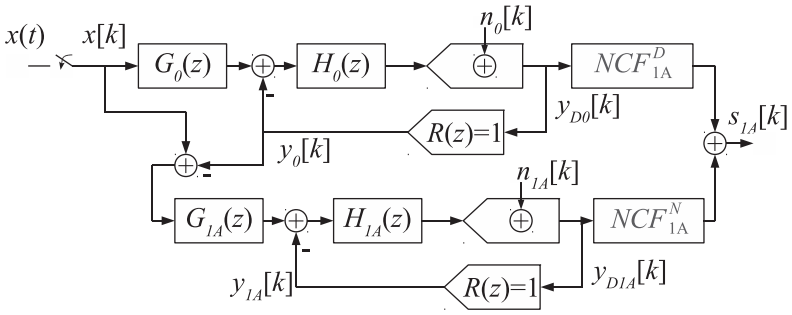


FIGURE 22 – L'architecture générale MSNBC TD

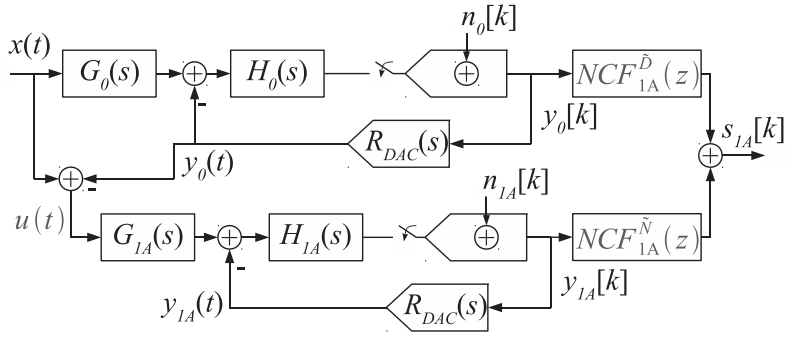
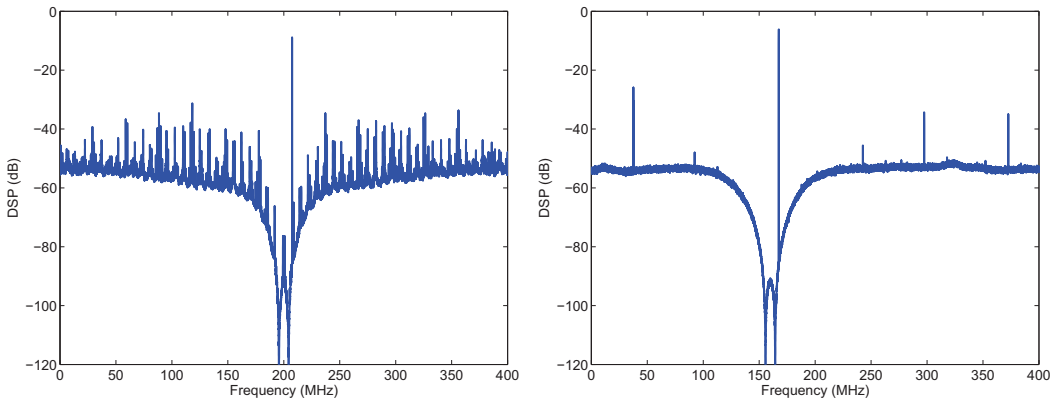


FIGURE 23 – L'architecture générale MSNBC TC



(a) Effets non linéaires dans les modulateurs $F_s/4$

(b) Réduction des effets non-linéaires pour les modulateurs non-$F_s/4$

FIGURE 24 – Comparaison de spectres pour différentes fréquences centrales

proposé est schématisé à la Figure 25.

Enfin, nous proposons une étude de l'espace de conception haut niveau de ce nouveau type de convertisseur par simulation. Les paramètres d'ordre de filtre de boucle et de quantification sont variés pour étudier les performances. Nous montrons que deux configurations sont possibles pour le modulateur primaire afin de respecter le cahier des charges. Nous montrons enfin que deux configurations sont aussi possibles pour le modulateur secondaire et que, conformément à l'Equation (7), le RSB, par suite de la suppression du bruit, est indépendant du modulateur primaire (Figure 26 et Figure 27). L'une des configurations

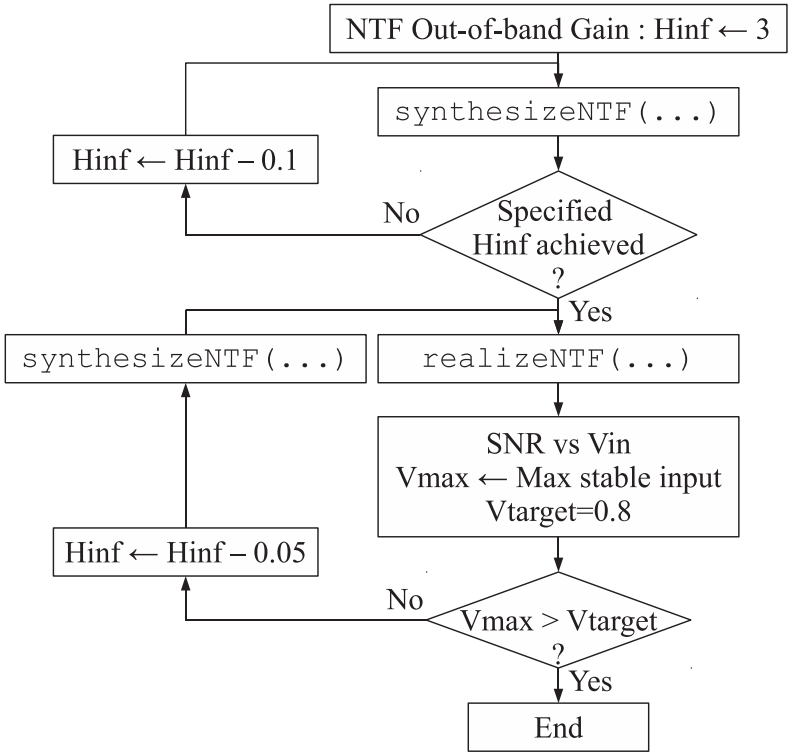
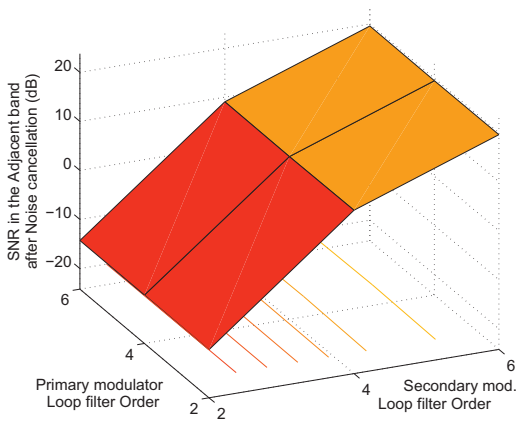
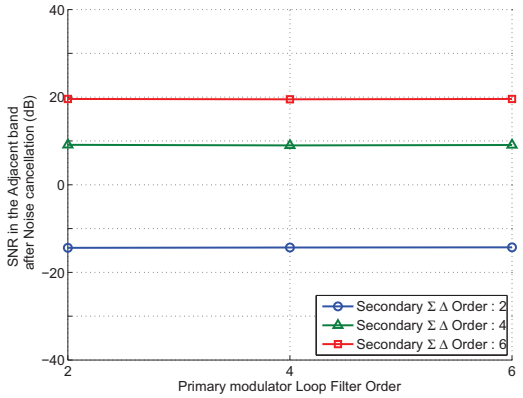


FIGURE 25 – Algorithme d'optimisation pour maximiser le RSB et la stabilité d'un modulateur

est illustrée par les spectres de la Figure 28.

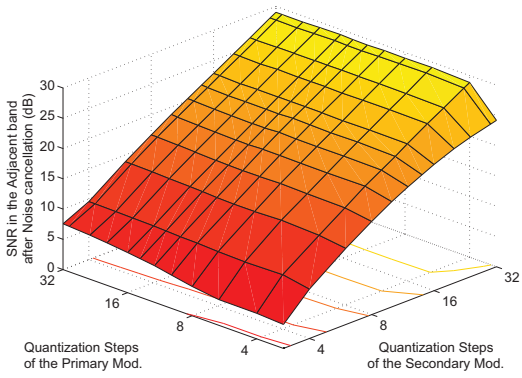


(a) Évolution globale du RSB

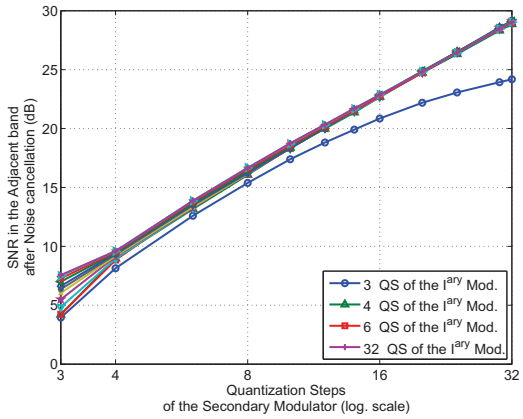


(b) Résultats détaillés : RSB par rapport à l'OFB du modulateur primaire

FIGURE 26 – RSB par rapport à l'ordre du filtre de boucle (OFB) de chaque modulateur dans l'architecture ΣΔ MSNBC



(a) Évolution globale du RSB



(b) Résultats détaillés : RSB par rapport au NPQ du modulateur secondaire

FIGURE 27 – RSB par rapport au nombre de pas de quantification (NPQ) de chaque modulateur dans l'architecture ΣΔ MSNBC

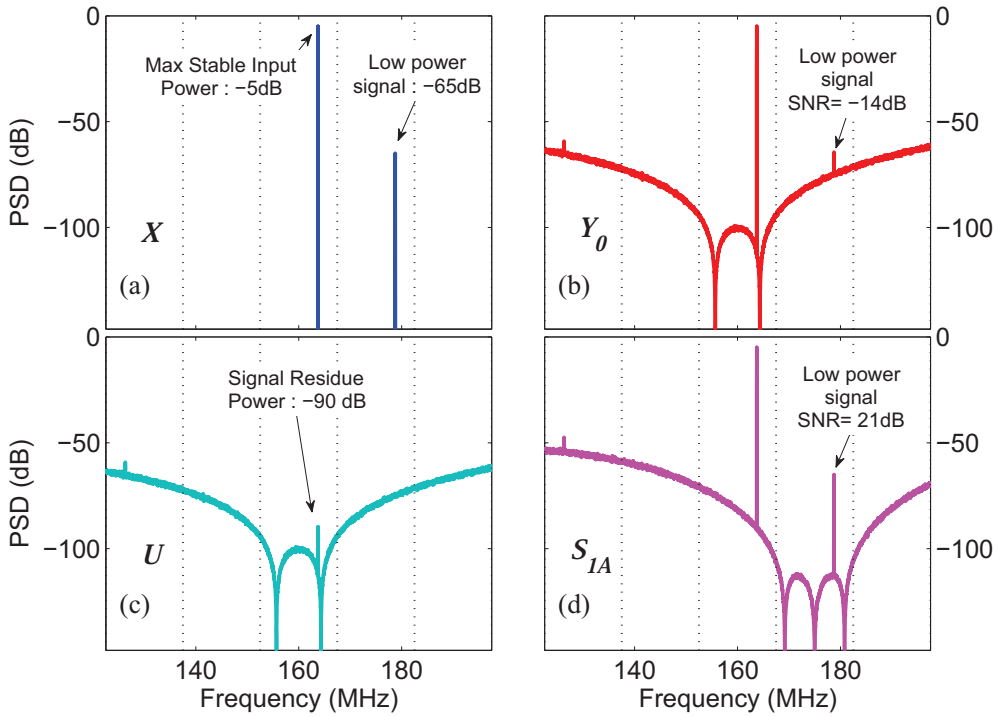


FIGURE 28 – Spectres dans la configuration choisie de convertisseur MSNBC

Conclusion

Dans le cadre de ce travail de thèse, nous avons proposé une nouvelle architecture mêlant décomposition fréquentielle et cascade de modulateurs ΣΔ passe bande. Cette architecture a été nommée MSNBC. Deux points essentiels ont déterminé son développement :

- le signal a une structure particulière du signal est décomposable en plusieurs bandes de fréquence et les modulateurs ΣΔ passe bande sont adaptés pour traiter ce type de signal.
- la volonté de s'affranchir des filtres analogiques de sélection pour chaque bande de faible puissance. Les modulateurs ΣΔ nous offrent des capacités de filtrage que nous exploitons dans cette architecture.

Une nouvelle fonction de transfert a été définie : la RSTF ; celle-ci modélise l'atténuation subie par le signal d'entrée quand on fait la soustraction de l'entrée du modulateur et de sa sortie. Nous avons montré que ses propriétés de sélectivité combinées à l'atténuation sont faibles, sauf dans le cas où la STF est strictement unitaire. Dans ce dernier cas, nous obtenons en théorie, une suppression complète du signal d'entrée et le signal restant de la soustraction est le bruit de quantification mis en forme.

Le second concept de cette architecture consiste à employer d'autres modulateurs ΣΔ passe bande pour numériser le bruit de quantification mis en forme du primaire. Cette numérisation comme toute numérisation classique par modulateur passe bande ne peut se faire que sur une bande limitée. En centrant les modulateurs sur les bandes adjacentes de la bande utile du primaire nous pouvons numériser le bruit et le supprimer de la bande considérée par un traitement numérique. Dans le cas où le modulateur secondaire a une STF non unitaire, ce traitement numérique demande l'usage de filtres numériques NCF dont nous avons développé la méthode de calcul. Dans le cas d'une STF unitaire, une simple addition suffit. Nous avons développé la théorie nécessaire à la conception d'un tel convertisseur dans le cas TD et aussi dans le cas TC.

Au cours de cette thèse, une attention particulière a été portée sur les techniques de simulations. De bonnes techniques de simulations fournissent rapidement des résultats précis, et déverrouillent certains mécanismes d'optimisation qui améliorent significativement les architectures. Ainsi, en se basant sur les outils de simulation de la boîte à outils Delta-Sigma nous proposons une optimisation des architectures TD permettant de maximiser le RSB et d'assurer un certain degré de stabilité. Enfin, des outils inspirés de la boîte à outil Delta-Sigma ont été développés pour la conception et la simulation des architectures TC.

Introduction

Meeting future communications needs requires to increase the capacity of the wireless networks. In addition, the evolution of telecommunications leads to a multiplication of standards with increasing complexity. The coexistence of these systems will require devices to be multi-mode, multi-band and multi-standard. In addition, the field of telecommunications will also face another major challenge: the spectrum limitation whose usage is regulated. To address this limitation, a basic solution is to use the latest digital modulation techniques that offer a better spectral efficiency. However, these modulations have, as disadvantage, a non-constant envelope. And simultaneously, the current trend is to use in base transceiver stations (BTS) a single power amplifier (PA) for multi-carrier transmissions. In both cases, any distortion in the transmission chain will reduce the quality of the signal and result in unwanted spectral regrowth. But the power amplifiers are renowned to be nonlinear.
Moreover, today, other constraints have to be taken into account such as the energy consumption, which has become a major political, economic and social issue. However, the need to reduce the degradations resulting from variable envelopes pushes to operate the power amplifier in a low efficiency mode.

Therefore it is essential to develop more efficient systems in terms of consumption through the use of new techniques and the integration of smart components.
Thus, the capacity and the consumption constraints identify the power amplifier as the critical element in the transmission chain that needs to be improved.

The CATRENE PANAMA [78] project set out to address this need with integrated systems, discrete systems and distributed systems applied to a set of target applications such as 3G/4G and millimetre-wave mobile communications handsets and transceiver base stations, avionics, mobile satellite communications and home networking. This project brings together leading European partners from the semiconductor, test tools, electronic design automation and academic worlds to focus on future power amplifiers and transmitter systems. Our involvement in this project allowed us to work in collaboration with some industrial partners and particularly with NXP.

There are a number of linearization techniques to improve the linearity of the power amplifiers and which enable, at the same time, to improve the efficiency. One of them, the digital predistortion (DPD), is of particular interest because it benefits from the technical advances of the digital part and communications systems increasingly use digital modulation.
Its implementation, in current and future emission chains, is a relatively low extra cost in the digital part, however it requires a measurement of the distortion generated by the amplifier and thus, a possibly dedicated, feedback path to convert the distorted analog radio-frequency (RF) signal to digital domain. In this system the analog-to-digital converter which is in charge of the measurement of the distorted signal must meet the requirements on the signal resolution and bandwidth. These needs are quite challenging in the

context of digital predistortion and, in addition, here too, its energy consumption must be as minimum as possible.

Problem statement

First, the latest communication systems use relatively wide bandwidths. The distorted signal contains unwanted signals called intermodulation products, and is characterized by a spectrum P times wider than the original, where P is the considered intermodulation order. In practice, we aim at digitizing at least intermodulation products of order 5. In addition, these signals are centered at a high transmission frequency. We realize that in this type of application, which is the digital predistortion, validating the sampling theorem establishes the frequency converter to very high values if we do not reduce the center frequency of the signal to a low value. Second, the resolution conversion of these distorted signals must be very high: because, on the one hand, multi-carrier signals have very high dynamics and on the other hand, the distortions may be small changes in the original signal.
Various techniques are used to increase the performance of Analog-to-Digital Converters (ADC) as time-interleaving often used with pipelined ADCs or the parallelization of processing such as processing with decomposition into smaller frequency bands. Among the various converters, sigma-delta ($\Sigma\Delta$) modulators architectures are of particular interest: a high accuracy can be achieved for band-pass signals centered around high frequency with few components. Despite a strong limitation of the converter bandwidths due to their operating principle based on over-sampling, recent literature reports some circuits whose bandwidths allow to consider a possible use for broadband telecommunication applications.

This thesis aims at developing an ADC for the measurement of the signal in the feedback path of transceiver systems in the context of digital predistortion in base stations. In particular, we are interested in developing a new architecture based on band-pass (BP) $\Sigma\Delta$ converter which can digitize this signal which can be decomposed in several sub-bands and with very high dynamic range. We propose an innovative structure exploiting the filtering properties of these converters, the cascading of several modulators and their use with different bands in parallel to convert the wideband signal.

Organization

In the first chapter, we introduce the target application of our A/D converter: the digital predistortion. Based on the characteristics of digital modulations we explain the impact of PAs on the amplified signal and the contradictory relationship between linearity and efficiency. We present the models most frequently used to model the distortions caused by the PA and we describe the technique that allows digital predistorter to linearize the response. Then we explain the requirements in terms of A/D conversion and we briefly present the state of the art of converters to explain the choice of $\Sigma\Delta$ modulators for the design of this new converter. Finally, the effect of quantization of the measurements on the performance of the DPD is illustrated by simulations.

The second chapter is devoted to the presentation of the A/D conversion by $\Sigma\Delta$ modulator. After a few reminders about the A/D conversion and $\Sigma\Delta$ modulation, we detail the different high-level design choices and the different main architectures published so far. We also present a state of the art of modulators to illustrate their essential characteristics. Then we discuss their design and their high-level simulation. We describe how to obtain the coefficient of a given architecture from a noise transfer function (NTF) that can be

almost of any kind, both in the discrete-time (DT) and continuous-time (CT) systems. Then we discuss the technique to perform fast and accurate simulations.

In the third chapter we present our new converter architecture. We recall the particular characteristics of the signal under consideration and we address the question of the choice of the center frequency. Then the operating principles of the architecture are described and illustrated by simulations in both cases, DT and CT. This new architecture is based on the exploitation of a new transfer function (RSTF) and the digitization of quantization noise on each band and its cancellation by digital processing. We then discuss the high-level design of this type of converter. We describe the nonlinear phenomenon of $\Sigma\Delta$ centered around $F_s/4$, which justifies our choice of center frequency for our simulations. Then, we propose an optimization algorithm to maximize the SNR while maintaining a degree of stability represented by the maximum stable input. This optimization is used to ensure that the modulators of all channels have the same stability characteristics, whatever their order or resolution of quantizer are. Finally, we present extensive simulation results to show the influence of each parameter of the architecture. As expected by theory, we find that the noise cancellation in the adjacent band is independent of the parameters of the primary modulator. Moreover, we can choose the set of parameters that achieve the target performances from these simulation results.

Chapter I

Linearization of power amplifiers

This first chapter is dedicated to the presentation of the context of this thesis. As the primary objective of this thesis focuses on the design of an A/D converter for the digital predistortion of power amplifiers, we begin by presenting the digital predistortion with its motivations.

We begin by presenting the characteristics of current communications systems. These systems are composed of a digital processing part and one other analog processing. They use digital modulation techniques known to transmit and receive information efficiently. We then give the general characteristics of these signals that help to explain the difficulties to transmit them at high power levels. And then we specify their requirements in the case of a specific standard that will be used as a case study in the design of the converter. After these very high-level considerations of the transmitter system, we focus on particular component of the chain : the RF power amplifier. Presenting the nonlinear effects of PAs we show that the characteristics of these signals impose significant constraints on the operation of the PA in contradiction with the power efficiency. This section will present the PA models used for the simulation and the digital predistortion technique. Finally, we present the A/D conversion in the context of linearization of PAs. We discuss the general conversion needs for this type of application, and we specify a scenario of transmission that we use to define the needs of our converter. We then present a state of the art to introduce the principal A/D converter architectures and their main features. Finally we illustrate the effect of quantization on the performance of DPD with simulation results.

I.1 Digital transceiver systems

I.1.1 Transceiver systems

A communication consists in the transmission of information, i.e. transmission of a signal, from a transmitter to a receiver. To implement this operation, telecommunication systems perform a number of transformations of the message to be transmitted to make it suitable for its propagation. These transformations can be characterized by the nature of the processed signal and intrinsically by the type of the operating electronics: digital or analog. Figure I.1 shows the general composition of a current transmitter describing the analog electronic part. The digital part performs the traffic handling and the coding of data to be transmitted. These data are converted into an analog signal by the digital-to-analog converters (DAC). This signal is filtered and it is used to modulate high frequency carriers in quadrature. The modulated signal is then amplified and is radiated by the antenna. The amplification stage is a critical block as it significantly impacts on the overall performances

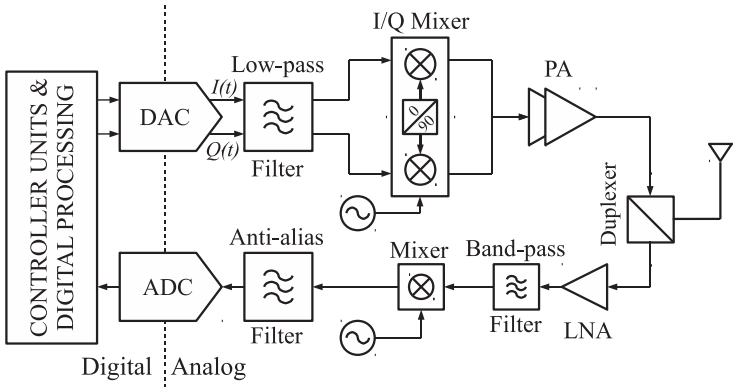


Figure I.1: Block diagram of a general digital transceiver

in terms of energy consumption and signal quality.
The receiving path is similar to the emitting path: processing stages are mainly reversed. The RF electromagnetic wave is intercepted by the antenna and the signal is guided to a low noise amplifier (LNA) to be amplified. The signal is filtered and down-converted to DC or to a given center frequency for analog-to-digital conversion depending on the type of the converter. Eventually the signal is decoded and processed in the digital part.

The digital part for the emitting path is described in Figure I.2.

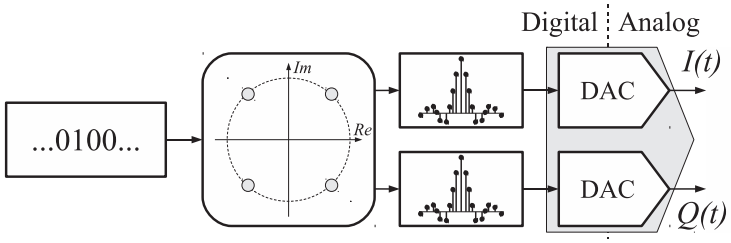


Figure I.2: Block diagram of a digital transmitter

First, the binary data are aggregated and represented by complex symbols whose value will modify physical parameters of the carrier (amplitude, frequency and or phase). This impulse train is up-sampled and filtered by a digital shaping filter in order to limit the bandwidth and to mitigate inter-symbol interferences (ISI). Then the signal is converted into its analog form.
In the receiver a reverse process of demodulation is done to extract the data.
We will now give some details on digital modulations to provide some information on the dynamic properties of the signal.

I.1.2 Digital modulations

I.1.2.1 Symbol mapping

Digital modulation is characterized by the fact that the message to be transmitted is in digital form [1]. In the case of a message originating from an analog source such as speech signal, the information output from the microphone must be digitized. We will explain the nature of this processing in Chapter II.

[1] An example of digital message is a text

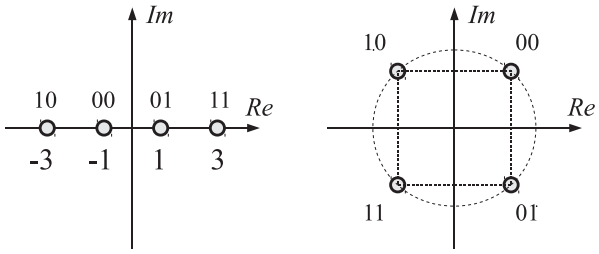
The digital signal consists of a series of coded samples of m-bit binary words. This bit sequence is an abstract quantity and it must be assigned to a physical representation such as an electric (more generally, electromagnetic) signal so that it can be transmitted. The basic idea is to modulate one parameter or more of this signal so a receiver can detect these modulations and extract the information. To modulate the electric signal, one associates to every n-bit word a unique symbol chosen from 2^n symbols, the alphabet. These symbols can be real (modulation of a single parameter) or complex (amplitude and phase modulation) and are called baseband complex symbols. One can refer to Appendix A for detailed derivations of this model. For example to encode 2-bit words we can either use an amplitude modulation with four discrete states:

$$\{-3, -1, 1, 3\}$$

Or we can use amplitude and phase modulation using four complex symbols:

- using a 4-state QAM [1]
$$\{-1 - i, -1 + i, 1 - i, 1 + i\}$$
- using QPSK [2] modulation
$$\left\{e^{-i\frac{3\pi}{4}}, e^{i\frac{3\pi}{4}}, e^{-i\frac{\pi}{4}}, e^{i\frac{\pi}{4}}\right\}$$

We can represent graphically the set of symbols on the complex plane as shown in Figure I.3 referred to as constellations.



(a) Digital AM (b) 4-QAM

Figure I.3: Constellations of digital modulations

I.1.2.2 Up-sampling and pulse shaping filter

The up-sampling and the pulse shaping filter are used to generate digitally the analog signal that will load the PA. From a transmission point of view, the filter limits the signal bandwidth while maintaining the useful content.

In the case of unitary channel model, this filter must meet a particular requirement. Its impulse response must be null at every symbol instant except the running one in order to maximize the symbol signal to noise ratio at the receiver. This property cancels, by definition, the inter-symbol interference and is called the Nyquist ISI criterion. A transmission satisfying this condition is said Nyquist channel.

[1] Quadrature Amplitude Modulation
[2] Quaternary Phase-Shift Keying

The raised-cosine (RC) filter is an example of filter used in telecommunications to satisfy the Nyquist ISI criterion. The impulse response of such a filter is given by:

$$h_{RC}(t) = \text{sinc}\left(\frac{t}{T}\right)\frac{\cos\left(\frac{\pi\beta t}{T}\right)}{1-\frac{4\beta^2t^2}{T^2}} \tag{I.1}$$

where T is the symbol period, $\text{sinc}(x) = \frac{\sin(\pi x)}{\pi x}$ and β is referred to as the roll-off factor. This factor β is related to the steepness of the frequency response and it depends inversely on the impulse response length. However, it does not change the 3dB-bandwidth.

It should be noted that in communication systems, this filter is split into two filters, one being placed in the transmitter, the other in the receiver. This decomposition is performed by making a filter whose squared frequency response is equal to that of the RC filter.
The root-raised-cosine filter (RRC) is defined in such a way and its frequency response $H_{RRC}(f)$ is:

$$|H_{RRC}(f)| = \sqrt{|H_{RC}(f)|}$$

It is worth noting that this filter does not satisfy the Nyquist ISI criterion. However, the combined transmit and receive filters form a RC filter.

I.1.2.3 Peak-to-Average Power Ratio

The complex envelope $\mathcal{E}(t)$ of an RF quadrature amplitude modulated carrier $p_{RF}(t)$:

$$p_{RF}(t) = I(t)\cos(\omega_0 t) - Q(t)\sin(\omega_0 t) \tag{I.2}$$

is given by the equation:

$$\mathcal{E}(t) = I(t) + jQ(t) \in \mathbb{C} \tag{I.3}$$

We can define the instantaneous power of the complex envelope:

$$p_{\text{inst}}(t) = \int_t^{t+\delta t} |\mathcal{E}(u)|^2 \mathrm{d}u \tag{I.4}$$

and the average power:

$$P_{\text{avg}} = \frac{1}{\Delta T}\int_0^{\Delta T} |\mathcal{E}(t)|^2 \mathrm{d}t \tag{I.5}$$

with $\delta t \ll T_{mod}$ and $\Delta T \gg T_{mod}$, T_{mod} is the period of the signal $\mathcal{E}(t)$.
The Peak-to-Average Power Ratio (PAPR) is defined by:

$$PAPR = 10\log_{10}\left(\frac{\max_t p_{\text{inst}}(t)}{P_{\text{avg}}}\right) \tag{I.6}$$

By definition the PAPR depends on the symbols modulation and on the pulse shaping filter. The Figure I.4 illustrates these quantities for a QPSK modulated signal (β=0.22). We note that the signal envelope varies significantly and these variations are at the heart of the problems of signal amplification. We will discuss more precisely the input/output (I/O) characteristic of a PA in the following sections, but we can already recall that a PA distorts the signals with high amplitude. One of the first techniques to ensure the quality of the signal was to operate the PA in its linear region all the time. This technique is called the back off. It is used to define an operating point yielding to a quasi-linear I/O characteristic. The definition of this operating point is based on the PAPR. Indeed, the PAPR indicates in a sense the minimum interval covered by the fluctuations of the

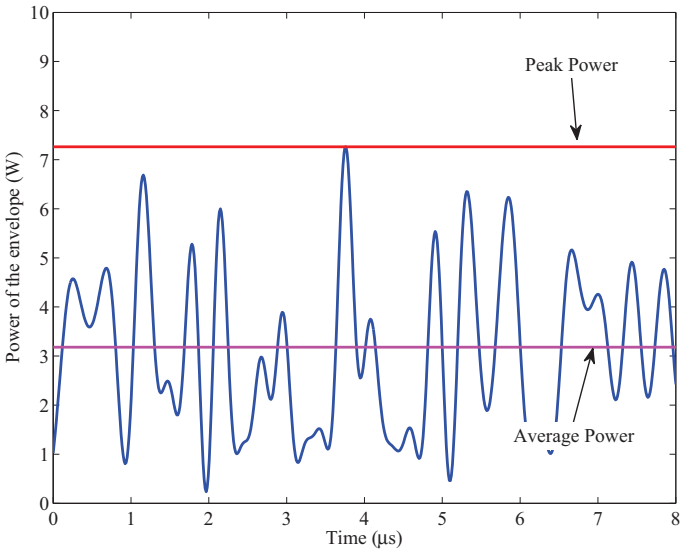


Figure I.4: Instantaneous power of the complex envelope of a QPSK signal.

envelope of the input signal. If part of this interval value overlaps the nonlinear region, there will be distortions. The technique of back off is to set the average power such that this interval is not overlapping the nonlinear region. The operating point is then backed off. However we will see that this technique has a fundamental drawback regarding the power consumption.

I.1.2.4 Multiple access

Another key feature of telecommunication systems is how the physical medium is shared. That is called the access method. There are mainly three methods:

- the *Time Division Multiple Access* (TDMA) method, where the time is divided into time slots in order to share the communication medium. Each network element transmits during a specific time interval.

- the *Frequency Division Multiple Access* (FDMA), where the frequency spectrum is divided in several channels. Each network element transmits using a specific frequency band. With this method simultaneous transmissions are possible. I include in this access mode OFDMA (Orthogonal Frequency-Division Multiple-Access) which is an advanced version of frequency multiplexing [36].

- the *Code Division Multiple Access* (CDMA)/*Spread spectrum multiple access* (SSMA), where sharing is achieved in an *abstract* way by making each binary message orthogonal to all others on the network. The feature of this technique is that transmission is done using a wide bandwidth in which the signal energy is spread. This access method combines naturally with the others as it is the case in 3rd generation communication standard UMTS [12]. A channel is then mainly characterized by its orthogonal code and multiple users can share the same frequency band at the same time.

I.1.3 Base transceiver stations features

In this work, we focus on a particular structure of the cellular network: the base transceiver station (BTS). A BTS is a transmission and reception system in a fixed location consisting of one or more receive/transmit antenna and electronic circuitry, used to handle cellular traffic. It serves as a bridge between all mobile users in a cell and connects mobile calls to the mobile switching center [1]. The BTS main feature is that it is connected to the grid and is therefore less subject to limitations regarding energy consumption. Therefore, it is possible to implement heavy data processing (management network or signal processing).

Installations typically have several antennas each serving a specific angular sector. There are two possible implementations to serve users (or channels) in a sector. The first is to use a complete transmit path for each channel involving as many power amplifiers as channels, and then combine the signals before the antenna. This implementation leads to large size systems and to limited flexibility in terms of radio resource management. The second possibility is more flexible and more compact. It uses a single amplifier for multiple carriers. They are combined in the digital domain before the DACs. This kind of system is referred to as multi-carrier system. The drawback of the technique is that the combined signals show an even higher PAPR. In order to maintain the level of linearity required by the communication standard, the amplifier may have to be backed off even more, impacting the efficiency of the amplifier.

This disadvantage can be reduced at the cost of digital signal processing as it is the case in digital predistorted systems.

I.1.4 Use case communication standard

In this thesis we develop a new architecture of A/D converter suitable for digitizing the signals for the digital predistortion technique. Since this study covers high-level design aspects (system level), the applied method turns out to be of a general scope and can be applied in any standard.
However, in the framework of the PANAMA project we apply this method to the case of WCDMA transmissions defined by the 3GPP. Standards using this technique are for example the UMTS and its evolution the HSDPA. UMTS is now well developed and established but still currently being expanded. For example, in late 2011, 40% of customers of mobile operators in France, use 3G networks [20]. This means that it is desirable to improve now the facilities to meet the future requirements of limited spectrum by the rapid increase in the number of users and the emergence of new standards; and for the future requirements of energy consumption reduction. So, in this work, we use UMTS as a use case to define the design constraints of our system. We considered some radio transmission aspects that are defined in [12] and in the *Test Model 1* defined in [13]. We chose to use the configuration *I-3* of the 4C-HSDPA (see Table 5.0aB in [12]) and all these considered aspects are summarized in Table I.1.

[1] Description from the Canadian Radio-television and Telecommunications Commission

Standard	3GPP WCDMA
Downlink (DL) Frequency Band	2110 - 2170 MHz
Number of DL carriers	3
Channel Spacing and Max. Channel Bandwidth	5MHz
Transmit pulse shaping filter	RRC with roll-off β=0.22 and symbol (chip) duration 1/3.84 μs
Modulation	QPSK

Table I.1: Considered 3GPP WCDMA specifications

I.2 RF Power amplifiers

In the previous section we presented some features of the digital signal to be transmitted. This signal, when converted to the analog domain, filtered and up-converted to the RF frequency has to be amplified. This is done by the power amplifier. We will see in this section that this component has the characteristic to be nonlinear and its efficiency also varies depending on the signal. We then present the main metrics used to characterize this type of component and the models the most commonly used to model PAs at system-level. Finally, we present the digital predistortion and its mathematical development at the system-level as well.

I.2.1 Effects and characterization of nonlinearity in RF power amplifiers

I.2.1.1 Power amplifiers main characteristics

The power amplifier role is to provide enough power for the signal to ensure its proper transmission.

Efficiency

Active components such as power amplifiers have two inputs and one output: a power input and a signal input and the amplified signal at the output. Ideally the entire supplied power P_{DC} should be transferred in the amplified signal power P_{OUT} but there are conversion losses and we have to consider the power loss P_{DISS} that is dissipated within the amplifier. The diagram in Figure I.5 illustrates the power balance of the system. The power balance

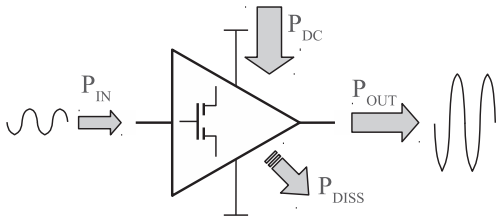


Figure I.5: Diagram of the power balance of a real amplifier.

equation is:

$$P_{\mathrm{IN}} + P_{\mathrm{DC}} = P_{\mathrm{OUT}} + P_{\mathrm{DISS}} \tag{I.7}$$

The fundamental quantity that reflects the ability to convert supply energy into useful energy is the efficiency η:

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{DC}}} \tag{I.8}$$

Other performance metrics are also used: the total efficiency η_{tot} and the power added efficiency (PAE), respectively defined by the following equations:

$$\eta_{\mathrm{tot}} = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}} + P_{\mathrm{DC}}} \xrightarrow[P_{\mathrm{DC}} \gg P_{\mathrm{IN}}]{} \eta \tag{I.9}$$

$$\mathrm{PAE} = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{P_{\mathrm{DC}}} \xrightarrow[P_{\mathrm{OUT}} \gg P_{\mathrm{IN}}]{} \eta \tag{I.10}$$

And this quantity can be extended to the overall performance of the transmitter so that it takes into account the contributions P_{Lin} of the (additional) equipment in charge of the linearization of the PA:

$$\eta_{\mathrm{Lin}} = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{DC}} + P_{\mathrm{Lin}}} \tag{I.11}$$

For some cases, theoretical efficiency calculations can be done considering that the input signal is a pure sine wave with maximum amplitude (i.e. a signal of constant envelope). However, in communication systems, signals are modulated such that the envelope is not constant. The former maximum efficiency becomes an average efficiency that can be calculated from the distribution of the signals since the efficiency of an amplifier depends on the amplitude of the signal envelope.
Usually the efficiency increases while the input power increases and it is maximum for the high power levels as explained in the following section.

Gain

Ideally an amplifier has a constant and unique gain such that its input and output power, P_{IN} and P_{OUT}, are related by the linear relationship:

$$P_{\mathrm{OUT}} = G^{\mathrm{cst}} \cdot P_{\mathrm{IN}}, \quad (\forall P_{\mathrm{OUT}}) \tag{I.12}$$

Actually, no amplifier can satisfy this relationship over its entire operating range and the gain depends, first, on the delivered power:

$$P_{\mathrm{OUT}} = G^{\mathrm{NL}}(P_{\mathrm{OUT}}) \cdot P_{\mathrm{IN}} \tag{I.13}$$

More precisely the static characteristic $G^{\mathrm{NL}} = f(P_{\mathrm{OUT}})$ can be divided into three regions shown in Figure I.6
For small output powers, the gain is constant, it is the linear region.
For the highest power levels, the gain decreases drastically. It is the saturation region of the amplifier: the output has reached its maximum level that is related to the supply voltage.
The transition from the linear region to the saturation region is continuous with a continuous derivative. It is the compression region.
An important point in this area is the *1dB compression point* P_{1dB}, the operating point where the actual gain is 1dB below the gain in the linear region. Typically the operating point of the PA will be chosen following the I/O characteristic toward small amplitudes starting from this point.
Other static linearity metrics are defined in the literature such as the 3rd order Intercept

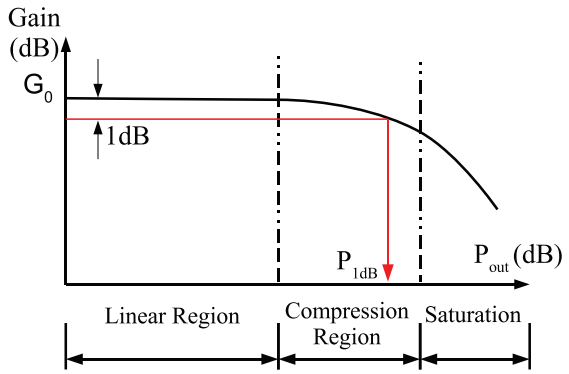


Figure I.6: Gain as a function of the output power

Point Input (IIP3) and the 3rd order Output Intercept Point (OIP3) [68] but they seem to be more appropriate for characterization of receiver amplifiers.

Figure I.7 shows an excerpt from the data sheet of the power amplifier transistor BLF6G22L-40P that shows a typical I/O characteristic and efficiency characteristic of PAs.

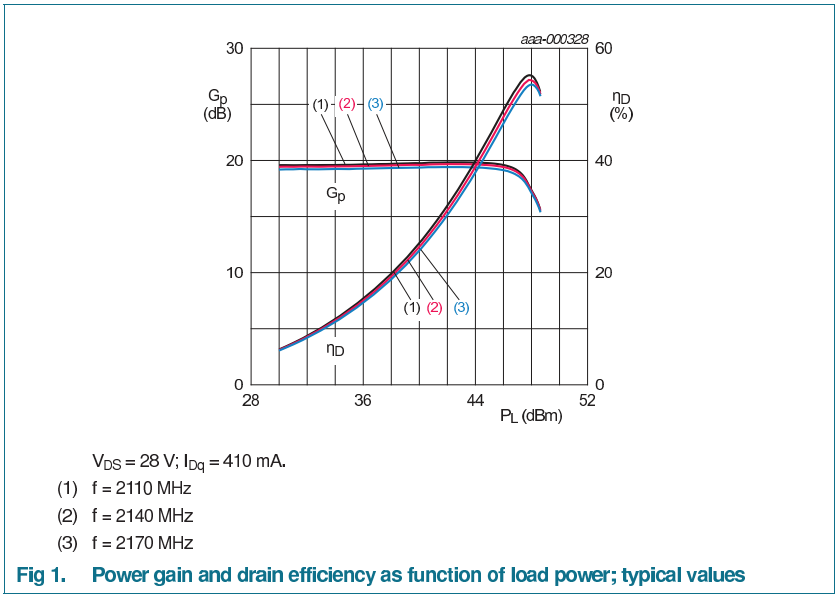


Figure I.7: Excerpt from the data sheet of the BLF6G22L-40P

The horizontal axis indicates the *RF* power P_L delivered to the load that is, the power of the *RF fundamental component* of the generated signal. Using our notation: $P_L = P_{\text{OUT}}$. The group of three curves denoted G_P refers to the vertical axis on the left hand side. Each curve represents the measurement of the gain $G_P = P_{\text{OUT}}/P_{\text{IN}}$ for three different values of frequency. These curves are very close indicating a relatively constant gain according to the frequency (in the operating band).

As shown schematically in Figure I.6, we observe that the gain remains constant between 30dBm and 44dBm. In this region, the amplifier is operated such that its output varies undistorted in the dynamic provided by the power supply of the PA.

Between 44dBm and 47dBm approximately, the gain decreases continuously at a relatively

low rate: the amplifier enters its nonlinear region because the amplifier is operated in discontinuous conduction regimes and linearity is sacrificed to increase the power of the fundamental RF component output.
Finally, beyond 47dBm, the gain drops sharply. The amplifier is then operated in conduction modes where the magnitude of the RF signal no longer increases due to the limitation of power supply.

The drain efficiency $\eta_D = P_{\mathrm{OUT}}/P_{\mathrm{DC}}$ was also plotted on this figure. Similarly, the measurement for the three frequencies is presented and the drain efficiency seems not to vary on the specified frequency band.
We see that the efficiency is very low for small values of power because the PA is operated in conduction modes such that DC power is much greater than the power of the signal generated which is, here, purely sinusoidal.
This efficiency is increased when the delivered power is increased since in the linear operating region, i.e. without interruption of conduction, efficiency is proportional to the RF delivered power as the DC component does not change.
Then, efficiency reaches a maximum around 47dBm. This is the best efficiency area. Here, the average supplied current to the amplifier results from a self-bias and the fundamental component of the distorted signal has reached its maximum which achieves high efficiency.
Finally, the efficiency drops by a few percent. We explain this reduction by a manifestation of the nonlinear capacitors that generate significant leakage currents and by an output signal waveform having a lower power of the fundamental and/or a higher DC component than the previous cases.

I.2.1.2 Nonlinearity characterization

AM/AM and AM/PM characteristics
The characteristic shown in Figure I.6 is often presented differently, with the raw data $P_{\mathrm{OUT}} = f(P_{\mathrm{IN}})$ and is called AM/AM characteristic [1]. This curve has its counterpart in terms of phase: $\varphi = g(P_{\mathrm{IN}})$ and it is referred to as the AM/PM characteristic [2]. These extracted characteristics called static characteristics can be used to fit a mathematical equation to relate the input and the output. Using a polynomial expression we can show that the nonlinear distortion has an impact on the signal spectrum. Indeed harmonic components are emerging. This is a critical disadvantage in telecommunication systems because pollution of frequency bands around the fundamental band also deteriorates the quality of communications in these frequency bands.

Realistic signals
Other type of signals can be used to characterize the nonlinear distortions. These stimuli include two-tones, multi-tones and actual modulated signals and allow to study the behavior of the PA with more and more details.
In the case of modulated signals, specific metrics have been defined to quantify the distortion undergone by the signal.

Adjacent Channel Power Ratio The first one is the adjacent channel power ratio (ACPR) that quantifies the spectral regrowth in adjacent frequency bands. Figure I.8 illustrates a typical situation where the amplifier is loaded by a modulated wideband signal.

[1] AM stands for Amplitude Modulation
[2] PM stands for Phase Modulation

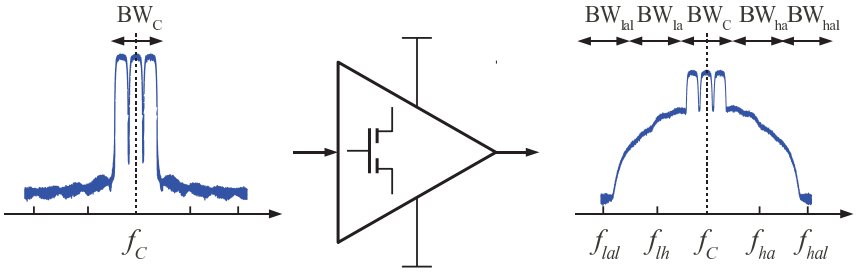


Figure I.8: Spectral regrowth for modulated wideband signals.

The spectrum of the output signal exhibits spectral regrowth in the adjacent frequency bands to the initial band. The general formula for the ACPR is:

$$ACPR_{\text{dBc}} = 10\log_{10}\left(\frac{\int_{BWc} P(f)\mathrm{d}f}{\int_{BWadj} P(f)\mathrm{d}f}\right) \tag{I.14}$$

where $P(f)$ is the power spectral density (PSD) of the signal, BW_C, the frequency band of the undistorted signal, and BW_{adj}, an adjacent frequency band.
One can find several similar definitions for this metric. For example, in the 3GPP WCDMA standard [12], this metric is referred to as Adjacent Channel Leakage power Ratio (ACLR) and it is defined as the ratio of the RRC filtered mean power centered on the assigned channel frequency to the RRC filtered mean power centered on an adjacent channel frequency.

Error Vector Magnitude The second commonly used metric is the Error vector magnitude (EVM). It can be expressed as a percentage (%) and measures, on the overall constellation, the dispersion of symbols obtained after amplification with respect to their ideal value [18]. It takes into account both the AM and PM effects.
Figure I.9 shows the constellation of a weakly distorted signal. The red dot represents the ideal position of a symbol to be transmitted and the green dotted line arrow represents the associated vector. Because of the distortion, the symbols have been scattered around the ideal position (purple dotted line arrow) and each point can be characterized by an error vector (magenta arrow). By calculating the variance of the error vectors the average error power is derived and it reflects with one figure the amplitude error and phase error.

I.2.1.3 Memory effects

Base stations are designed to handle multi-carrier non constant envelope signals with bandwidth spanning over at least 10MHz. Under such conditions, another distortion type becomes significant: the memory effects. These distortions result from thermal and electrical phenomena and the gain becomes dependant on the previous states of the PA.
The effect is visible on AM/AM and AM/PM characteristics where the measurement points are dispersed and the characteristics look like scatter plots. Figure I.10 shows the small dispersion of points when the PA exhibits small memory effects.

I.2.2 Power amplifier response modeling

The defined metrics and the different distortion phenomena presented in previous section are essential in the interpretation of the first step required in the correction of PAs that is

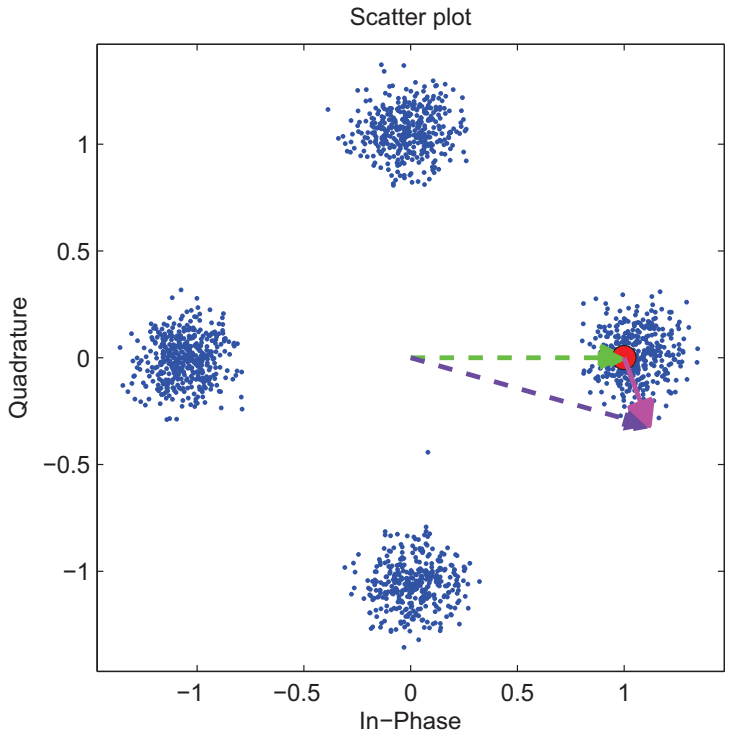


Figure I.9: The error vector magnitude principle

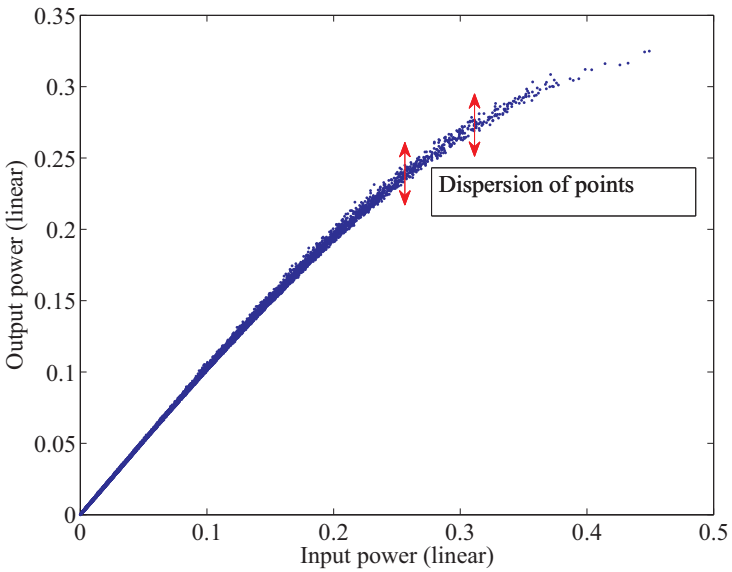


Figure I.10: AM/AM Characteristic with small memory effect

the characterization of PAs.
This section details the main models that are used to simulate the actual behavior of the PA.

I.2.2.1 Behavioural modeling principles

Nowadays, due to the cost and complexity of various telecommunication equipments, efficient simulation (fast and accurate) of such systems is mandatory in order to anticipate any difficulties in the physical implementation. Circuit simulation techniques such as Harmonic Balance provide efficient nonlinear circuit simulation for simple or realistic signals. However, these circuit level analysis techniques turn out to be unsuitable for the simulation of subsystems and complete systems because the amount of data to be processed becomes intractable or simulation time is too long.

System modeling allows abstraction by replacing the circuit description by a behavioral model of relatively simple structure typically a mathematical function. In our case, this mathematical function $f_{NL}(\cdot)$ relates the input signal $p_{RF}(t)$ to the output signal $a_{RF}(t)$ of the device to be modeled:

$$a_{RF}(t) = f_{NL}(p_{RF}(t)) \tag{I.15}$$

This equation can be written using the baseband equivalent model that provides a compact model reflecting only the dynamics of the modulating signal, which are considerably slower than the dynamics of the RF signal. This is particularly useful for numerical time simulations since sampling can be reduced.
Similarly to the definition of the complex envelop $\mathcal{E}(t)$ in the baseband model:

$$p_{RF}(t) = \Re\left(\mathcal{E}(t)\,\mathrm{e}^{j\omega_0 t}\right) \tag{I.16}$$

the distorted amplified complex envelop $a_{\mathcal{E}}(t)$ output by the PA is defined by:

$$a_{RF}(t) = \Re\left(a_{\mathcal{E}}(t)\,\mathrm{e}^{j\omega_0 t}\right) \tag{I.17}$$

where ω_0 is the RF carrier pulsation. Then, the Equation (I.15) can be written as:

$$a_{\mathcal{E}}(t) = \widetilde{f_{NL}}\left(\mathcal{E}(t)\right) \tag{I.18}$$

where $\widetilde{f_{NL}}(\cdot)$ is a complex valued equivalent of $f_{NL}(\cdot)$.

In the remainder of this section we briefly present the nonlinear functions that are frequently used to model PA. These functions are referred to as *PA models* and are classified according to their general features.

I.2.2.2 Memoryless models

These models are constructed from the static AM/AM and AM/PM characteristics that are extracted experimentally. These models assume that the output of the PA depends only on the value of the input at the same instant. The general relationship between input and output is written as:

$$a_{\mathcal{E}}(t) = F[A(t)] \cdot \mathrm{e}^{j\Phi[A(t)]+j\phi(t)} \tag{I.19}$$

where $F[\cdot]$ and $\Phi[\cdot]$ are respectively the conversion function AM/AM and AM/PM and $A(t)$ and $\phi(t)$ are defined by:

$$\begin{cases} A(t) &= |\mathcal{E}(t)| \\ \phi(t) &= \arg\left(\mathcal{E}(t)\right) \end{cases} \tag{I.20}$$

As mentioned earlier, one can extract from experimental data, the parameters value of polynomial models by performing curve fitting. Among the most widely used models there are also Saleh's models and complex polynomials [77, 45].

I.2.2.3 Memory models

The second category of model includes memory models. The most common are those based on Volterra series, which is the most general model. Memory polynomials, Hammerstein models and Wiener models are particular cases of Volterra series [18]. The memory polynomials model is a popular model and we give its expression to illustrate how memory effects are modeled.

Memory polynomials

First of all, we assume that, signals are sampled with period Ts and we denote by $x[n] = x(nTs)$ the ideal sample at nTs of the analog signal $x(t)$. In the memory polynomial model it is assumed that:

$$a_{\mathcal{E}}[n] = \sum_{m=0}^{M} F_m(\mathcal{E}[n-m]) \tag{I.21}$$

$$= F_0(\mathcal{E}[n]) + F_1(\mathcal{E}[n-1]) + \dots F_M(\mathcal{E}[n-M]) \tag{I.22}$$

with $F_m(x) = \sum_{k=1}^{K} h_{mk}x^k$, $h_{mk} \in \mathbb{C}$. The h_{mk} are the memory polynomial model coefficients of the amplifier and their number depends on M, the memory order and K, nonlinearity order.

If M is null, we find the equation of plain polynomial models. We observe that the memory is modeled by the appearance of term dependent on previous input samples.

I.2.3 Non-constant envelop signal amplification

I.2.3.1 Linearity–efficiency trade-off

The impact of the power amplifier on the performance of base stations is twofold. First, PA is one of the BTS devices that consumes the most energy. The overall station efficiency is largely determined by the PA efficiency. Increasing the efficiency is equivalent either to increase the emitted power for the same power consumption or to consume less energy for the same transmission power.

Second, the amplifier also impacts the quality of the signal and also the adjacent channels. But, as mentioned before, when the amplifier operates in its linear region, the power amplifier efficiency is very low, whereas this efficiency reaches its maximum in the nonlinear region. Therefore, a trade-off should be done between linearity and efficiency when operating the PA.

The absolute constraint is to meet standard specifications in terms of linearity so the issue of consumption was essentially avoided in the past and the PA operated in its linear region. However, given that energy has become a major social and economic issue, there is a clear willingness to change the technique. In order to operate the PA in its nonlinear high efficiency region, additional devices will be used to correct distortions i.e. linearize the response system.

There are a large number of linearization techniques and they are usually categorized in two groups [35]. The first group includes techniques aiming at increasing efficiency but maintaining linearity such as the LINC [1], Doherty and EER [2] techniques. The second group consists of techniques aiming at making the system as linear as possible by signal processing methods such as Feedforward, Feedback and Predistortion techniques.

[1] Linear Amplification using Nonlinear Components

[2] Envelope Elimination and Restoration

I.2.3.2 Digital predistortion

The digital predistortion consists in digitally preventing the effect of distortions generated by the amplifier. This correction is applied by adding in the transmission chain a predistortion block before the PA as shown in the diagram in Figure I.11.

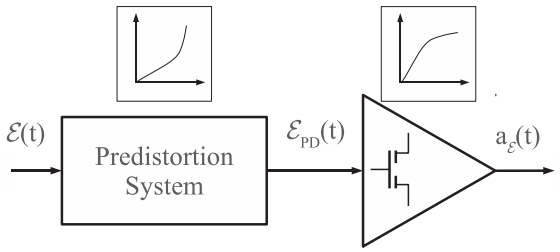


Figure I.11: Simplified diagram of the Digital Predistortion

The signal $\mathcal{E}(t)$ is the complex envelope of the signal to be amplified. It is processed by the predistortion system whose complex output is $\mathcal{E}_{\mathrm{PD}}(t)$. This signal is amplified and distorted by the PA and the result is denoted $a_{\mathcal{E}}(t)$. More precisely, we can write the equation:

$$a_{\mathcal{E}}(t) = G \cdot f_{PA}(f_{PD}(\mathcal{E}(t))) \tag{I.23}$$

where $\mathcal{E}(t)$ is the envelope to be amplified, $G \cdot f_{PA}(\cdot)$ the amplification function of memoryless amplifier and $f_{PD}(\cdot)$ the predistortion function. Ideally, we should have:

$$a_{\mathcal{E}}(t) = G \cdot \mathcal{E}(t) \tag{I.24}$$

where G is the linear gain of the chain.
This equation is true when:

$$\boxed{f_{PD} = f_{PA}^{-1}} \tag{I.25}$$

The predistortion block has to implement the inverse function of the PA.

This technique is preferably implemented in the digital domain since it benefits from the huge technological advances in digital electronics and flexibility. The predistortion has the further advantage of being easily implementable adaptively making the system more robust to variations in the characteristics of the PA caused by aging and temperature or the operating point variations. Figure I.12 shows the detailed block diagram of a transmission system with digital distortion.

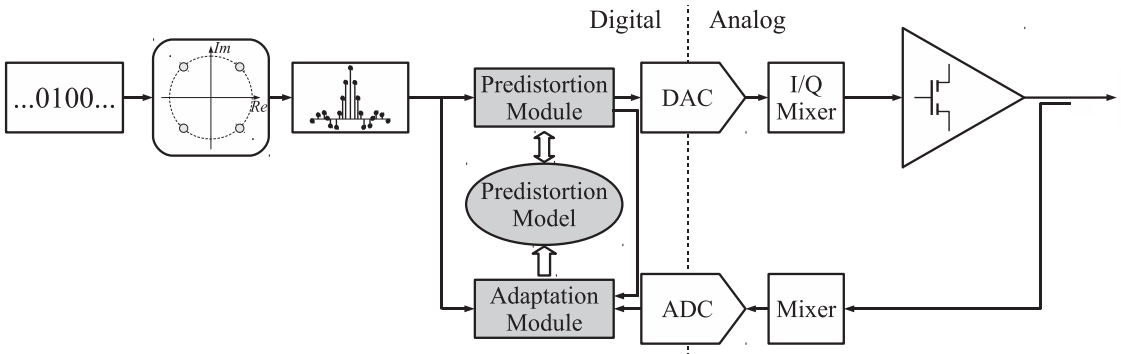


Figure I.12: Detailed diagram of the Digital Predistortion

The predistortion module that implements the predistortion function f_{PD} is located between the pulse shaping filter and the DACs. This module can be implemented in different ways depending on the predistortion model. More precisely, the predistortion module can be implemented as tabulated values using *look-up tables* (LUT) or as a mathematical function that the module will evaluate when it will calculate the predistorted value. For example, the function can be a polynomial expression.
The feedback path is required for measuring distortions and extracting the predistortion function f_{PD} by the adaptation module. This module is located just after the ADC as data has not to be decoded.
In the literature on predistortion implementations, the DAC, ADC and mixer blocks are assumed to be invisible to the system. For the mixer, this coincides with the use of the baseband model. Regarding the DAC and ADC, these blocks are usually transparent to the system because the resolution of each largely exceeds the minimum actual needs of the system.
This is logical since these studies mainly focus on the implementation of the DPD with constraints sufficiently large such as the circuit complexity and convergence that hide the question of the robustness of the system to faults, such as quantification error. However, in some studies, the blocks are optimally sized using simulations [83, 31, 59, 53, 67].
Thus in the next section (§ I.2.3.3), which introduces the two main learning methods and a predistortion model, these DAC and ADC blocks will not be represented. In addition, the signals are represented by their complex baseband equivalent.

I.2.3.3 Adaptation module

Learning methods
There are two techniques to implement the adaptation block that are based on two learning methods: the direct or the indirect learning. These methods can be seen as equivalent in results however they differ fundamentally on their implementation. From a system level point of view, both methods can be used to extract the coefficients of any predistortion model (Saleh, polynomial, memory polynomial...).

Direct learning The operating principle of the direct learning method is represented in Figure I.13. This learning method involves estimating the function f_{PD} directly — online — by minimizing with successive attempts the error δ between the ideal $\mathcal{E}$ and the actual output envelope $a_{\mathcal{E}}$ of the PA. This is usually the method used for LUT-based corrections.
For example, for one output sample, several iterations can be done to find f_{PD} to minimize the error δ. This implementation should provide good convergence results but it needs high processing rates. Moreover, in order to cope with signal variations, this minimization should be done on several output samples. In this case, we can reduce the number of iterations for a given sample to one and use a processing rate equal to the sample rate but the convergence may be longer.
This learning method is used in [14, 47, 53, 60, 65] and references therein.

Indirect learning The operating principle of the indirect learning method is shown in Figure I.14. This learning method consists in estimating non-directly the function f_{PD}, identifying *a posteriori* a postdistortion function f_{POST} also by minimizing the error δ. When the data can be stored for latter processing, the method can be divided into two steps: a *learning phase* and a *correction phase*. During the learning phase, once sufficiently

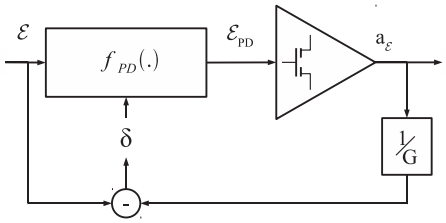
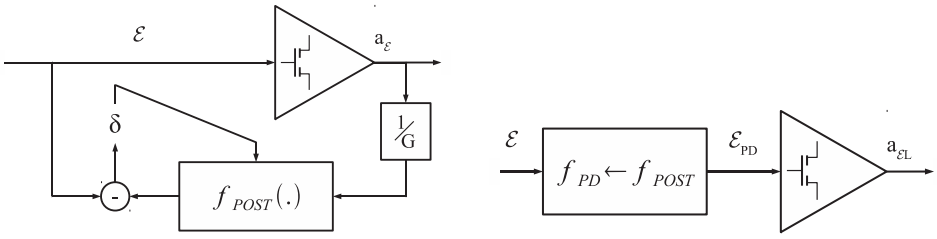


Figure I.13: Diagram of the direct learning method

data are available for processing, the postdistortion function f_{POST} is optimized in order to minimize the error δ between the ideal complex envelop $\mathcal{E}$ and the actual distorted envelop $a_\mathcal{E}$. Then, when this calculation finishes, the postdistortion function f_{POST} is used as the predistortion function f_{PD}. The predistortion is applied to the ideal signal $\mathcal{E}$ to generate the predistorted signal $\mathcal{E}_{PD}$ that is amplified and distorted by the PA. The linearized output is $a_{\mathcal{E}\mathrm{L}}$.
It is usually the chosen method for the identification of predistortion models using memory models [48, 18, 49] that is why it will be used for our predistortion simulations.



(a) Learning Phase (b) Correction Phase

Figure I.14: Diagrams of the indirect learning method

This learning method is also used in [53, 60, 65].

As stated in [65] and references therein, this method may exhibit some drawbacks. First, it seems to be sensitive to measurement errors. We can understand this phenomenon with the matrix formulation of the predistorter function in § I.2.3.3. The second drawback comes from the fact that nonlinear filters are not commutative and using the postdistortion function as the predistortion function does not guarantee optimal correction.

Predistortion models
The role of the adaptation module is to identify the function f_{PD} that will linearize the response of the system. This identification is based on specific model functions for f_{PD}.
Predistortion models are based on PA models and the most common are plain polynomials models, memory polynomials and Volterra series (general case).
We detail here a method for estimating f_{PD} using the memory polynomial model. This description provides a particularly compact formulation of the problem and of its solution. This will give us the trends in terms of algorithmic complexity. Moreover, this development also provides the details for an implementation on MATLAB for fast system simulations.

Matrix formulation of the predistortion using memory polynomials We consider for the formulation of the problem the system structure depicted in Figure I.12. In order to derive the base equations, we assume, as previously mentioned, that the DAC and

ADC have infinite resolution so that they do not introduce quantization errors and can be ignored. Therefore, the system is assumed to be analog valued as there is no quantization. Moreover, we assume the system to be ideally and completely sampled at the period $T_{\mathrm{SAMP}} = T_{\mathrm{SYMB}}/k_{\mathrm{INT}}$ where T_{SYMB} is the symbol period and k_{INT} is the interpolation coefficient of the up-sampler and pulse shaping filter. We adopt the common notation $x[n] = x(n\,T_{\mathrm{SAMP}})$ where $x[n]$ is the ideally sampled signal $x(t)$ at $t = nT_{\mathrm{SAMP}}$. Finally we use the baseband equivalent model allowing to ignore the mixers in the system. Figure I.15 shows the simplified system diagram.

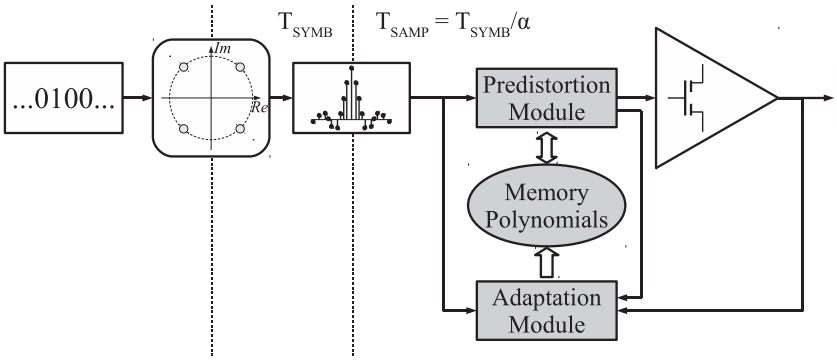


Figure I.15: Diagram of the considered system

We use the indirect learning method to solve the problem and the system during the learning phase is depicted in Figure I.16. During this phase, the ideal complex envelope $\mathcal{E}[n]$ is amplified and distorted by the nonlinear function $G \cdot f_{PA}(\cdot)$ that models the PA response. The output samples $a_{\mathcal{E}}[n]$ are normalized by the linear gain G giving the normalized samples $\widetilde{a_{\mathcal{E}}}[n]$. These samples are stored in an ideal unlimited memory with the ideal undistorted samples $\mathcal{E}[n]$. Then, the postdistortion function $f_{POST}(\cdot)$ is calculated so that the error $\delta[n] = \mathcal{E}[n] - \widehat{\mathcal{E}}[n] = \mathcal{E}[n] - f_{POST}\left(\widetilde{a_{\mathcal{E}}}[n]\right)$ is minimized.

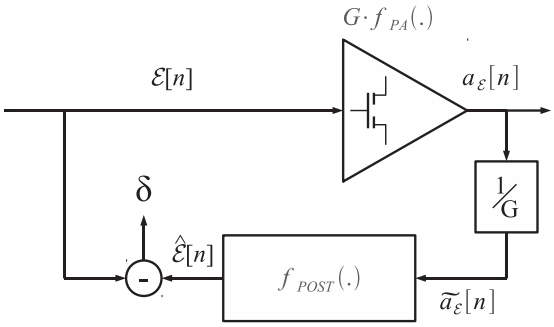


Figure I.16: Signals of the considered system.

In our system, we model the PA response $f_{PA}(\cdot)$ with a memory polynomial model with parameters (K_{PA}, M_{PA}) [1]. Therefore, the predistortion function will be modelled using memory polynomials with parameters (K_{PD}, M_{PD}).

Now we detail the expressions of each signal in the system in order to derive the optimal solution for $f_{POST}(\cdot)$.

[1] K is the nonlinearity order and M is the memory order

By definition, the amplified and distorted signal $a_{\mathcal{E}}[n]$ is:

$$a_{\mathcal{E}}[n] = G \cdot f_{PA}\left(\mathcal{E}[n], \mathcal{E}[n-1], \cdots, \mathcal{E}[n-M_{PA}]\right)) \tag{I.26}$$

And we have (§ I.2.2.3) $f_{PA}(\cdot)$ that is a memory polynomial:

$$f_{PA}\left(x_0, x_1, \cdots, x_{M_{PA}}\right) = \sum_{m=0}^{M_{PA}} \sum_{k=1}^{K_{PA}} h_{mk} \left|x_m\right|^{k-1} x_m \tag{I.27}$$

where h_{mk} are the nonlinear and filter coefficients. In a similar way, we have $\widehat{\mathcal{E}}[n]$ that is equal:

$$\widehat{\mathcal{E}}[n] = f_{POST}\left(\widetilde{a_{\mathcal{E}}}[n], \widetilde{a_{\mathcal{E}}}[n-1], \cdots, \widetilde{a_{\mathcal{E}}}[n-M_{PD}]\right) \tag{I.28}$$

$$= \sum_{m=0}^{M_{PD}} \sum_{k=1}^{K_{PD}} w_{km} \ \left|\widetilde{a_{\mathcal{E}}}[n-m]\right|^{k-1} \widetilde{a_{\mathcal{E}}}[n-m] \tag{I.29}$$

with $\widetilde{a_{\mathcal{E}}}[n] = \frac{1}{G} a_{\mathcal{E}}[n]$ and w_{km} the correction coefficients to be determined.
In order to calculate the w_{km} coefficients, we have to solve $K_{PD} \times (M_{PD}+1)$ equations. To derive the solution, we write the equation system under a matrix form where the system linearly depends on the vector of unknowns. We adopt the following matrix notation:

$$\vec{a_{\mathcal{E}}}[n] = \begin{pmatrix} a_{\mathcal{E}}[n] \\ a_{\mathcal{E}}[n-1] \\ \vdots \\ a_{\mathcal{E}}[n-N] \end{pmatrix} \tag{I.30}$$

$$\mathbf{E}^{\mathcal{E}}[n] = \begin{pmatrix} \mathcal{E}[n] & |\mathcal{E}[n]|\,\mathcal{E}[n] & \cdots & |\mathcal{E}[n]|^{K_{PA}-1}\,\mathcal{E}[n] & \mathcal{E}[n-1] & \cdots & |\mathcal{E}[n-M_{PA}]|^{K_{PA}-1}\,\mathcal{E}[n-M_{PA}] \\ \mathcal{E}[n-1] & & & & \mathcal{E}[n-2] & & \\ \vdots & \vdots & & \vdots & \vdots & & \\ \mathcal{E}[n-N] & |\mathcal{E}[n-N]|\,\mathcal{E}[n-N] & \cdots & |\mathcal{E}[n-N]|^{K_{PA}-1}\,\mathcal{E}[n-N] & \mathcal{E}[n-N-1] & \cdots & |\mathcal{E}[n-N-M_{PA}]|^{K_{PA}-1}\,\mathcal{E}[n-N-M_{PA}] \end{pmatrix} \tag{I.31}$$

$$\vec{h} = \mathbf{vec}\begin{pmatrix} h_{10} & h_{11} & \cdots & h_{1M_{PA}} \\ h_{20} & \vdots & & \vdots \\ \vdots & \vdots & & \vdots \\ h_{K_{PA}0} & h_{K_{PA}1} & \cdots & h_{K_{PA}M_{PA}} \end{pmatrix} = \begin{pmatrix} h_{10} \\ h_{20} \\ \vdots \\ h_{K_{PA}0} \\ h_{11} \\ \vdots \\ h_{K_{PA}1} \\ h_{12} \\ \vdots \\ h_{K_{PA}M_{PA}} \end{pmatrix} \tag{I.32}$$

Using the same structures for $\mathbf{E}^{\widetilde{\mathbf{a}_\varepsilon}}[n]$ and $\vec{w}$, we can model the entire system with the following matrix equations:

$$\vec{a_\mathcal{E}}[n] = G \cdot \mathbf{E}^{\mathcal{E}}[n] \times \vec{h} \tag{I.33}$$

$$\vec{\widetilde{a_\mathcal{E}}}[n] = \frac{1}{G}\, \vec{a_\mathcal{E}}[n] \tag{I.34}$$

$$\vec{\hat{\mathcal{E}}}[n] = \mathbf{E}^{\widetilde{\mathbf{a}_\varepsilon}}[n] \times \vec{w} \tag{I.35}$$

The vector error of N samples is:

$$\vec{\delta}[n] = \vec{\mathcal{E}}[n] - \vec{\hat{\mathcal{E}}}[n] \tag{I.36}$$

And the minimum square error solution is:

$$\vec{w} = \underbrace{\left(\mathbf{E}^{\widetilde{\mathbf{a}_\varepsilon}H}\mathbf{E}^{\widetilde{\mathbf{a}_\varepsilon}}\right)^{-1}\mathbf{E}^{\widetilde{\mathbf{a}_\varepsilon}H}}_{\text{pseudo inverse matrix of } \mathbf{E}^{\widetilde{\mathbf{a}_\varepsilon}}}\ \vec{\mathcal{E}}[n] \tag{I.37}$$

where $\mathbf{M}^H$ is the transposed conjugate of matrix $\mathbf{M}$. This calculus is efficiently implemented on MATLAB using the \ operator.

This formulation by matrix inversion gives some information about the algorithmic complexity to solve this problem which is $O\left((K_{PD}\, M_{PD})^3\right)$. It shows that the digital predistortion requires relatively large computational resources making its implementation difficult in an embedded system, which is not the case for BTSs. Some formulation reduce the size problem by only keeping the odd order nonlinear components. In addition, this formulation clearly shows the direct relationship between the computed $\vec{w}$ and the samples of signal $\widetilde{a_\mathcal{E}}$.

I.3 A/D conversion for linearization of power amplifiers

I.3.1 Acquisition requirements

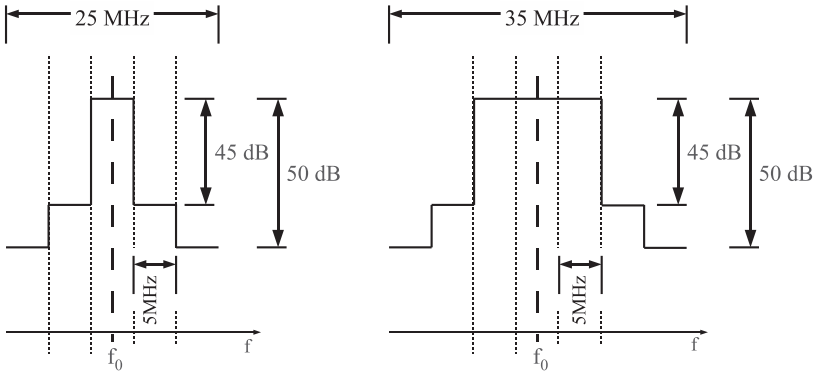
In order to accurately characterize the behaviour of the PA, the measurement path has to meet several requirements. More precisely, the dynamic range and linearity feedback measurement path should exceed the targeted linearity performance. Moreover due to the spectral regrowth generated by the 3rd, 5th, and higher-order intermodulation (IM) products, the distorted signal spans over at least three times the initial bandwidth. Currently, the considered bandwidth is usually at least five times the initial one so that 5th order nonlinear components can be corrected. Recalling the Figure I.12 we identify the ADC as the critical device of the feedback path. It is straightforward that the predistortion accuracy will depend on the accuracy of the ADC. High dynamic range and linearity is equivalent to high resolution for the ADC and the spectral regrowth implies dealing with wideband signals.

However, as in all communication systems, the ADC resolution is subject to the trade-off accuracy-speed–consumption and therefore we also want that consumption to be as minimum as possible.

I.3.2 Specification of the transmission scenario

The first step in designing an ADC is to specify the optimal resolution i.e. the one that fulfills the dynamic constraints but using the minimum one such that hardware complexity

is the lowest. However, in [37, 38] we notice the need for performing full system simulations, that include a DPD algorithm, an adaptation module, a predistorter module, a PA model, a DAC and an ADC, to determine the best estimate of the resolution. At the time of definition of specification, none of the DPD parameters were defined, so we used another approach to derive the target performances of the ADC.
The proposed method consists in analyzing the spectral composition of the distorted signal in the UMTS standard to extract the minimum performances of the feedback path ADC. Document [12] provides the spectral constraints that must be satisfied by the PA output signal. The constraints are given in term of spectral emission mask and minimum ACLRs. We retained the ACLR constraints and the diagrams in Figure I.17 illustrate the limit spectral composition of the distorted signal in two cases: single and multi-carrier.



(a) Mono-carrier signal (b) Multi-carrier signal

Figure I.17: Minimum ACLR Spectrum diagram for 3GPP WCDMA signals

These ACLR constraints can be used to construct a spectral profile of the worst linearization case. However, from the ADC point of view, this case will be the best case since the difference between the power of the useful band and the distortions is smaller.

Ideally, the predistortion technique should produce infinite ACLRs. In practice, they are limited by the initial signal synthesis and the model accuracy. Then, the predistortion should maximize them so that standard constraints are satisfied.
We have chosen, as the best case linearization correction, an ACLR of 60dB for the first adjacent band. In terms of data conversion, this signal is difficult to process. Indeed distortions powers are very small compared to the fundamental band.

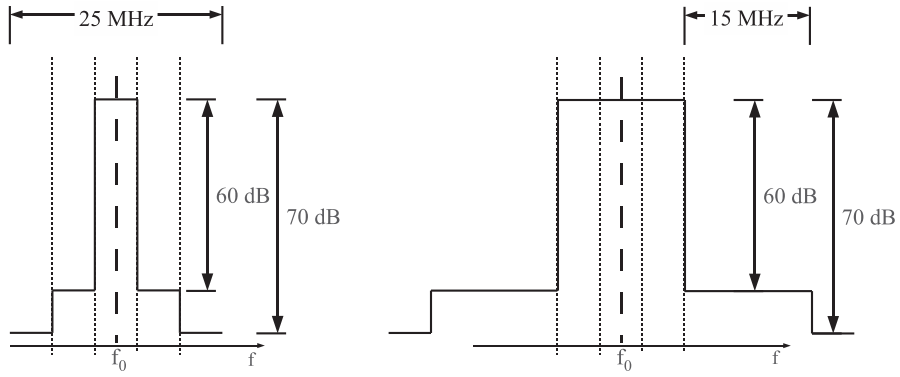
The diagrams in Figure I.18 show the assumed spectral composition of the signal to digitize at the output of the linearized amplifier.

In summary, the ADC must have a dynamic conversion of at least 70 dB and a bandwidth of 75MHz if we want the main band and its adjacent bands (related to IM5) to be digitized.
Given the expected signal characteristic and the rough target performance of the application, we propose to review the published ADC circuits providing the first orientations toward the most adapted ADC architectures.

I.3.3 High performance A/D converters

I.3.3.1 Performance metrics

Reviewing the ADC circuits requires to introduce the performance metrics in order to compare the architectures. There are numerous parameters to characterize ADCs, however,



(a) Mono-carrier signal (b) Multi-carrier signal

Figure I.18: Expected ACLR Spectrum diagram for the ADC specifications

three of them are sufficiently to distinguish their main characteristics.
The first one is the resolution, expressed as Signal to Noise Ratios (SNR) [1] or Effective Number Of Bits (ENOB). It represents the actual accuracy of the converter that is usually lower than the stated resolution because of non-idealities. This quantity will be further discussed in Section II.1.1. Of course, the higher the SNR, the more accurate the ADC.
The second performance parameter is the conversion bandwidth or the Digital Output Rate (DOR). For *Nyquist* converter, i.e. flash, pipelined and Successive-Approximation-Registers (SAR) ADCs, the classical bandwidth is equal to the half of the sampling frequency and the DOR is equal to the sampling frequency. For oversampled converters, not to say $\Sigma\Delta$ converters, the conversion bandwidth is a small fraction of the sampling frequency. Then, the conversion bandwidth is linked to the sampling frequency by the Oversampling Ratio (OSR) that we will define in Section II.1.1. In this case, the DOR is twice the bandwidth. The wider the bandwidth, the higher the data rates.
The power consumption is the last fundamental performance parameter. The less the power consumption, the longer the battery life or the lower the operating expense for grid connected equipments.
In this section we focus on the SNR and DOR parameters.

I.3.3.2 Classical architectures

Figure I.19 shows the distribution of ADCs according to their DOR and their SNR. Each ADC type is distinguished by a specific marker shape and color. The data in this figure were collected from Murmann's ADC survey [25].

Flash converter

The flash converter is the basic data converter architecture. As it is expressed by its name, it is the fastest data converter and consequently, it is used for applications requiring very large bandwidth. However, it can be used only for limited resolution converters because of the number of required comparators and resistors which increases exponentially with the resolution, resulting in prohibitive increased energy consumption. Indeed, an n-bit data converter requires $2^n - 1$ comparators connected to reference voltages generated with a 2^n resistor string.

[1] or Signal to Noise and Distortion Ratios (SNDR)

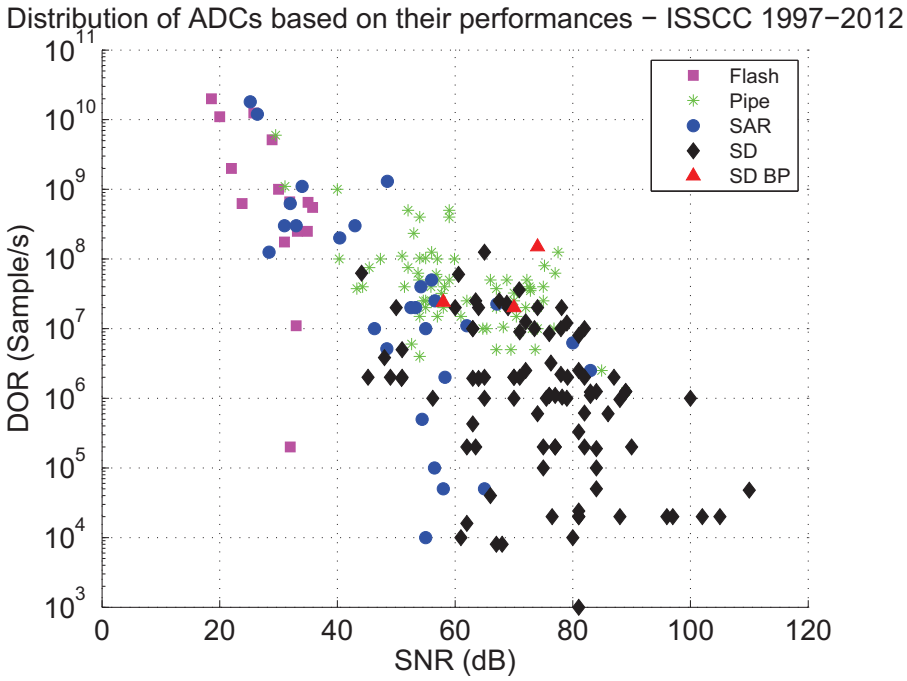


Figure I.19: ADC Overview - Distribution of published ADC according to their performances

This explains the distribution of the points in Figure I.19. Indeed, we can see that Flash converters address very wide bandwidths up to tens of GHz but with resolution limited to 6 bits. As a matter of fact, they are usually used in the other architectures as the quantizer block.

Pipelined converters

Pipelined architecture is a multi-stage converter in which several similar low resolution stages are cascaded to process the analogue input value and provide the digital one. One stage consists of a sampling circuit — Sample and Hold (S/H), an m-bit sub-ADC (flash ADC), and an m-bit D/A converter that converts the digital result into an analog voltage subtracted from the input signal. Thanks to the (S/H) circuit of each stage, they all work simultaneously. Thus, the throughput rate of this type of converter is independent of the number of used stages . However, because of its structure, the ADC produces a certain constant latency.

One of the first issues to deal with in order to obtain accurate converters is the mismatch between each stage. These non-idealities generate distortions that can be mitigated by adding redundant bits in each stage.

We can see in Figure I.19 that this type of converter is distributed over a large interval of bandwidth and resolution. We can divide two parts showing that this architecture can be used to convert very wide bandwidths (DOR $\approx$ 100MHz) with moderate resolution ($\leq$ 10 bits) or wide bandwidths (DOR $\leq$ 25MHz) with high resolutions capable of almost 14 bits.

Successive approximation ADCs

Successive-Approximation-Register (SAR) ADCs are multi-step converters using only one stage to process successive approximations of the signal. A SAR converter uses a register to provide a binary code to the DAC while a comparator successively evaluates if the es-

timated quantized registered value is greater than the input analog signal. Consequently, an n-bit SAR converter needs n steps to quantize the sampled analog input.
First limitations arise from the fact that n approximations and comparisons must be performed in each sampling period (compared to one single cycle for flash converter). Since each approximation step requires a certain amount of time, the conversion speed is directly affected by the number of bits of the converter. Other limitations result from the non-idealities of the DAC which mainly determine the accuracy of the converter.
On the Figure I.19, we summarize their distribution to a fictitious line starting in high DORs ($\approx$ 10GHz) and low resolution ($\approx$ 25dB) and ending in the low DORs ($\approx$ 100kHz) and moderate resolution ($\approx$ 60dB). This characteristic illustrates the fundamental limitation of SAR ADCs and the balance between resolution and speed.

$\Sigma\Delta$ converters
Oversampling allows to improve converters resolution. $\Sigma\Delta$ converters rely on the combination of this technique and quantization error shaping technique enabling very high resolution converter. The $\Sigma\Delta$ converter consists of a $\Sigma\Delta$ modulator followed by a digital decimation filter. The modulator samples the input analogue signal at a rate F_s which is much higher than the signal Nyquist frequency $2BW$.
The oversampling ratio (OSR) defined previously quantifies the degree of oversampling. The digital output is fed back through a digital to analog converter and subtracted from the input signal. The result of the subtraction is passed through a loop filter to finally be quantized by a coarse ADC. The loop filter determines the noise shaping which can be high-pass type or band-stop type, where, the noise is respectively filtered around either DC or at a given frequency. This shaping process is modeled by the noise transfer function (NTF). Very simple $\Sigma\Delta$ converters including a comparator as a quantizer can provide very high SNR for high OSR meaning that the bandwidth of these ADCs is limited by the fact that the clock frequency needs to be relatively high. Moreover, increasing the noise filtering order allows to increase the SNR but the resulting modulator faces stability issues even for ideal components. Finally, the resolution of the modulator can also be improved by increasing the resolution of the quantizer. We detail the composition and operation of this type of converter in Chapter II
Here also, nonlinearity errors in the DAC will limit the performance.
$\Sigma\Delta$ modulators are positioned as converters achieving very high resolutions up to nearly 16 bits but with limited bandwidths , most of them converting with DOR $\leq$ 40MHz. However, we can see that with the pipeline architecture, they mostly occupy the upper right area of the plot that is the highest performances area.

This ADC review shows that the fastest and most accurate ADCs are done using pipelined architectures and $\Sigma\Delta$ modulators. The $\Sigma\Delta$ overview [40] also reports modulators that can achieve performances in the same range as discussed in § I.3.2

I.3.3.3 Parallel architectures

Parallelism is a solution to overcome speed limitations.

Time interleaving is a technique that increases the bandwidth of data converters. It is based on the fact that sampling with R channels is equivalent to sampling with a single ADC with an R times higher sampling rate. The speed requirement of each channel is then relaxed by the factor of R at the expense of using multiple ADCs. However, at high speeds, mismatches between channels, due to process variation, are a critical issue: gain, offset and input bandwidth mismatches are parameters that reduce the achievable dynamic

range and linearity.
The channel ADCs are usually implemented as Pipelined [66, 30, 33, 56], SAR [42, 16] or discrete-time ΣΔ [52, 28] ADCs.

Another parallel structure uses frequency multiplexing. Indeed, for example band-pass (BP) ΣΔ modulators can process specific frequency bands. So, one can find a combination so that each band-pass modulator process one frequency band with narrow bandwidth independently from each other and reconstruct the signal so that the whole final bandwidth is covered. This concept is discussed in [22] and a thorough study is provided in [19].

In this section we have reviewed the main types of converters. We have seen through their distribution according to their performances that pipeline and ΣΔ converters are suitable for our application in the sense that these converters can achieve similar performance to our need in dynamic range (70dB<) and bandwidth (45 to 75 MHz). Given the capacity of BP ΣΔ modulators for digitizing a particular signal band and given the particular structure of the signal to be digitized we will focus on an implementation based on parallel BP ΣΔ modulator.

However, these needs have been estimated on the basis of an extremely effective correction of the nonlinearity. To estimate more precisely the needs of the ADC, we studied, by simulation of a particular case, the effect of the feedback data quantization on the performance of the correction. In the next section we discuss these simulations.

I.3.4 Data conversion quantization simulations in DPD

We want to study by simulation the effect of the quantification of measurement data. However, before, we emphasize that as any digital system the process of DPD is entirely quantized. And the ADC is not the only source of quantization error of the complete system. In the most general case the quantization errors appear in all digital processing blocks (see Figure I.12, page 59: in the source symbol generator, in the digital pulse shaping filter, in the computation blocks applying and identifying the model, in the DAC and in the ADC.

One of the most frequently studied quantization error is the quantization of the LUT when the DPD is implemented by this mean [75, 53].
However, the measurement signal itself must also meet certain accuracy as shown with the following simulation results. These results were obtained during collaboration with Agilent as part of the PANAMA project, using the System Vue software.

Simulation results using System Vue

The System Vue Software has been useful to perform our initial simulations of DPD system with quantization. It provides a graphical programming tool (such as Simulink) and dedicated 3GPP simulation blocks. The built model divided the DPD process in four sequential steps:

1. the generation of a three-carrier WCDMA baseband signal
2. an acquisition phase of an amplified and distorted signal by a nonlinear power amplifier.
3. an identification block of the memory polynomial predistortion function
4. a correction phase for the DPD from which ACLRs are extracted

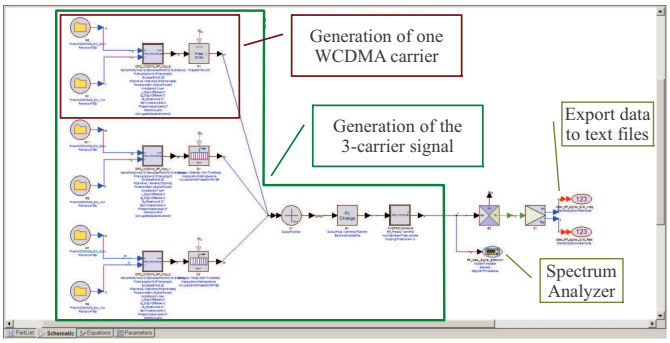


Figure I.20: Annotated picture of the schematic editor

Appendix B presents detailed diagrams of each part of the model.
Figure I.20 shows the System Vue schematic editor.
This schematic is the one used to generate the signal to be amplified and we have highlighted some elements to explain the basic structure of this schematic. The red rectangle shows the main blocks to generate one WCDMA carrier. The green one shows the complete structure to generate the three adjacent carriers. Then the spectrum of this signal can be displayed with the spectrum analyzer block and the data are saved as ASCII data to text files for the following simulation steps.

In order to study the quantization effect on the DPD performances, the simulated acquisition phase was achieved in three cases:

- in the ideal case: measurement samples were not quantized;
- data were quantized by an ideal Flash;
- data were quantized by an ideal $\Sigma\Delta$ modulator.

The first case was used as the basis to the construction of the second and third case.

For the quantized data, we first studied the influence of the resolution in the case of the Flash quantizer. The Figure I.21 presents the simulation results of DPD when measurements are quantized by the Flash ADC for different values of resolution.
The curve denoted ACLR5 represents the ratio of power in the band of 5 MHz centered around the highest frequency carrier and its adjacent band centered at +5MHz.
The curve denoted ACLR10 is calculated using the power of the band at +10MHz from the carrier.
As expected, for low resolution measurement the performances of the DPD are low. The ACLRs increase with resolution and reach a threshold at 10-bit after which the resolution has no effect.
We can further note that in this particular case of DPD, the number of bits required to meet the standard's requirements is 5 bits. This value seems quite low but we think that the effect of quantization is strongly attenuated by the identification process of the model that relies on minimizing the squared error (as shown Part I.2.3.3). However we do not have the exact implementation details of the adaptation block.

The second step of this simulation work was to check the proper operation of the DPD using an ideal $\Sigma\Delta$ modulator achieving 5 bits of resolution in a band conversion of 3×15=45MHz (correction of the bands associated with the IM3 products). The spectra of Figure I.22 show the results of the different processing. The plot 1 is the distorted output of the PA. We can see the spectral regrowth over the adjacent bands. Here, we can note

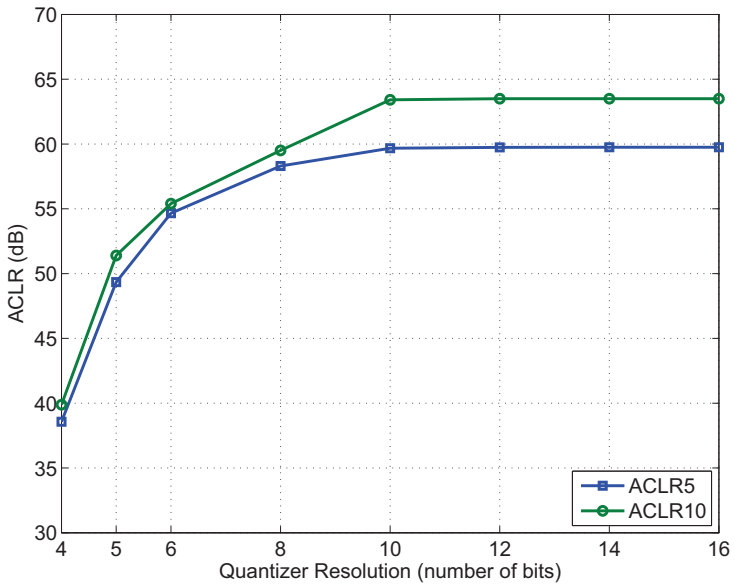


Figure I.21: ACLR as a function of the resolution of fed back data

that the spectral regrowth is limited to less than the adjacent 15MHz.
The plot 2 is the ideally predistorted signal. In this case, the model has been calculated from samples that are not quantized. We can note the very good correction as the power levels of adjacent bands are very low.
The plot 3 shows the spectrum of the linearized signal with a model calculated from quantized data with an ideal Flash converter. We can see that the distortion power levels have been reduced in the adjacent bands to some extent. However, for the farthest bands, the distortion level has been increased. We can also note the asymmetric correction that results from the noised estimated model.
The plot 4 shows the spectrum in the last case, where the model is calculated from quantized data sampled by a $\Sigma\Delta$ modulator designed to be equivalent to the Flash ADC. We can note similar spectrum characteristics to the previous case.

The Table I.2 gives the resulting ACLR5 and ACLR10 in each DPD case. In the ideal case, we can see the ACLRs are approximately 60dB. These ACLRs correspond approximately to our expected signal for the DPD feedback ADC.
Secondly, the ACLRs in the case of quantized data by a flash, are around 50dB. These ACLRs meet the standard requirements that states at least 45dB ACLR for the ACLR5 and 50dB for the ACLR10.
Finally, ACLR performances in the case of the $\Sigma\Delta$ modulator are slightly greater than in the flash quantizer although the $\Sigma\Delta$ converter has been designed to achieve the same performances of the Flash converter.

	ACLR5	ACLR10
Ideal – No Quant.	59.4 dB	63.5 dB
Flash Quantizer	49,3 dB	51,4 dB
$\Sigma\Delta$	51,4 dB	55,6 dB

Table I.2: Simulated ACLR performances

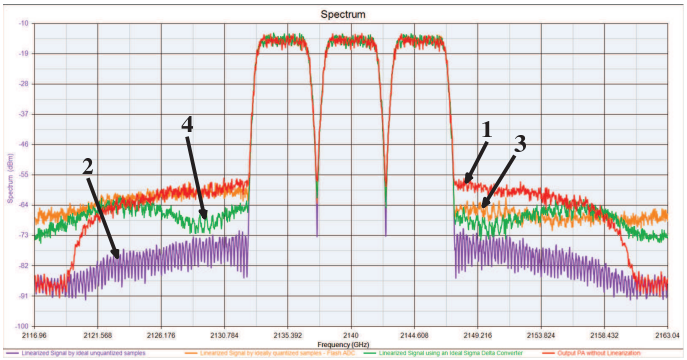


Figure I.22: Simulated output spectra for systems without DPD and with ideal and quantized data DPD: 1- Distorted Output PA ; 2- Linearized Signal by ideal unquantized samples ; 3- Linearized Signal using flash ADC ; 4- Linearized Signal using $\Sigma\Delta$ converter

These simulations showed the effect of the ADC quantization on the correction performance. For low ADC resolution values the DPD achieves reduced performances. We have seen that beyond 10-bit quantization, the ADC has no effect on the correction since the ACLRs remain at the same values. And, in this case, a 5-bit ADC is required to meet the 3GPP requirement on ACLRs. Finally we validated $\Sigma\Delta$ approach that yield similar results to the plain ideal flash quantizer.

I.4 Conclusion

In this chapter, we introduce the context of the work in this thesis that is the linearization of the PAs. We have seen that the current modulations are characterized by non-constant envelope signals. This is particularly the case in the base stations emitting several carriers simultaneously. However, these signals will be affected by nonlinearity from the PA, which has a saturation effect for the high power level. This will degrade the signal quality, degradation that can also be observed in the frequency domain in the form of spectrum regrowth. To analyze this phenomenon, mathematical models of varying complexity have been developed to simulate various distortions generated by the PA: modulation amplitude, phase and memory effect. In addition, a multitude of technique has been and is currently developed to correct these distortions. And we chose the DPD as part of study for this thesis. We have introduced the requirements of this technique in terms of A/D converter and we have defined a transmission scenario providing the approximate expected performance of the ADC. Reviewing the main ADC architectures we have seen that the pipeline and $\Sigma\Delta$ converters were the architectures to providing the widest bandwidths with the highest resolutions. Finally, to refine the discussion, we have shown by simulations the quantization effect the ADC. In this particular case of simulation, a 5 bit quantization meets the requirements of the standard.

Chapter II

System-level design and simulation of ΣΔ converters

Progress in digital electronics pushes to reduce the number of processing performed in the analog part. Indeed, digital processes are becoming more and more efficient as VLSI technology (Very Large Scale Integration) allows their implementation with very high densities (thus reducing the surface) with a low cost and these circuits consume less and less energy. However, in some areas, such as telecommunications, every system must use at some point, a transmission media of analog nature. It must therefore have an interface linking the analog world and digital world. Development in these areas is driven by needs for efficient analog-to-digital conversion. In addition, this function must provide information as accurate and fast as possible to digital processing stages with low energy consumption.

These general constraints are also true for ADC for digital predistortion systems particularly the accuracy and speed. As described in Chapter I, there is a wide variety of ADC [25, 40] and the technique based on ΣΔ modulation has appropriate characteristics for telecommunications and DPD requirements. Indeed, these converters can achieve very high resolutions for narrowband signals and, advances in design enable their use for wideband applications. In addition, this component reduces the consumption of the system since its composition is relatively simple and its principle of operation (the oversampling) reduces the constraints of the anti-aliasing filter (in some cases this filter will even be useless).

This Chapter presents the high-level design and simulation methodology for Discrete-Time (DT) and Continuous-Time (CT) ΣΔ converters and is organized as follows. In Section II.1, with a short recall on the bases of analog-to-digital conversion, we present the fundamental concepts for ΣΔ conversion. Then we review the high-level design choices to implement these converters and a state of the art of ΣΔ modulators is provided to extract some characteristics of each type of implementation. In Section II.2, we detail the design methodology to achieve a given noise transfer function using particular architectures for both discrete-time and continuous-time systems. Then, we discuss the simulation issue and provide a solution to the simulation of continuous-time systems.

II.1 ΣΔ Modulators fundamentals

The general architecture of a ΣΔ converter is shown in Figure II.1. This type of ADC is composed of two main modules: a ΣΔ modulator and a digital decimation filter. The modulator is a mixed-signal element that consists in a loop composed of an analogue filter (integrators and/or resonators), an ADC (that digitizes the signal) and a D/A converter

(DAC), which feeds back the analogue estimate of the ADC. Although ΣΔ modulators use low resolution ADCs, they have the ability to provide high resolution signals. This is possible because their operation is based on three techniques: *oversampling*, *quantization noise shaping* and *decimating filtering*. The process of filtering and decimating eliminates a part of the quantization noise by means of low pass filtering and therefore, increases the resolution of the signal while reducing the sampling rate to the Nyquist rate. Strictly speaking this operation combines the two processes at the same time and is usually implemented in multiple stages, but to make it simple, the whole processing block will be referred to as decimation filter throughout this thesis.

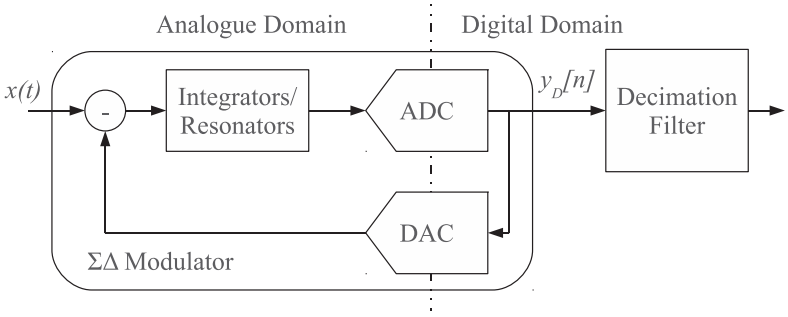


Figure II.1: Diagram of the general structure of ΣΔ converter

II.1.1 The fundamental parameters

II.1.1.1 Ideal analog-to-digital conversion

Sampling effect

The sampling process converts the continuous-time signal in a discrete-time signal. We can show through distribution theory that, in the frequency domain, this process generates duplicates of the input signal spectrum at each multiple of the frequency sampling. Therefore, given an input signal whose bandwidth is B, there is a minimum sampling frequency in order to preserve the entirety of the input signal. This is stated by the Nyquist theorem [1] which sets this minimum sampling frequency to $2B$, twice the input signal bandwidth. This frequency is referred to as *Nyquist frequency*. Then *oversampling* is sampling at a higher rate than the Nyquist frequency and we define the oversampling ratio (OSR) as:

$$OSR = \frac{F_s}{2B} \tag{II.1}$$

The oversampling technique allows to relax the constraints on the anti-aliasing filter that ensures the bandwidth limitation of the input signal to avoid distortions since duplicates are separated by a wider range of frequency.

Quantization effect

Quantization is the process during which an analogue signal is associated with a discrete level equivalent and to a finite number of bits. Figure II.2 shows the relationship between the output of an ideal quantizer and its input. We assume, without loss of generality that the output quantized values are between $-x_{max}$ and x_{max}. q is referred to as quantization step or quantum and here, is equal to:

$$q = \frac{2x_{max}}{2^n} \tag{II.2}$$

[1] also known as Shannon theorem or sampling theorem

where n is the number of bits used to code the discrete levels.

The quantization introduces an error e which is the difference between the actual value x and the discrete level that has been associated $\mathcal{A}(y_D)$:

$$e(x) = x - \mathcal{A}(y_D) \tag{II.3}$$

This error is represented as a function of the input in Figure II.3.

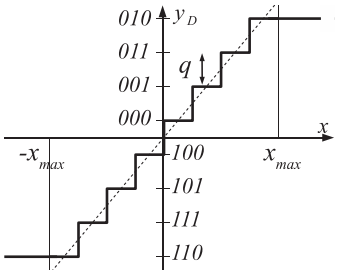


Figure II.2: Input/Output characteristic of a 3-bit quantizer

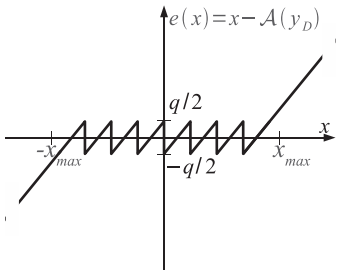


Figure II.3: Quantization error of a 3-bit quantizer

We can note that the quantization error is bounded by $-\frac{q}{2}$ to $\frac{q}{2}$ as long as the input remains in the non-overloading interval $[-x_{max}; x_{max}]$.

Assuming the latter and that the quantization error is uncorrelated from sample to sample, the quantization error can be modeled as a random process with a uniform distribution of support $\left[-\frac{q}{2}; \frac{q}{2}\right]$. Its variance gives the quantization noise power:

$$\sigma_e^2 = \int_{-\frac{q}{2}}^{\frac{q}{2}} \frac{1}{q} e^2 \, \mathrm{d}e = \frac{q^2}{12} \tag{II.4}$$

Despite these assumptions are not always true, particularly for low resolutions, this model gives good results for resolutions higher than 8 bits.

When the signal is sampled at the sampling frequency F_s, the power spectral density of the error is defined on the interval $\left[-\frac{F_s}{2}; \frac{F_s}{2}\right]$. Finally, we can assume that the quantization error signal has a flat power spectral density — a.k.a. white noise signal. Then its power spectral density is given by:

$$PSD_e(f) = G_e = \frac{q^2}{12\, F_s} \tag{II.5}$$

II.1.1.2 The oversampling

Since the total quantization noise power depends only on the resolution of the quantizer, we can note that, for a fixed resolution of the quantizer, the power spectral density level decreases as the frequency sampling F_s increases. This effect is illustrated in Figure II.4 that shows the spectrum of a digitized signal for different sampling frequencies with the same quantizer step.

Therefore, in the presence of oversampling, the power of the quantization noise in the frequency interval $[-B; B]$, referred to as in-band noise power, can be expressed as:

$$\sigma_{e_{inband}}^2 = G_e \times 2B = \frac{q^2}{12\, OSR} \tag{II.6}$$

where OSR is the oversampling ratio. As $OSR > 1$ we have $\sigma_{e_{inband}}^2 < \sigma_e^2$ meaning that oversampling reduces the (quantization) noise in the useful bandwidth.

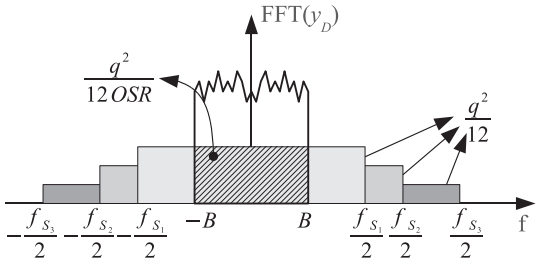


Figure II.4: Diagram of the spectrum of a digitized signal: effect of oversampling on the in-band noise power

As introduced in Section I.3.3.1, one of the fundamental metric used to evaluate the performance of a quantizer is its signal-to-noise power ratio (SNR) and we can calculate the theoretical maximum value. To estimate the signal power, the common assumption is to use a sinusoidal input whose amplitude is set to the theoretical maximum of the non-overloading interval x_{max}. Therefore, the maximum SNR can be expressed as:

$$SNR = \frac{\sigma^2_{sig}}{\sigma^2_{e_{inband}}} = \frac{\frac{x^2_{max}}{2}}{\frac{q^2}{12\,OSR}} = \frac{3}{2}\,OSR\,2^{2n} \tag{II.7}$$

SNR are always calculated in decibel:

$$SNR_{dB} = 10\log_{10}(OSR) + 6.02n + 1.76 \text{ dB} \tag{II.8}$$

II.1.1.3 The noise shaping

In addition to oversampling, noise shaping allows to further increase the accuracy of the digitized signal. Thanks to a kind of filtering, we can spectrally shape the quantization noise so that its power spectral density is low in the signal band. This is the second fundamental technique is used in ΣΔ modulators.

Consider the fundamental structure of ΣΔ modulators shown in Figure II.1. Assuming that the ADC can be modeled as an additive white noise and an ideal DAC, the structure can me modeled as a two input linear system as shown in Figure II.5. The ideal DAC assumption allows us, here and in the rest of the manuscript, to consider the digital output value as its analog value in the case of discrete-time modulators.

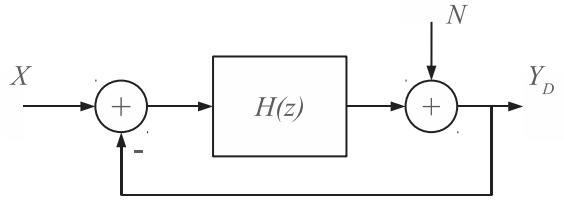


Figure II.5: Fundamental block diagram model of a ΣΔ modulator

This system can be represented by transfer functions applied to both the input signal and the quantization noise:

$$Y_D(z) = STF(z)\,X(z) + NTF(z)\,N(z) \tag{II.9}$$

where

$$STF(z) = \frac{H(z)}{1 + H(z)} \tag{II.10}$$

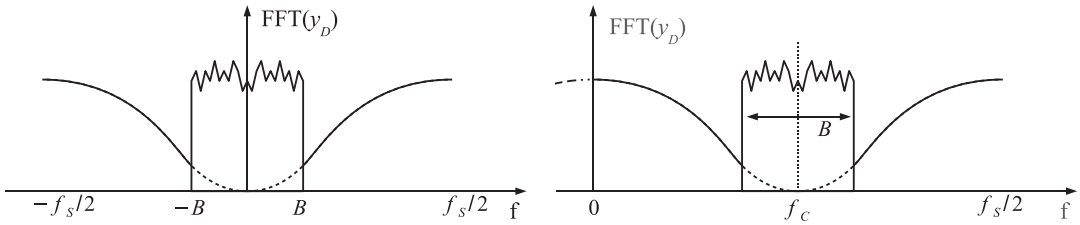
$$NTF(z) = \frac{1}{1 + H(z)} \tag{II.11}$$

STF and NTF respectively stand for signal transfer function and noise transfer function.

The first step to design ΣΔ modulators is to choose a loop filter H such that its gain is high in the signal band and low outside. Consequently, *in the signal band*:

$$\begin{cases} |STF(f)|^2 & \approx 1 \\ |NTF(f)|^2 & \approx 0 \end{cases} \tag{II.12}$$

Then we can build the noise transfer function so that it performs the desired noise shaping depending on the input signal. Indeed, if the signal is centered around a frequency (different from 0) we can use a band-stop NTF filter to shape the quantization noise out of the signal band. Figure II.6 shows the shaping of the quantization noise in a low-pass case (the signal is centered around DC) and in a band-pass case (the signal is centered around a frequency different from 0).



(a) Low-pass case (b) Band-pass case

Figure II.6: Different types of quantization noise shaping

To derive the theoretical SNR of this type of converter, we assume that the signal is in low frequency. Then the modulator to be used is a low-pass modulator. For a simple modulator, we can model the NTF by:

$$NTF(z) = \left(1 - z^{-1}\right)^L \tag{II.13}$$

where L is the filtering order. Thus, the magnitude of the NTF in the normalized frequency domain ($\nu = f/F_s$) is given by:

$$|NTF(\nu)|^2 = \left|1 - \mathrm{e}^{-j2\pi\nu}\right|^{2L} = 4^L \sin^{2L}(\pi\nu) \tag{II.14}$$

Assuming a high OSR, i.e. $F_s \gg B$, we can approximate the sin function to its first order Taylor expansion to calculate the in-band noise power:

$$\sigma^2_{e_{inband}} = \int_{-B}^{B} G_e \, |NTF(f)|^2 \, \mathrm{d}f = \int_{-B}^{B} \frac{q^2}{12\,F_s} \, |NTF(f)|^2 \, \mathrm{d}f \tag{II.15}$$

$$\sigma^2_{e_{inband}} \approx \frac{q^2}{12} \frac{\pi^{2L}}{(2L+1)\,OSR^{2L+1}} \tag{II.16}$$

Compared with simple oversampling ADC, this technique provides more quantization noise suppression in the band of interest. The SNR is then given by:

$$SNR = \frac{3}{2} 2^{2n} OSR^{2L+1} \frac{2L+1}{\pi^{2L}} \tag{II.17}$$

And it can be approximated by:

$$SNR_{dB} \approx 10 \log_{10} \left(\frac{2L+1}{\pi^{2L}} \right) + (2L+1) 10 \log_{10}(OSR) + 6.02n + 1.76 \tag{II.18}$$

We can note a large improvement of the SNR for a given loop filter order L: it is increased by $3(2L+1)$dB for every doubling of sampling rate meaning that the equivalent resolution converted in bits is increased by $L + \frac{1}{2}$ bits. Although this equation is obtained from ideal behavior considerations and approximations, it is the starting point of the design of ΣΔ modulators to evaluate and choose the right combination of values to obtain a target resolution.

II.1.1.4 Stability

Despite the seeming simplicity of ΣΔ modulators with respect to their performances, this type of component may suffer from problems that can be observed even in simulations where the building blocks are ideal. Indeed, high order ΣΔ modulators may suffer from stability issues resulting in signals values growing indefinitely or to saturation in real systems.
Besides, the presence of a strong nonlinearity in the loop (the quantizer) causes the stability analysis to be more complex. Several methods can be used to analyze the stability such as parametric root-loci studies [73, 82, 74], Quasi-Linear-Stability Analysis [70], Describing Functions [21, 55, 46], State-space Models [71, 29, 50]. However one of the simplest techniques is to perform extensive simulations to estimate accurately the actual performances of the modulator in terms of peak SNR and maximum stable input amplitude.
In the latter case, a simple sweep of the input sinusoid amplitude allows to extract the SNR characteristic of the modulator. A typical characteristic is shown in Figure II.7 in which we can note the drop of the SNR when the input amplitude is exceeding a certain threshold.

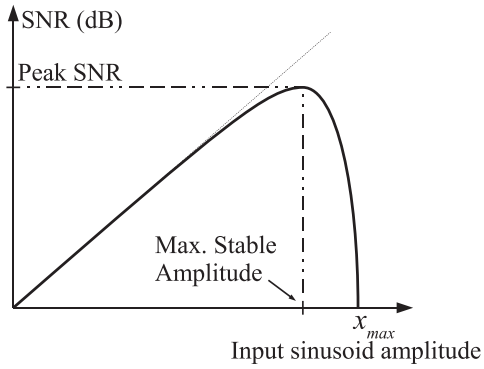


Figure II.7: Typical SNR relation with the signal input amplitude

This stability issue will be addressed in Section III.3.2 where an optimization method is proposed to ensure stability up to a given input amplitude while maximizing the SNR.

II.1.1.5 Digital decimating filter

The last element of a ΣΔ converter is the decimation filter. This filter is a digital filter which prevents aliasing of the quantization noise in the signal band during the decimation process that reduces the over-sample frequency to the Nyquist frequency. For low-pass modulators, they are very efficiently implemented using Cascaded integrator-comb (CIC) filters and Nyquist filters (whose Half-band filters are a special case) [54, 11]. In addition, high decimating and filtering orders can also be efficiently implemented by choosing poly-phase implementations [1]. However in the case of band-pass modulators, the filter design requires either an adapted frequency planning or substantially more hardware resources (because word-length, coefficient filter resolution and/or filter orders need to be increased) to enable the frequency down-conversion and out-of-band noise filtering to maintain the SNR. The first case is achieved by selecting a center frequency at $F_s/4$ or $3F_s/4$, which allows to minimize the complexity of digital circuits as explained later.

II.1.2 Design choices

According to the nature of the loop filter, we can distinguish different types of ΣΔ modulators.

II.1.2.1 Low-pass and band-pass modulators

As briefly mentioned earlier, ΣΔ modulators can digitize baseband signals or band-pass signals. This can be done using an adapted noise transfer function that pushes the quantization noise outside the signal band. In the same way as low-pass modulators have low-pass type loop filters, band-pass modulators have band-pass loop filters. Usually, the design of band-pass (BP) modulators starts from an equivalent low-pass (LP) modulator since a simple transformation can be applied in the transfer function to obtain the desired noise shaping. Shifting the LP modulator to the desired center frequency can be done using the following transformation [62, 72]:

$$z^{-1} \leftrightarrow -z^{-1}\frac{z^{-1}-\frac{p}{2}}{1-\frac{p}{2}z^{-1}} \tag{II.19}$$

where p is the parameter that defines the new center frequency F_c and is equal to:

$$p = 2\cos\left(2\pi\frac{F_c}{F_s}\right) \tag{II.20}$$

This transformation keeps all the properties of the original LP modulator such as resolution and stability.
A common transformation is to place the center frequency at the quarter of the sampling frequency: $F_c = \frac{F_s}{4}$. The resulting transformation consists in replacing z^{-1} with $-z^{-2}$. This choice of F_c leads to very simple digital processing to move the signal from F_c to DC at the output of the modulator. Indeed, the frequency down-conversion is achieved by multiplying the output by the sampled sinusoids:

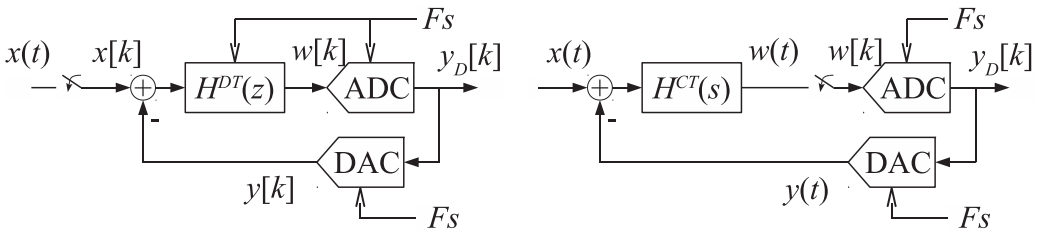
$$\cos\left(2\pi\frac{F_c}{F_s}n\right) = \{1, 0, -1, 0, \cdots\} \tag{II.21}$$

$$\sin\left(2\pi\frac{F_c}{F_s}n\right) = \{0, 1, 0, -1, \cdots\} \tag{II.22}$$

[1] A lot of academic materials can be found on the subject and [76] is a relevant one and [69] is an overview and tutorial on filter design with MATLAB that may help for simulations

II.1.2.2 Discrete-time and continuous-time modulators

In the literature, ΣΔ modulators are mainly implemented using either DT circuits such as switched capacitor circuits, either CT circuits such as GmC or OTA-RC circuits [40]. Figure II.8a and Figure II.8b show the conceptual differences between DT and CT modulators. In the DT case, the signal is sampled before reaching the first element of the



(a) Discrete-time modulator (b) Continuous-time modulator

Figure II.8: Block diagram of ΣΔ modulators implementations

modulator whereas in CT modulators, the signal is sampled at the input of the quantizer. This enables, in the CT case, to reduce even more the constraints on the anti-alias filter [58].

However the design of CT modulators is slightly more difficult as their analysis involves both discrete-time and continuous-time signals with their associated transforms: Z-transform for DT and Laplace transform for CT.

As in the previous case, the design of CT modulators usually starts from a DT expression of the desired NTF. The calculation of a CT modulator from a DT one is based on transformation from Z-domain to Laplace domain. However, an additional parameter has to be taken into account: the DAC waveform response. Indeed, according to this waveform, the continuous-time signal output from the loop filter $H(s)$ will be different [58].

Several methods exist to calculate the coefficients from a DT to a CT implementation such as the impulse-invariant transformation and the modified Z-Transform [58]. In this work, we used the impulse-invariant transformation in order to obtain the CT equivalent modulators and this transformation is detailed in the Section II.2.2.2.

II.1.2.3 Modulators architectures

There are different ways to implement in a circuit the previously obtained theoretical transfer function. Indeed, the elementary electronic circuits perform simple signal processing functions and when we can find an assembly of these elementary circuits producing the desired transfer function, there are sometimes other assemblies that do the same.
Thus, there are a number of basic architectures to achieve the loop filter transfer function [82, 61].

Single loop modulators

In this work, for simplicity and simulation purposes, we use general architectures that are able to implement any NTF.
For the DT case, we use the cascade-of-resonators feedback form (CRFB) that is discussed in [61, 73, 11]. Figure II.9 shows an example of this architecture.
For the CT case, integrators can not be delaying or non-delaying such as is the CRFB architecture. Therefore we use the CT cascade-of-integrators feedback form (CT-CIFB) shown in Figure II.10 These basic architectures are used to build modulators known as

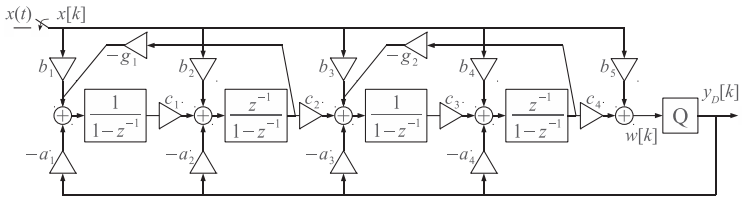


Figure II.9: A 4-th order CRFB modulator

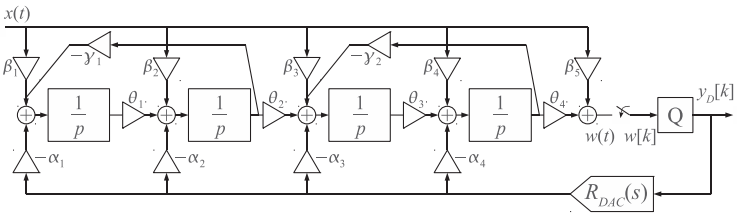


Figure II.10: A 4-th order CT-CIFB modulator

single loop as they use only one quantizer and one DAC.

As shown in the Equation (II.18), increasing the noise shaping order significantly improves the theoretical performances of the modulator. However, theoretical studies [82] have shown that the stability of modulators deteriorates when the order of the loop filter increases and the oversampling is low. Cascading several modulators solves the problem of increasing the filter order without degrading stability.

Cascaded modulators

Cascaded modulators are composed of several low order modulators — whose stability is guaranteed — that are cascaded to achieve higher order noise shaping. These modulators are characterized by the use of multiple quantizers and DACs and by the use of digital filters called *noise cancellation filters* (NCF) to achieve the right noise shaping. These NCFs are derived from the transfer functions achieved in each modulator.

As for single loop architectures, cascaded modulators can be implemented using either DT or CT circuitry. However, the design of the latter requires further developments as will be shown in the remaining of the section.

Classic cascade - MASH structure The Multi-stAge noise SHaping (MASH) structure is the simplest cascaded modulator structure [82]. Its block diagram is shown in Figure II.11 for the DT case: The principle of this architecture is to digitize the difference

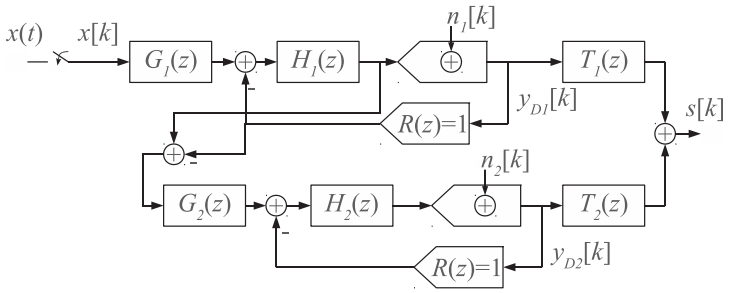


Figure II.11: DT MASH Architecture

between the input of the quantizer and the output of the DAC at each clock pulse. Thus each modulator processes the quantization error made by the previous stage.
For DT implementations, the required cancellation noise filters $T_1(z)$ and $T_2(z)$ are easily derived so that the noise contribution of each stage is null except for the last modulator of the chain:

$$S(z) = \frac{T_1(z)G_1(z)H_1(z)}{1+H_1(z)}X(z) + \left(\frac{T_1(z)}{1+H_1(z)} - \frac{T_2(z)G_2(z)H_2(z)}{1+H_2(z)}\right)N_1(z) + \frac{T_2(z)}{1+H_2(z)}N_2(z) \tag{II.23}$$

$$\frac{T_1(z)}{1+H_1(z)} - \frac{T_2(z)G_2(z)H_2(z)}{1+H_2(z)} = 0 \quad \Leftrightarrow \quad \frac{T_1(z)}{T_2(z)} = \frac{G_2(z)H_2(z)\left(1+H_1(z)\right)}{1+H_2(z)} \tag{II.24}$$

In the case of CT implementations, this filter identification requires taking into account additional information. In [63, 64, 10], a CT cascaded modulator is derived from a DT cascaded modulator so that noise cancellation filters are the same in both cases. It is shown that the CT modulator needs additional connections between every state variables and the input of later stages. Therefore the hardware complexity is increased and the circuit is more prone to mismatches. In [80, 79] a direct synthesis methodology is described to calculate the noise cancellation filters from any cascaded CT modulator, in particular, without adding connections. This methodology is summarized below as the technique has been useful to derive our own noise cancellation filters in the proposed new architecture.
The Figure II.12 shows the structure of a CT MASH modulator.

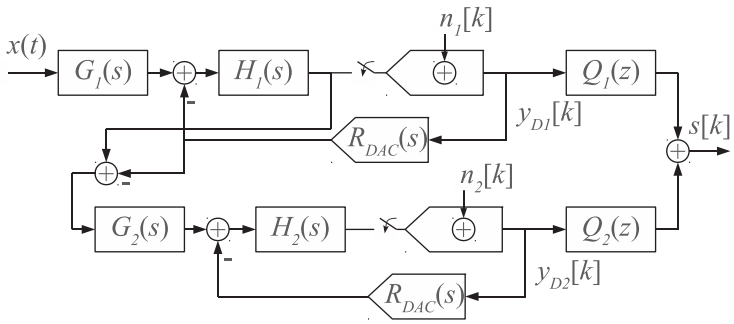


Figure II.12: CT MASH Architecture

The derivation of the noise cancellation filters consists in writing the exact transfer functions achieved all along the cascaded modulator. The required cancellation noise filters $Q_1(z)$ and $Q_2(z)$ should satisfy the following Equation (II.25) (details of the calculation are given in Appendix C).

$$\frac{Q_1(z)}{Q_2(z)} = \frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_s}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_s}\right]} \tag{II.25}$$

We can see that the relation between Q_1 and Q_2 is different from Equation (II.24). We note the dependence on the DAC response, both in the numerator and the denominator.

Advanced cascaded structures Classic MASH modulators exhibit some drawbacks such as a higher digital circuit complexity and a proneness to mismatches between analogue parameters and digital filters. Newer architectures based on cascading avoid these disadvantages by adding extra DACs, in place of digital filters, to feedback the signal to

the input of the cascaded modulator. The Multi-Stage Closed Loop (MSCL) architecture is the first structure of this type[27]. A variant of this architecture, called Sturdy MASH (SMASH) was published in 2006[57]. An example of this structure is shown in Figure II.13.

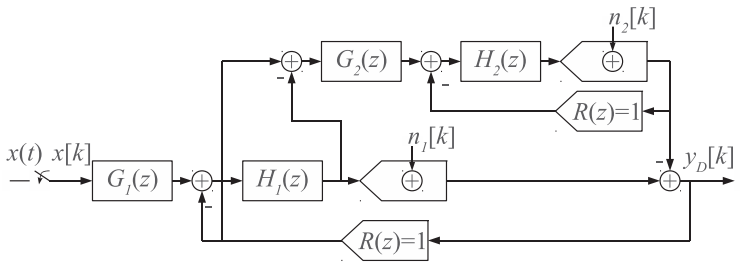


Figure II.13: A Sturdy MASH Modulator

The MSCL architecture was extended in 2011[81] introducing the Generalized MSCL (GMSCL) structure. An example of this structure is shown in Figure II.14.

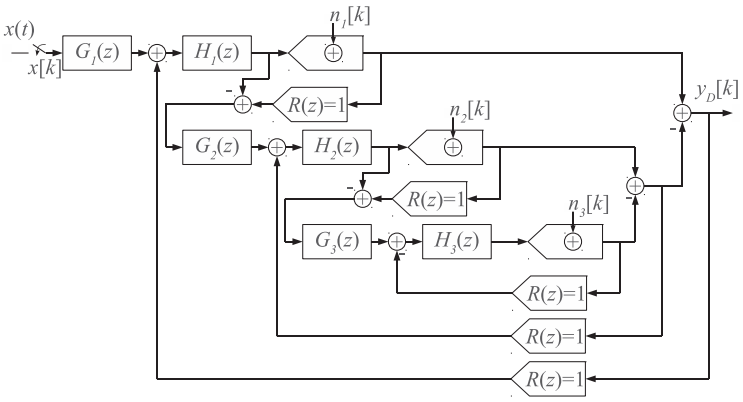


Figure II.14: A Generalized MSCL Modulator

These techniques improve the resolution for a given bandwidth and low resolution quantizers with a limited extra cost in terms of circuit.

Parallel architectures

Parallel architectures enable the digitization of wideband signals. Several architectures based on this technique have been proposed such as the time-interleaved ΣΔ (TIΣΔ) architecture and the frequency band decomposition (FBD).

Time-interleaved ΣΔ Time interleaving is a technique that increases the bandwidth of ADCs using M channels sampling the signal. The speed is then equivalent to the use of one single ADC M times faster. Figure II.15 shows the structure of the TIΣΔ architecture. The speed requirement of each channel is then relaxed by a coefficient M at the cost of using multiple ADCs and only channel sub-ADC has to be designed. However, this technique exhibits some drawbacks. The power consumption is straightforwardly higher; however [51] showed that the increase is linear compared to a single ADC providing the same bandwidth and resolution performances which presents an exponential growth. Moreover, mismatches between channels, due to process variations, are a very limiting issue: gain, offset and input bandwidth mismatches are non-idealities that reduce achievable performances since

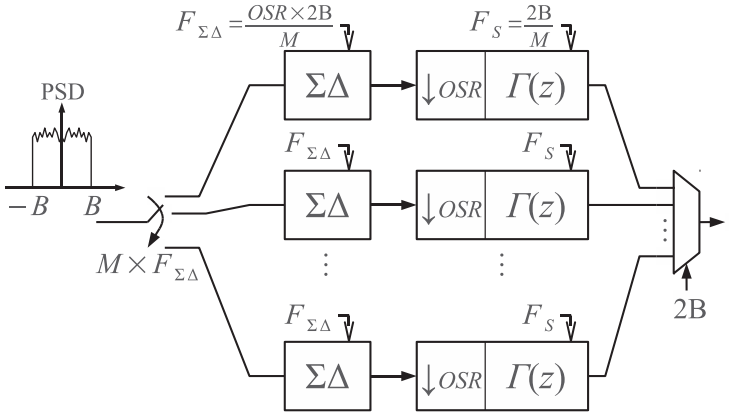


Figure II.15: The time-interleaved ΣΔ architecture

distortion spurs occur in the digitized signal. Another issue occurring in this architecture is the clock skew as paths to each channel can not be equal. Techniques are being developed to reduce the effect of all these non-idealities [39, 43, 9].

Frequency band decomposition This architecture consists of parallel band-pass modulators. The entire frequency range to digitize is divided into M sub-bands that each modulator processes independently [23, 24, 34]. Each modulator is followed by a digital decimating filter that eliminates the out-of-band quantization noise. The complete digitized signal is built adding every channel signal. This architecture usually includes a low-pass and a high-pass modulator in order to handle all the frequencies from DC to $F_s/2$ [19]. This architecture is depicted in Figure II.16. This architecture has the advantage of not

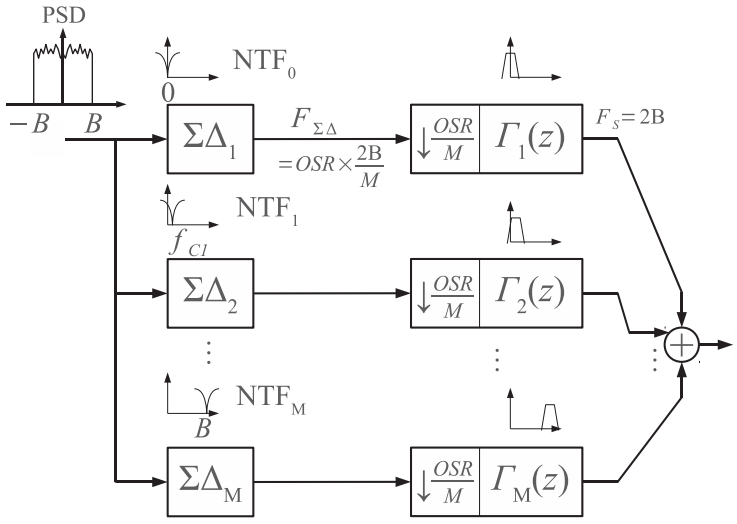


Figure II.16: The Frequency Band Decomposition ΣΔ architecture

creating nonlinearity due to the mismatch between channels but its complexity is very high because it requires to design M different modulators and high order digital filters to ensure good signal reconstruction [23, 19].

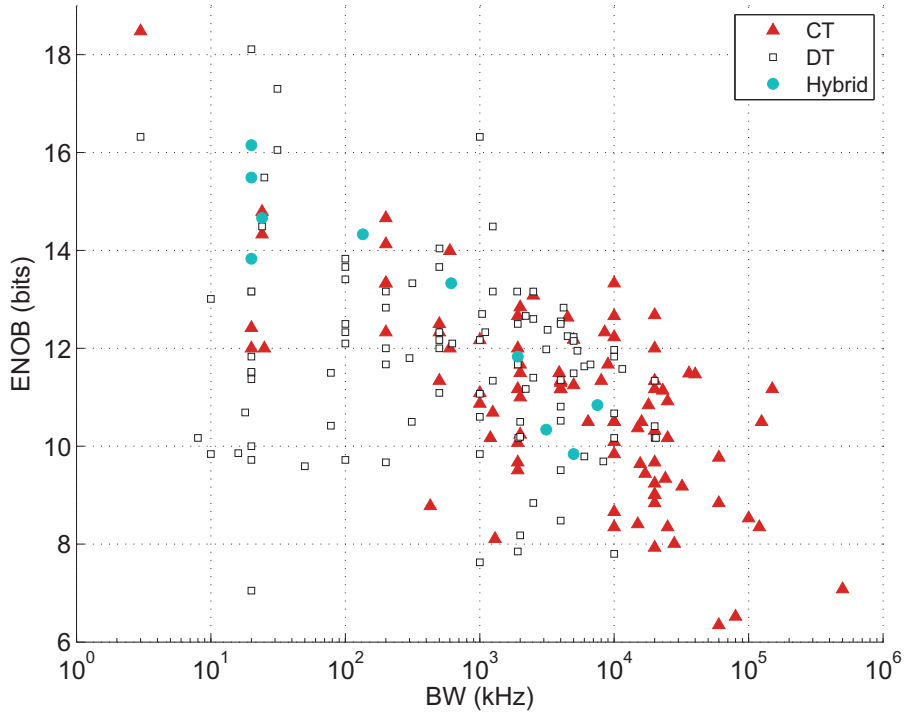
II.1.3 State of the art of ΣΔ

To conclude this overview of ΣΔ modulators, we present in this section a state of the art of modulator circuits published during the last 6 years in ASSCC, CICC, ESSCIRC ISSCC, JSSC and VLSI.
The Figure II.17a and Figure II.17b show the distribution of the modulators according to their performances and distinguish the DT, CT or hybrid feature of the modulators. The hybrid modulators are a third type of modulators that tries to take advantage of the benefits of both circuit techniques. The performance metrics used here are the resolution given with the ENOB, the signal bandwidth BW and the Figure of Merit (FoM). The FoM is a figure calculated with the power consumption, the ENOB and the bandwidth. It allows to compare different circuits with various performances and several FoM may be found in the literature. We used the FoM defined by:

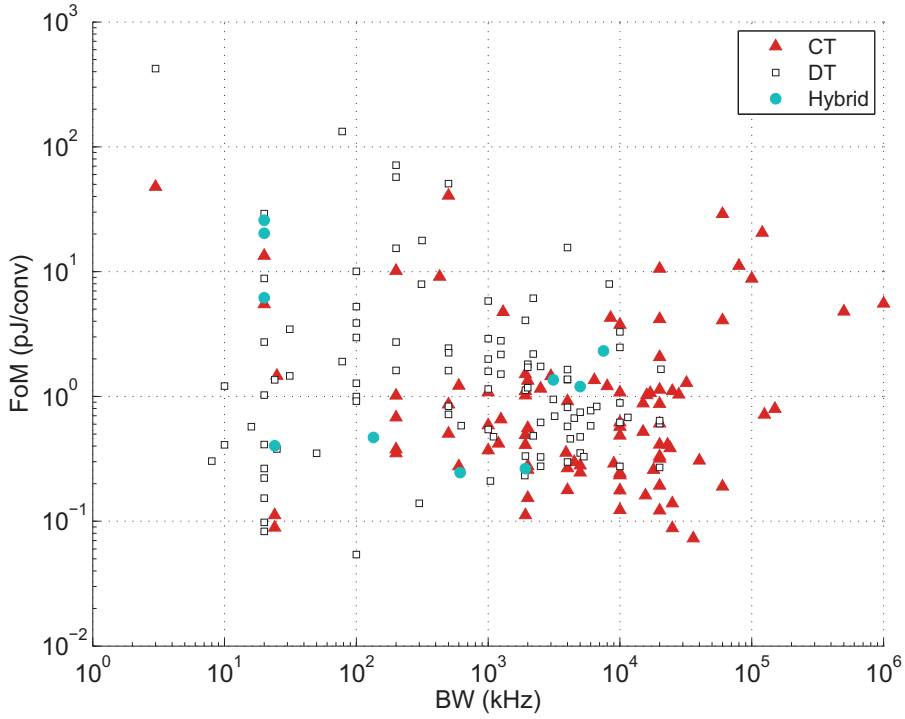
$$\mathrm{FoM} = \frac{\mathrm{P(W)}}{2^{\mathrm{ENOB(bits)}} \times 2\,\mathrm{BW(S/s)}} 10^{12} \tag{II.26}$$

where P is the power consumption of the modulator. The smaller the FoM value, the *better* the modulator. Figure II.18a and Figure II.18b display the same performances, showing further details on each type of modulators.
Figure II.17a clearly shows that most CT modulator can convert higher bandwidths than their DT counterparts. In addition, we note that several of these modulators convert bandwidths wider than 10 MHz for resolutions higher than 12 bits.
Figure II.17b illustrates that this type of modulator is also suitable for low power consumption applications while the bandwidth is wider than 1MHz.
Figure II.18a illustrates that in the DT case, the cascaded architectures allow to extend the bandwidth while maintaining a high resolution in comparison with the DT single loop modulators (DT-SL). It is not possible to draw the same conclusion for CT implementations as our inventory reports only one such converter [1].
Figure II.18b provides deeper insights for the comments on Figure II.17b. We note here that, the majority of modulators in the wideband and low FoM region are the CT-SL modulators.

[1] Its performances are: 67dB SNR at 10MHz bandwidth with 208MHz clock frequency and 10.5mW i.e. 0.573pJ/conv step

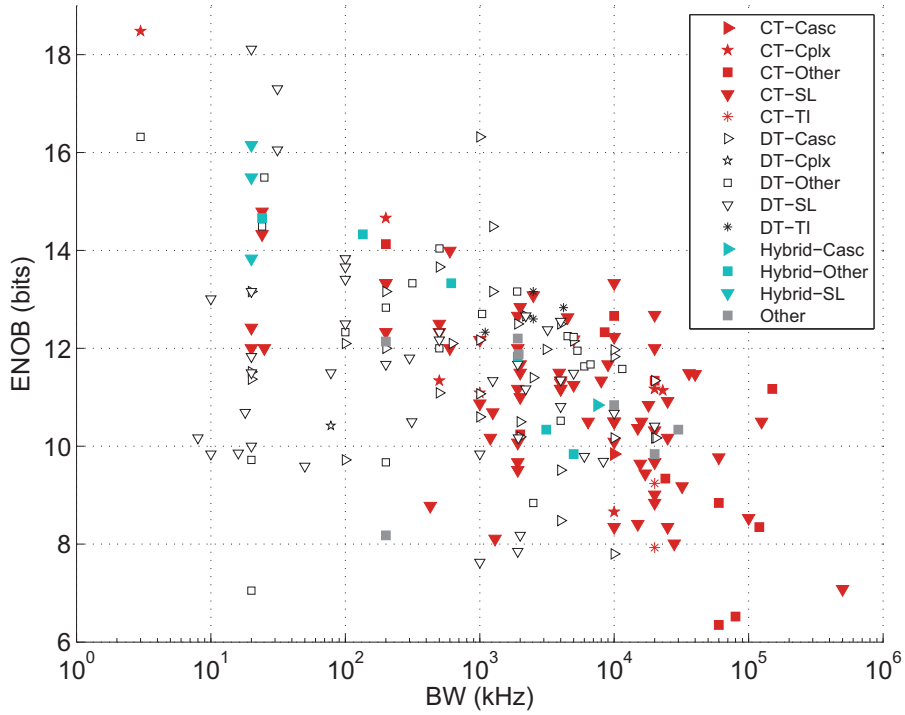


(a) Resolution versus Bandwidth

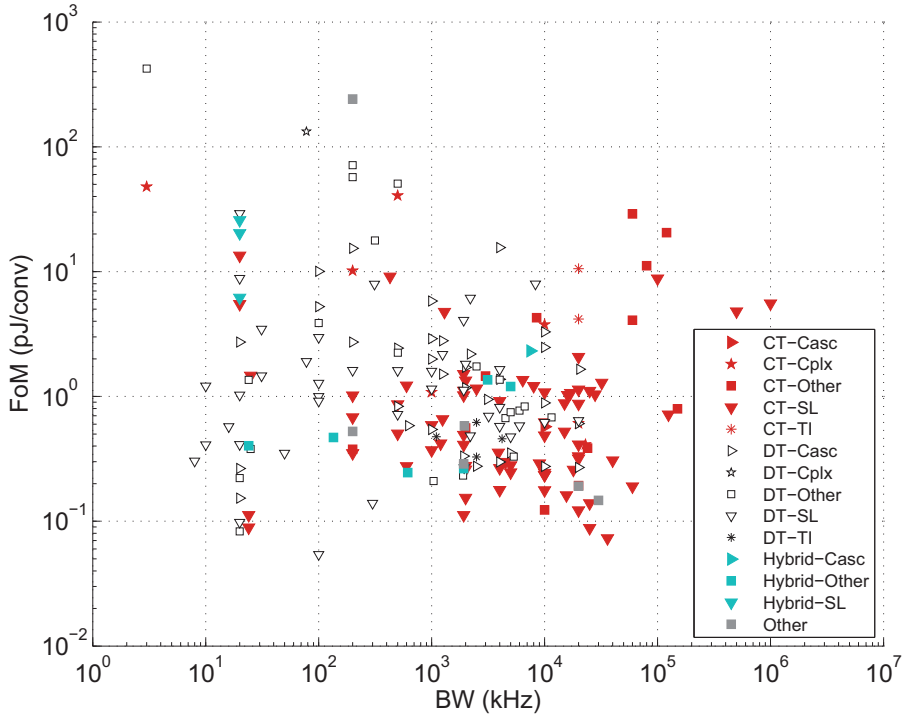


(b) Figure of Merit versus Bandwidth

Figure II.17: State-of-the-art of ΣΔ modulator circuits — General view



(a) Resolution versus Bandwidth



(b) Figure of Merit versus Bandwidth

Figure II.18: State-of-the-art of ΣΔ modulator circuits — Detailed view

II.2 System-level design and simulation

We describe now the method we used to design and simulate high-level models of DT and CT modulators during this thesis. This methodology is limited to the highest levels of design modulators and represents the early stages of the complete design of a modulator.

II.2.1 Top–down and bottom–up design methodology

The complete design of any integrated circuit (IC) further comprises a step of *top–down* design where the high-level parameters are decomposed and transcribed to specify the performances of each functional block. This decomposition continues refining the composition of the blocks at each step to reach the level of design where the handled blocks are the basic components of circuits: transistors, resistors, capacitors and inductors. At the end of each step of decomposition, a reverse *bottom–up* extraction step of the blocks performances is made to verify the design.

Besides the difficulty of reaching high performance circuits, the design of ΣΔ modulators can be tricky and involves design choices that influence the expected performance of sub-circuits even at the high-level design steps (architecture, values of coefficients). The multitude of high-level modulator parameters requires alone a design methodology and in this thesis, we focused on these high-level steps of design. Moreover, we discuss high order and band pass modulators. The design of these systems is a little different from low order modulators because the architectures have a number of parameters that makes impossible an exhaustive study of the influence of each of them, such as those presented in [82]. This process is detailed in the following section in which we largely refer to the MATLAB Delta-Sigma Toolbox [11], a well-known tool for the high-level design of ΣΔ modulators. It provides numerous functions to synthesize, simulate modulators and extract their performances.

II.2.2 System-level design of high order ΣΔ modulators

II.2.2.1 Discrete-time modulators

The fundamental parameters

The design process of a ΣΔ modulator starts from the fundamental target performances: effective resolution and conversion bandwidth. From Equation (II.18), the designer can derive multiple combinations of the fundamental parameters n, L and OSR to achieve the target performances. The final choice will be based on further optimizations in order to relax the design constraints and/or taking into account other considerations such as the power consumption.

Noise Transfer Function synthesis

The next step is the construction of a NTF in Z-domain. This can be done from scratch for special purpose or using the `synthesizeNTF()` function from the Delta-Sigma Toolbox. The design procedure from scratch begins with the choice of the type of approximation to use (i.e. Butterworth, Chebyshev or elliptic) and the definition of the filter specifications. Then, the transfer function can be calculated. This filter should be stable and the derived loop filter H from Equation (II.11) should be causal.

The design procedure using the Delta-Sigma Toolbox functions is simple because all the necessary optimizations are automatically performed, for the user, according to the pro-

Input/Output argument	Description
`order`	Loop filter order
`OSR`	The oversampling ratio of the modulator
`opt`	A flag for zeros optimization (`opt` = 0 disables the zeros placement optimization)
$\mathtt{H_{inf}}$	The out-of-band gain of the noise transfer function
$\mathtt{f_0}$	The center frequency of the modulator ($\mathtt{f_0} \neq 0$ yields a NTF for BP modulators)
`ntf`	Discrete-time noise transfer function

Table II.1: Input/Output arguments of the `synthesizeNTF()` function

vided parameters. The general form of the `synthesizeNTF()` function is:

$$\mathtt{ntf = synthesizeNTF(order, OSR, opt\ , H_{inf}, f_0)} \tag{II.27}$$

where the meaning of the parameters is given in Table II.1 . [1]
If the optimum zeros placement is requested, the function computes automatically the zeros frequencies pairs based on the oversampling ratio and analytical results. Furthermore, the function performs an iterative loop that places poles so that the NTF out-of-band gain is equal to the specified out-of-band gain (for Butterworth type filter). This parameter is of primary interest as its value significantly impacts the peak SNR of the modulator and its maximum stable input amplitude. This parameter will be further discussed in Section III.3.2.1.

Architecture and coefficient mapping
As mentioned in Section II.1.2.3, different architectures are available to us to implement the NTF. The Delta-Sigma Toolbox provides two main types of architecture that are commonly used: the single-stage architecture with multiple feedbacks (FB) and the single-stage architecture with feedforward paths (FF) [61, 73, 11]. Different configurations are also available: the cascade of integrators with multiple feedback (CIFB) or with feedforward (CIFF), and the cascade of resonators with multiple feedback (CRFB) or with feedforward (CRFF). These architectures have enough parameters to implement any NTF. Other architectures exist, particularly, having an additional feedback path between the DAC output and the adder at the quantizer input. From our point of view, as long as the system can be written as linear block diagram we can calculate the coefficients to implement any NTF. Calculating the coefficients of the architecture is done by equating the numerically valued transfer function $H^{target}(z)$ of the loop filter (open loop system) with the literal transfer function $H^{litt}(z)$ obtained from the block diagram architecture.
The method used in the toolbox and that is suitable to high-order modulators relies on estimating the parameters of a linear system. The linear system is built around the coefficients a_i as explained in Appendix D where we give the method for calculating the coefficients. We detail the method since we had to adapt it and implement it to design continuous-time modulators (Section II.2.2.2).
Figure II.19 shows the result of this mapping. The first step of the method is to ignore the coefficients c_i and determine the coefficients g_i and a_i that build the NTF^{target}.

[1] The reader is referred to the toolbox manual [11] for further description on values of each argument.

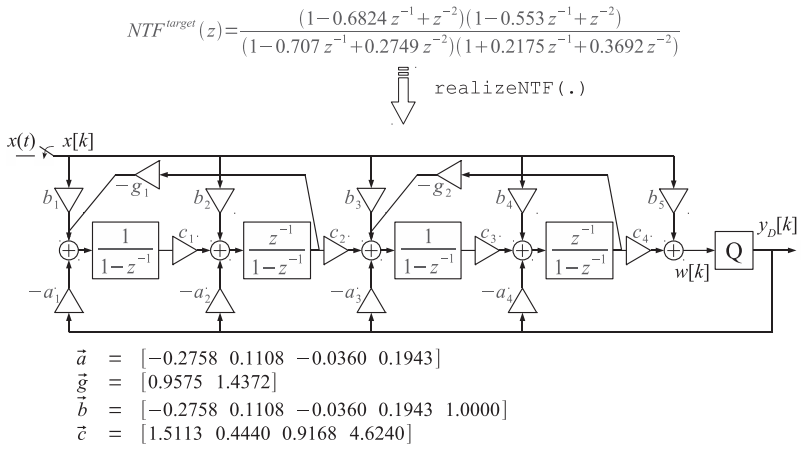


Figure II.19: An example of coefficient mapping onto the CRFB architecture.

Then the coefficients b_i are calculated so that they realize the $STFtarget$.
Finally, simulations are used to extract the dynamics of the signals at each node of the circuit and the coefficients c_i are used to adapt these dynamics such that they are not too large.
This process of high-level design is completed by the system simulations. This last step is discussed in Section II.2.3.

II.2.2.2 Continuous-time modulators

In the past, most work on ΣΔ is focused on DT implementation. Thus, tools and architectures have been consistently developed and optimized for this type of modulator. The design of CT modulator can benefit from all that previous experience by starting working on the loop filter DT $H^{target}(z)$. This method allows rapid development through discrete-time simulation and the accumulated experience of these systems in terms of architecture. This procedure is usually used but direct design from the continuous-time transfer functions, as in [58], is possible in light of the discussed mapping method, NTF extraction and simulation methods in this thesis report.
As previously mentioned, for low-pass modulator, the continuous-time architecture can coincide with that of the discrete-time modulator [32, 62, 58]. In contrast, for band-pass modulators, the architecture must include more parameters such as additional DACs [62] or additional connections to each integrator [15]. In all these cases the design of continuous-time loop filter is made from the discrete-time NTF.

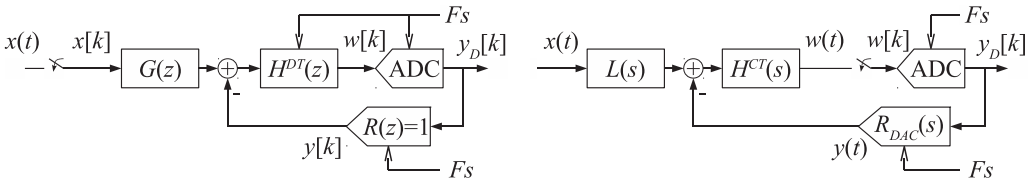
Noise Transfer Function synthesis

In this section we detail the impulse-invariant transformation to derive the equivalent loop filters that realize the same NTF^{target} in both CT and DT systems and we also detail the literal expressions of this transformation for the well known NRZ-DAC case[1].

The discrete-time–continuous-time equivalence The key point of DT–CT equivalence is to preserve the SNR achieving the same NTF in each modulator. As each NTF depends on the open loop filter (cf. Equation (II.11)), the equivalence expression will be drawn on this loop filter.

[1] NRZ stands for Non-Return to Zero

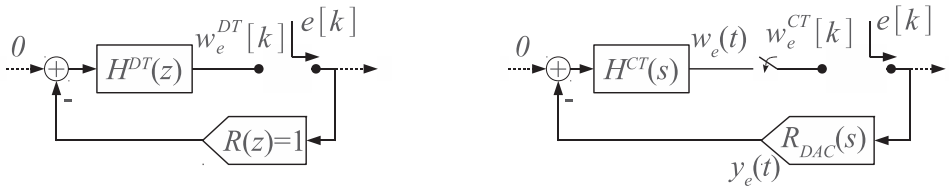
Every ΣΔ modulator can exactly be modeled in the forms presented in Figure II.20a and Figure II.20b whether it is DT or CT.



(a) Discrete-time modulator (b) Continuous-time modulator

Figure II.20: Block diagram of generalized ΣΔ modulators

In order to ensure the equivalence of the noise transfer functions, it is necessary to consider the quantization error path in the open loop system. The diagrams Figure II.21a and Figure II.21b show each system in open loop configuration regarding the quantization error path.



(a) Discrete-time modulator (b) Continuous-time modulator

Figure II.21: Open loop quantization error path

The DT–CT equivalence using the impulse-invariant transformation relies on equating the impulse response of the DT system [1] to the sampled impulse response of the CT system. The time domain equation is:

$$w_e^{DT}[n] = w_e^{CT}(t)_{|t=nT_s} \tag{II.28}$$

$$\Leftrightarrow \quad \mathcal{Z}^{-1}\left[H^{DT}(z)\right] = \mathcal{L}^{-1}\left[\mathcal{R}_{DAC}(s)\cdot H^{CT}(s)\right](t)_{|t=nT_s} \tag{II.29}$$

where $H^{DT}(z)$ is the equivalent loop filter transfer function in Z-domain, $\mathcal{R}_{DAC}(s)$ and $H^{CT}(s)$, respectively, the Laplace transfer functions of the DAC response and of the loop filter. $\mathcal{Z}^{-1}$ and $\mathcal{L}^{-1}$ are the inverse transform of each domain, the first one resulting in an inherently sampled signal and the second one in a continuous signal that is sampled at the instants $t = nT_s$.
It is worth to note that this equation provides a true equivalence. It can be used as well to obtain the loop filter transfer function of a CT modulator from a DT modulator as for the reverse.

For DACs with waveforms such as NRZ (Non-Return-to-Zero), RZ (return-to-zero) and HRZ (Half-delay RZ), analytic relations can be written between the parameters of the residue [2] forms of the Laplace transfer function and of the Z-domain transfer function [62]. In these cases, we note that the order of the transfer functions is conserved, but the topology is not always the same. In particular, for high order modulators, one has to add

[1] inherently sampled
[2] see `residuez` and `residue` in MATLAB help

new signal paths such as additional DACs [62, 32] or additional feedback paths splitting the resonators [15]. For example, in order to implement the equivalent CT modulator of the DT modulator shown in Figure II.22, [62] proposes to use several DACs with different waveform response.

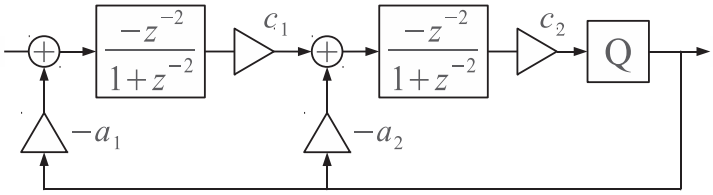
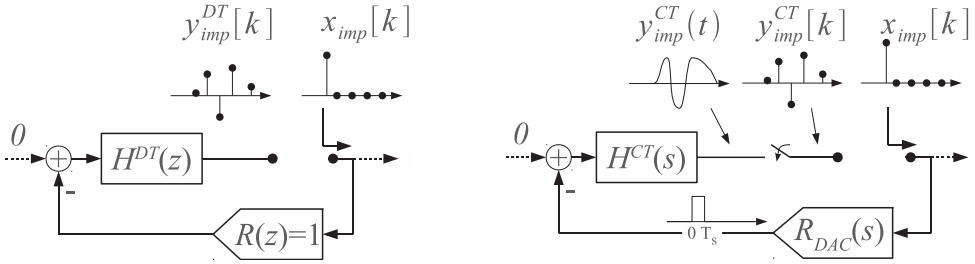


Figure II.22: DT Band-pass ΣΔ modulator with ideal resonators

The case of a NRZ-DAC For simulation purposes, we choose a NRZ-DAC [1] and we provide in this section the analytic expressions relating both loop filters.
We consider the depicted systems in Figure II.23:



(a) Discrete-time modulator (b) Continuous-time modulator

Figure II.23: Open loop impulse response diagrams

In order to derive the equivalence, we consider the discrete-time system Figure II.23a where a (DT) pulse excites the DAC and the DT filter $H^{DT}(z)$; and we also consider the continuous-time system Figure II.23b where a (DT) pulse excites the NRZ-DAC [2] and the CT filter $H^{CT}(s)$ whose output is sampled at the rate T_s. We want the (sampled) signals $y_{imp}^{DT}[k]$ and $y_{imp}^{CT}[k]$ to be the same:

$$y_{imp}^{DT}[k] = y_{imp}^{CT}[k] \ , \ \forall k \in \{0, 1, 2 \cdots\} \tag{II.30}$$

To derive the equivalence we start from the CT system and we calculate its (CT) impulse response $y_{imp}(t)$. There are different ways to do this calculation and we provide here a formulation of this calculation of the impulse response different from [62] though strictly equivalent. The fundamental assumption is that the CT loop filter transfer function $H^{CT}(s)$ has only single poles [3]. Therefore, its Laplace transform can be written in the following residue form:

$$H^{CT}(s) = \sum_{m=1}^{N} \frac{a_m^{CT}}{s - p_m^{CT}} \tag{II.31}$$

[1] for the simplicity of its model
[2] with a pulse width of T_s
[3] This condition is satisfied when all the NTF zeros are separated

where p_m^{CT} are the poles of the transfer function and a_m^{CT} the associated residue coefficients. Equivalently, its impulse response can be written as:

$$h^{CT}(t) = \sum_{m=1}^{N} a_m^{CT} \mathrm{e}^{p_m^{CT} t} \Theta(t) \tag{II.32}$$

where $\Theta(t)$ is the unit step function [1].
By definition, the impulse response $y_{imp}(t)$ is equal to:

$$y_{imp}^{CT}(t) = h^{CT} * r_{DAC}(t) \tag{II.33}$$

and as we assume the DAC to be an ideal NRZ-DAC, its impulse response is as follows:

$$r_{DAC}(t) = \Theta(t) - \Theta(t - T_s) \tag{II.34}$$

Substituting each term in Equation (II.33), we obtain:

$$y_{imp}^{CT}(t) = \sum_{m=1}^{N} a_m^{CT} \left(\underbrace{\left\langle \mathrm{e}^{p_m^{CT} t} \Theta(t) \right\rangle * \langle \Theta(t) \rangle}_{\blacksquare} - \underbrace{\left\langle \mathrm{e}^{p_m^{CT} t} \Theta(t) \right\rangle * \langle \Theta(t - T_s) \rangle}_{\clubsuit} \right) \tag{II.35}$$

We calculate the term ■:

$$\left\langle \mathrm{e}^{p_m^{CT} t} \Theta(t) \right\rangle * \langle \Theta(t) \rangle = \int_{-\infty}^{\infty} \mathrm{e}^{p_m^{CT} u} \Theta(u) \Theta(t - u) \, \mathrm{d}u \tag{II.36}$$

$$= \begin{cases} \int_0^t \mathrm{e}^{p_m^{CT} u} \, \mathrm{d}u & \text{if } t > 0 \\ 0 & \text{otherwise} \end{cases} \tag{II.37}$$

$$= \frac{1}{p_m^{CT}} \left(\mathrm{e}^{p_m^{CT} t} - 1 \right) \Theta(t) \tag{II.38}$$

And the term ♣ is equal to:

$$\left\langle \mathrm{e}^{p_m^{CT} t} \Theta(t) \right\rangle * \langle \Theta(t - T_s) \rangle = \int_{-\infty}^{\infty} \mathrm{e}^{p_m^{CT} u} \Theta(u) \Theta(t - u - T_s) \, \mathrm{d}u \tag{II.39}$$

$$= \begin{cases} \int_0^{t - T_s} \mathrm{e}^{p_m^{CT} u} \, \mathrm{d}u & \text{if } t - T_s > 0 \\ 0 & \text{otherwise} \end{cases} \tag{II.40}$$

$$= \frac{1}{p_m^{CT}} \left(\mathrm{e}^{p_m^{CT} (t - T_s)} - 1 \right) \Theta(t - T_s) \tag{II.41}$$

Substituting ■ by Equation (II.38) and ♣ by Equation (II.41) in Equation (II.35), we get:

$$y_{imp}^{CT}(t) = \sum_{m=1}^{N} \frac{a_m^{CT}}{p_m^{CT}} \left(\left(\mathrm{e}^{p_m^{CT} t} - 1 \right) \Theta(t) - \left(\mathrm{e}^{p_m^{CT} (t - T_s)} - 1 \right) \Theta(t - T_s) \right) \tag{II.42}$$

$$= \begin{cases} 0 & \text{if } t < 0 \\ \sum_{m=1}^{N} \frac{a_m^{CT}}{p_m^{CT}} \mathrm{e}^{p_m^{CT} t} \left(1 - \mathrm{e}^{-p_m^{CT} t} \right) & \text{if } 0 \leq t < T_s \\ \sum_{m=1}^{N} \frac{a_m^{CT}}{p_m^{CT}} \mathrm{e}^{p_m^{CT} t} \left(1 - \mathrm{e}^{-p_m^{CT} T_s} \right) & \text{if otherwise} \end{cases} \tag{II.43}$$

[1] also referred to as Heaviside function

The sampled version of y_{imp}^{CT} at sampling times $t = kT_s$ gives the DT loop impulse response equivalent:

$$y_{imp}^{DT}[k] = y_{imp}^{CT}[k] = \begin{cases} 0 & \text{if } k \leq 0 \\ \sum_{m=1}^{N} \frac{a_m^{CT}}{p_m^{CT}} \, \mathrm{e}^{p_m^{CT} k T_s} \left(1 - \mathrm{e}^{-p_m^{CT} T_s}\right) & \forall \; k > 0 \end{cases} \tag{II.44}$$

Therefore, the Z transfer function of this sampled signal is by definition:

$$H^{DT}(z) = \sum_{k=-\infty}^{+\infty} y_{imp}^{DT}[k] \, z^{-k} \tag{II.45}$$

$$= \sum_{k=1}^{+\infty} \left(\sum_{m=1}^{N} \frac{a_m^{CT}}{p_m^{CT}} \, \mathrm{e}^{p_m^{CT} k T_s} \left(1 - \mathrm{e}^{-p_m^{CT} T_s}\right) \right) z^{-k} \tag{II.46}$$

$$= \sum_{m=1}^{N} \frac{a_m^{CT}}{p_m^{CT}} \left(1 - \mathrm{e}^{-p_m^{CT} T_s}\right) \sum_{k=1}^{+\infty} \mathrm{e}^{p_m^{CT} k T_s} \, z^{-k} \tag{II.47}$$

$$= \sum_{m=1}^{N} \frac{a_m^{CT}}{p_m^{CT}} \left(1 - \mathrm{e}^{-p_m^{CT} T_s}\right) \mathrm{e}^{p_m^{CT} T_s} \, z^{-1} \frac{1}{1 - \mathrm{e}^{p_m^{CT} T_s} \, z^{-1}} \tag{II.48}$$

$$= \sum_{m=1}^{N} \frac{a_m^{CT}}{p_m^{CT}} \left(\mathrm{e}^{p_m^{CT} T_s} - 1\right) \frac{z^{-1}}{1 - \mathrm{e}^{p_m^{CT} T_s} \, z^{-1}} \tag{II.49}$$

$$\tag{II.50}$$

Then we can directly deduce the residue form of the DT transfer function:

$$H^{DT}(z) = \sum_{m=1}^{N} \frac{a_m^{DT} z^{-1}}{1 - p_m^{DT} \, z^{-1}} \tag{II.51}$$

where the new coefficients are:

$$a_m^{DT} = \frac{a_m^{CT}}{p_m^{CT}} \left(\mathrm{e}^{p_m^{CT} T_s} - 1\right) \tag{II.52}$$

$$p_m^{DT} = \mathrm{e}^{p_m^{CT} T_s} \tag{II.53}$$

The reader is also referred to [62] for the case of multiple poles and other square type DAC responses.

Architecture and coefficient mapping

Similarly to the DT case, the loop filter has to be implemented with a given architecture. A brief description of the coefficient mapping of high-order modulators is given in this section. The detailed calculation are provided in the Appendix E.

As mentioned previously, we use as a test case architecture, the CT-CIFB structure illustrated in Figure II.10 that is replicated here for convenience in Figure II.24.

For this type of architecture, the derivation of the coefficients is done based on the same type of expressions as in the DT case. We only use single pole transfer functions though multiple pole transfer functions could be used. The first steps are to set the γ_i coefficients and the α_i coefficients the implement the theoretical transfer function of the loop filter derived from the DT–CT equivalence. Then, the β_i coefficients are derived from an estimate of the wanted $STF(j\omega)$. Finally, the θ_i coefficients can be set to limit the dynamics

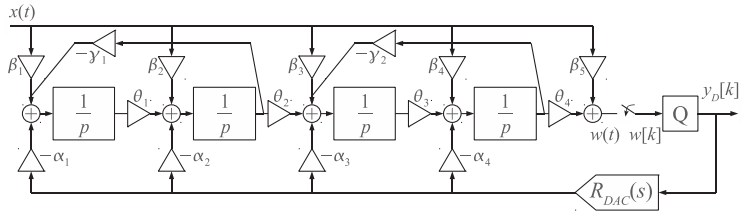


Figure II.24: A 4-th order CT-CIFB modulator (duplicate)

at each node of the modulator and the simulation of the system can be done using the method discussed in the following Section II.2.3.

II.2.3 Dynamic performance simulations

II.2.3.1 Simulation tools

An important step in circuit design is the simulation phase. At any design level, simulations should be as fast as possible and should maintain maximum accuracy.
At high-level design, these simulations are based on relatively simple equations that describe time behavior of circuit blocks.
For discrete-time systems, these equations are *recurrence relations* and are derived from Z transfer functions:

$$\frac{A(z)}{B(z)} = \frac{z^{-1}}{1-z^{-1}} \quad \Leftrightarrow \quad a[n] - a[n-1] = b[n-1] \tag{II.54}$$

For continuous-time systems, these equations are *differential equations* and can also be derived from the Laplace transfer functions:

$$\frac{A(p)}{B(p)} = \frac{1}{p} \quad \Leftrightarrow \quad a(t) = \int_0^t b(u)\mathrm{d}u \quad \Leftrightarrow \quad \dot{a}(t) = b(t) \tag{II.55}$$

As for all simulation systems, we face two problems: the time of development of the simulation system and the execution time of the simulation [1].

In the case of ΣΔ modulators, we identify three methods to perform simulations: a description node by node, a matrix description via state-space representation and simulation using specific tools providing graphical representation of functional blocks such as schematics or block diagrams.

The first method is suitable for systems in which there are few equations (low order modulator). It allows to easily model nonlinear imperfections in blocks such as Slew Rate. However, in discrete-time systems it requires to pay attention to the scheduling of calculations and on the other hand, it is not suitable for simulation of continuous-time systems.
Programming languages used for this simulation method are essentially MATLAB and C. The first one is characterized by its ease of use. The second one is characterized by execution speed that is incomparable to any other simulation system but may require a bit longer development time.

The second method is suitable for all systems but requires a data formatting work and matrix handling. It is based on the state-space representation of systems and is used in

[1] Often, the longer the development, the shorter the simulation time

the Delta-Sigma Toolbox [1]. This method consists in representing all the time equations of the system in the form of a matrix product.
Then the privileged programming language for this description is MATLAB. However, despite a small extra cost of development, the use of C language enables accurate and extremely fast simulations.

The third method is defined by the use of some specific simulation tool rather than by the representation of the parameters in the algorithm. We are dealing with simulation software providing a development environment where the elements are represented graphically by block functions such as Simulink or Xcos. Here, the simulation algorithm of the system is managed by the program development environment and the user does not typically need to write code.
This method is suitable for the analysis of small systems for the ergonomics of the modeling but it is difficult to use for large systems and especially to perform many simulations with parameters randomization.
Indeed, for example, in the case of Simulink, the basic simulation workflow includes a step for verifying the compliance of the diagram with Simulink rules, a compilation stage and at the end, the simulation run phase. However, the first two steps are unnecessary in the context of repeated simulation where the only modified element is the input signal.
We experimented with several simulation methods that avoid the repetition of these first steps as the use of vectorization [2] but this method was incompatible with continuous-time simulations.
Another method is to generate a C-based executable using the Simulink Coder toolbox. This technique has greatly accelerated the simulations but its performance is still limited by a generation of configurations files that takes a significant time for each simulation.

Table II.2 summarizes the key simulation techniques that we experimented with the characteristics of each.

[1] cf. section *Modulator Model details* in the User Guide
[2] Technique of constructing signals matrices where each column represents a random realization of the signal.

Description Method	Development Environment	Ease of development	Simulation Time	Size of tractable systems	DT Systems	CT systems
Node by node	MATLAB	Very easy	Fast	Small	Yes	No
	C language	Easy	Very fast	Small	Yes	No
State Space	MATLAB	Very easy	Fast	Large	Yes	Yes
	C language	Average	Very fast	Large	Yes	Yes
Simulink	Simple workflow	Easy/Average	Slow	Small to Average	Yes	Yes
	Simulink Coder	Easy/Average	Fast	Small to Average	Yes	Yes

Table II.2: Simulation techniques summary

It appears that the C-coded state space simulation technique is the best method with relatively limited development effort, for execution speed and large tractable systems.
This method is implemented in the Delta-Sigma Toolbox for the simulation of discrete-time modulators.
We will detail the simulation technique in the case of continuous-time system as a significant part of this thesis. Its state-space basis has already been introduced [44] but to our knowledge, it is not used for simulations.

II.2.3.2 CT state-space simulation

As described in Section II.1.2.3 we use the CT-CIFB structure as modulator architecture which we reproduce the diagram Figure II.25. $x_i(t)$ represent the output continuous-time

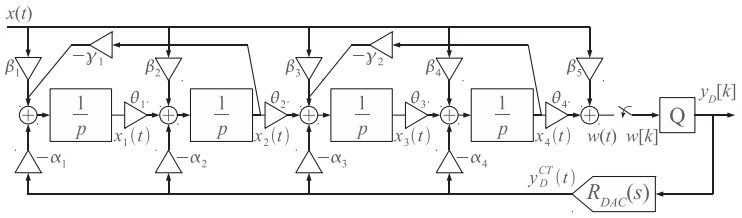


Figure II.25: The state variables in the CT-CIFB modulator

signal from the continuous-time integrator i. In the same way as for the discrete-time systems, the system can be described as follows:

$$\begin{cases} \begin{pmatrix} \dot{x_1}(t) \\ \dot{x_2}(t) \\ \dot{x_3}(t) \\ \dot{x_4}(t) \end{pmatrix} = \begin{pmatrix} 0 & -\gamma_1 & 0 & 0 \\ \theta_1 & 0 & 0 & 0 \\ 0 & \theta_2 & 0 & -\gamma_2 \\ 0 & 0 & \theta_3 & 0 \end{pmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \\ x_4(t) \end{pmatrix} + \begin{pmatrix} \beta_1 & -\alpha_1 \\ \beta_2 & -\alpha_2 \\ \beta_3 & -\alpha_3 \\ \beta_4 & -\alpha_4 \end{pmatrix} \begin{pmatrix} x(t) \\ y_D^{CT}(t) \end{pmatrix} \\ w(t) = \begin{pmatrix} 0 & 0 & 0 & \theta_4 \end{pmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \\ x_4(t) \end{pmatrix} + \begin{pmatrix} \beta_5 & 0 \end{pmatrix} \begin{pmatrix} x(t) \\ y_D^{CT}(t) \end{pmatrix} \end{cases} \tag{II.56}$$

i.e.

$$\begin{cases} \vec{\dot{\mathbf{X}}}(t) = \mathbf{A_{CT}} \cdot \vec{\mathbf{X}}(t) + \mathbf{B_{CT}} \cdot \begin{pmatrix} x(t) \\ y_D^{CT}(t) \end{pmatrix} \\ w(t) = \mathbf{C_{CT}} \cdot \vec{\mathbf{X}}(t) + \mathbf{D_{CT}} \cdot \begin{pmatrix} x(t) \\ y_D^{CT}(t) \end{pmatrix} \end{cases} \tag{II.57}$$

To perform the simulation of this CT system we must sample the system. In particular, we show that the equations system II.57 can be time-discretized assuming a zero order hold for the input $\begin{pmatrix} x(t) \\ y_D^{CT}(t) \end{pmatrix}$:

$$\begin{cases} \vec{\mathbf{X}}_D((k+1)T_{step}) = \mathbf{A_{DT}} \cdot \vec{\mathbf{X}}_D(k\,T_{step}) + \mathbf{B_{DT}} \cdot \begin{pmatrix} x_{S/H}\,(k\,T_{step}) \\ y_{S/H}\,(k\,T_{step}) \end{pmatrix} \\ w_D(k\,T_{step}) = \mathbf{C_{DT}} \cdot \vec{\mathbf{X}}(k\,T_{step}) + \mathbf{D_{DT}} \cdot \begin{pmatrix} x_{S/H}(k\,T_{step}) \\ y_{S/H}(k\,T_{step}) \end{pmatrix} \end{cases} \tag{II.58}$$

where:

$$\mathbf{A}_{DT} = \exp\left(\mathbf{A}_{CT} T_{step}\right) \tag{II.59}$$

$$\mathbf{B}_{DT} = \mathbf{A}_{CT}^{-1}(\mathbf{A}_{DT} - I)\mathbf{B}_{CT} \text{ if } \mathbf{A}_{CT} \text{ is non-singular} \tag{II.60}$$

$$\mathbf{C}_{DT} = \mathbf{C}_{CT} \tag{II.61}$$

$$\mathbf{D}_{DT} = \mathbf{D}_{CT} \tag{II.62}$$

and T_{step} is the computation time step (or computation sample time).
But if T_{step} is very small compared to the characteristic time constants of the system, in this case the sampling period T_s of the quantizer and the minimum signal period T_{sig} (e.g. $T_{step}/T_s < 10^{-2}$ and $T_{step}/T_{sig} < 10^{-2}$) we can approximate:

$$\dot{\vec{\mathbf{X}}}(t) \approx \frac{\vec{\mathbf{X}}(t + T_{step}) - \vec{\mathbf{X}}(t)}{T_{step}} \tag{II.63}$$

and the sampled sequence $\vec{\mathbf{X}}_D(k\,T_{step})$ calculated by the discretized system at the period T_s is a good estimate of the CT signal $\vec{\mathbf{X}}(t)$ sampled at the same moment.
Therefore, to simulate a continuous-time system it will be assumed that the entire system is sampled at a very small T_{step} and we will use the matrix equations II.58.
And this calculation is already implemented in the Delta-Sigma Toolbox except that in the DT case $T_{step} = T_s$ whereas in the CT case $T_{step} \ll \{T_s, Tsig\}$. Therefore, we can reuse the code of the toolbox with some modifications in order to simulate CT $\Sigma\Delta$ modulators.
This modification concerns the inclusion of the DAC. Indeed, while in the discrete-time the DAC response waveform is not involved, in continuous-time, it is fundamental to mention it. For reasons mentioned previously, we choose to use a NRZ-DAC. Other DAC waveforms can be used as long as the calculation of the loop filter takes this data into account.
Therefore, the algorithmic implementation of the DAC is simply to keep the same value $y_{S/H}\,(k\,T_{step})$ for $T_s/T_{step} = k_{step}$ calculation iteration.
Figure II.26 illustrates the implementation of this simulation technique. The input signal,

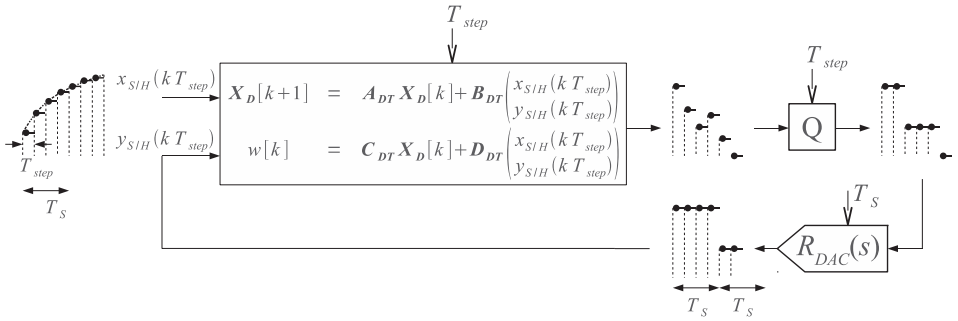


Figure II.26: Implementation diagram of the discretized state space model of a CT modulator

originally continuous-time, is sampled at the period T_{step} and it is one of the two inputs of the equation system. The second input signal, is also sampled at the same time step is the DAC output. This output is maintained for k_{step} computation steps because the DAC (and the ADC in theory) works at the rate $T_s = k_{step} \times T_{step}$. For practical reasons of coding, we have chosen to model the ADC to digitize at the period T_{step}, which does not affect the simulation as long as the DAC changes its output only at the instant kT_s.
Finally, by construction, each piece of computation iteration of the equations provides a

sample.
We give in Appendix F the C-code that implements this technique and that we used for the simulation of CT modulators in this thesis.

II.3 Conclusion

In this chapter we recalled the basic concepts of the A/D conversion with ΣΔ converters. The over-sampling, the noise shaping, the stability and the decimation filter were briefly explained. We have also presented the different existing architectures and we extracted main features of DT and CT modulators from a state of the art. Then we described the high-level design methodology of ΣΔ modulator. We detailed the principles of mapping a NTF on a given architecture and the fast simulation techniques that we used to extract performance modulators. In particular, we adapted the design methodology of DT modulators to design our CT modulators and we fully described the state-space simulation technique for CT systems that can be implemented reusing some code provided by the Delta-Sigma Toolbox.
This chapter provides the foundation base, both in terms of theory and simulation, which helped develop the new architecture we propose in the next chapter.

Chapter III

Multi-Stage Noise Band Cancellation Architecture

In the previous chapter, we present different architectures based on $\Sigma\Delta$ modulators and discuss some of their features. We have seen that cascaded architectures enable the design of high resolution converters and the parallel frequency decomposition architectures have been proposed to convert wide-band signals.
We develop, in this chapter, a new architecture taking advantage of these two techniques. It uses a kind of frequency band decomposition and digitization of the shaped quantization noise and its cancellation in the digital domain.
Using the previous methods for designing and simulating modulators, we show that this architecture, which is designed to digitize distorted signals output from BTS power amplifiers, allows wide-band digitization of signals with high resolutions.

III.1 Introduction

In Chapter I we introduced the DPD, a technique used to improve the linearity of the PA and hence their efficiency. This technique is based on digital processing that consists in predistorting, in an inverse way of the PA, the signal to be transmitted so that, once amplified (and distorted), the signal is the least altered as possible compared to the ideal signal.
For this purpose the DPD system calculates an inversion model of the response of the PA from measurements on the distorted signal. These measurements are made through the digitization process done by an ADC.
Currently these components are pipelined ADCs because they provide large dynamic range and wide-band conversion. However, we think that this type of converter is not the most suitable for this application. Indeed, Figure III.1 shows simulated output spectra of a PA emitting three WCDMA carriers with and without DPD.
We can see that the power of the distorted signal with and without DPD, is not equally distributed in the spectrum: it is made up of a high power central signal band (of 15MHz), that corresponds to the initial wanted signal, and of unwanted lower power adjacent signal bands resulting from intermodulation (IM) products. Regarding the distorted signal with DPD, we note that the level of power of adjacent bands has been lowered.
In a running installation, the ADC in the feedback path should be able to digitize both signal cases: the first case occurring at the start-up and the second case occurring in adaptive systems when the PA have been previously linearized and the DPD system updates its PA model to cope with possible variations.

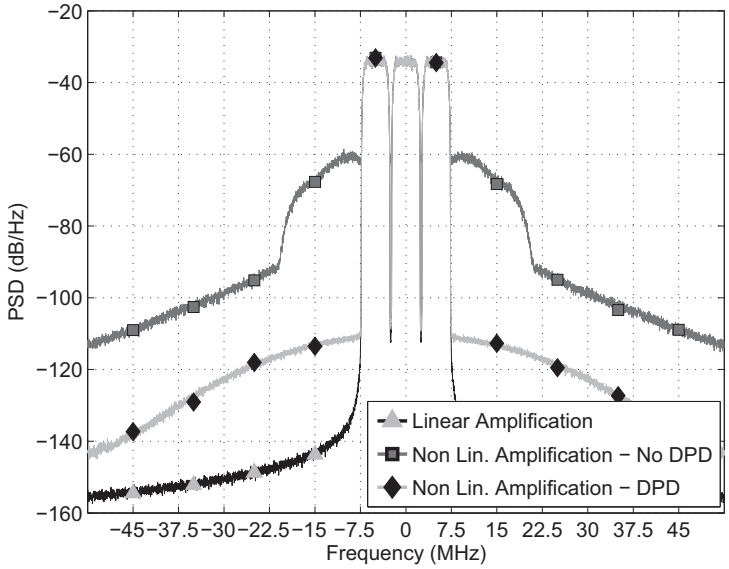


Figure III.1: Simulated output spectra of the transmitter with and without predistortion for a three-carrier WCDMA signal

From the DPD point of view, this second case is, by definition, the best case since the emitted signal has a better quality. But from the ADC point of view, this case is the toughest since low power adjacent bands should not be hidden by the quantization noise. We observe that by using a pipeline ADC to digitize this signal type we oversize the converter. Indeed, if we imagine that each band is separated of the distorted signal, the low-power signals may be digitized independently of the high power band, with a higher resolution. In addition, this band processing can be performed directly by using BP $\Sigma\Delta$ modulators whose specificity is to be able to digitize only signals around a certain center frequency. Moreover, the power consumption of $\Sigma\Delta$ modulators is usually lower compared to their equivalent pipelined architectures.
Thus, the most natural solution seems to digitize the distorted signal using multiple parallel BP $\Sigma\Delta$ converters processing each part of the signal. However, plain frequency band decomposition architecture (FBD) [19] is not possible in our case because, apart from the natural difficulty in designing wide-band BP $\Sigma\Delta$ modulators, the main difficulty of this architecture is in the separation of each frequency band. Otherwise converters centered on low power bands will also process the highest power band and these converters will have to be over-sized too.

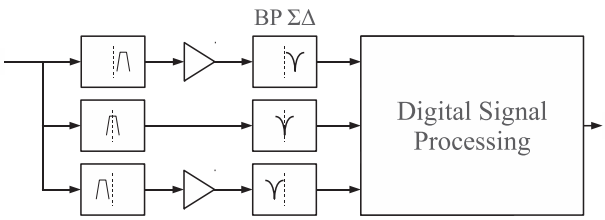


Figure III.2: An implementation of the FBD architecture using high order analog filters to optimize each path dynamic range

To isolate the low power, signal bands we should use the architecture shown in Figure III.2 where the bands are selected by filters having very small transition bands. This feature results in high order analog filters and therefore probably expensive implementation area and power consumption.
In addition, we can see a similar implementation in hybrid filter bank systems. They are also parallel architectures as shown in Figure III.3. In such systems, each channel consists of an analog band-pass filter referred to as analysis filter, an ADC and a digital filter referred to as synthesis filter.

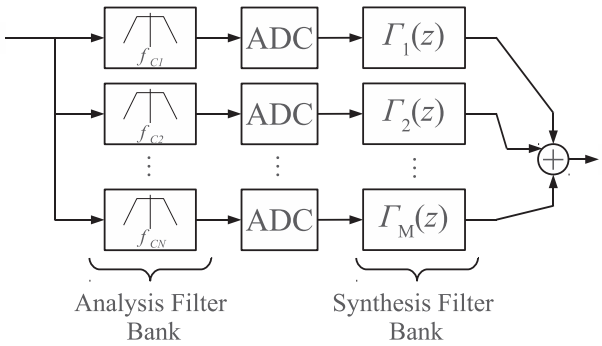


Figure III.3: Hybrid Filter Bank Architecture

One of the difficulties in the realization of these components in advanced CMOS technologies is a low robustness of hybrid filter banks to cope with deviations from analog parameters [17]. And, the design of ΣΔ modulators includes enough parameters subject to variation to increase the design complexity by adding analog filter banks.
Thus, we do not wish to use analog filters to separate low power bands. To do so, we will exploit the natural ability of ΣΔ modulators to achieve filtering.
We begin first by defining the signal that we use throughout our discussion and the expected performance of the converter.

III.1.1 Test signal specifications and converter requirements

The conventional design of converters always starts with the analysis of the target application needs to express the bandwidth and resolution. Usually these requirements are deduced from telecommunications standards and some knowledge of the signal processing chain. As we introduced in Chapter I, our application case does not clearly defines the requirements for the resolution of the feedback path converter. However, based on the feedback experience provided by the project partners, we defined a set of specifications for each signal band.

III.1.1.1 Test signal specifications

First we assume that the signal to be converted has a spectral profile as the one described in § I.3.2 reproduced here in Figure III.4. This signal consists of several bands of width $BW = 15\text{MHz}$. The high power band corresponds to the three WCDMA carriers to transmit. The first 15MHz adjacent bands result mainly from 3rd order distortions and are assumed to be 60dB lower than the main band. The following 15MHz resulting from 5th order distortions are assumed to be 70dB lower than the main band.
For the preliminary tests of § III.1.5 we assume that each band is made of a white signal

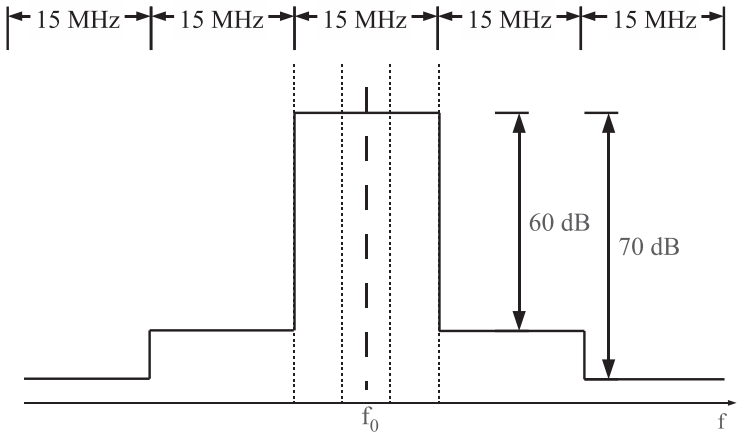


Figure III.4: Assumed signal spectral profile

whose combination meets the spectral profile. However, in order to extract the performance of a ΣΔ modulator by simulation, one must use a simpler signal such as a sinusoid. Therefore, for SNR simulations we use a signal composed of two sinusoids: a high power that is placed close to one edge of the main band, and another 60dB (or 70dB) lower, also placed near one edge of the considered band.

III.1.1.2 Converter requirements

To ensure proper operation of the DPD, the required SNRs have been defined on each band of the signal. We denote SNR_{BPr} and SNR_{BAdj}, the SNR in the main band and in the adjacent band, respectively. The main band should have an SNR of $SNR_{BPr} = 62$dB which corresponds to a resolution of 10 bits, and the adjacent band should have an SNR of $SNR_{BAdj} = 20$dB that is a resolution of about 3 bits.
Since this signal is set 60dB below the main signal, once recombined, the signal would have a dynamic conversion of 80dB approximately for 45MHz bandwidth. [1]

III.1.2 Center frequency

As we use BP ΣΔ modulators the question center frequency of arises. If for conventional band-pass ΣΔ modulator this issue is crucial since it significantly impacts the complexity of the digital part (see Section II.1.2.1), in the context of this thesis, this parameter is of lesser importance.
The main reason is that by definition, the frequency decomposition inevitably places the center frequency of all the modulators, at any frequencies except possibly two, one to $F_s/4$ and one to $3F_s/4$. Thus, by definition, this architecture includes a relatively complex digital part because of these non-$F_s/4$ modulators.
The second reason is that the architecture and design methodology we propose is independent of the center frequency of the overall converter. However, in the perspective of full design of the converter, some information is provided by the project partners to set this

[1] As this work is being written, we have not been able to confirm or disprove the optimality of this specification, as we do not have a PA and a DPD algorithm to test ; but, as our basic signal is assumed to be a worst case and in light of simulation results of the Section I.3.4 we think that the specifications given in this work slightly oversize the component compared to its optimum specification. However, this may allow a certain error margin to overcome the non-idealities of realization.

parameter. The sampling frequency of the converter is assumed to be $F_s = 800\text{MHz}$ and the signal may be located around $F_c = 200\text{MHz}$ approximately.

Thus, we consider the design of the converter centered around $F_c = F_s/4$. All the modulators being clocked at the same frequency F_s, the system will consist of a modulator centered $F_s/4$, the other would be centered on $F_s/4 \pm k \times BW$.
However, the development of advanced simulation tools has highlighted a nonlinear behavior of $\Sigma\Delta$ modulators centered around $F_s/4$, designed by the Delta-Sigma Toolbox. After some tests, we found that decentering the $\Sigma\Delta$ modulator far enough from $F_s/4$ makes the simulated modulators linear (§ III.3.1.2). In order to avoid the problem of nonlinearity in the simulations, we have performed the simulations with $F_c^{new} = 160\text{MHz}$.
This change in frequency is, originally solely for simulation purposes to analyze the architecture and a realization with $F_c = 200\text{MHz}$ should be done provided the nonlinearity issue is solved.
That is why, in this manuscript some simulation results (mainly at the beginning) will be presented centered around $F_c = 200\text{MHz}$ but spectrum resulting from advanced simulations will be presented centered around $F_c^{new} = 160\text{MHz}$.

Now that we have specified the performance to achieve on the test signal , we explain the initial idea of a new architecture to convert this signal. We will comment on the performances with respect to performance target.

III.1.3 Description of a new converter architecture

We saw in Chapter II, that in $\Sigma\Delta$ modulators, the signal to be digitized is affected by a filter modeled by the STF and the quantization noise is shaped by the NTF.
The Figure III.5 shows intuitive operation of the modulator $\Sigma\Delta$. This (not rigorous) diagram illustrates the operation of the initial idea of the converter architecture that we wanted to develop in this thesis. The signal is assumed to be made up of a band of high

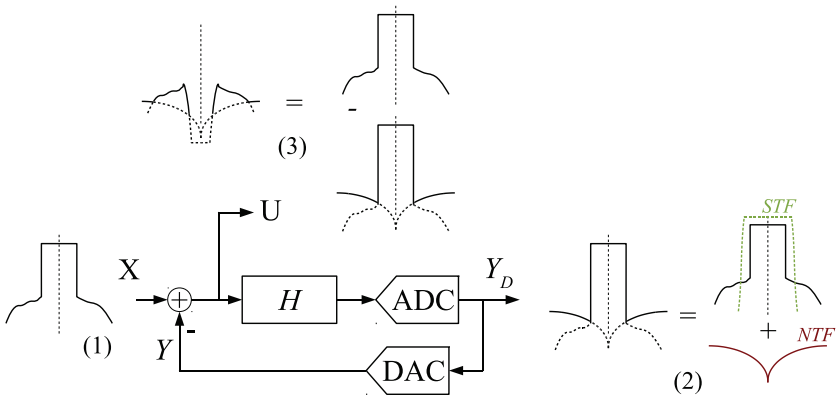


Figure III.5: Diagram of a new architecture where the signal is filtered

power and low power adjacent bands (1). It is also assumed that the STF is such that at the output of modulator, only the high power main band is selected, adjacent bands having been filtered. Then, the output of the modulator consists of that part of the signal and the shaped quantization noise (2). Considering the signal u constructed by subtracting $x - y$, where y is the analog converted version of y_D, one can assume that the signal will be attenuated on its main band (3). And if the noise level is sufficiently low, then, we

would have been able to filter the signal from the main band and keep only the adjacent bands. Then it would be sufficient to use other BP ΣΔ modulators centered on each adjacent band to accurately digitize (4). The detailed study show that the hypothesis on the STF is not quite right and that filtering cannot be as selective as we imagined. In addition, the level of shaped quantization noise will also play a role in the development of this proposed architecture. However, the principle of subtracting the signal is still valid and we will elaborate on this point in the next section where we define and study the model of performed filtering.

III.1.4 The Residual Signal Transfer Function

III.1.4.1 Definition

The Residual Signal Transfer Function (RSTF) is the model of the filtering achieved when subtracting the analog fed back output of a ΣΔ to its analog input. In the case of discrete-time architectures, this filter is exactly and concisely modeled as a Z transfer function. In the case of continuous-time architecture, the model can not be factorized in the same way as in the discrete-time case and we can not define a transfer function. Therefore we define the RSTF and study it rigorously only for the discrete-time case.
We consider the diagram in Figure III.6.

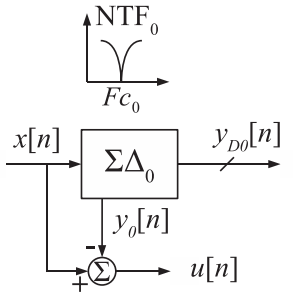


Figure III.6: RSTF definition — General diagram

y_{D0} is the digital output of the modulator and y_0 is its analog converted version. It is the signal fed back by the modulator DAC.
Using the linear model for the quantizer of the modulator, the signal u can be written in the Z-domain as a composition of X and N_0, respectively the Z-transform of the input signal x and of the quantization noise n_0 of the modulator $\Sigma\Delta_0$:

$$U(z) = X(z)\, RSTF(z) - N_0(z)\, NTF_0(z) \tag{III.1}$$

Leading to the following definition for the RSTF:

$$\boxed{RSTF(z) \stackrel{\text{def}}{=} 1 - STF_0(z)} \tag{III.2}$$

STF_i and NTF_i denote the signal transfer function and the noise transfer function of the modulator i.
We can note from this definition an interesting property: if the STF is unitary ($STF(z) = 1$), the resulting RSTF is equal to zero. Therefore, the signal provided to secondary paths will be only the (negative) shaped noise.

III.1.5 Detailed example: the 4-th order BP ΣΔ modulator

III.1.5.1 Theoretical analysis

In order to illustrate the effect of a non-null RSTF (non unitary STF) with a theoretical analysis, we study the BP modulator shown in Figure III.7.

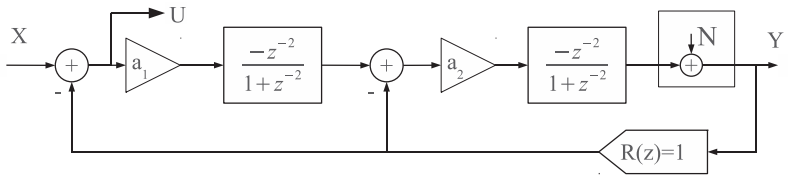


Figure III.7: A 4-th order BP ΣΔ modulator with two ideal DT resonators

In this architecture, the signal u is at the output of the first subtrator since there are no *feed-in* paths and feedback coefficients are equal to one.
We can show that the Z-transform of the modulator output can be written as follows:

$$Y(z) = X(z)STF(z) + N(z)NTF(z) \tag{III.3}$$

where $X(z)$ and $N(z)$ are respectively the input and noise $Z-$transform and, the signal transfer function $STF(z)$ and the noise transfer function $NTF(z)$ are:

$$STF(z) = \frac{a_1 a_2}{z^4 + (2-a_2)z^2 + a_1 a_2 - a_2 + 1} \tag{III.4}$$

$$NTF(z) = \frac{z^4 + 2z^2 + 1}{z^4 + (2-a_2)z^2 + a_1 a_2 - a_2 + 1} \tag{III.5}$$

Therefore, the RSTF is:

$$RSTF(z) \overset{\text{def}}{=} 1 - STF(z) = \frac{z^4 + (2-a_2)z^2 + 1 - a_2}{z^4 + (2-a_2)z^2 + a_1 a_2 - a_2 + 1} \tag{III.6}$$

The numerator and the denominator of these transfer function are factorizable so we provide in Table III.1 the zero/pole analysis of each function. Each cell in the table shows, according to its row and its column, the zeros or poles of the considered transfer function. Regarding the zeros, it is possible to extract the literal theoretical frequency values because they are either fixed or dependent on a single (real) parameter. However, regarding the poles, it is not possible to extract the frequency values and only the complex value is given.

		STF	NTF	RSTF
Zeros	Z-value	$\{\varnothing\}$	$\left\{-j^{(2)}, j^{(2)}\right\}$	$\left\{\pm j, \pm(a_2-1)^{1/2}\right\}$
	Equivalent frequencies	$\{\varnothing\}$	$\left\{-\frac{F_s}{4}{}^{(2)}, \frac{F_s}{4}{}^{(2)}\right\}$	If $a_2 < 1$ $\left\{-\frac{F_s}{4}{}^{(2)}, \frac{F_s}{4}{}^{(2)}\right\}$ If $a_2 \geq 1$ $\left\{0^{(2)}, -\frac{F_s}{4}, \frac{F_s}{4}\right\}$
Poles (Z-value)		$\left\{\pm\left(\frac{a_2-2\pm(a_2(a_2-4a_1))^{1/2}}{2}\right)^{1/2}\right\}$		

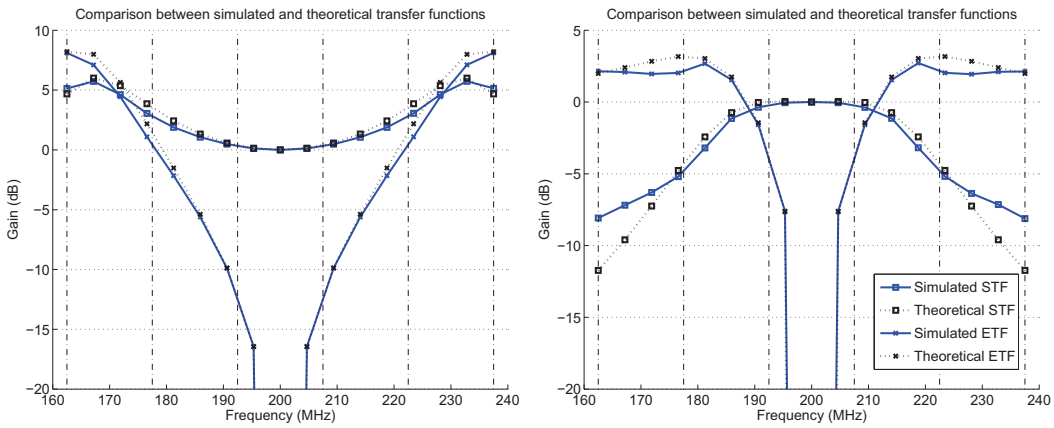
Table III.1: Theoretical zeros and poles of each transfer function

The first observation is that these transfer functions have all the same poles. Therefore,

their frequency responses tend to be at their maximum level around the same frequencies. Secondly, the RSTF has at least two notches at the frequencies $\pm F_s/4$: depending on a_2, it can have two notches (each of order 2) or three notches: one at DC (order 2), one at $F_s/4$ and the other at $-F_s/4$ [1].
These notches will attenuate the signals that are around the frequencies $\pm F_s/4$.

III.1.5.2 Simulation results

The $\Sigma\Delta$ modulator depicted in Figure III.7 has been simulated for a frequency sampling of $F_s = 800$MHz with the sets of coefficients $\{a_1 = 0.5,\ a_2 = 0.5\}$ and $\{a_1 = 0.18,\ a_2 = 0.4\}$ with a 3-bit quantizer (so that the quantizer gain can be approximated to 1).



(a) $\{a_1 = 0.5,\ a_2 = 0.5\}$ (b) $\{a_1 = 0.18,\ a_2 = 0.4\}$

Figure III.8: Comparison between simulated and theoretical transfer functions

Figure III.8 shows the STF (output of the modulator) and the RSTF (first subtrator) for both the theoretical and simulated cases [2]. Vertical dash-dot lines show the delimitations of bands 15MHz wide.
We can notice that simulated and theoretical results are almost identical. The difference comes from that the actual gain of the quantizer is not always equal to one, even for a 3-bit quantizer. In our case, this difference vanishes when the quantizer resolution is greater than 3 bits.
As a_1 and a_2 are numerically valued, we can now calculate the values of zeros and poles and extract the equivalent frequencies.
Table III.2 gives these theoretical numerical values of zeros and poles for the case

[1] But this 3-notches case should not occur since we should have $a_2 < 1$ because of stability issues
[2] The simulated points have been obtained with several simulations sweeping the frequency of the input signal and calculating the power of the sine in the output with a DFT.

$\{a_1 = 0.5,\, a_2 = 0.5\}$. As expected, the RSTF shows a notch at $F_s/4$ and both transfer functions have their maximum gain at $5/24F_s \approx 167$ MHz and $7/24F_s \approx 233$ MHz.

		STF	NTF	RSTF
Zeros	Z-value	$\{\varnothing\}$	$\left\{-j^{(2)}, j^{(2)}\right\}$	$\left\{\pm j, \pm\frac{j}{\sqrt{2}}\right\}$
	Equivalent frequencies	$\{\varnothing\}$	$\left\{-\frac{F_s}{4}^{(2)}, \frac{F_s}{4}^{(2)}\right\}$	$\left\{-\frac{F_s}{4}^{(2)}, \frac{F_s}{4}^{(2)}\right\}$
Poles	Z-value	$\left\{\pm\left(\frac{\sqrt{3}}{2}\right)^{1/2} e^{j\frac{5}{12}\pi}, \pm\left(\frac{\sqrt{3}}{2}\right)^{1/2} e^{-j\frac{5}{12}\pi}\right\}$		
	Equivalent frequencies	$\left\{\pm\frac{5}{24}F_s, \pm\frac{7}{24}F_s\right\}$		

Table III.2: Theoretical zeros and poles values for $\{a_1 = 0.5,\, a_2 = 0.5\}$

For the case $\{a_1 = 0.18,\, a_2 = 0.4\}$ the equivalent frequencies of the poles are:

$$\pm\frac{1}{4\pi}\left(\arctan(2\sqrt{5}) + \frac{\pi}{2}\right) F_s \approx \pm\,186\text{MHz} \tag{III.7}$$

$$\pm\left(\frac{1}{4\pi}\left(\arctan(2\sqrt{5}) + \frac{\pi}{2}\right) - \frac{1}{2}\right) F_s \approx \pm\,214\text{MHz} \tag{III.8}$$

We have good agreement for the theoretical frequencies of the RSTF and the observed frequency response.

III.1.5.3 Performance analysis

In this section, we study the performance of filtering performed by the RSTF in these examples in relation to the expected performance. We consider the signal defined in § III.1.1.1 consisting of white signals in bands of 15MHz. In addition, we assume that a single-bit quantizer is used and despite some minor differences, the transfer functions are those performed by the modulator.
Using the expressions of STF, NTF and RSTF, we can estimate the average power of the signal and noise in each band of the modulator and subtractor output. Indeed, the power spectral density (PSD) of the signal, filtered by the STF, in the output of the modulator is:

$$PSD_{X,Y}(\nu) = PSD_X(\nu) \times |STF(\nu)|^2 \tag{III.9}$$

The PSD of the shaped noise is:

$$PSD_{N,Y}(\nu) = PSD_N(\nu) \times |NTF(\nu)|^2 \tag{III.10}$$

And the PSD of the signal in the output of the subtractor is:

$$PSD_{X,U}(\nu) = PSD_X(\nu) \times |RSTF(\nu)|^2 \tag{III.11}$$

The PSD [1] of the input signal, assuming a normalized power of 1 in the main band, is:

$$PSD_X(\nu) = \begin{cases} 1/BW & \text{if } \nu \in F_c + \left[-\frac{BW}{2}; \frac{BW}{2}\right] \\ 10^{-6}/BW & \text{if } \nu \in (F_c \pm BW) + \left[-\frac{BW}{2}; \frac{BW}{2}\right] \\ 10^{-7}/BW & \text{if } \nu \in (F_c \pm 2\times BW) + \left[-\frac{BW}{2}; \frac{BW}{2}\right] \end{cases} \tag{III.12}$$

[1] Assumed to be expressed in W/Hz

To calculate the noise PSD, we assume that the voltage references are also normalized to 1 ($x_{max} = 1$):

$$PSD_N(\nu) = \frac{q^2}{12F_s} \text{ with } q^2 = \frac{2}{2^{Nb}} = 1 \text{ since } Nb = 1 \text{ bit} \tag{III.13}$$

The normalization of both the power in the main band and the quantizer references may be questionable and we clarify the approach we take here in this analysis of calculated powers. The values we computed in the following tables are not to be taken as absolute values. Here we will only compare the ability of the RSTF to remove the main band and not to modify the adjacent bands. Therefore, we will only compare the signal, band to band or at the subtraction point and the output of the modulator. Eventually, the choice of normalizing x_max has the vocation to assign a numerical value to the noise power. We could have drawn almost the same conclusions without having to calculate the noise power in the band. However, this value can be used to illustrate the phenomenon that has been verified subsequently, during time simulations, which is, for a low resolution quantizer, the low-power signal is hidden in the noise. So we know here that the SNR is valid in the order of magnitude.

Table III.3 and Table III.4 show the synthesis of these calculations.

	Principal Band (dB)		1st Adjacent Band (dB)		Following Adjacent Band (dB)	
	Subtractor Output	Modulator Output	Subtractor Output	Modulator Output	Subtractor Output	Modulator Output
Signal Power after Filtering	-17	0	-63	-58	-63	-65
Noise Power after Shaping	-54		-31		-17	
SNR	37	54	-32	-27	-46	-48

Table III.3: Signal and Noise power in each band for the case $\{a_1 = 0.5, a_2 = 0.5\}$

	Principal Band (dB)		1st Adjacent Band (dB)		Following Adjacent Band (dB)	
	Subtractor Output	Modulator Output	Subtractor Output	Modulator Output	Subtractor Output	Modulator Output
Signal Power after Filtering	-8	0	-58	-61	-67	-78
Noise Power after Shaping	-43		-25		-21	
SNR	35	43	-33	-36	-46	-57

Table III.4: Signal and Noise power in each band for the case $\{a_1 = 0.18, a_2 = 0.4\}$

First observe Table III.3 and the row giving the powers of the signal after filtering. The *Subtractor Output* column and the *Modulator Output* column are respectively the result after filtering by the RSTF and the STF.
We note that in the subtractor output, the signal will be effectively reduced in the main band (-17dB instead of the original 0dB). In the adjacent band, it will be somewhat attenuated (reduction by 3dB) and in the next band, it will be amplified (increased by 7dB).
These values can be found very roughly by observing the frequency response of the RSTF Figure III.8a.
It becomes apparent that in this case, the attenuation of the main band is too low (it should be at least 60dB) and adjacent bands should not be attenuated or should be amplified more strongly.

In the second case $\{a_1 = 0.18, a_2 = 0.4\}$, we test a configuration where the poles are placed such that adjacent bands should not be attenuated. This is verified in Table III.4 (-58dB and -67dB). Unfortunately (unsurprisingly) the attenuation of the main band is even lower (-8dB). We need to increase the filter order to improve this parameter.

Designed ideal RSTF

We propose to estimate the order of the RSTF filter necessary to meet our filtering needs. We consider the following filter specification shown in Figure III.9 that can be deduced directly from the composition of the assumed signal:

$$\begin{aligned} A_{stop} &= 60\text{dB} \\ A_{ripple} &= 1\text{dB} \\ f_{pass1} &= 191\text{MHz} \\ f_{stop1} &= 194\text{MHz} \\ f_{pass2} &= 206\text{MHz} \\ f_{stop2} &= 209\text{MHz} \\ F_s &= 800\text{MHz} \end{aligned}$$

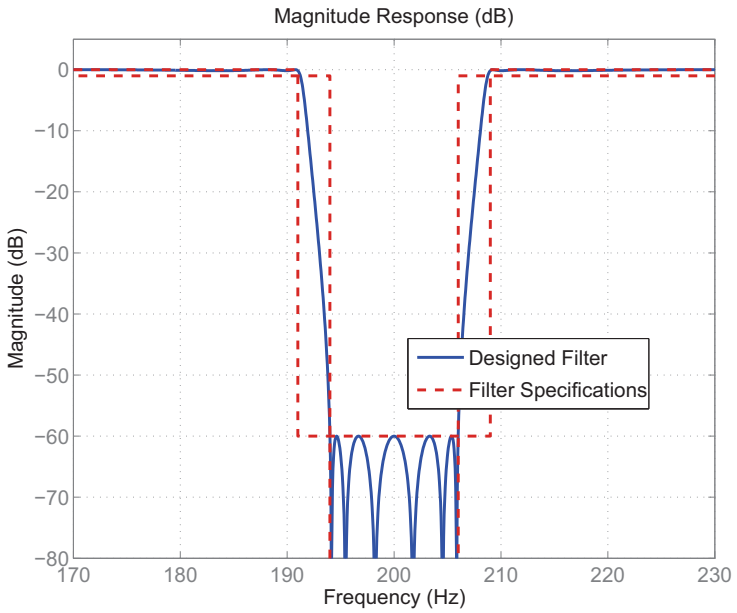


Figure III.9: Frequency response of the designed RSTF (12th order)

The best case minimum order is 12 (Elliptic approximation):

$$RSTF^{\text{design}}(z) = \frac{0.7558+4.5241z^{-2}+11.2941z^{-4}+15.0516z^{-6}+11.2941z^{-8}+4.5241z^{-10}+0.7558z^{-12}}{1+5.4614z^{-2}+12.4677z^{-4}+15.2272z^{-6}+10.4934z^{-8}+3.8687z^{-10}+0.5963z^{-22}} \quad \text{(III.14)}$$

Assuming the modulator structure shown in Figure III.10:

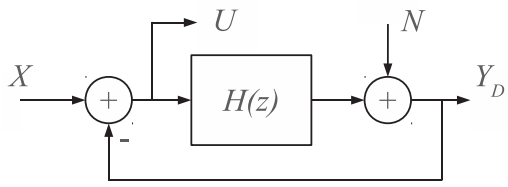


Figure III.10: Simplified ΣΔ modulator model

we can derive:

$$STF^{\text{design}}(z) = 1 - RSTF^{design}(z) = \frac{0.2442+0.9373z^{-2}+1.1736z^{-4}+0.1756z^{-6}-0.8007z^{-8}-0.6554z^{-10}-0.1596z^{-12}}{1+5.4614z^{-2}+12.4677z^{-4}+15.2272z^{-6}+10.4934z^{-8}+3.8687z^{-10}+0.5963z^{-12}} \quad \text{(III.15)}$$

$$NTF^{\text{design}}(z) = RSTF^{\text{design}}(z) = \frac{0.7558+4.5241z^{-2}+11.2941z^{-4}+15.0516z^{-6}+11.2941z^{-8}+4.5241z^{-10}+0.7558z^{-12}}{1+5.4614z^{-2}+12.4677z^{-4}+15.2272z^{-6}+10.4934z^{-8}+3.8687z^{-10}+0.5963z^{-22}} \quad \text{(III.16)}$$

Figure III.11 shows the frequency responses of these filters.

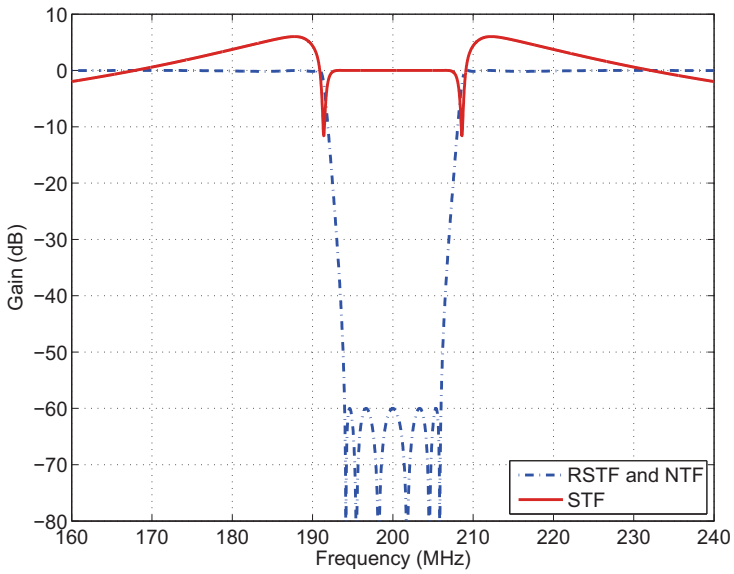


Figure III.11: STF and NTF frequency responses in the case of a designed RSTF

In addition, Table III.5 shows the synthesis of calculations of powers for each band:
We note the principal band is attenuated by 35dB, that is better than the previous cases but it is not sufficient. Although the adjacent bands are not affected, this filter configuration is still to low.

	Principal Band (dB)		1st Adjacent Band (dB)		Following Adjacent Band (dB)	
	Subtractor Output	Modulator Output	Subtractor Output	Modulator Output	Subtractor Output	Modulator Output
Signal Power after Filtering	-35	0	-60	-56	-70	-69
Noise Power after Shaping	-57		-22		-22	
SNR	22	57	-38	-34	-48	-47

Table III.5: Signal and Noise power in each band for the case of a designed RSTF

Moreover, for all the three cases, the noise power is much larger than the signal in the adjacent bands are hidden in it (all the SNR are negative). Let us make a little infringement to the introduction remark about the absolute values of SNR. Suppose the value of SNR in the latter case is valid (-38dB). For example, for the latter case, we should use a 10-bit quantizer [1] in order to provide to the secondary modulators, the required SNR on the adjacent bands [2].
Finally, except for the second case, the adjacent bands SNRs are better at the output of the modulator than at the subtrator output.

This detailed analysis highlights three main points:

- We validated the principle of RSTF and we can calculate this transfer function precisely from the architecture (provided a sufficiently large number of bits)
- However, the RSTF is not able to attenuate the principal band only without demanding large circuit resources.
- And the shaped quantization noise is also usually larger than the useful signal in the adjacent bands and here, for example, a 10-bit quantizer would required to provide 20dB SNR on the first adjacent band (8-bit actually) [3]. This would also largely increase circuit resources.

Therefore, we decided to focus on the digitization of the shaped noise instead of the filtered signal. The interest is two fold:

- The RSTF is not required to be a high order band-stop filter and should only provide sufficient attenuation on the input signal.
- The shaped noise appears naturally larger than the signal in the adjacent bands.

III.2 Noise band digitization and cancellation

Figure III.12 shows the conceptual diagram of the new architecture.

[1] Here we have -38dB SNR and we used a mono-bit quantizer ; in order to have a 20dB SNR we should reduce the noise by 58dB that corresponds to 9 more bits

[2] (✠) In the final simulations (Figure III.16, page 119 and Figure III.41, page 137) we can observe that the SNR is -14 dB in the adjacent band for a 2-bit quantizer which would require a quantizer of 8 bits in total to achieve 20dB SNR in the adjacent band at the subtraction point

[3] See footnote (✠)

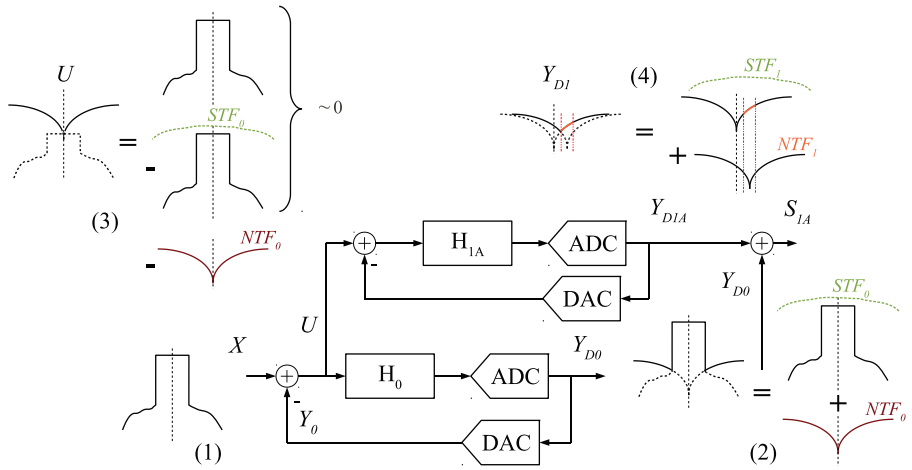


Figure III.12: Diagram for an intuitive explanation of the new architecture of noise digitization

Again, we introduce the operation of the new architecture with a (not rigorous) annotated diagram. The signal (1) is identical to that of Figure III.5. The output of the first modulator (2) has been corrected since the STF modulators are typically approximately flat over a wide band around the operating band. In light of the conclusions of the previous part we have also updated the signal representation in (3). Indeed, if the primary STF does not distort the signal too much, then the initial part of the signal is fully attenuated and there remains only the shaped quantization noise (with a negative coefficient). This quantization noise is in turn digitized on the adjacent band by the secondary modulator. Its output (4) is then made of the noise to digitize, added to the inherent shaped noise of the secondary modulator. By adding the two signals, if the secondary STF does not distort the signal too much, we remove the common parts of (4) and (2), i.e. the quantization noise of the primary modulator in the adjacent band since (4) contains a negative version. This mechanism is illustrated in Figure III.13.

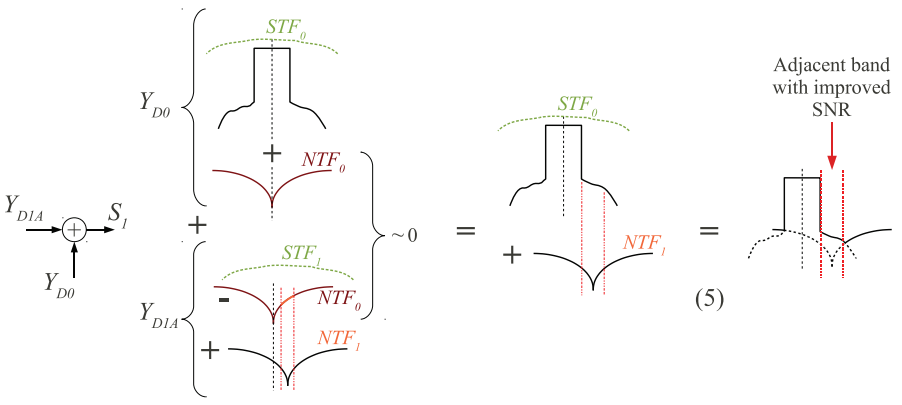


Figure III.13: Intuitive explanation of the noise cancellation in the digital part

Finally, we have to select the adjacent band with a digital filter to only get the adjacent band with improved resolution.

III.2.1 Linear model analysis

Figure III.14 shows a general diagram of this architecture that we refer to as Multi-Stage Noise Band Cancellation Architecture (MSNBC).

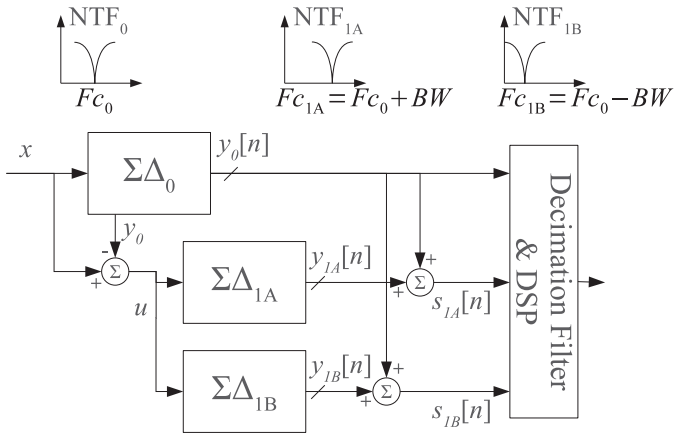


Figure III.14: The MSNBC ΣΔ architecture

The primary modulator $\Sigma\Delta_0$ is centered around the frequency Fc_0. It digitizes the signal x and its analog fed back output is subtracted to its input, generating the signal denoted u. This signal is processed by secondary modulators $\Sigma\Delta_{nX}$ and under a condition [1] we add directly the digital outputs of the secondary modulators to the primary output, generating the signals s_{nX}.

Now we derive the linear model equations of the architecture that provide the formal justification of the operation of the system.
According to the linear model of ΣΔ modulators, the Z-transform Y_{1A} of the output y_{1A} of the modulator $\Sigma\Delta_{1A}$ is given by:

$$Y_{1A}(z) = U(z)STF_{1A}(z) + N_{1A}(z)NTF_{1A}(z) \tag{III.17}$$

Expanding U with Equation (III.1), we get:

$$\begin{aligned} Y_{1A}(z) = {} & STF_{1A}(z)\left(X(z)\,RSTF(z) - N_0(z)\,NTF_0(z)\right) \\ & + N_{1A}(z)\,NTF_{1A}(z) \end{aligned} \tag{III.18}$$

So S_{1A}, the Z-transform of the signal s_{1A}, is:

$$\begin{aligned} S_{1A}(z) = {} & X(z)\left(STF_0(z) + STF_{1A}(z)\,RSTF(z)\right) \\ & + N_0(z)\,NTF_0(z)\left(1 - STF_{1A}(z)\right) \\ & + N_{1A}(z)NTF_{1A}(z) \end{aligned} \tag{III.19}$$

As previously mentioned, we assume here that all the STF are equal to 1 so that distortions from filtering are avoided. Therefore, the RSTF vanishes and Equation (III.19) becomes:

$$S_{1A|STF_i=1}(z) = X(z) + N_{1A}(z)\,NTF_{1A}(z) \tag{III.20}$$

This equation shows that adding the output of the primary modulator to the output of secondary modulators cancels out the noise of the primary modulator and replaces it by the noise of the secondary. Then, the signal in the adjacent band can be selected using a digital signal processing as if one had used a dedicated ΣΔM but without the use of an analog filter.

[1] $STF_{nX} = 1$

III.2.2 Simulation results

To validate the operating principle of the overall architecture, we simulate the whole system using an input signal consisting of two sinusoids (see § III.1.1.1).
We synthesized two CRFB [1] ΣΔM clocked at F_s = 800MHz, each having a 2-bit quantizer, using the MATLAB Delta-Sigma Toolbox [11]. Both modulators are 4th order and their zeros are optimized for the center frequencies F_{c0}=160MHz and F_{c1A}=175MHz (1st adjacent band). The bandwidth of each modulator is BW=15MHz and their feed-in coefficients are set so that the implemented STF are equal to 1. This can be done setting these coefficients to the same value as the feedback coefficients and the feed-in coefficient before the quantizer to 1.
A detailed view of the simulated system is shown in Figure III.15. The system was simu-

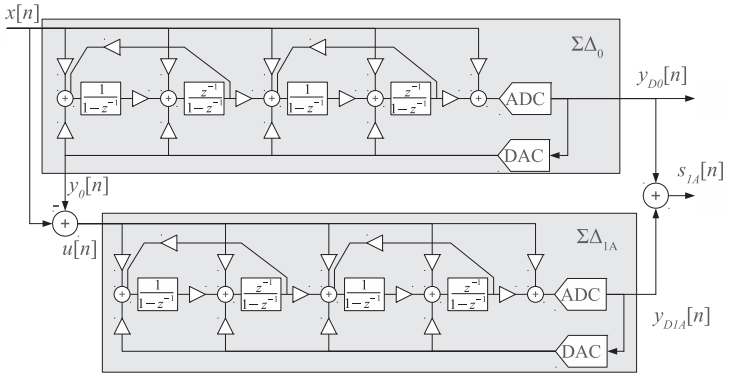


Figure III.15: Simulated system for architecture validation (4th order CRFB modulators)

lated with an input made up of a high power sinusoid in the central band and a 60dB lower sinusoid in the adjacent band as shown in Figure III.16(a). This input signal simulates the high dynamic range characteristics of a distorted output PA signal and makes possible the calculation of SNR with the power spectral density of the signal. Figure III.16(b) shows the output signal spectrum of the primary ΣΔM and the low power signal is almost hidden by the shaped quantization noise. The high power signal can be digitized by the primary ΣΔM as the SNR in the central band is 68dB. And the SNR of the low power signal in the adjacent band is very low (-14dB) only due to the fact that the primary ΣΔM has been designed to digitize the central band.
Figure III.16(c) shows the spectrum of the signal U. It illustrates the actual quasi-suppression of the input signal and the fact that this signal is almost the shaped noise only. We notice a residue of the input high power sinusoid. In real circuits, this residue is expected to be even higher since the subtraction will be affected by non-idealities. However, here, we impute this residue to small mismatches due to rounding in numerical simulations.
In Figure III.16(d) we can see the low power signal that now emerges from the noise and its SNR is 9dB.

We can note that the SNR in the principal band meets the requirements, but the SNR in the adjacent band is too low. We will see in Section III.3.3.2 that increasing the order of the secondary modulator (to a 6th order) provides sufficient SNR in the adjacent band.

[1] cascade-of-resonators feedback form Section II.1.2.3

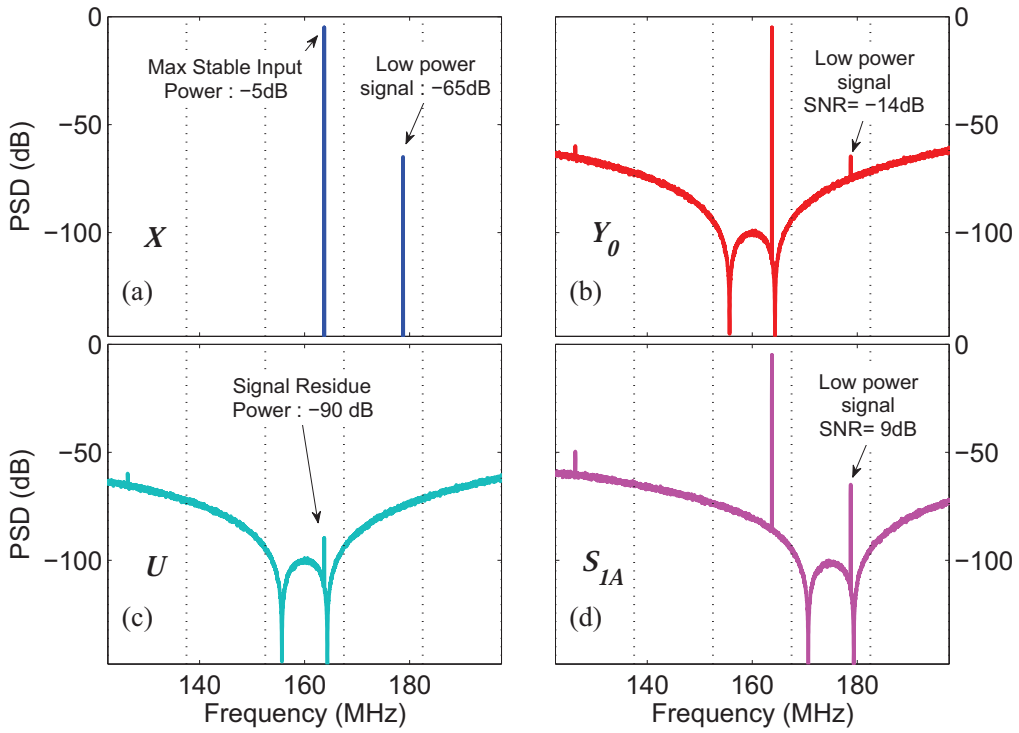


Figure III.16: Simulated output spectra of the architecture

III.2.3 General case formulation

All along the previous parts, we assumed and simulated modulators with $STF = 1$. However, this not always the case as illustrated by the example in § III.1.5 and it is particularly true for CT systems.

In order to obtain the right noise suppression we will have to process the output of each modulator. This is performed by Noise Cancellation Filters (NCF). The Figure III.17 shows the structure of the General MSNBC architecture.

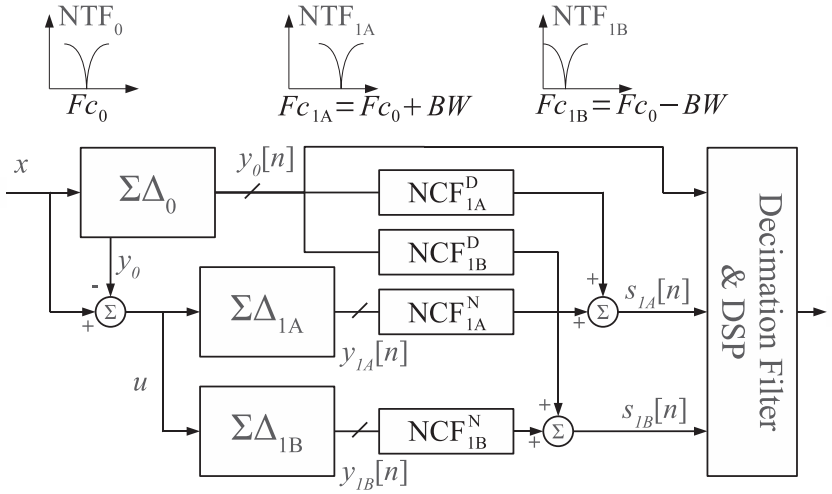


Figure III.17: The general MSNBC Architecture

To clarify the problem discussed here, we must separate the action of the STF of each

modulator. Indeed, in this paragraph, the added processing to the system only affects the action of the secondary modulator — the secondary STF. It affects the signal U — the quantization noise — which should be removed with the addition, regardless of the STF of the primary modulator.
However, the primary STF is also important but is secondary in this paragraph because it plays another role: it impacts the signal suppression in U. On account of that we want to attenuate the signal in U and digitize the quantization noise by the secondary modulator, we have a strong interest in this primary STF to be unitary.

III.2.3.1 NCF calculation in the general DT case

In the general DT case, all the signals are assumed to be sampled. Figure III.18 shows the fundamental structure of the architecture.

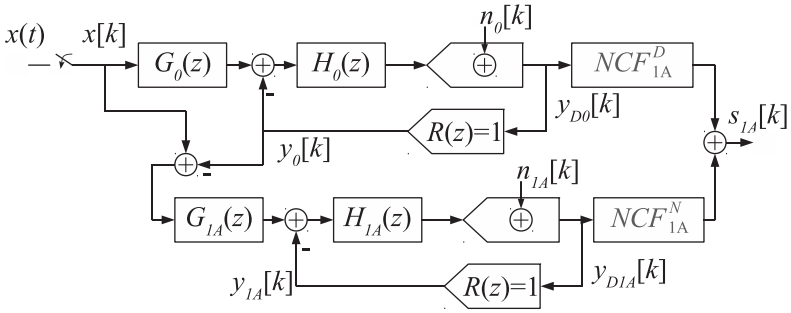


Figure III.18: The general DT MSNBC Architecture

We can write the Z-transform Y_{1A} of the output y_{1A} of the modulator $\Sigma\Delta_{1A}$:

$$Y_{1A}(z) = STF_{1A}(z)\left(X(z)\,RSTF(z) - N_0(z)\,NTF_0(z)\right) + N_{1A}(z)\,NTF_{1A}(z) \tag{III.21}$$

So S_{1A}, the Z-transform of the signal s_{1A}, is:

$$S_{1A} = NCF^D_{1A}(z)\cdot Y_0(z) + NCF^N_{1A}(z)\cdot Y_{1A}(z) \tag{III.22}$$

Expanding the expression of $Y_{1A}(z)$:

$$\begin{aligned} S_{1A} = X(z)\left(NCF^D_{1A}(z)\cdot STF_0(z) + NCF^N_{1A}(z)\cdot RSTF(z)\cdot STF_{1A}(z)\right) \\ + NTF_0(z)\cdot N_0(z)\left(NCF^D_{1A}(z) - NCF^N_{1A}(z)STF_{1A}(z)\right) \\ + NCF^N_{1A}(z)\cdot NTF_{1A}(z)\cdot N_{1A}(z) \end{aligned} \tag{III.23}$$

We deduce from Equation (III.23) that the term affecting $N_0(z)$ vanishes if:

$$\frac{NCF^N_{1A}(z)}{NCF^D_{1A}(z)} = \frac{1}{STF_{1A}(z)} \tag{III.24}$$

We define:

$$NCF^N_{1A}(z) = \text{Numerator}\left(\frac{1}{STF_{1A}(z)}\right) \tag{III.25}$$

$$NCF^D_{1A}(z) = \text{Denominator}\left(\frac{1}{STF_{1A}(z)}\right) \tag{III.26}$$

so that NCF are FIR filters that ensures stability of filtering.
As previously mentioned, we can note here that the STF of the primary modulator has no effect on the noise suppression as NCF expressions depend only on the STF of the secondary modulator.

Example

We provide here the derivation of the NCF for the same configuration as Section III.2.2 but the secondary modulator is modified so that its STF is not 1. To achieve this, one has to set to 0 all the feed-in coefficients except the first one (i.e. $b_i = 0$, $i \in [2 : N^{\Sigma\Delta} + 1]$). Figure III.19 shows the detailed structure of the simulated system.

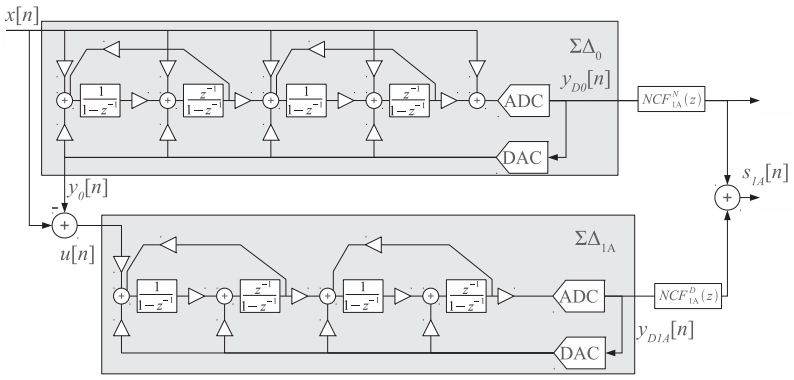
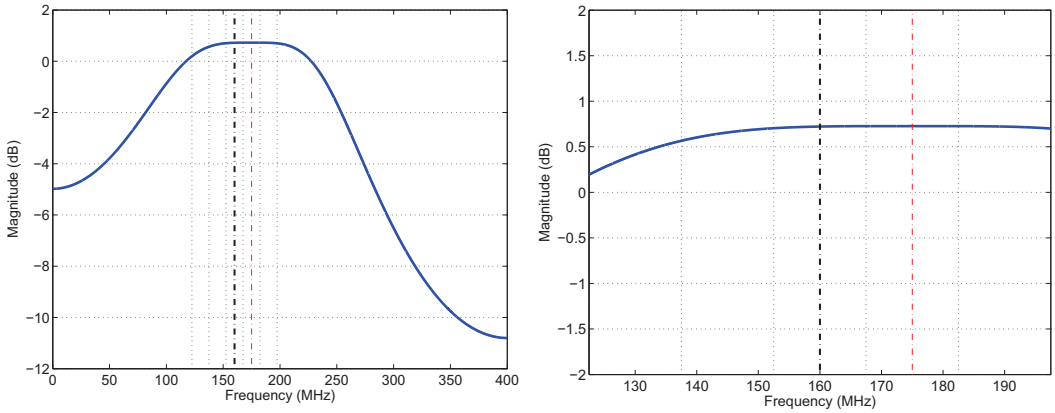


Figure III.19: Detailed diagram of the simulated system with the secondary STF non-unitary

In this example, the secondary STF is:

$$STF_{1A}(z) = \frac{-0.6582z^{-2}}{1 - 0.3827z^{-1} + 0.5769z^{-2} - 0.1749z^{-3} + 0.1485z^{-4}} \tag{III.27}$$

and its frequency response is shown in Figure III.20a and Figure III.20b.



(a) Overview

(b) Detailed view centered on the principal band

Figure III.20: Frequency response of the STF of the secondary modulator

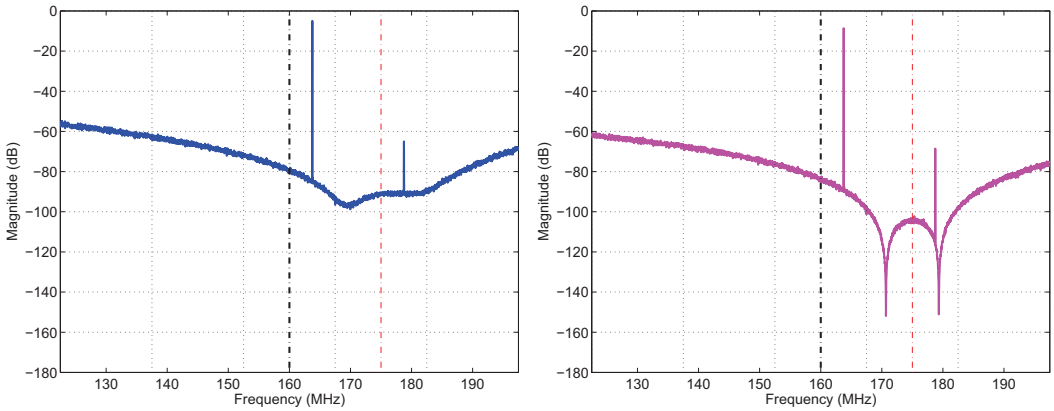
Vertical dot lines show the limits of the considered bands. The bold black dash-dot line shows the center $F_c = 160$MHz of the principal band and the thin red one shows the center $F_{Adj} = 175$MHz of the adjacent band of interest. The secondary STF exhibits a non-selective band-pass characteristic: it is somewhat flat (the gain of the flat region is 0.73dB) for 75MHz centered around F_{Adj} and attenuates the other frequencies with a maximum attenuation of 10.8dB at $F_s/2$.

We deduce from the theoretical section the noise cancellation filters:

$$NCF_{1A}^{N}(z) = 1 - 0.3827z^{-1} + 0.5769z^{-2} - 0.1749z^{-3} + 0.1485z^{-4} \quad \text{(III.28)}$$

$$NCF_{1A}^{D}(z) = -0.6582z^{-2} \quad \text{(III.29)}$$

Figure III.21a shows the spectrum resulting from the direct addition of y_{D1A} and y_0. It shows poor (non optimal) noise suppression and the SNR in the adjacent band is approximately 2dB. Figure III.21b shows the output spectrum of the general structure using the noise cancellation filters. The noise suppression is the same as the unitary STF case and the SNR is also 9dB.



(a) Unfiltered outputs added directly (b) Filtered outputs before addition

Figure III.21: Output spectrum of s_{1A}

III.2.3.2 NCF calculation in the general CT case

In the general CT case, the input signal x, the feedback y_0 and the signal u are continuous-time. Figure III.22 details the structure of the fundamental part of the general CT MSNBC architecture.

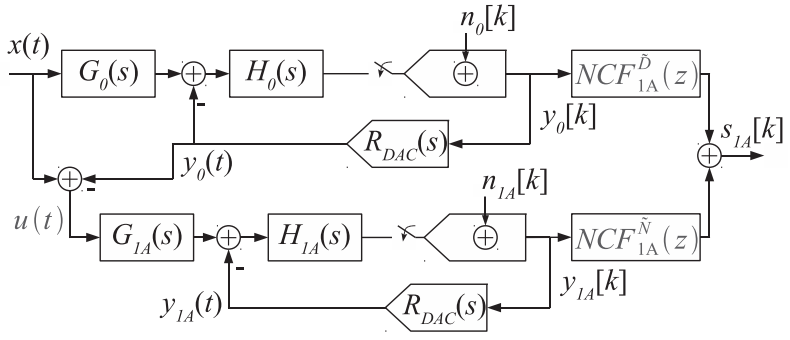


Figure III.22: The general CT MSNBC Architecture

Similarly to the previous chapter, we derive the NCF filters writing the expressions of

$Y_0(z)$, $Y_{1A}(z)$ and $S_{1A}(z)$:

$$Y_0(z) = \frac{1}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_0(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} N_0(z) + \frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_0(s)G_0(s)X(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_0(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} \tag{III.30}$$

$$Y_{1A}(z) = \frac{1}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} N_{1A}(z) + \frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)G_{1A}(s)U(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} \tag{III.31}$$

$$U(s) = X(s) - \mathcal{R}_{DAC}(s)\cdot\mathcal{L}\left\langle y_{0[k]}\right\rangle(s) \tag{III.32}$$

$$S_{1A}(z) = NCF_{1A}^{\tilde{D}}(z)\cdot Y_0(z) + NCF_{1A}^{\tilde{N}}(z)\cdot Y_{1A}(z) \tag{III.33}$$

We can show that the term affecting $N_0(z)$ in $S_{1A}(z)$ vanishes when:

$$\frac{NCF_{1A}^{\tilde{N}}(z)}{NCF_{1A}^{\tilde{D}}(z)} = \frac{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)G_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} \tag{III.34}$$

Again, we define:

$$NCF_{1A}^{\tilde{N}}(z) = \text{Numerator}\left(\frac{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)G_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}\right) \tag{III.35}$$

$$NCF_{1A}^{\tilde{D}}(z) = \text{Denominator}\left(\frac{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)G_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}\right) \tag{III.36}$$

so that the noise cancellation filters are FIR filters and that ensures the stability of filtering on each channel.

Example

We also simulated a CT system were noise cancellation filters are needed. The Figure III.23 depicts the simulated system. It is very similar to the diagram shown in § III.2.3.1, however all the integrators are continuous-time and the coefficients are, *a priori*, different. Besides, these coefficients are computed from the DT NTF of the § III.2.3.1 using a DT-CT transform (Impulse Invariance Response) given that NRZ DACs will be used. The feed-in coefficients of the primary modulator are set so that its estimated STF is approximately 1 in order to provide good signal suppression. As shown in the diagram, the feed-in coefficients of the secondary modulator are set to 0 (except the first one) (i.e. $\beta_i = 0$, $i \in \left[2 : N^{\Sigma\Delta}+1\right]$).

In this case we have:

$$H_{1A}(s) = \frac{0.759s^3 - 0.4803s^2 + 1.114s - 1.624}{s^4 + 3.781s^2 + 3.564} \tag{III.37}$$

$$H_{1A}(s)G_{1A}(s) = \frac{-0.6717}{s^4 + 3.781s^2 + 3.564} \tag{III.38}$$

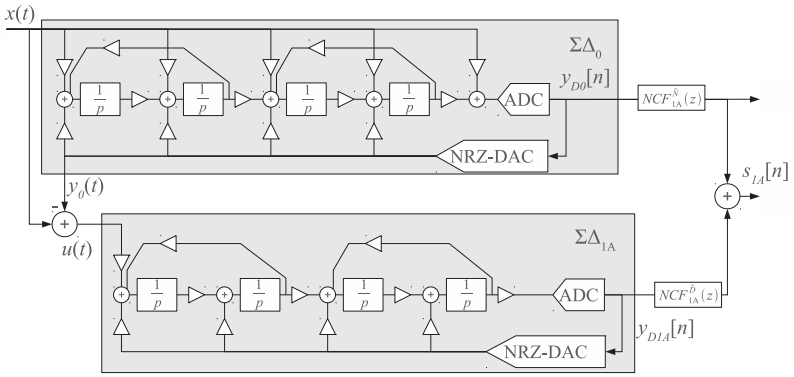
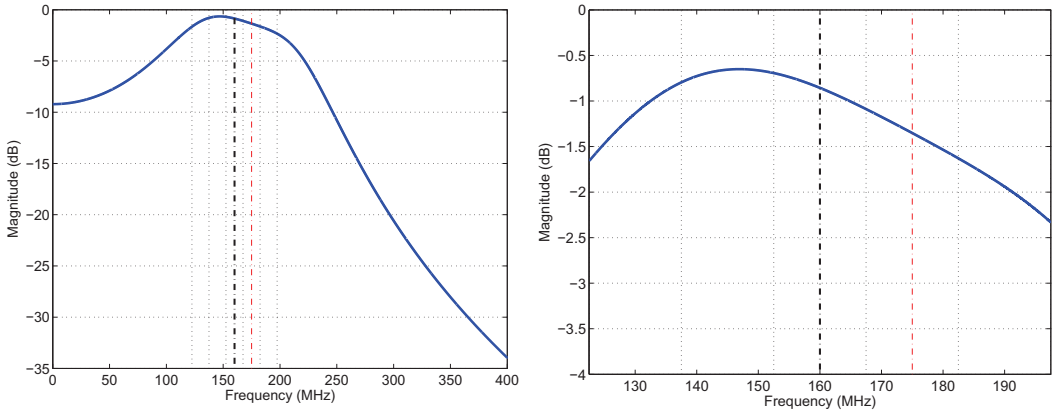


Figure III.23: Detailed diagram of the simulated system with a non-unitary secondary STF for a continuous-time implementation

And an approximation of the secondary modulator STF is given by [62]

$$\begin{aligned} STF_{1A} &\approx \frac{H_{1A}(j\omega)G_{1A}(j\omega)}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]_{|z=\mathrm{e}^{j\omega T_S}}} \\ &= \frac{-0.6717}{(j\omega)^4+3.781(j\omega)^2+3.564} \\ &\times \frac{1-0.7799\ \mathrm{e}^{-j\omega T_S}+2.148\ \mathrm{e}^{-2j\omega T_S}-0.7799\ \mathrm{e}^{-3j\omega T_S}+\mathrm{e}^{-4j\omega T_S}}{1-0.5133\ \mathrm{e}^{-j\omega T_S}+0.9346\ \mathrm{e}^{-2j\omega T_S}-0.2845\ \mathrm{e}^{-3j\omega T_S}+0.2716\ \mathrm{e}^{-4j\omega T_S}} \end{aligned} \tag{III.39}$$

Figure III.24a and Figure III.24b show the frequency response of the transfer function in Equation (III.39) with the same annotations as in § III.2.3.1.



(a) Overview

(b) Detailed view centered on the principal band

Figure III.24: Frequency response of the estimated STF of the secondary modulator

The secondary STF exhibits, in this case also, a non-selective band-pass characteristic. But its gain is not flat at all: there is a maximum around 146MHz with −0.65dB and attenuates the other frequencies with a maximum attenuation of 34dB at $F_s/2$. Thus, here, the signal will experience attenuation.

Using the impulse-invariant transformation [1], we derive:

$$\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)G_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right] = \frac{-0.02463z^3 - 0.2192z^2 - 0.2192z - 0.02463}{z^4 - 0.7799z^3 + 2.148z^2 - 0.7799z + 1} \tag{III.40}$$

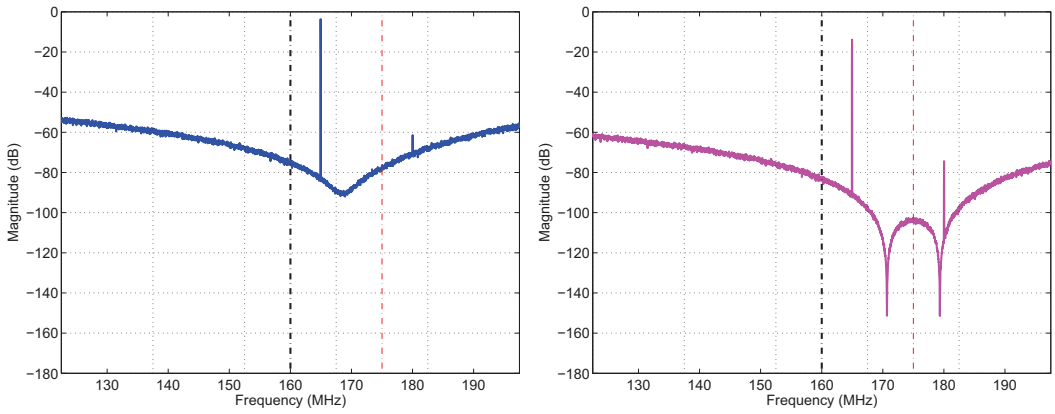
$$1 + \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right] = \frac{z^4 - 0.5133z^3 + 0.9346z^2 - 0.2845z + 0.2716}{z^4 - 0.7799z^3 + 2.148z^2 - 0.7799z + 1} \tag{III.41}$$

Then:

$$NCF_{1A}^{\tilde{N}}(z) = 1 - 0.5133z^{-1} + 0.9346z^{-2} - 0.2845z^{-3} + 0.2716z^{-4} \tag{III.42}$$

$$NCF_{1A}^{\tilde{D}}(z) = -0.02463z^{-1} - 0.2192z^{-2} - 0.2192z^{-3} - 0.02463z^{-4} \tag{III.43}$$

Figure III.25a shows the spectrum of the output while no correction have been done and the noise suppression is not achieved. Figure III.25b shows the result using noise cancellation filters. The noise suppression is achieved, however, as anticipated by the frequency response of the STF, the signal has been attenuated and the SNR in the adjacent band is now 2dB. This value is lower than the expected one as the attenuation shown in by the estimate STF is about 1-2dB and we have not yet identified the source of the additional attenuation.



(a) Unfiltered outputs added directly (b) Filtered outputs before addition

Figure III.25: Output spectrum of s_{1A} in the continuous-time case

[1] implemented in MATLAB using the `c2d(.,'zoh')` function

Particular case in CT system: NCF-less configuration
In CT implementation, the design of modulators so that NCF are not necessary is less obvious than in DT implementation. We show that in CT-CIFB architecture, if all the feed-in coefficients (except the one before the quantizer) are equal to the feedback coefficients (i.e. $\alpha_i = \beta_i,\ i \in \left[1 : N^{\Sigma\Delta}\right]$) and the remaining one set to one ($\beta_{N^{\Sigma\Delta}+1} = 1$), we have:

$$\frac{1 + \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_{1A}(s)G_{1A}(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} = 1 \tag{III.44}$$

This means no filtering is needed for the cancellation of the noise.
However, in this case, the *STF* is not unitary.

III.2.4 Conclusion

In this section we detailed the principle and the analysis of the noise band cancellation. This technique consists of digitizing the shaped noise of the primary modulator, using ΣΔ modulators centered on adjacent bands. Then, depending on the STF of the secondary modulator, the noise cancellation can be done either directly adding the output of the modulators or, using noise cancellation filters.
Some examples showed the achievable performances for a configuration composed of two 4th modulators using 2-bit quantizers. We have seen that the SNRs in the adjacent band were lower than the target performances and we need to increase either the order or the resolution of the quantizer of the secondary modulator.

III.3 High-level design methodology of the converter

We propose in this section a methodology for high-level design of a MSNBC converter. We start by discussing nonlinear phenomena observed by simulation in ΣΔ modulators centered at $F_s/4$ and this will have justified to change the center frequency modulators for the simulation of our converter. Then we propose an optimization methodology to maximize stability modulators as secondary channels may process signals of high amplitude occasionally. Finally, we present the results of intensive simulations to explore the design parameter space to show the influence of each parameter and select a configuration yielding the good performances.

III.3.1 Nonlinear effects in $F_s/4$ modulators

III.3.1.1 Noise power spectral density variance reduction

ΣΔ modulators are *noisy* systems that need to be simulated several times to extract their average characteristics. Figure III.26 shows the spectrum of the output of a modulator centered around $F_s/5$ [1] using a single realization of simulation and Figure III.27 shows the average spectrum of several realizations of simulations ($N_{realiz} = 100$) by changing on each realization, the initial phase of the sine wave input. If a calculation of the SNR is performed from the PSD of Figure III.26, the SNR may change ten percent or so, from one realization to another, and taking the average leads to a fixed estimate of the SNR. Moreover, harmonic distortions of the signal are easily discernible in Figure III.27 whereas they are mostly invisible in the first spectrum.

[1] This center frequency is chosen on purpose in order to avoid non linear phenomena as explained in the following section

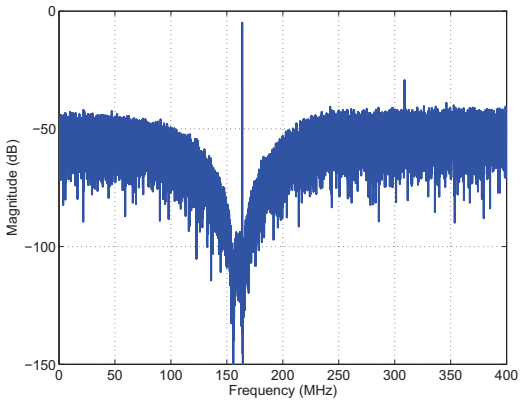


Figure III.26: One realization spectrum — High variance of the Noise PSD

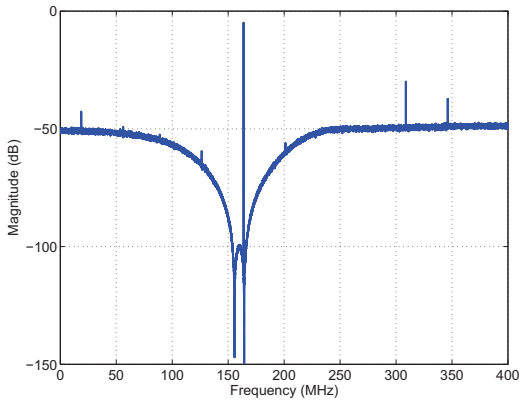


Figure III.27: Average spectrum over 100 realization — Low variance of the Noise PSD

To choose the number of realizations required to obtain near ideal average results with acceptable simulation time, we have here the possibility to simulate the system many times and plot the standard deviation of the averages over N_{realiz} realizations compared to the average over 500 realizations of a single point of the noise PSD Figure III.28.

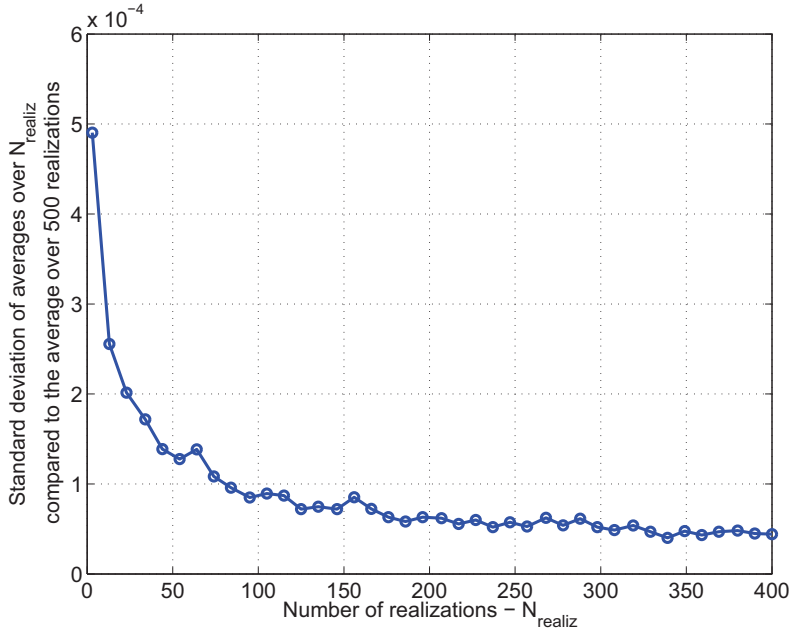


Figure III.28: Standard deviation of the empirical averages over N_{realiz} realizations compared to the empirical average over 500 realizations

We note that from $N_{realiz} = 100$, the error decreases with a low and constant rate. We therefore choose this value as a good trade-off between simulation time and accuracy. The simulation time required to run $N_{realiz} = 100$ simulations is 1s on our desktop computer [1]. Thus, the calculations of SNR and spectra are obtained from the average spectrum over

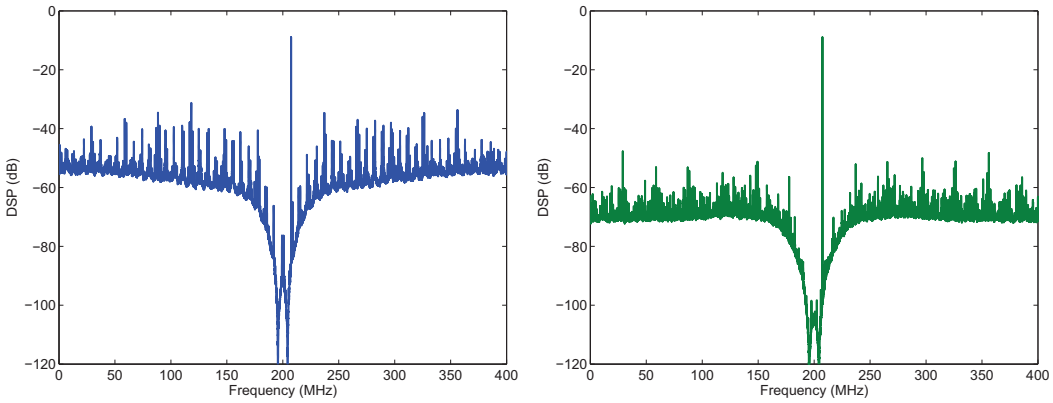
[1] 1: Intel Xeon Quad Core 2.67GHz, 4GB RAM

100 realizations, defined by:

$$PSD^{\text{average}}(\nu) = \frac{1}{N_{realiz}} \sum_{k=1}^{N_{realiz}} PSD^{\text{realization k}}(\nu) \tag{III.45}$$

III.3.1.2 Nonlinear Effects in $F_s/4$ modulators

Using the previous method, we observed large nonlinear effects in modulators centered around $F_s/4$; effects that are invisible when the spectra are not or little averaged. The observed nonlinear effect is the emergence of spurious signals in the output spectrum of the modulator. Figure III.29a and Figure III.29b show the phenomenon with the simulation of a 4-th order modulator with respectively 2-bit and 4-bit quantizer.



(a) 2-bit quantizer (b) 4-bit quantizer

Figure III.29: Nonlinear effects in $F_s/4$ modulators

As previously mentioned, the spectra were averaged over 100 realizations, indicating that the displayed spurious signals are not noise but rays resulting from deterministic periodic signals.
Then we implemented a simulation tool to vary the frequency and amplitude of the sinusoid and the resolution of the quantizer to try to analyze this nonlinear behavior. Figure III.30 shows the window of the tool.
We were able to verify that the spurious signals are not strictly dependent on the frequency and the amplitude of the signal which excludes generation by harmonic distortion.
When we detected this phenomenon, we did not have the certainty of its origin nor the means to fix it. However, we noticed that choosing a center frequency sufficiently far from $F_s/4$ the modulator loses the nonlinear behavior. This is illustrated in Figure III.31a and Figure III.31b where spurious signals are mainly harmonic distortions.

Thus, we chose to center the overall frequency converter such that the frequency band associated with the PA distortions of order 5 (highest band of frequencies) is digitized without these nonlinear phenomena, i.e. the associated modulator is centered on $F_{cIM5} = 190$MHz. This implies that the main band is centered on $F_c = 190 - 2 \times 15 = 160$MHz.

We know at the present time that these spurious signals are not the result of numerical phenomena caused by computer simulation, but they indeed come from the dynamics of the modulator. These spectral rays result from the establishment of cycles in the modula-

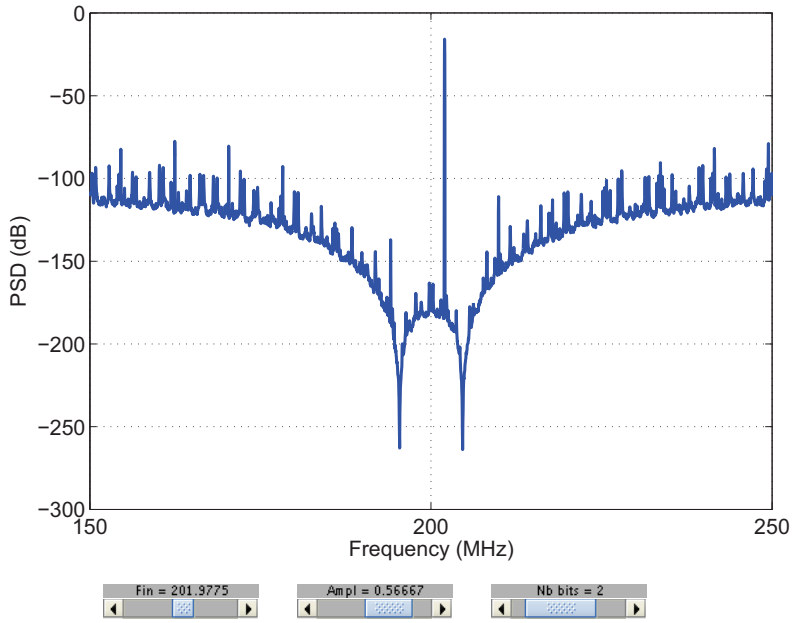
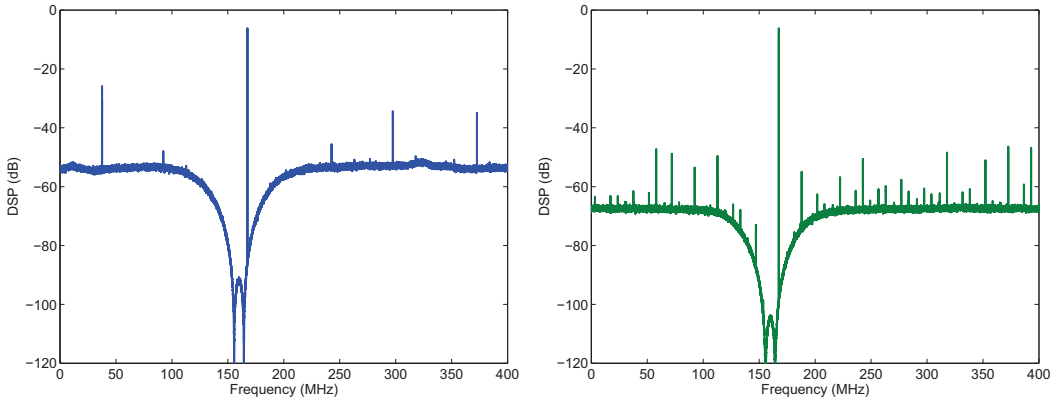


Figure III.30: Simulation tool to study the nonlinear effects in modulators

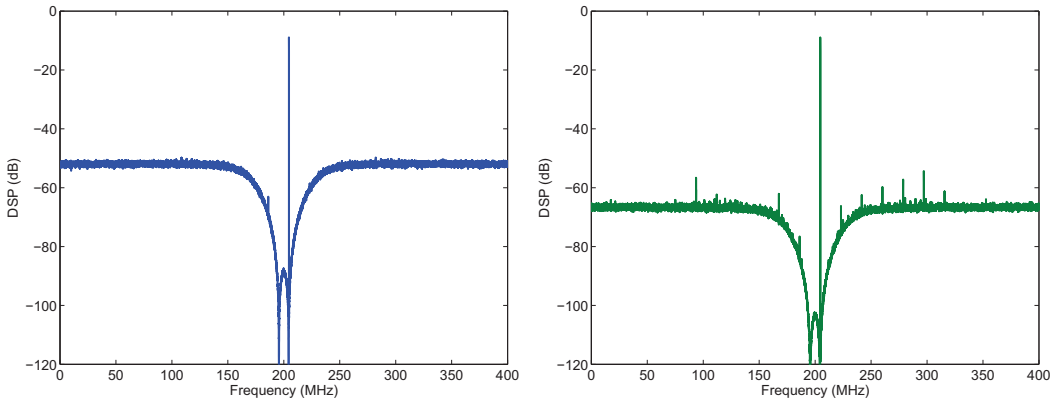


(a) 2-bit quantizer (b) 4-bit quantizer

Figure III.31: Reduced nonlinear effects in non-$F_s/4$ modulators — $F_c = 160$MHz

tor which generates in the output, periodic patterns[1]. However, we could not develop the mathematical and simulation tools for this cycles analysis though we are confident in that an analysis of the state spaces could reveal a topology explaining each periodic pattern. We also know that these cycles can be *broken* adding some noise (dithering). To not affect the measurement of the SNR, it is necessary to spectrally shape the noise injected either by adding it at the quantifier, either by shaping it by the NTF and injecting it to the modulator input. We should always make sure that its power is not greater than the noise generated by the modulator. The Figure III.32a and Figure III.32b show a simulation where this shaped noise has been injected at the input of the modulator where we note the suppression of the spurious tones.

[1] We think that time-frequency analysis would enable the study of the occurrence of spurious frequencies and sequencing technique would enable the study of the periodic pattern in the time domain.



(a) 2-bit quantizer (b) 4-bit quantizer

Figure III.32: Breaking periodic pattern with additive NTF-shaped noise is $F_s/4$ modulators

III.3.1.3 Conclusion

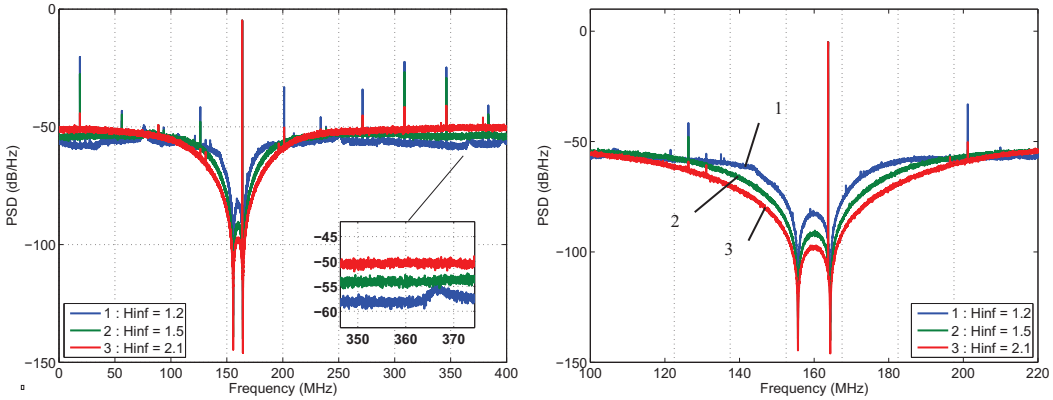
In this section we have seen with simulations, a nonlinear behavior in $\Sigma\Delta$ modulators centered around $F_s/4$. To avoid this problem in our simulations to extract the performances we choose to center the overall converter on a frequency far enough from $F_s/4$ so that each modulator operates without these cycles nonlinearities. This frequency is $F_c = 160$MHz.

III.3.2 Optimization of each path

We propose in this section an optimization methodology to maximize stability modulators as secondary channels may process signals of high amplitude occasionally. As mentioned in Chapter II ([82]), there are different methods to analyze theoretically the stability of modulators such as the variable gain quantizer and its root loci analysis or the Describing functions. In this thesis, we used a third method which is the study of the maximum input amplitude stable. This non-formal method, is based on the extraction by simulation, of the maximum value of the input of the modulator for which it is stable and allows to estimate empirically the ability of the modulator to absorb high power signals.
We also know that the modulators are gaining stability when the resolution of the quantizer increases but decreases as the order of the loop filter increases. However, when the filter order and the resolution of the quantizer are fixed, we can still change a third parameter affecting the modulator stability: the NTF and more specifically, its maximum *out-of-band gain*.

III.3.2.1 NTF Out-of-band Gain

The *out-of-band gain* (OOBG) is one of the parameters proposed by the Delta-Sigma Toolbox to design the NTF. As mentioned in [11], increasing this parameter (denoted `Hinf`) yields to higher SNR but it reduces the maximum input stable amplitude as the stability of the modulator depends on it. Conversely, reducing it yields to lower SNR but the modulator is more stable.
Its effect on the NTF frequency response is shown in Figure III.33a and Figure III.33b. These figures show the output spectra for different out-of-band gain. The magnified part of the Figure III.33a shows the actual effect of the parameter. Indeed, we note a different power level for each line. In the Figure III.33b, we see the reduction of the noise inside the



(a) Entire frequency range (b) Detail of the spectrum

Figure III.33: Effect of the NTF out-of-band gain (OOBG) - 4th order 2-bit quantizer modulator

bandwidth and also in the surrounding frequency bands when the OOBG is increased. So tuning this parameter allows to increase or decrease the SNR for a given set of loop filter order and quantizer resolution. However the possible values of OOBG yielding a stable modulator are limited and this is shown in the Figure III.34.

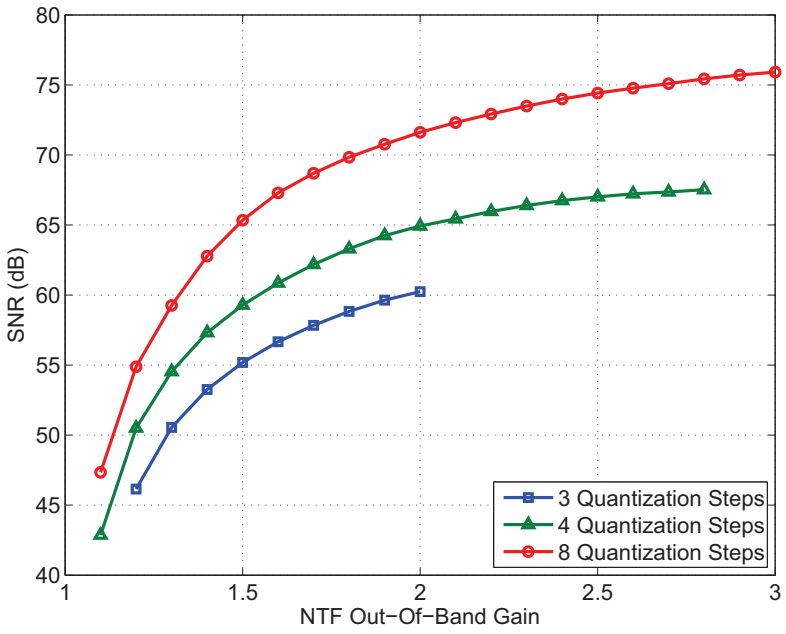


Figure III.34: SNR vs. OOBG

Figure III.34 shows the SNR obtained by simulation as a function of the OOBG for different quantizer resolution. Each curve has been drawn for the values of OOBG for which the modulator is stable with input amplitude of 0.8. It is the reason why each curve ends at different values of OOBG and since stability increases with the number of quantization steps, the maximum allowable value of OOBG is greater when it increases.

III.3.2.2 Optimization algorithm

Based on these results, we propose an empirical design method of high order stable ΣΔ modulator based on the evaluation of the maximum stable input. Indeed, if for the target maximum value, the modulator is unstable, it will require to reduce the NTF OOBG which will increase stability at the expense of SNR. Using the tools provided by the Delta-Sigma Toolbox, this optimization can be carried out quickly.
The optimization algorithm is depicted is Figure III.35.

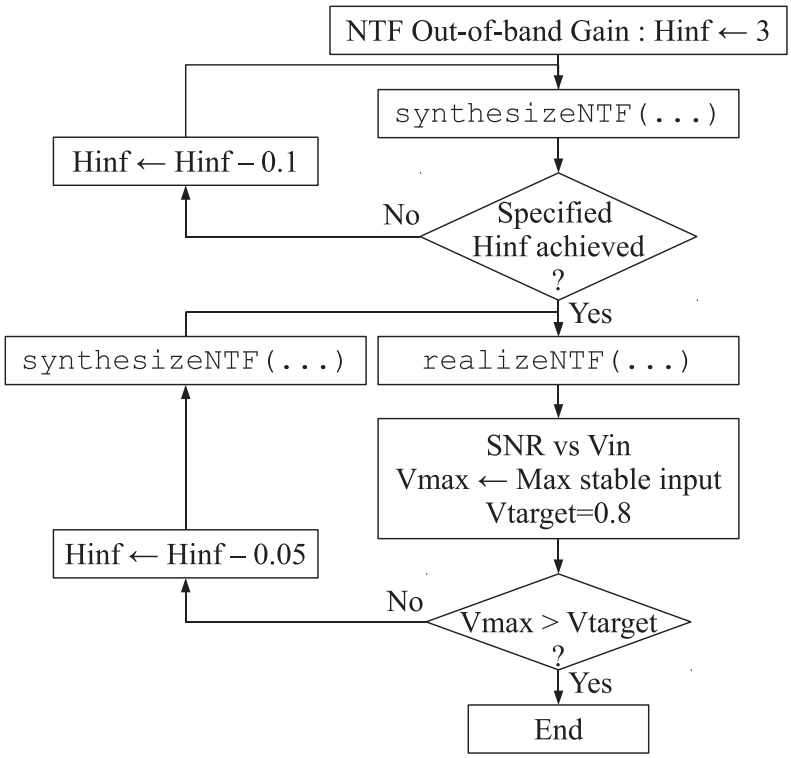


Figure III.35: Optimization algorithm to maximize SNR and stability of a modulator

It starts by initializing the OOBG parameter `Hinf` to a large value (3). This would imply a highly unstable modulator yielding a maximum SNR. However, for low order transfer function, this first value may not be achievable by `synthesizeNTF()` so, in this case, there is a loop to decrease the value until a transfer function is found.
Then, this NTF is mapped to the given architecture and a sweep of the input amplitude `Vin` allows to extract the maximum stable amplitude `Vmax`. In order to have smooth and accurate extracted performance characteristics, we perform as mentioned earlier, for each amplitude value, an average of several realizations (~ 100) where the phase origin of the input sinusoid is randomly changed.
After that, `Vmax` is compared to the minimum wanted value `Vtarget` which is set to 0.8 of the full scale. This target value has been chosen arbitrarily but it ensures a quite large input dynamic range.
Usually, for the first loop executions, the value of `Vmax` is lower than `Vtarget`, so the OOBG is decreased so that `Vmax` increases in the second loop. Then, the reduction of `Hinf`, the NTF synthesis, the mapping and the extraction of `Vmax` are done until the `Vtarget` is reached.

Optimization example

We applied this algorithm to the design of a sixth order CRFB BP modulator. The modulator includes a 3-bit quantizer and it is designed to be centered around $F_c = 160$MHz and its NTF zeros are optimally distributed in the band. Figure III.36 shows the SNR vs. Vin characteristic for two cases: the first one is where `Hinf` is kept to its default value 1.5; and the second case is the result of the optimization yielding a `Hinf`= 3.3. We note that in the first case, the SNR does not drop even with input amplitude at full scale. However, actually, the modulator exhibits nonlinear behaviors but remains stable. In the second case, the peak SNR is 18.6dB higher than the previous case and the modulator becomes unstable for Vin> −2dB i.e. Vin> 0.7943 which is approximately the target amplitude.

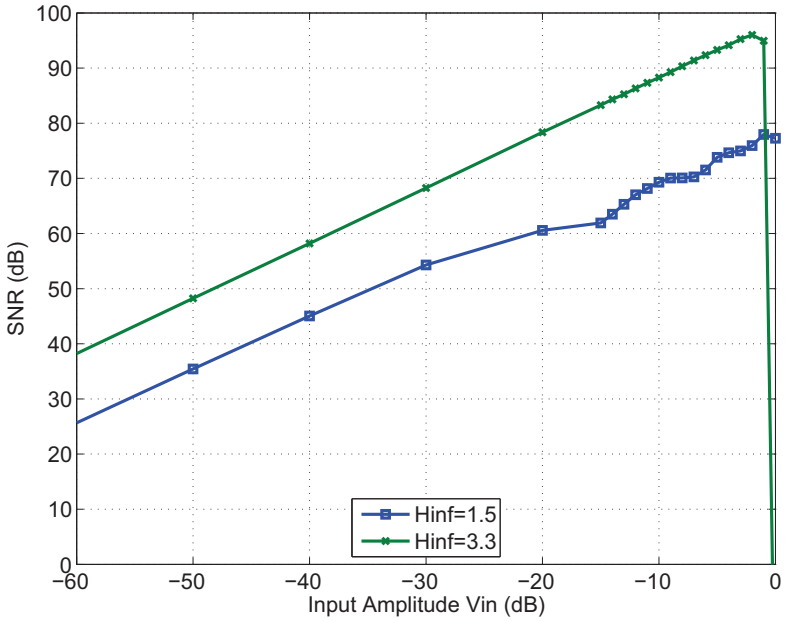


Figure III.36: SNR vs. Vin characteristics comparison

We use this methodology to optimize each path of the modulator so that the SNR is maximized on each path while the modulator should remain stable. This is of particular interest for the secondary modulators as they process the shaped noise. Indeed, this signal may exhibit high peak amplitude occasionally as it results from the input signal and its estimate version — the digitized version.

III.3.3 Design space study

Now that we are able to design robust modulators, we explore the design parameters space to analyze the influence of each parameter and choose from simulation results, a suitable configuration to achieve the specified performance of the modulator.
We recall that the overall converter should be able to convert an output signal from PA by providing:

- $SNR_{BPr} = 60$dB on the principal band
- $SNR_{BAdj} = 20$dB on the adjacent band.

In addition, these SNR are measured on a particular signal simulating a distorted signal with 60dB ACPR and as before, we use a signal composed of two sinusoids.

III.3.3.1 Design of the primary modulator

We begin by presenting the study of the performance of primary modulator. The design of this modulator is a matter of classical design and to justify the choice of its parameters we present the simulation results obtained after optimization.
Figure III.37 shows the SNR as a function of the design parameters of the modulator: the loop filter order and the number of quantization steps.

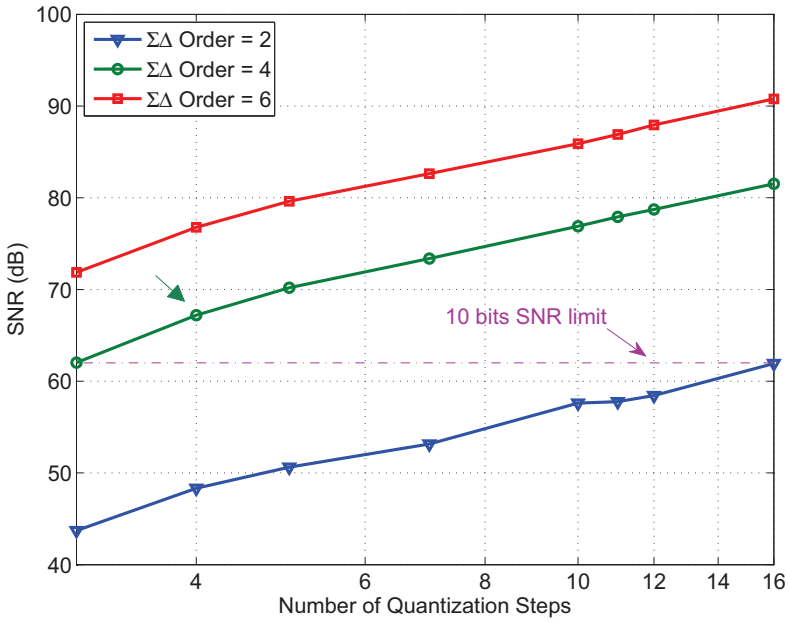


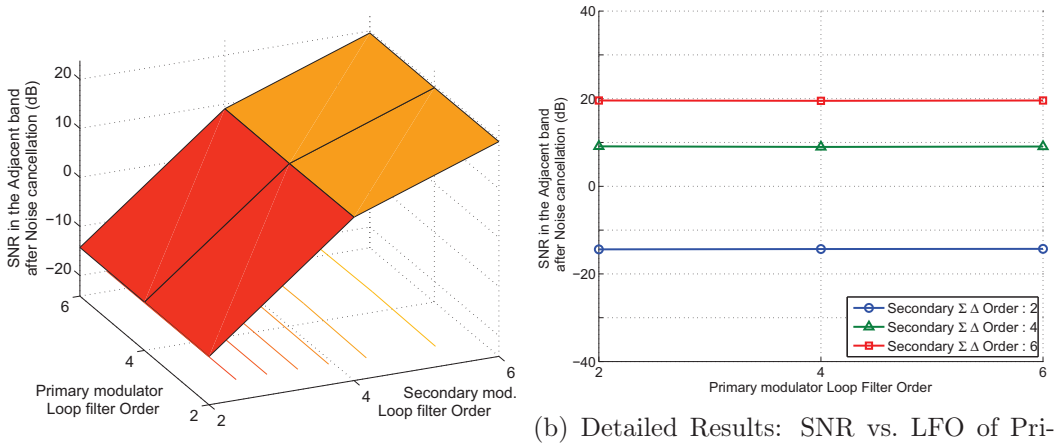
Figure III.37: SNR performances of the primary modulator

From these simulations we see that it is not possible to achieve 10 bits of resolution with a 2nd order modulator and a quantizer of less than 4 bits (16 levels). However, increasing the order of the modulator to 4, we can perform this 10-bit resolution from a quantization of 1.5 bits (3 levels). We choose a 2 bit quantizer (green arrow) to provide some flexibility for implementation and the achieved SNR is 67dB.

III.3.3.2 Design of the secondary modulator

We focus now on the secondary modulator that digitizes the first adjacent band.
To design it, we explore the space of parameters to investigate their influence on performance. For this, we choose to work on the simple case of discrete-time modulators with STF equal to 1 preventing the use of noise cancellation filters.
We divide the exploration of the space of parameters in two stages: first, we set the resolution of the two quantizers to 2 bits (4 levels) and we vary the order of each modulator; second, conversely, we set the modulators order to 4 and we vary the resolution of each modulator.
Here too, each configuration is optimized (i.e. stabilized) according to its parameter values.

Figure III.38 shows the simulation results of the first phase of exploration. The SNR in the adjacent band is shown after noise cancellation.
Figure III.38a shows an overview of performance in the considered space of parameters which are: the order of each modulator (resolution quantizers is set to 2 bits). At first



(a) SNR overall evolution

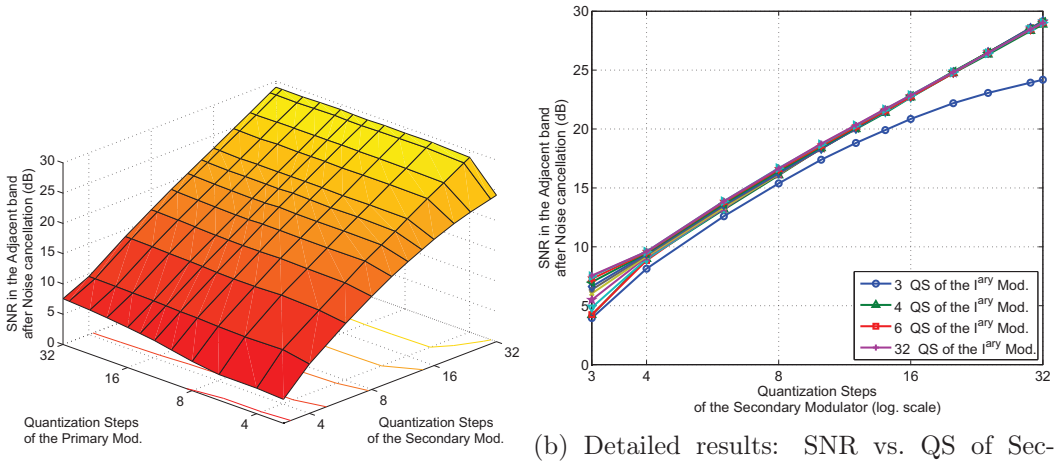
(b) Detailed Results: SNR vs. LFO of Primary Modulator

Figure III.38: SNR vs. loop filter order (LFO) of each modulator in MSNBC ΣΔ architecture

glance of this 3D surface, we observe that the SNR depends on the order of the secondary modulator but not on the primary. This is clearly confirmed by Figure III.38b which is a projection of the results of the previous figure on the primary modulator plane. It plots the SNR according to the order of the primary loop filter and the different curves correspond to each value for the secondary modulator. We can see the SNR is strictly constant with respect to the order of the primary, and when the order of the secondary modulator is changed, the SNR also changes.
This result is in perfect agreement with the Equation (III.20) which states that the signal after noise cancellation, depends only on $X(z)$, the input signal and $N_{1A}(z)NTF_{1A}(z)$, the noise of the secondary modulator.
Regarding the simulated performance, we find that if we set the resolution of quantizers to 2 bits, it is necessary and sufficient to use a 6th order modulator for the secondary channel to achieve 20dB SNR, whatever the order of the primary modulator.

Second, we set the modulators order to 4 and we vary the resolution of each quantizer. Figure III.39 shows the results of SNR in the adjacent band after noise cancellation extracted from the simulations.
Figure III.39a gives an overview of the influence of each parameter. There is a dependence of SNR as a function of the secondary modulator quantizer, however, the SNR appears to be independent of the quantization of the primary channel.
This is confirmed by Figure III.39b which is a projection of the results of Figure III.39a on the secondary modulator plane [1]. Here, the SNR is represented as a function of the number of quantization steps of the secondary modulator and each plot corresponds to a different value for the primary modulator.
We note that, except for the cases where the number of quantization steps of each modulator is equal to 3, the curves are superposed meaning that the SNR is independent of the primary modulator and depends only on the secondary modulator. This result is also in agreement with Equation (III.20).
Finally, these simulations show that, 4th order modulators require at least 3.5 bits for the quantizer ($\log_2(12) \approx 3.6$bits) of the secondary modulator to achieve 20dB SNR in the adjacent band.

[1] For reasons of readability we changed here the projection plane in comparison with Figure III.38b



(a) SNR overall evolution

(b) Detailed results: SNR vs. QS of Secondary Modulator

Figure III.39: SNR vs. number of quantization steps (QS) of each modulator in MSNBC $\Sigma\Delta$ architecture

These two design space studies are consistent with the equations is Section III.2 and provide to us two sets of parameters for the secondary modulator to achieve the target performances. Eventually, we have chosen the 2-bit 6th order configuration for the secondary modulator as part of our first solution. However further lower level study should be done to assert which of the two configurations is the best to design. However, it leads to a convenient configuration where all the quantizers and DACs are the same for all channels.

To conclude this design space study, we provide the spectra of the signals in the architecture composed of the 4-th order modulator with 2-bit quantizer centered around $F_c = 160\text{MHz}$ and of the 6th order 2-bit quantizer centered around $F_{cIM3} = 175\text{MHz}$. The architecture of each modulator is a CRFB structure as shown in Figure III.40 that depicts the simulated system. Finally, similarly to the design rules of the exploration phase, we set the feed-in coefficients of the modulators so that their STF are equal to 1.

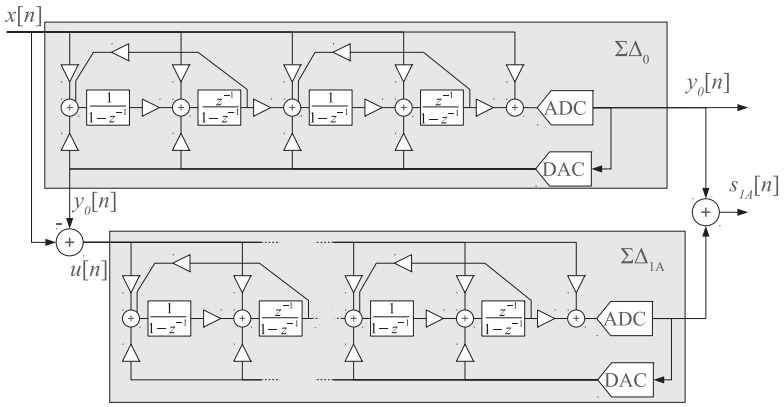


Figure III.40: Diagram of the final MSNBC converter with a 4th order and a 6th order respectively for the primary and for the secondary modulator

Figure III.41(a) shows the spectrum of the signal consisting of two sinusoids which is injected into the converter. This signal is digitized in a conventional manner by the primary modulator which output spectrum is shown in Figure III.41(b). Meanwhile, the signal

resulting from the subtraction $x - y_0$ is injected into the secondary modulator. This signal has almost only traces of the original signal when the STF are unitary as it is case here and verified by Figure III.41(c). Otherwise, the signal will include an attenuated version of the original signal and always the shaped quantization noise from the primary modulator. This noise is in turn digitized on an adjacent band by the secondary modulator. Once digitized, the digital values are added so as to obtain a noise cancellation in the considered adjacent band as shown in Figure III.41(d). We observe the characteristic shape of the secondary NTF of order 6 which consists of three separate notches in the band. The SNR obtained in this band is approximately 21dB.

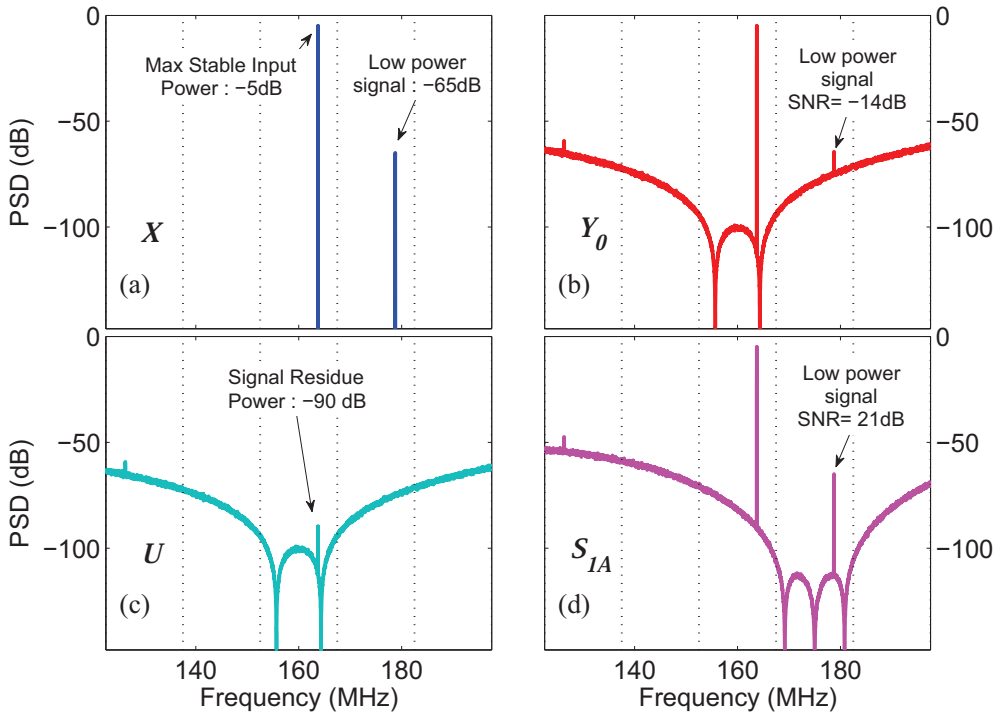


Figure III.41: Spectra in the selected configuration of MSNBC converter

In this design space study we addressed the design of the first adjacent modulators. However the results for the further adjacent bands can easily be expected from this study as the equation Equation (III.2) states that the remaining noise is only the noise from the secondary modulator. Therefore, as the signal in these bands is assumed to be 10dB lower than in the first adjacent bands, we should subtract 10dB to every result obtained in this section to estimate the performance in these bands.

III.4 Conclusion

In this section we introduced a new architecture converter optimized for the digitization of distorted signals output of PA base stations. In this architecture, we define a new transfer function performed in $\Sigma\Delta$ modulators: the RSTF, to model the filtering experienced by the signal in $u = x - y_0$. We use this filter to provide to the secondary modulator only the shaped quantization noise to be digitized in bands. This noise is then canceled in the

digital domain. We have developed several particular cases and the general case where the modulators can have STF not equal to 1 and verified theoretical developments by simulations. The exploration of the parameter space allowed us to select a configuration achieving the initial targeted performance.

Conclusion

Contributions of the thesis

The topic of this thesis is the development of innovative architectures for the processing of wideband signals of base station PAs. Indeed, these systems must be corrected to compensate for their nonlinear distortion effects and to improve the energy efficiency of BTS. To meet these requirements, we have chosen the parallel processing to increase converters' bandwidth. Given the particular composition of the signal to be digitized, we have developed a new architecture to reduce consumption and facilitate the digitization of adjacent low power bands.

Proposed architecture

In this thesis, we proposed a new architecture using band-pass $\Sigma\Delta$ modulators and combining parallel frequency decomposition and a kind of cascade of the modulators. This architecture was named Multi-Stage Noise Band Cancellation (MSNBC). Its development was driven by two key points:

- a specific structure of the signal that is decomposable into several frequency bands. Band-pass $\Sigma\Delta$ modulators are suitable to process this type of signal.
- the wish to avoid selective analog filters for each low power bands. $\Sigma\Delta$ modulators offer us filtering capabilities that we exploit in this architecture.

The Residual Signal Transfer Function (RSTF)

We know the STF and NTF as the transfer functions that model the filtering undergone by the signal through the modulator and the shaping of the quantization noise. We have defined a new transfer function: the RSTF, which models the attenuation experienced by the input signal when doing the subtraction of the modulator input and its output (converted to analog domain). We have shown that this filter is of the same order as the STF and NTF in the studied architecture. The order of these transfer functions being, a priori, not very high, the resulting RSTF can not at the same time reduce significantly the main band power and not attenuate the adjacent bands. This fact makes impossible to use this signal shaping for band-stop filtering. However, a special case of STF (unitary STF) provides, in theory, a RSTF equal to zero, meaning a complete signal suppression. This implies that the remaining signal of the subtraction is the shaped quantization noise .

Noise digitization and digital cancellation

The second concept of this architecture is to employ other band-pass $\Sigma\Delta$ modulators to digitize the shaped quantization noise of the primary modulator. This digitization, like any

conventional digitization using band-pass $\Sigma\Delta$ modulator, can only be done on a limited band. Centering the modulators on the adjacent bands next to the central band, we can digitize and remove the noise of the considered adjacent band with a digital processing. Such processing requires, if the secondary modulator has a non-unitary STF, the use of digital FIR filters (NCF) which we detailed the calculation method. Otherwise, in the case of a unitary STF, a simple addition is sufficient.

Simulation techniques and optimization

In this thesis, we paid special attention to simulation techniques. Good simulation techniques allow to obtain accurate results quickly and unlock some optimization mechanisms that improve significantly architectures.
Thus, based on the simulation tools provided by the Delta-Sigma Toolbox, we propose an optimization of DT architectures to maximize the SNR and ensure a certain level of stability. And, we also propose an extension of the toolbox to the design and simulation of CT architectures.

Future work

In this thesis we laid the groundwork for the design of this new type of converter. the logical steps that would follow this work should focus on the implementation of the digital part and the lower level aspects of the analog part.

In the first point we should make the design of the digital part including the noise cancellation filters (NCF) (if needed) and the (conventional) decimation filters. One of the issues of this architecture, as in all cascade architectures resides in these NCFs. Indeed, they should be operated, a priori, at the over-sampling frequency because the signal is filtered and decimated thereafter and probably should require high coding resolution of their coefficients. But this disadvantage may be less expensive than the cost to increase the analog part to reach the same performances. For this digital processing design, we would refer to the cascaded CT modulators literature, as a starting point, where these filters have been necessarily used.

In the second point we would study the robustness of the architecture to the common non-idealities of parallel architectures such as gain error between channels and synchronization errors, in particular their impact on the subtraction and then noise digitization and cancellation. Also, the robustness of the architecture to the common non-idealities of other architectures based on a digital signal reconstruction should be considered. Indeed, the mismatch of digital NCF regarding the actual values of analog components will impact the performance of this architecture, similarly to the case of hybrid filters banks architectures.

To conclude, the REFLEX [1] project has been planned to complement this work focusing on the digital processing. This project aims at developing the algorithm to compute the coefficients for a DPD from the information provided by a converter using the architecture developed in this thesis. This information has the characteristic to be provided per band, possibly using multiple data rates, and the proposed innovation is to directly exploit this information to build a model of predistortion.

[1] Rétroaction Flexible

Appendix A

RF Band-pass QAM and equivalent baseband model

Synchronous demodulation shows that the separation of two carriers mixed with a sum is possible if these carriers are in quadrature. This principle is the basis of vector modulations, also called Quadrature Amplitude Modulation (QAM).

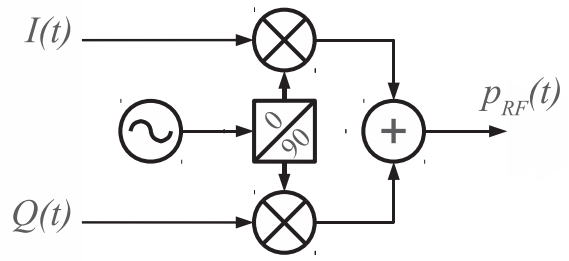


Figure A.1: Block diagram of the Quadrature Amplitude Modulation

The signals I(t) and Q(t) -which can be independent or not- are "multiplexed" in the QAM carrier, a priori without increasing the bandwidth (contrary to frequency multiplexing). The modulated carrier signal is as follows:

$$p_{RF}(t) = I(t)\cos(2\omega_0 t) - Q(t)\sin(\omega_0 t) \tag{A.1}$$

with

$$I(t) = \sum_{k=-\infty}^{\infty} i_k \cdot h(t - kT_s) \tag{A.2}$$

$$Q(t) = \sum_{k=-\infty}^{\infty} q_k \cdot h(t - kT_s) \tag{A.3}$$

where i_k and q_k are discrete real values and T_s the symbol period.
The modulated carrier can also be written as:

$$\Re\left\{\mathcal{E}(t) \cdot \mathrm{e}^{i\omega_0 t}\right\} \tag{A.4}$$

where

$$\mathcal{E}(t) = I(t) + iQ(t) \text{ is referred to as } \textit{complex envelop} \text{ or } \textit{equivalent baseband signal} \tag{A.5}$$

Appendix B

System Vue models

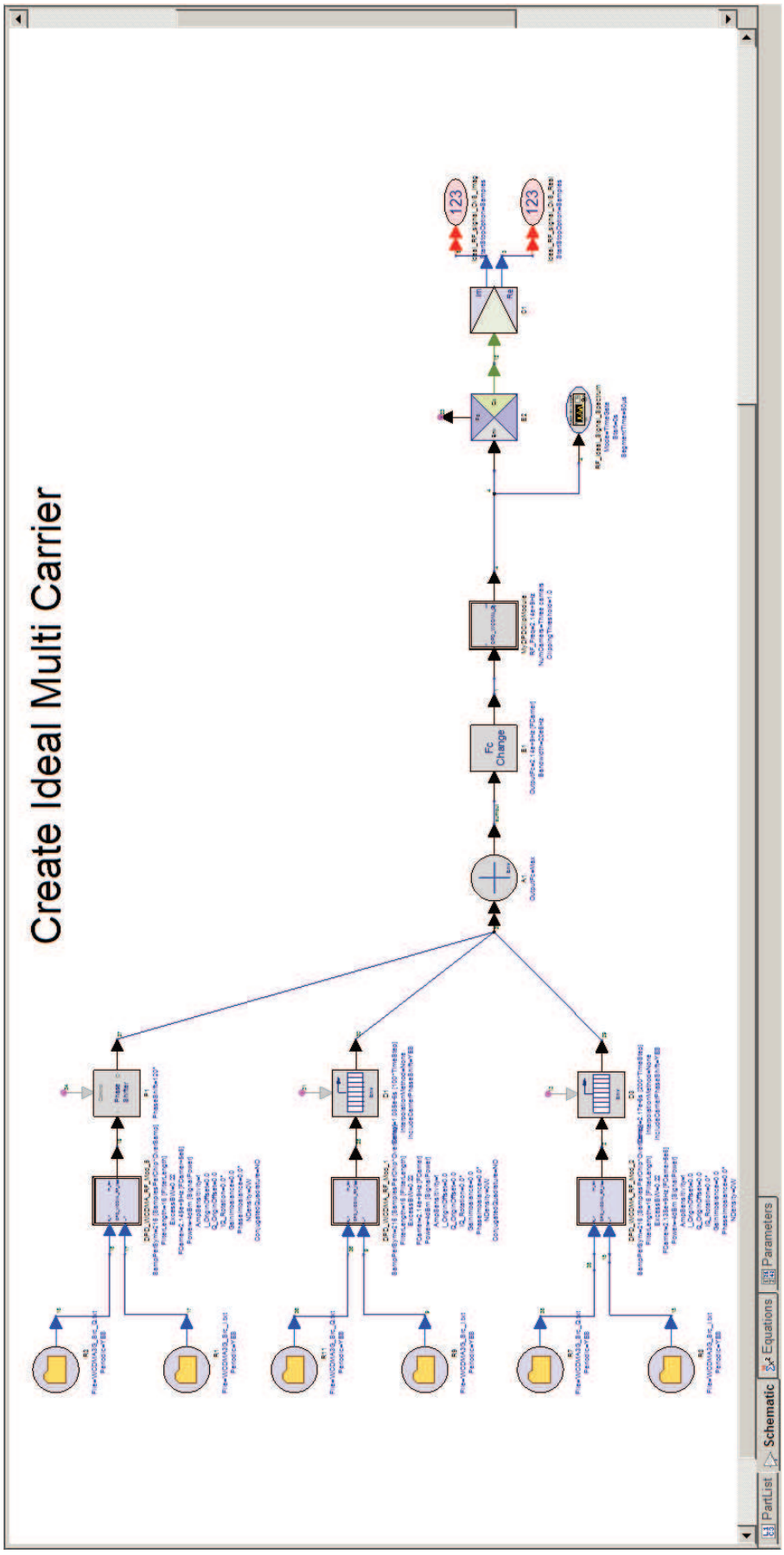


Figure B.1: Model to create the ideal signal to be transmitted

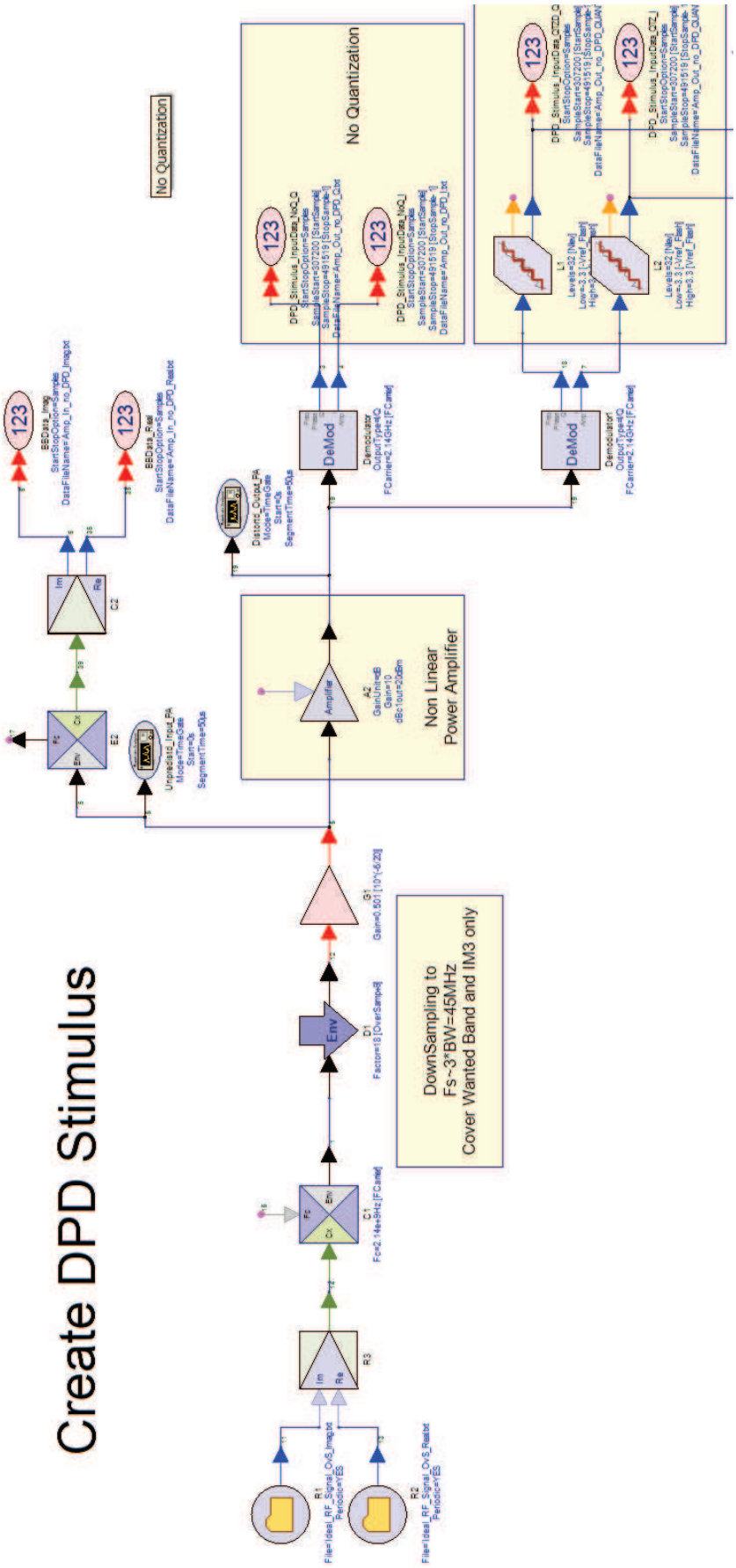


Figure B.2: Model to simulate distorted data acquisition for the unquantized and the Flash ADC cases

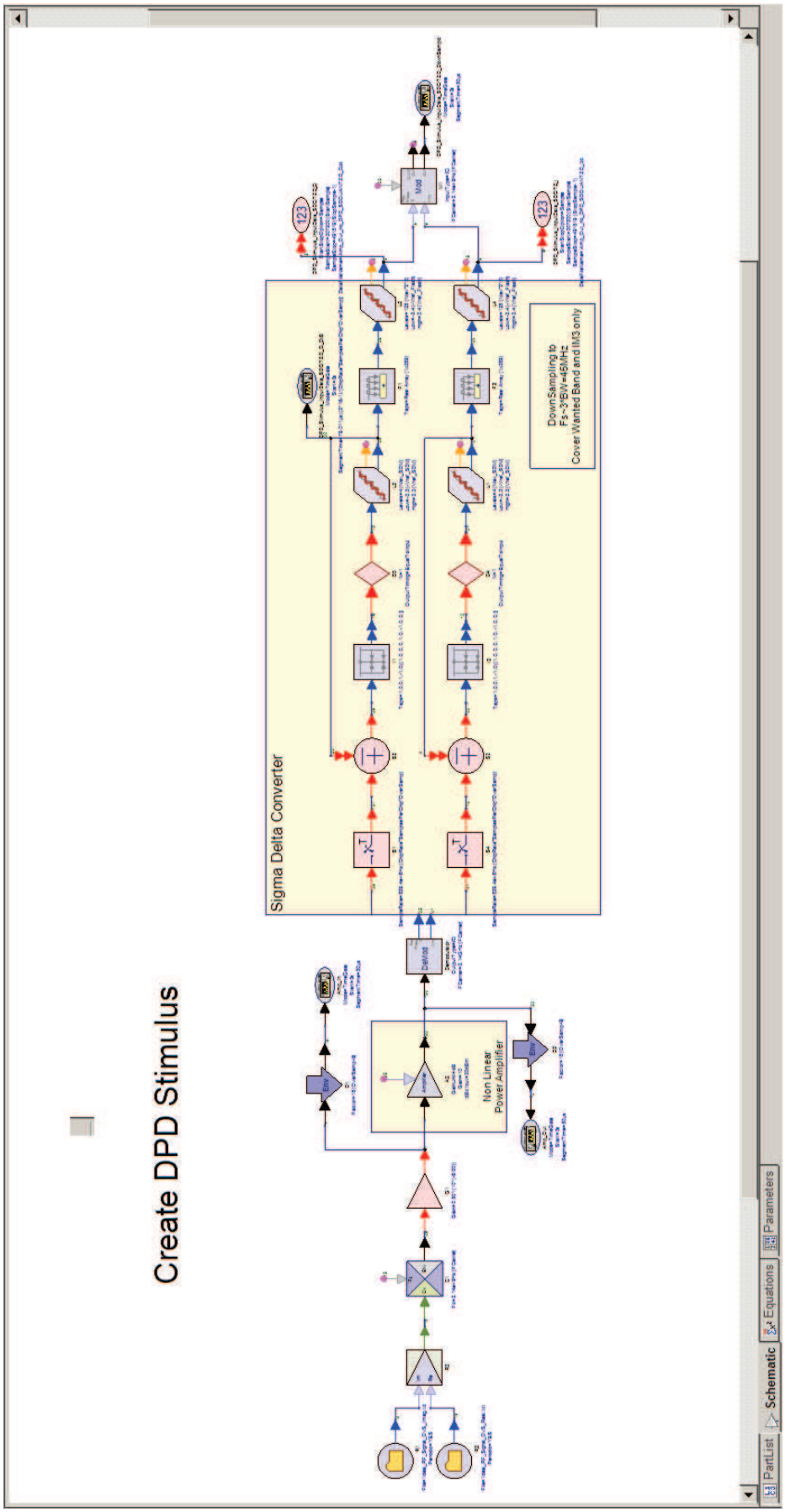


Figure B.3: Model to simulate distorted data acquisition for the ΣΔ ADC case

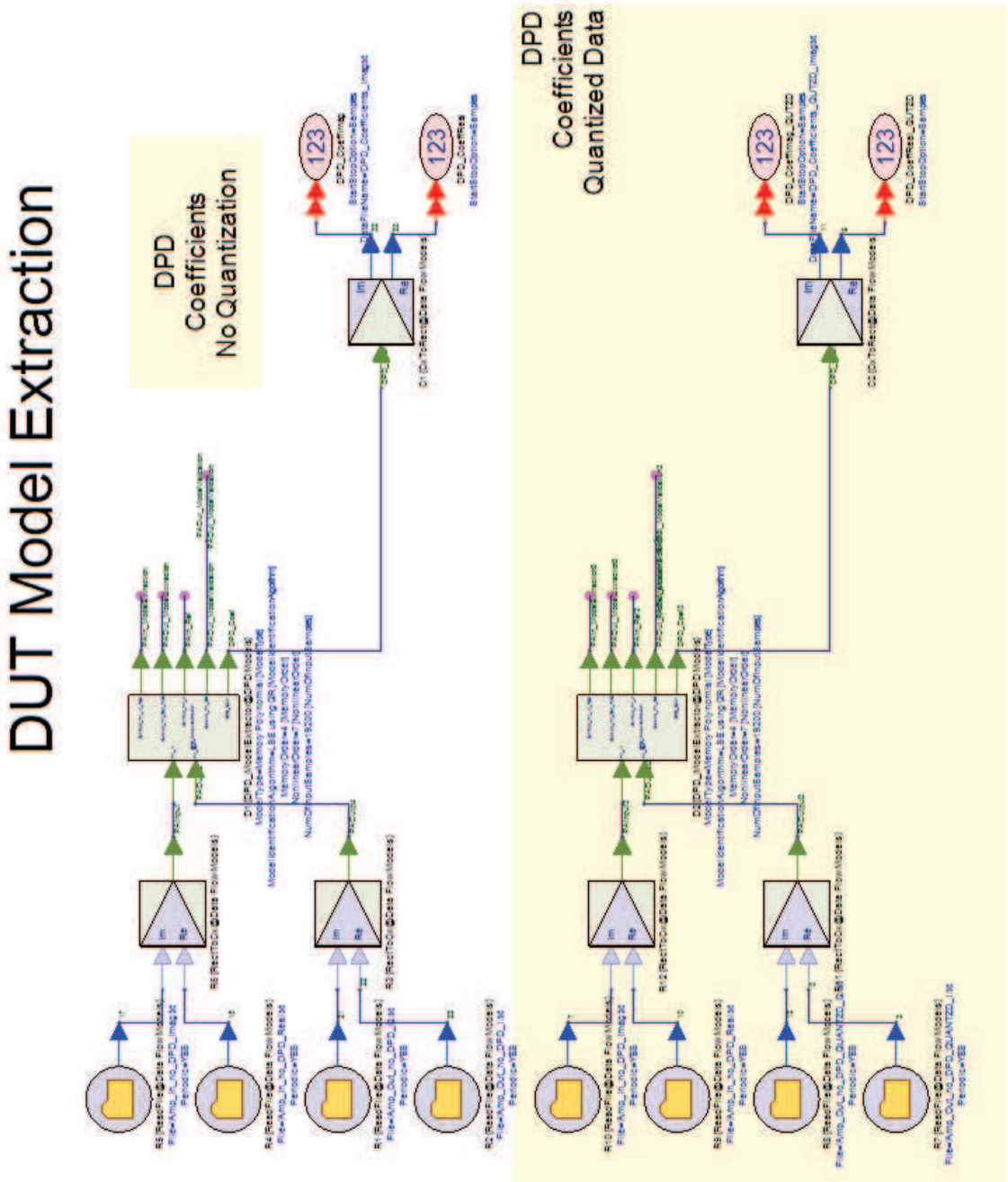


Figure B.4: Model of the extraction phase

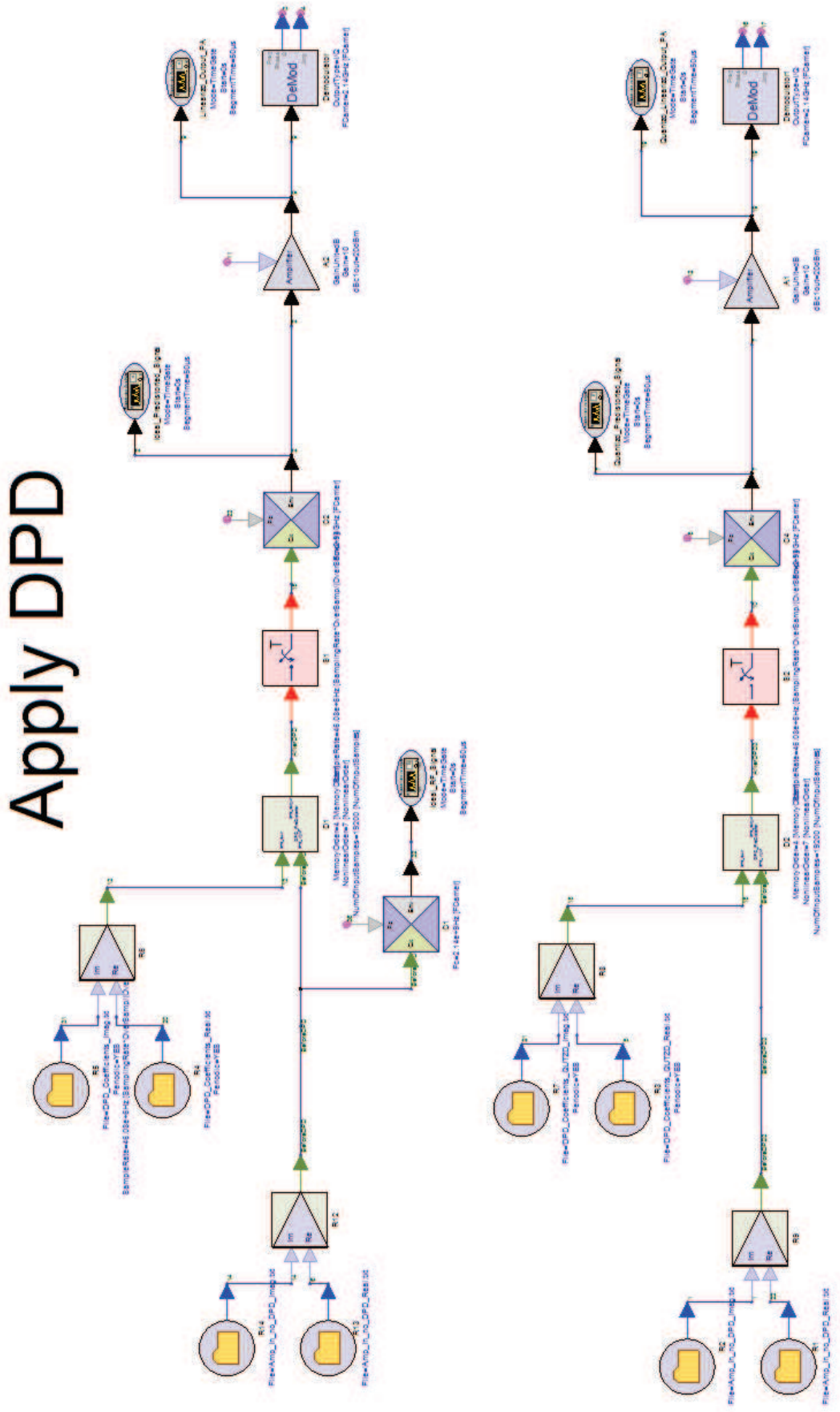


Figure B.5: Model to simulate the transmission with predistortion

Appendix C

Noise Cancellation Filter derivation for CT MASH modulators

The derivation of noise cancellation filters for CT MASH modulators is based on the detailed expression of the actual transfer functions in the modulator. We have to use in this calculation the Z-transform of a sampled inversed Laplace transform $\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle\cdot\right\rangle_{|t=kT_S}\right]$ also known as *star operator* [41, 26]. The star notation is a very convenient —short— notation, however, as many short notations, it may lead to a loss of precision (as some details are hidden) and we prefer to keep the long notation to underline the multiple steps of this transformation to avoid misunderstandings.

The system we consider is depicted below:

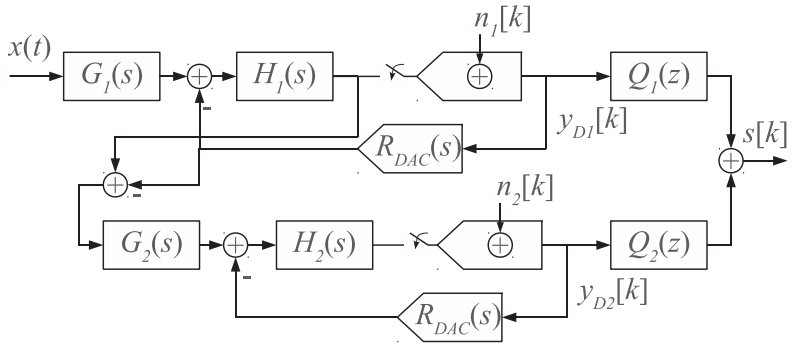


Figure C.1: CT MASH Architecture

The first step is to write the time equations of the output of each modulator, then transform it into the Z-domain.

$$y_{D1}[k] = n_1[k] + \mathcal{L}^{-1}\left\langle H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S} - \mathcal{L}^{-1}\left\langle H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S} * y_{D1}[k] \quad \text{(C.1)}$$

$$Y_{D1}(z)\left(1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]\right) = N_1(z) + \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S}\right] \quad \text{(C.2)}$$

$$Y_{D1}(z) = \frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} + \frac{1}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} N_1(z) \quad \text{(C.3)}$$

For the second stage:

$$\begin{aligned} y_{D2}[k] = n_2[k] &+ \mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S} \\ &- \mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S} * y_{D1}[k] \\ &- \mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S} * y_{D2}[k] \end{aligned} \tag{C.4}$$

$$\begin{aligned} Y_{D2}(z) = N_2(z) &+ \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S}\right] \\ &- \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right] Y_{D1}(z) \\ &- \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right] Y_{D2}(z) \end{aligned} \tag{C.5}$$

$$\begin{aligned} Y_{D2}(z) = &\frac{1}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} N_2(z) \\ &+ \frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} \\ &- \frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} Y_{D1}(z) \end{aligned} \tag{C.6}$$

The output filtered sum $S(z)$ is equal to:

$$S(z) = Q_1(z)\,Y_{D1}(z) + Q_2(z)\,Y_{D2}(z) \tag{C.7}$$

Expanding $Y_{D2}(z)$ with Equation (C.6), we get:

$$\begin{aligned} S(z) = &\left(Q_1(z) - Q_2(z)\frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}\right) Y_{D1}(z) \\ &+ Q_2(z)\frac{1}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} N_2(z) \\ &+ Q_2(z)\frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} \end{aligned} \tag{C.8}$$

$$\begin{aligned} S(z) = &\left(Q_1(z) - Q_2(z)\frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}\right) \\ &\times \left(\frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} + \frac{1}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} N_1(z)\right) \\ &+ Q_2(z)\frac{1}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} N_2(z) \\ &+ Q_2(z)\frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)G_1(s)X(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} \end{aligned} \tag{C.9}$$

The term related to $N_1(z)$ in $S(z)$ vanishes if and only if:

$$\frac{Q_1(z)}{Q_2(z)} = \frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)G_2(s)H_1(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_2(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]} \tag{C.10}$$

STF

Furthermore, we note from Equation (C.3) that it is not possible to calculate the exact STF of the first modulator as in general $\mathcal{L}^{-1}\left\langle H(s)X(s)\right\rangle_{|t=kT_S} \neq \mathcal{L}^{-1}\left\langle H(s)\right\rangle_{|t=kT_S} \circledast x(t)_{|t=kT_S}$. However, provided that the continuous-time front-end filter $G(s)$ sufficiently attenuates the replica spectrum of the input signal at higher frequencies [62], the STF of a CT modulator can be estimated by:

$$STF(j\omega) \approx \frac{H(j\omega)G(j\omega)}{1+\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H(s)\mathcal{R}_{DAC}(s)\right\rangle_{|t=kT_S}\right]}_{|z=\mathrm{e}^{j\omega T_S}} \tag{C.11}$$

This approximate STF can be used for both the primary and secondary modulators using the G and H of interest.

Appendix D

Derivation of the architecture parameters in the discrete-time case

The estimation of the parameters of the architecture to perform a given DT $NTF^{target}(z)$ is to equate the numerically valued transfer function $H^{target}(z)$ of the loop filter (open loop system) with the literal transfer function $H^{litt}(z)$ obtained from the block diagram of the architecture. In the Delta-Sigma Toolbox, this procedure is efficiently implemented for the CRFB, CIFB, CRFF and CIFF architectures [1]. We develop this method since we adapt it later in this report to the design of continuous-time modulators.
Let us consider the example architecture Figure II.9 whose open-loop system is given below Figure D.1.

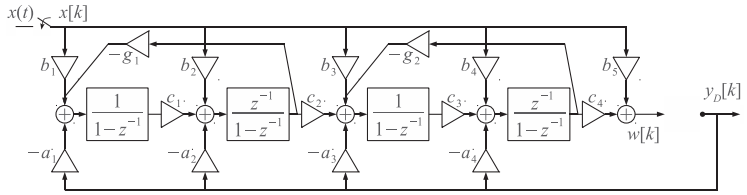


Figure D.1: A 4-th order CRFB modulator in open loop configuration

This diagram shows a fundamental characteristic of the addressed architecture by the toolbox: they all include coefficients noted a_i, b_i, g_i and c_i.
The coefficients c_i are scaling coefficients of signals and do not play an important structural role in the first place. They are all assumed equal to 1.
The coefficients b_i only affect the input signal and do not change the loop filter in terms of quantization noise. We do not use them for the moment.
Thus the system is summarized by the block diagram Figure D.2 where $G_1(z) = \frac{z}{z-1}$ and $G_2(z) = \frac{1}{z-1}$
The transfer function between A and B can be written with the following form:

$$H^{litt}(z) = \frac{B(z)}{A(z)} = -\begin{pmatrix} a_1 & a_2 & a_3 & a_4 \end{pmatrix} \begin{pmatrix} K_1(z) \\ K_2(z) \\ K_3(z) \\ K_4(z) \end{pmatrix} \tag{D.1}$$

[1] `realizeNTF()`

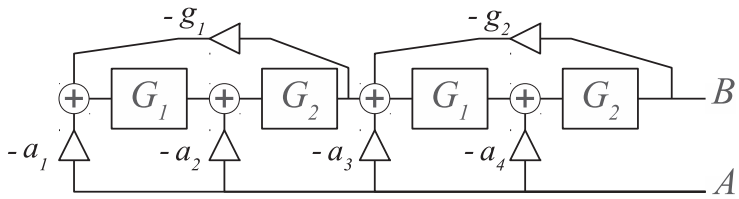


Figure D.2: 4-th order CRFB modulator in open loop configuration for the parameters estimation

with

$$K_1 = \frac{G_1G_2}{1+g_2G_1G_2}\frac{G_1G_2}{1+g_1G_1G_2}$$
$$K_2 = \frac{G_1G_2}{1+g_2G_1G_2}\frac{G_2}{1+g_1G_1G_2}$$
$$K_3 = \frac{G_1G_2}{1+g_2G_1G_2}$$
$$K_4 = \frac{G_2}{1+g_2G_1G_2}$$

The coefficients g_i can be easily obtained by equating the denominator of $H^{target}(z)$ and that of $H^{litt}(z)$. Now the system depends linearly on the coefficients a_i.
We build the following matrix system estimating each transfer function $K_i(z)$ for N (random) points in the complex Z-plane and the transfer function $H^{target}(z)$ en on these points:

$$\begin{pmatrix} a_1 & a_2 & a_3 & a_4 \end{pmatrix} \underbrace{\begin{pmatrix} K_1(z_1) & K_1(z_2) & \cdots & K_1(z_N) \\ K_2(z_1) & K_2(z_2) & \cdots & K_2(z_N) \\ K_3(z_1) & K_3(z_2) & \cdots & K_3(z_N) \\ K_4(z_1) & K_4(z_2) & \cdots & K_4(z_N) \end{pmatrix}}_{\kappa} = \begin{pmatrix} H^{target}(z_1) & H^{target}(z_2) & \cdots & H^{target}(z_N) \end{pmatrix} \quad \text{(D.2)}$$

The estimated coefficients $\widehat{a_i}$ are obtained from the computation of κ^+, the pseudo-inverse of the matrix κ. One can check the validity of the estimated coefficients calculating the achieved transfer function using Equation (D.1).

$$\begin{pmatrix} \widehat{a_1} & \widehat{a_2} & \widehat{a_3} & \widehat{a_4} \end{pmatrix} = \begin{pmatrix} H(z_1) & H(z_2) & \cdots & H(z_N) \end{pmatrix} \times \kappa^+ \quad \text{(D.3)}$$

D.1 STF Implementation

Similarly we can write the transfer function between the classic modulator input and the quantizer input that defines the coefficients b_i:

$$G^{litt}(z) = \begin{pmatrix} b_1 & b_2 & b_3 & b_4 & b_5 \end{pmatrix} \begin{pmatrix} K_1(z) \\ K_2(z) \\ K_3(z) \\ K_4(z) \\ 1 \end{pmatrix} \quad \text{(D.4)}$$

And from the diagram Figure II.9, we can write the following equation:

$$\begin{aligned} Y_D(z)(z) = N(z) \left(b_5 + b_4K_4(z) + b_3K_3(z) + b_2K_2(z) + b_1K_1(z)\right) X(z) \\ - \left(a_4K_4(z) + a_3K_3(z) + a_2K_2(z) + a_1K_1(z)\right) Y_D(z) \end{aligned}$$

i.e.

$$Y_D(z) = \frac{1}{1 + H^{litt}(z)} N(z) + \frac{G^{litt}(z)}{1 + H^{litt}(z)} X(z) \tag{D.5}$$

with

$$H^{litt}(z) = a_4 K_4(z) + a_3 K_3(z) + a_2 K_2(z) + a_1 K_1(z) \tag{D.6}$$

$$G^{litt}(z) = b_5 + b_4 K_4(z) + b_3 K_3(z) + b_2 K_2(z) + b_1 K_1(z) \tag{D.7}$$

The terms affecting $N(z)$ and $X(z)$ are by definition, respectively, the $NTF^{litt}(z)$ and the $STF^{litt}(z)$. We note that $STF^{litt}(z) = G^{litt}(z) \cdot NTF^{litt}(z)$ Thus, given a $STF^{target}(z)$ and its associated $NTF^{target}(z)$, we can identify the coefficients $\mathbf{b} = (b_1, b_2, ...)$ such that:

$$G^{litt}(\mathbf{b}, z) = G^{target}(z) \stackrel{\text{def}}{=} \frac{STF^{target}(z)}{NTF^{target}(z)} \tag{D.8}$$

A simple case is $STF^{target}(z) = 1$. Then $b_i = a_i$ for $i \in \left[1 : N^{\Sigma\Delta}\right]$ and $b_N^{\Sigma\Delta} = 1$ where $N^{\Sigma\Delta}$ is the order of the modulator. Conversely, if the coefficients b_i are set, we can extract the achieved $STF(z)$.

Appendix E

Derivation of the architecture parameters in the continuous-time case

The estimation of the parameters of the CT architecture that performs a given $NTF(z)$ consists in equating the numerically valued transfer function $H^{target}(s)$ of the loop filter (open loop system) with the literal transfer function $H^{litt}(s)$ obtained from the block diagram of the architecture.
Here we use the same method as in the discrete-time case. The fundamental difference is that the integration blocks are identical and equal to $\frac{1}{p}$: the diagram Figure E.1 illustrates the open loop system under consideration (derivative of the diagram of Figure II.10): The direct path coefficients, the feed-in coefficients, the local feedback coefficients and

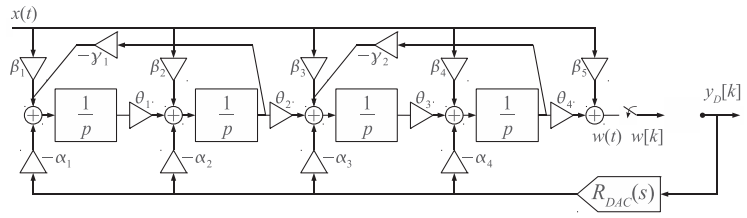


Figure E.1: A 4-th order CT-CIFB modulator in open loop configuration

the distributed feedback coefficients are respectively denoted θ_i, β_i, α_i and γ_i. These coefficients are a priori different from those calculated for a DT architecture.
Assuming the coefficients θ_i are equal to 1 and a zero input, we obtain the diagram shown in Figure E.2 The CT transfer function between A and B is:

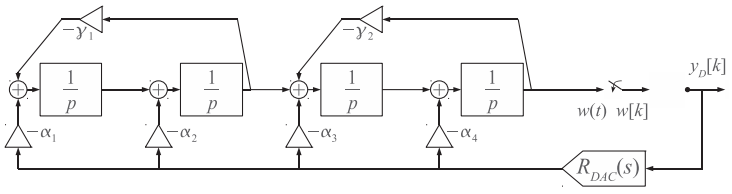


Figure E.2: A 4-th order CT-CIFB modulator in open loop configuration for the parameters estimation

$$H^{litt}(s) = \frac{B(s)}{A(s)} = -\begin{pmatrix}\alpha_1 & \alpha_2 & \alpha_3 & \alpha_4\end{pmatrix}\begin{pmatrix}K_1^{CT}(s)\\ K_2^{CT}(s)\\ K_3^{CT}(s)\\ K_4^{CT}(s)\end{pmatrix} \tag{E.1}$$

with

$$\begin{aligned}K_1^{CT}(s) &= \frac{1}{s^2+\gamma_2}\frac{1}{s^2+\gamma_1}\\ K_2^{CT}(s) &= \frac{1}{s^2+\gamma_2}\frac{s}{s^2+\gamma_1}\\ K_3^{CT}(s) &= \frac{1}{s^2+\gamma_2}\\ K_4^{CT}(s) &= \frac{s}{s^2+\gamma_2}\end{aligned}$$

We easily deduce the value of the coefficients γ_i by equating the denominator of $H^{target}(s)$ and that of $H^{litt}(s)$. The coefficients α_i are then obtained by inversion of the matrix system developed below.
The matrix is constructed by estimating each transfer function $K_i^{CT}(s)$ on N points in the complex plane (Laplace variable) and also the transfer function $H^{target}(s)$ in these same points:

$$\begin{pmatrix}\alpha_1 & \alpha_2 & \alpha_3 & \alpha_4\end{pmatrix}\underbrace{\begin{pmatrix}K_1^{CT}(s_1) & K_1^{CT}(s_2) & \cdots & K_1^{CT}(s_N)\\ K_2^{CT}(s_1) & K_2^{CT}(s_2) & \cdots & K_2^{CT}(s_N)\\ K_3^{CT}(s_1) & K_3^{CT}(s_2) & \cdots & K_3^{CT}(s_N)\\ K_4^{CT}(s_1) & K_4^{CT}(s_2) & \cdots & K_4^{CT}(s_N)\end{pmatrix}}_{\kappa^{CT}}$$
$$= \begin{pmatrix}H^{target}(s_1) & H^{target}(s_2) & \cdots & H^{target}(s_N)\end{pmatrix} \tag{E.2}$$

To obtain the coefficients α_i, we right-multiply each member of the equality by the pseudo-inverse matrix of κ^{CT}.

Appendix F

C code for the simulation of CT modulators by discretized CT state space model

F.1 The `simulateDSM_DCTSS` function

```
#include "mex.h"
#include "simulateDSM_DCTSS.h"

/*
 * simulateDSM_DCTSS.c
 * simulate CT DSM from its oversampled discretised state space
     representation
 * and outputs oversampled signals
 *
 * This is a MEX-file for MATLAB
 *
 */

/* Simulate the modulator using the DT SS representation. */
/* For efficiency, store the state in xn and compute from x. */
/* (These variables may be recycled internally, depending
   on the output variables requested.) */

#ifdef __STDC__
void simulateDSM_DCTSS()
#else
simulateDSM_DCTSS()
#endif
{
     int i,j,t, qi;
     double *pABCD, *ptr, *pxn, tmp;

     for( t=0; t<N; ++t ){ /* [xn;y] = ABCD*[x;u;v]; x=xn;*/
          /*mexPrintf("%d ",t);
          mexPrintf("\n");*/
          /* Compute y = C*x + D1*u and thence v for each quantizer */
          for( qi=0; qi<nq; ++qi){
               tmp = 0;
```

```
            for(i=0, pABCD=ABCD+order+qi, ptr=x; i<order; ++i, pABCD+=
                ABCD_rows)
            tmp += (*pABCD) * *ptr++;
            for(i=0, ptr=u; i<nu; ++i, pABCD+=ABCD_rows)
            tmp += (*pABCD) * *ptr++;
            if( py!=0 )
            *py++ = tmp;
            if (t % kOvS==0)
                v[qi] = quantize(tmp, nlev[qi]);
            else
                    v[qi]=*(v-nq);

        }

        /* Next compute xn = A*x + B*[u;v], */
        for( i=0, pxn=xn; i<order; ++i ){
            tmp=0;
            pABCD=ABCD+i;
            for( ptr=x, j=0; j<order; ++j, pABCD += ABCD_rows )
            tmp += *pABCD * *ptr++;
            for( ptr=u, j=0; j<nu; ++j, pABCD += ABCD_rows )
            tmp += *pABCD * *ptr++;
            for( ptr=v, j=0; j<nq; ++j, pABCD += ABCD_rows )
            tmp += *pABCD * *ptr++;
            *pxn++ = tmp;
            }
        u += nu;
        v += nq;
        if(xMax!=0){
            for( i=0; i<order; ++i){
            double abs=fabs(xn[i]);
            if( abs > xMax[i] )
                xMax[i] = abs;
            }
        }
        if(saveState){
            x = xn;
            xn += order;
        }
        else { /* swap x and xn */
            double *xtmp = x;
            x = xn;
            xn = xtmp;
        } /* if(saveState) */
    } /* for( t=0 .... ) */
}



/* The gateway function */
void mexFunction(    int nlhs, mxArray *plhs[],
                     int nrhs, const mxArray *prhs[])
{
    /* Variable declarations here */

    /* C code here */
```

```
    checkArgs(nlhs, plhs, nrhs, prhs);
    /* Print the variables being used
    mexPrintf("x=\n");          printMatrix(x,order,1);
    mexPrintf("\nABCD=\n");     printMatrix(ABCD,order+nq,order+nu+nq);
    */
    simulateDSM_DCTSS();
}
```

F.2 Header file

```
/*
 * simulateDSM_DCTSS.h
 * File header for simulateDSM_DCTSS.c
 *
 * Defines
 *  - quantize(...)
 *  - fatalError(...)
 *  - initializeX(...)
 *  - checkArgs(...)
 *
 * This is a MEX-file for MATLAB
 *
 */

#include <stdio.h>
#include <math.h>
#include "mex.h"

/* Global variables */
/* In an effort to make the code more readable and to cut down on the
   overhead
   associated with function calls, I have made many variables global.
      */
char *cmdName = "simulateDSM_DCTSS";
int
    order,      /* The order of the modulator. */
    nu,         /* The number of inputs, inferred from size(u,1). */
    nq,         /* The number of quantizers, inferred from nlev */
    N,          /* The number of time steps. */
    ABCD_rows,  /* The number of rows in ABCD */
    saveState,  /* Flag: keep track of the states. */
    kOvS;
double
    *u,         /* Points into the input array. */
    *v,         /* Points into the output array. */
    *x,         /* The current state. */
    *xn,        /* Points (in)to the (output) state array. */
    *xMax,      /* Points to the state maxima output array. */
    *py,        /* Points to the quantizer input output array. */
    *ABCD,      /* The ABCD array (col-wise) description of the
       moduator. */
    *nlev,      /* The number of quantizer levels. */
    default_nlev=2;

#ifdef __STDC__
double quantize(double yy, int nLevels)
```

```
#else
double quantize(yy, nLevels)
double yy;
int nLevels;
#endif
{
    double vv;
    if(nLevels%2) { /* Mid-tread quantizer */
        vv = 2*floor(0.5*(yy+1));
        if( vv > nLevels )
            vv = nLevels-1;
        else if( vv < -nLevels )
            vv = 1-nLevels;
    }
    else { /* Mid-rise quantizer */
        vv = 2*floor(0.5*yy)+1;
        if( vv > nLevels )
            vv = nLevels-1;
        else if( vv < -nLevels )
            vv = 1-nLevels;
    }
    return vv;
}

/* The following function is for debugging purposes only */
#ifdef __STDC__
void printMatrix(double *x, int m, int n)
#else
printMatrix(x, m, n)
double *x;
int m, n;
#endif
{
int i,j;
for(i=0; i<m; ++i){
    for(j=0; j<n; ++j)
        mexPrintf("%8.3f ",x[i+m*j]);
    mexPrintf("\n");
    }
}

#ifdef __STDC__
void fatalError(char *s)
#else
fatalError(s)
char *s;
#endif
{
    char msg[1024];
    sprintf(msg, "%s: %s", cmdName, s);
    mexErrMsgTxt(msg);
}

#ifdef __STDC__
void initializeX(const mxArray *M_x0)
#else
```

```
initializeX(M_x0)
mxArray *M_x0;
#endif
{
    int i;
    double *x0 = mxGetPr(M_x0);
    if( mxGetM(M_x0)!=order || mxGetN(M_x0)!=1 )
        fatalError("x0 must be an order x 1 column vector.");
    for(i=0; i<order; ++i)
        x[i] = *x0++;
}

void checkArgs( int nlhs, mxArray *plhs[],
                int nrhs, const mxArray *prhs[])
{
    int form;

    /* Verify the rhs (input) arguments */
    if( nrhs < 3 )
        fatalError("At least three input arguments are needed.");
    if( !mxIsDouble(prhs[0]) )
        fatalError("The input vector does not contain double-precision
            data.");

    u = mxGetPr(prhs[0]);
    nu = mxGetM(prhs[0]);
    N = mxGetN(prhs[0]);
    nq = 1;
    nlev = &default_nlev;
    if(nrhs>=4)
        if( !( mxIsEmpty(prhs[3]) || mxIsNaN(*mxGetPr(prhs[3])) ) ){
            nq = mxGetM(prhs[3]) * mxGetN(prhs[3]);
            nlev = mxGetPr(prhs[3]);
        }

    const mxArray *arg2=prhs[1];

    /* Determine the form of the modulator */
    if( mxIsClass(arg2,"zpk") ){                    /* NTF in zpk form */
        fatalError("ZPK input ! Unsupported input format. Provide the
            modulator under ABCD discretized SS representation");
    }
    else if( mxIsStruct(arg2) ){                    /* Obsolete NTF form */
        fatalError("Struct input ! Unsupported input format. Provide
            the modulator under ABCD discretized SS representation");
    }
    else if( mxIsNumeric(arg2) ){
        if( mxGetN(arg2)==mxGetM(arg2)+nu && mxIsDouble(arg2) ){
            form = 1;                           /* ABCD form */
            order = mxGetM(arg2)-nq;
        }
        else if( mxGetN(arg2)==2 ){
            fatalError("Unsupported input format. Provide the modulator
                under ABCD discretized SS representation");
        }
        else
```

```
            fatalError("ABCD must be an order+nq by order+nu+nq matrix.
                ");
    }
    else
        fatalError("The second argument is neither a proper ABCD matrix
            nor an NTF.");

    if( form==1 ){                  /* ABCD form */
        ABCD = mxGetPr(arg2);
    }
    else
        fatalError("Internal error. form != 1 !");

    ABCD_rows = order + nq;

    if (mxIsNumeric(prhs[2]) && !mxIsComplex(prhs[2]) && (mxGetM(prhs
        [2])==1 && mxGetN(prhs[2])==1)){
        kOvS=mxGetScalar(prhs[2]);
    }
    else{
        fatalError("kOvS is not valid.");
    }

    plhs[0] = mxCreateDoubleMatrix(nq,N,mxREAL);
    v = mxGetPr(plhs[0]);

    x = (double *)mxCalloc(order,sizeof(double));
    if(nrhs>=5){
        if( !( mxIsEmpty(prhs[4]) || mxIsNaN(*mxGetPr(prhs[4])) ) )
            initializeX(prhs[4]);
        }

    /* Verify the lhs (output) arguments */
    saveState=0;
    py=0;
    xMax=0;
    switch(nlhs){
        case 4:
            plhs[3] = mxCreateDoubleMatrix(nq,N,mxREAL);
            py = mxGetPr(plhs[3]);
        case 3:
            plhs[2] = mxCreateDoubleMatrix(order,1,mxREAL);
            xMax = mxGetPr(plhs[2]);
        case 2:
            plhs[1] = mxCreateDoubleMatrix(order,N,mxREAL);
            xn = mxGetPr(plhs[1]);
            saveState=1;
            break;
        case 1:
            break;
        default:
            fatalError("Incorrect number of output arguments.");
    }
    if( !saveState )
        xn = (double *)mxCalloc(order,sizeof(double));
```

```
}
```

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