Broadband direct RF digitization receivers

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Broad-band Direct RF Digitization Receivers

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A Céline,
Louis et Martin

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Abstract

The Holy Grail radio receiver architecture for Software Radio makes uses of direct RF digitization. The early RF signal digitization theoretically provides maximum re-configurability of the radio front-end to multiple bands and standards, as opposed to analog-extensive front-ends.

In addition, in applications for which a large portion of the RF input signal spectrum is required to be received simultaneously, the RF direct digitization architecture could provide the most power-and-cost-effective front-end solution. This is typically the case in centralized architectures, for which a single receiver is used in a multi-user environment (data and video gateways) or in re-multiplexing systems. In these situations, this highly-digitized architecture could dramatically simplify the radio front-end, as it has the potential to replace most of the analog processing.

In this Ph.D thesis, we study the trade-offs, from RF to DSP domains, which are being involved in direct RF digitization receivers. The developed system-level framework is applied to the design of a cable multi-channel RF direct digitization receiver. Special focus is provided on the design of an optimum RF signal conditioning, on the specification of time-interleaved analog-to-digital converter impairments, including clock quality, and on some algorithmic aspects (automatic gain control loop, RF front-end amplitude equalization control loop). The two-chip implementation is presented, using BiCMOS and 65nm CMOS processes, together with the block and system-level measurement results. The solution is highly competitive, both in terms of area and RF performance, while it drastically reduces power consumption.

Synthèse

Contexte

Les communications numériques ont évolué pour répondre à la demande des consommateurs pour accroître l'accès à la navigation Internet, TV, vidéo à la demande, jeux interactifs et de réseaux sociaux. Cette augmentation de débit de données est obtenue en utilisant des techniques avancées de traitement du signal, des modulations plus complexes, et des bandes passantes plus larges de signal. Par conséquent, des récepteurs haute performances capables de traiter des signaux large bande passante, sont nécessaires pour les équipements de communication grand-public hauts de gamme, et pour les équipements d'infrastructure. Par exemple, cela inclut les passerelles domestiques Cable & Satellite, les émetteurs-récepteurs d'infrastructures cellulaires, la détection du spectre de TVWS.

Comme la bande passante du signal accroît sans cesse dans ces applications, l'utilisation de récepteurs à bande étroite peut devenir non efficace en termes de puissance. En outre, la pression sur les coûts peut rendre les récepteurs multicanaux plus rentable qu'une multitude de récepteurs à bande étroite. Fig 1 montre un récepteur satellite typique: une unité extérieure translate la bande satellite 10 GHz dans la gamme à 950 MHz-2150 MHz. Comme plusieurs canaux 36 MHz sont nécessaires pour permettre à l'utilisateur de regarder et enregistrer simultanément plusieurs vidéos HD, un récepteur à large bande capturant la pleine bande 950 MHz-2150 MHz pourrait remplacer plusieurs récepteurs RF de 36 MHz.

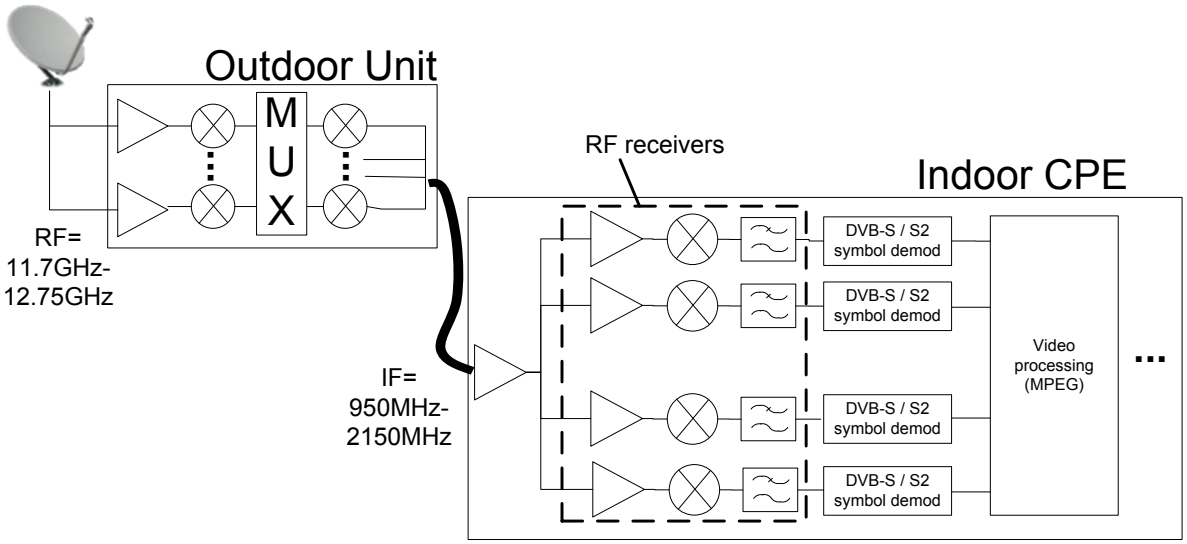


Fig 1. Satellite broadband multi-channel reception

Dans les récepteurs utilisés en défense, radio-astronomie, infra-structure de télécommunications qui nécessitent de multiples récepteurs, les avancées dans les procédés CMOS peuvent ouvrir la porte à la mise en œuvre de traitement du signal avancé. L'utilisation de ces techniques n'est généralement pas viable pour des applications à large bande, puisque l'utilisation de récepteurs à large bande en parallèle n'est actuellement pas compétitif en puissance et en taille / poids. Par exemple, dans les communications numériques et les applications radars en S-band/L-band, la polyvalence et les avantages en performance que la formation numérique de faisceaux (Fig 2, droite) peut apporter, par rapport à la formation analogique de faisceaux (Fig 2, à gauche), ne sont pas possibles en raison de l'absence de récepteurs à large bande et faible puissance.

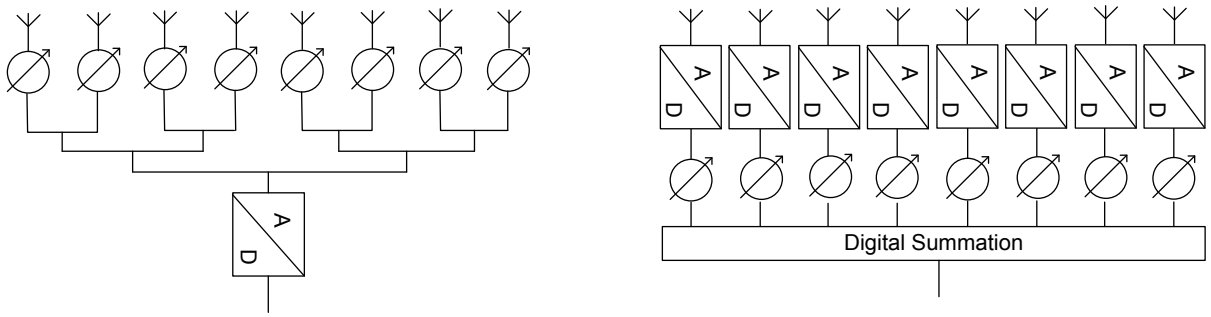


Fig 2. Gauche: Formation analogique de faisceaux. Droite: Formation numérique de faisceaux

Objectifs de recherché identifiés

La recherche des récepteurs hautement intégrés, dans la gamme DC-3 GHz, et la capture de signaux de quelques centaines de MHz de bande passante est ciblé dans ce travail. Les récepteurs à numérisation directe RF sont attrayants pour ces applications à large bande, mais plusieurs étapes doivent être prises en compte afin de fournir des solutions performantes.

Les activités de recherche identifiées comme nécessaires pour relever ces défis sont les suivantes:

- Conception au niveau système des récepteurs à numérisation directe RF, de la RF au traitement de signal numérique, en prenant en compte les aspects à large bande et les compromis entre le coût, la consommation d'énergie, les performances RF et la taille.
- Conception de CAN faible puissance, haute performance dans une technologie CMOS
- Conception de chaîne de sélection du canal numérique à faible puissance et haute vitesse
- Conception d'un conditionnement optimal de signal RF qui détend les exigences sur le CAN
- Démontration de la performance du système complet, du traitement de signal RF à la bande de base

Cette thèse présente la conception au niveau système de récepteurs à échantillonnage et numérisation directs RF, de la théorie à la réalisation et mesures pour un récepteur câble multi-canal. Cette activité a impliqué plus de 20 personnes chez NXP, y compris les concepteurs RF, analogiques, à signaux mixtes et numérique, les intégrateurs, ingénieurs d'application, les ingénieurs logiciels, chef de projet, marketing.

En outre, il est également le résultat d'un partenariat fort avec quelques entreprises partenaires et clients de l'industrie semi-conducteurs. L'auteur agit comme un architecte de système et de circuits intégrés, et ingénieur principal.

Les principales contributions de cette thèse sont les suivants:

- L'analyse et la conception au niveau système des récepteurs à échantillonnage et numérisation directs RF
    - L'analyse théorique de la distorsion non-linéaire large-bande, pour les stratégies d'échantillonnage passe-bas et passe-bande
    - L'analyse théorique des défauts des convertisseurs analogique-numérique haute-vitesse (pureté horloge, bruit de quantification, erreurs d'entrelacement temporel, bruit dépendant du signal) dans un contexte de réception large bande
- La conception d'un conditionneur de signal RF optimisé pour une application, incluant:
    - Un égaliseur RF programmable multi-pente, utilisant une seule inductance, avec son algorithme de contrôle

- Une boucle de contrôle de gain mixte combinant un détecteur RMS et un détecteur crête

- Contribution à la réalisation d'un produit récepteur RF multi-canaux, à numérisation directe, meilleur que l'état de l'art en consommation d'énergie, coût (surface de silicium), et équivalent aux récepteurs existants sur les aspects performances RF.

Etat de l'art des récepteurs RF

Les techniques de traitement du signal sont passés en revue, du mélangeur radiofréquence, à l'échantillonnage, au analogique-numérique. L'état de l'art des récepteurs radio est établi, motivant les travaux sur l'architecture à numérisation directe.

L'état de l'art des récepteurs radio DC-3 GHz utilise la classification suivante:

• Les récepteurs à temps continu (Fig 3, à gauche): ils sont basés sur un mélangeur RF à temps continu. Le traitement de signal ultérieur est également essentiellement réalisé en utilisant des techniques à temps continu, jusqu'à l'échantillonneur et le CAN.

• Les récepteurs à temps discret (Fig 3, à droite): ils sont basés sur un circuit d'échantillonnage RF, qui parfois réalise également une translation de fréquence. Le traitement de signal analogique à temps discret peut être utilisé pour relâcher les contraintes sur la dynamique du CAN. Alternativement, la numérisation peut être effectuée directement en sortie de l'échantillonneur.

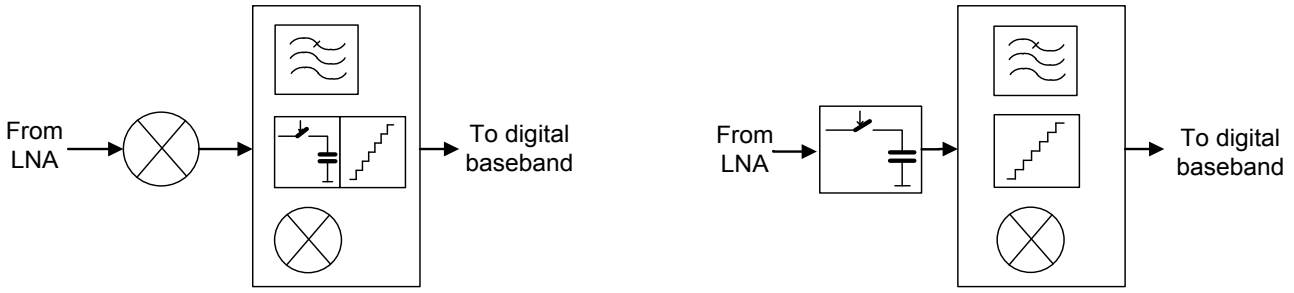


Fig 3. Gauche: récepteur à temps continu, droite: récepteur à temps discret

Pour les applications qui nécessitent la réception d'un canal à bande étroite, les architectures homodyne, low-IF et les récepteurs à temps discret sont les architectures les plus appropriées (coût, taille, puissance).

Pour les applications qui nécessitent la sélection d'un signal de bande passante modérée, les architectures à IF numérique, à IF large bande ou homodyne sont les plus appropriées (coût, taille, puissance).

Dans le cadre des récepteurs opérant dans la bande RF DC-3 GHz et nécessitant la réception de plusieurs canaux RF sur une bande de 1 GHz, une solution à base de mélangeur nécessiterait plusieurs récepteurs parallèles, chacun capturant une sous-bande. Une mise en œuvre possible utilise un mélangeur complexe et l'échantillonnage et la numérisation des signaux analytiques.

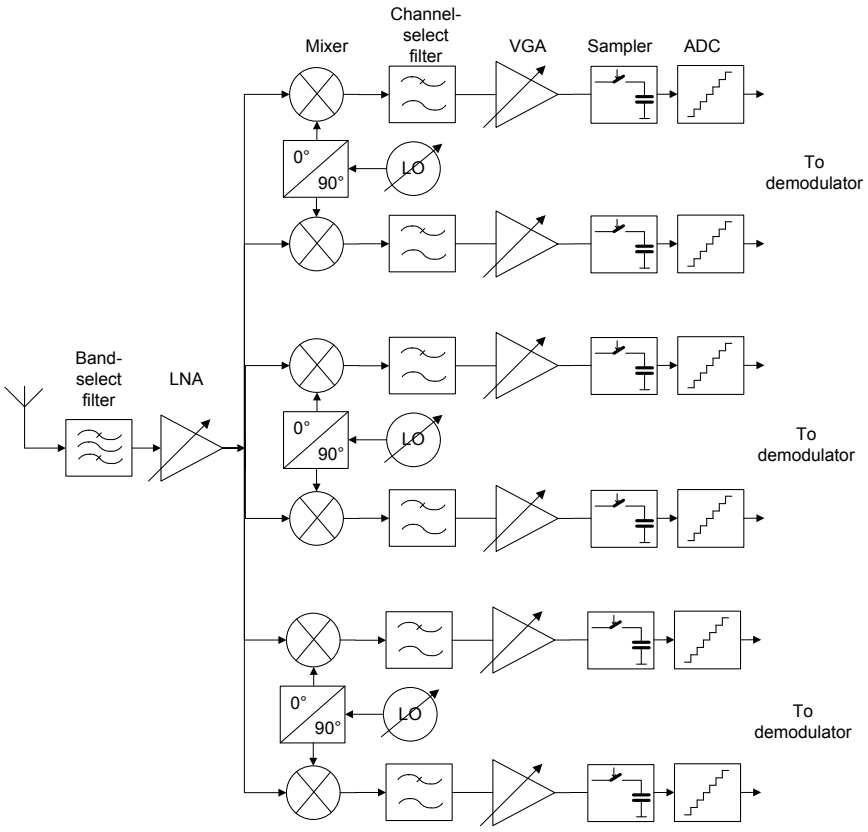


Fig 4. Découpe en sous-bandes avec des mélangeurs et utilisant des signaux analytiques

Comme étudié dans [66] pour des applications dans la gamme DC-1GHz, utilisant des signaux analytiques, une décomposition en sous-bandes avec conversion de fréquence analogique semble impliquer un coût plus élevé, sans apporter d'avantage significatif sur la consommation d'énergie, par rapport à des récepteurs à numérisation directe. En outre, cette décomposition en sous-bandes met une limite sur la largeur de bande maximale pouvant être capturée. L'architecture est donc limitée à la réception de plusieurs canaux à bande étroite, et doit être considérée comme un moyen d'étendre la bande passante et la dynamique des CAN existants.

Les récepteurs à numérisation directe ont le potentiel de fournir une réception très haut débit, à faible puissance et de faible taille dans plusieurs types d'applications:

- **Applications à "forte densité", dans lesquelles une forte proportion du spectre du signal d'entrée est requis.**

Ces applications sont généralement multicanaux avec un grand nombre de voies, ou des applications UWB. Ici, la numérisation directe RF a aussi la particularité de permettre le traitement du signal numérique sur la bande complète du signal RF.

- **Applications "multi-octave":**

Dans ces applications, les mélangeurs RF posent de sérieux défis et influencent fortement l'architecture du récepteur, notamment en raison du mélange avec des harmoniques LO. L'échantillonnage direct RF simplifie l'architecture et résout ces problèmes.

La numérisation directe comporte plusieurs avantages supplémentaires, par rapport aux autres architectures de récepteurs, qui viennent avec la numérisation:

- Accordabilité: un signal RF à l'intérieur de la bande passante d'entrée ADC (ou du moins dans une zone de

Nyquist) peuvent être traitées, car pas de filtre RF à bande étroite est utilisé. La sélection du canal numérique peut être accordable à faible coût, en particulier dans les technologies CMOS avancées

- Flexibilité: comme la bande du signal RF complet est disponible en format numérique, de nouvelles techniques de traitement du signal, qui ne sont pas possible avec les récepteurs analogiques, peuvent être appliquées à la numérisation directe des récepteurs:
    - FFT large bande (détection de spectre pour la radio cognitive, l'observation du spectre dans les applications militaires, les communications ultra large bande)
    - filtrage à phase linéaire (sélection de canal pour les récepteurs des systèmes de communication)
    - corrections numériques (post-correction de distorsion non linéaire large bande par exemple)

Cadre de conception pour les récepteurs à échantillonnage et numérisation directs

Le cadre de conception au niveau système pour les récepteurs à échantillonnage et numérisation directs RF est établi au chapitre 2, reliant les spécifications du système de communication aux défauts du récepteur radio, avec un accent particulier sur les aspects échantillonnage, numérisation, y compris à la distorsion non linéaire large bande, les défauts d'entrelacement temporel des CAN et la pureté de l'horloge d'échantillonnage.

Les contributions du bruit de récepteur sont analysées, en tenant compte du bruit thermique du frontal RF, et de la quantification et de la saturation de l'ADC. La distorsion non linéaire dans un système à large bande est examiné, ce qui permet d'étudier l'impact de la stratégie d'échantillonnage (passe-bas, passe-bande) sur les performances du système.
L'impact des disparités entre les CAN à entrelacement temporel est également étudié, en fournissant des expressions qui permettent de spécifier les décalages dans un environnement large bande.
Le transfert du bruit de phase, à partir du signal d'horloge vers le signal échantillonné, y compris dans la bande, et dans les régions éloignées de bruit de phase, sont mis en équations. Ceci permet de prendre en compte l'impact du bruit de phase sur des modulations en quadrature, ainsi que le mélange réciproque avec les canaux adjacents ou brouilleurs.

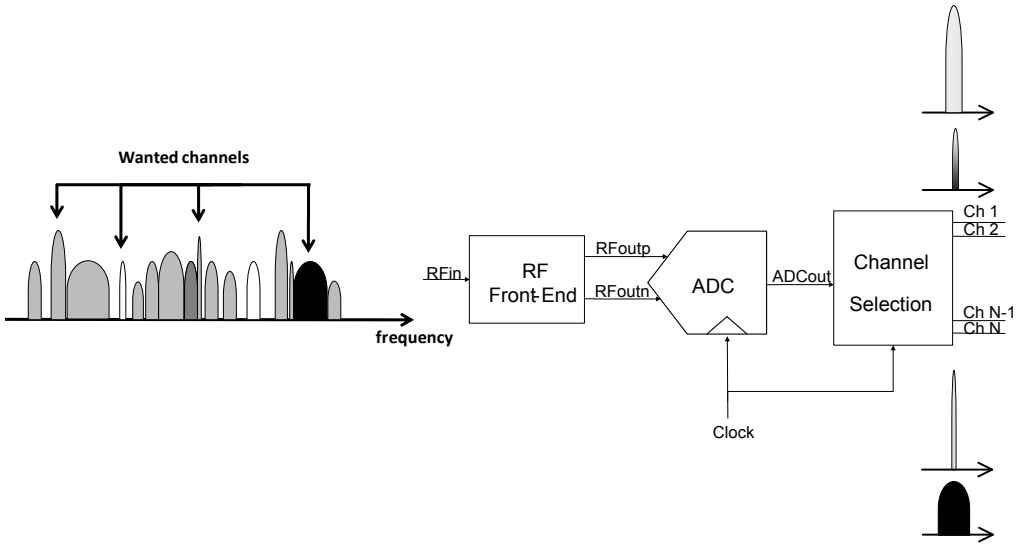


Fig 5. Récepteur à numérisation directe RF

La performance d'un CAN peut être représentée graphiquement en fonction du facteur de charge, pour différentes résolutions de CAN, et en supposant un signal d'entrée qui occupe la bande de Nyquist complet [DC; Fs / 2]:

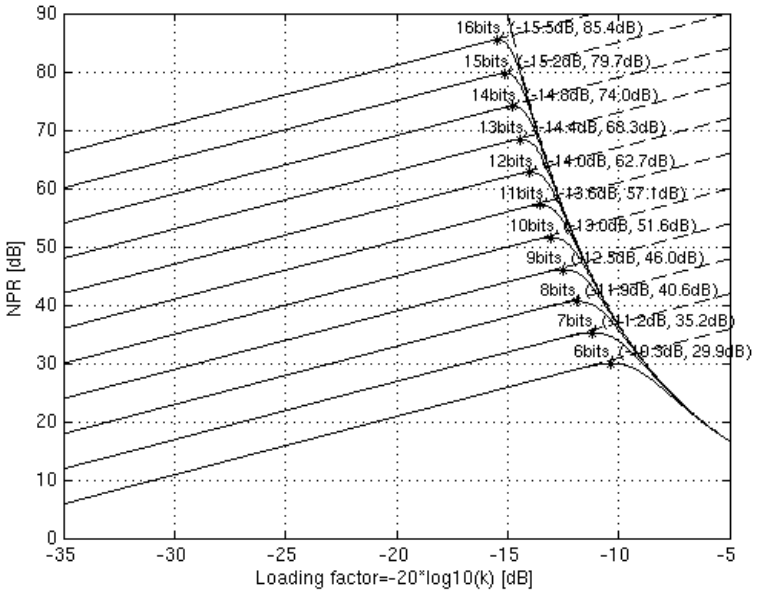


Fig 6. Rapport signal à bruit & facteur de charge optimum pour différentes résolutions de CAN (signal Gaussien)

Pour des facteurs de charge faibles, le système est limité par le bruit de quantification / bruit thermique. Dans ce cas, la sensibilité du NPR au facteur de charge est très faible (1 dB de perte NPR pour 1 dB d'atténuation du signal)

D'autre part, pour des facteurs de charge plus élevés, le système est limité par le bruit de saturation du CAN. Dans une telle situation, le NPR est très sensible au facteur de charge.

Compte tenu de cette sensibilité, il est généralement nécessaire pour l'ADC d'être utilisé légèrement en dessous du facteur de charge optimal. La conception de la boucle de contrôle automatique de gain (CAG) peut être critique, en fonction de la dynamique de la voie de communication et les brouilleurs RF potentiels.

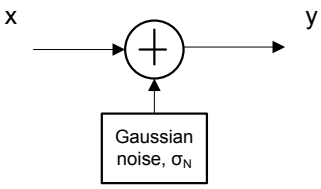
Le plancher de bruit d'un CAN de type Nyquist à signaux forts est généralement supérieur par rapport aux petits signaux. Cette dégradation des performances près de la pleine échelle du CAN peut être due à:

• L'augmentation du bruit thermique, causé, par exemple, par un rejet de dégradation du bruit généré par les sources de courant utilisé dans les structures différentielles

• La distorsion non linéaire d'ordre élevé

Si cette dégradation est négligée, la performance de bruit du CAN (SNR) est spécifiée au facteur de charge plus faible, l'impact sur les performances du système est inconnu. Alternativement, la performance du CAN peut être sur-spécifiée à pleine échelle, afin d'avoir une marge de sécurité sur les performances du système. Comme les CAN sont le goulot d'étranglement dans les récepteurs à numérisation directe RF, aucune des deux approches n'est satisfaisante. Nous sommes donc à la recherche d'une méthode analytique pour déterminer l'impact de la dégradation de bruit des CAN à forts signaux.

L'approche proposée consiste à modéliser ce phénomène par un bruit gaussien, dont l'amplitude dépend du signal. Le modèle proposé est illustré dans la Fig 7:



$$\sigma_N(x) = f(x)$$

Fig 7. Modèle proposé pour le bruit dépendant du signal

De toute évidence, la dégradation de bruit pour des signaux d'entrée gaussiens a beaucoup moins d'impact que pour des signaux sinusoïdaux. En effet, pour 12 dB de dégradation du plancher de bruit à grande échelle, en supposant une dépendance du second ordre, la performance ADC pour un signal gaussien n'est dégradée que de 1,7 dB avec un facteur de charge de -12-dB. En comparaison, le SNR de l'onde sinusoïdale est dégradé de 8,6 dB.

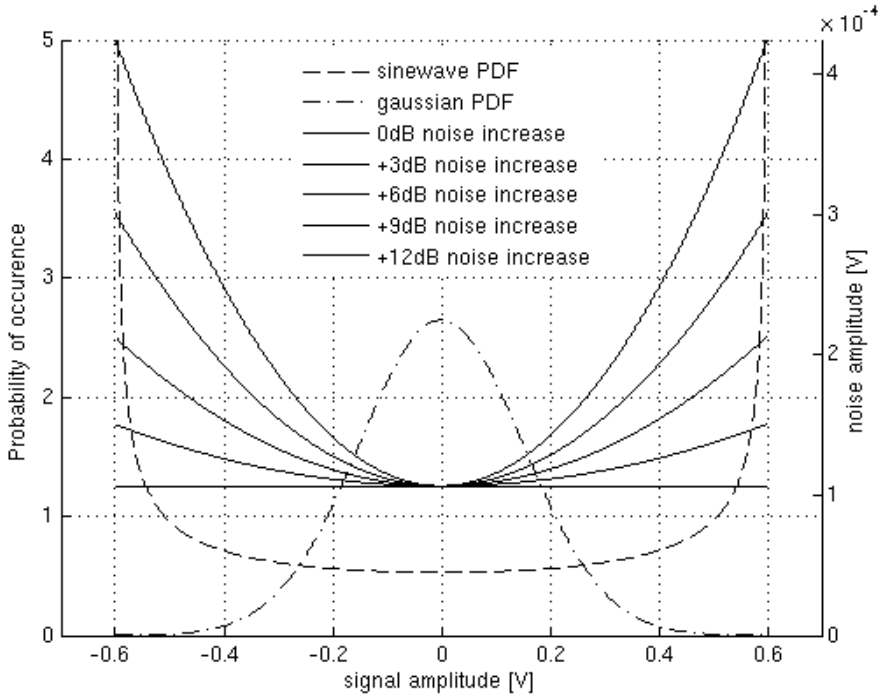


Fig 8. Fonction de probabilité (signal sinusoïdal, signal gaussien), et bruit dépendant du signal

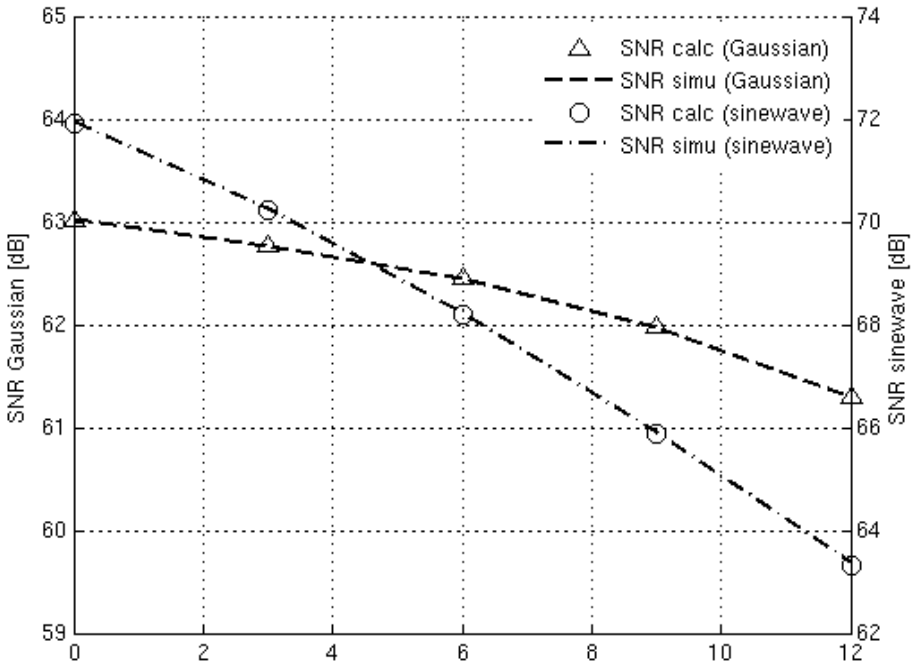


Fig 9. SNR calculé et simulé en fonction de la dégradation de bruit à forts signaux (gauche: signal sinusoïdal; droite: signal gaussien)

Par conséquent, pour les systèmes dans lesquels les signaux gaussiens sont traités, l'effort de conception doit porter sur la réduction du bruit à petit signal, tandis que la dégradation de bruit admissible pour signaux de niveau élevé peut être facilement évaluée en utilisant la théorie développée.

Cette analyse peut également être adaptée à différentes distributions de signaux d'entrée et à différents profils de dégradation de bruit, en fonction du contexte d'application. En outre, l'analyse et ses conclusions sont également valables pour des fonctions analogiques RF et IF.

La distorsion non-linéaire est étudiée dans le contexte des récepteurs large bande. Cette analyse permet notamment de comparer l'impact de la non-linéarité du frontal RF pour plusieurs stratégies d'échantillonnage.

Fig 10 donne un aperçu de l'impact sur la stratégie d'échantillonnage distorsion non linéaire, en signalant la réjection de non-linéarité du frontal RF que le filtre anti-repliement peut apporter, pour les zones de Nyquist de un à quatre:

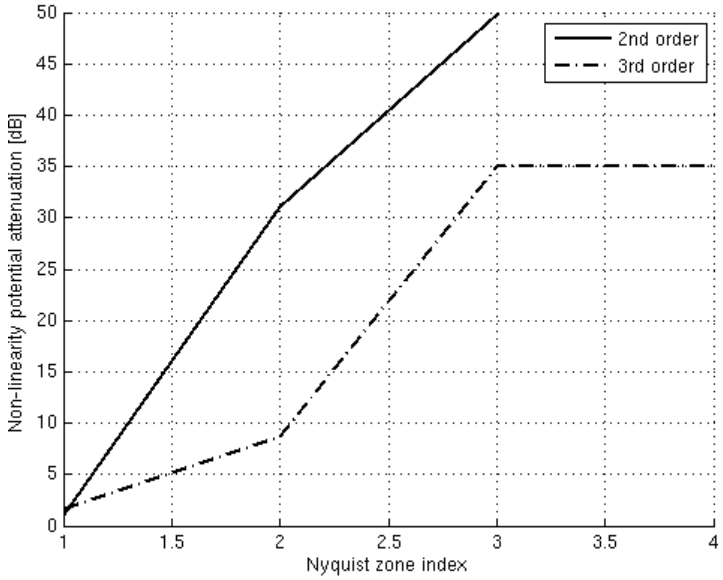


Fig 10. Amélioration potentielle de distorsion non-linéaire, en fonction de la stratégie d'échantillonnage

Le frontal RF convertit l'entrée RF asymétrique en un signal de sortie différentiel. Cependant, en pratique, les sorties ne sont pas parfaitement équilibrés ni en gain ni en phase. Comme montré dans [78], la principale conséquence est une annulation non idéale de la distorsion non-linéaire du second ordre. L'analyse présentée ci-dessous combine l'impact des déséquilibrages de gain et de phase sur la distorsion non linéaire du second ordre.

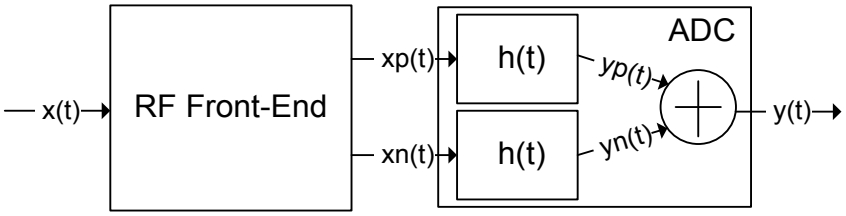


Fig 11. Interface entre le frontal RF et l'échantillonneur

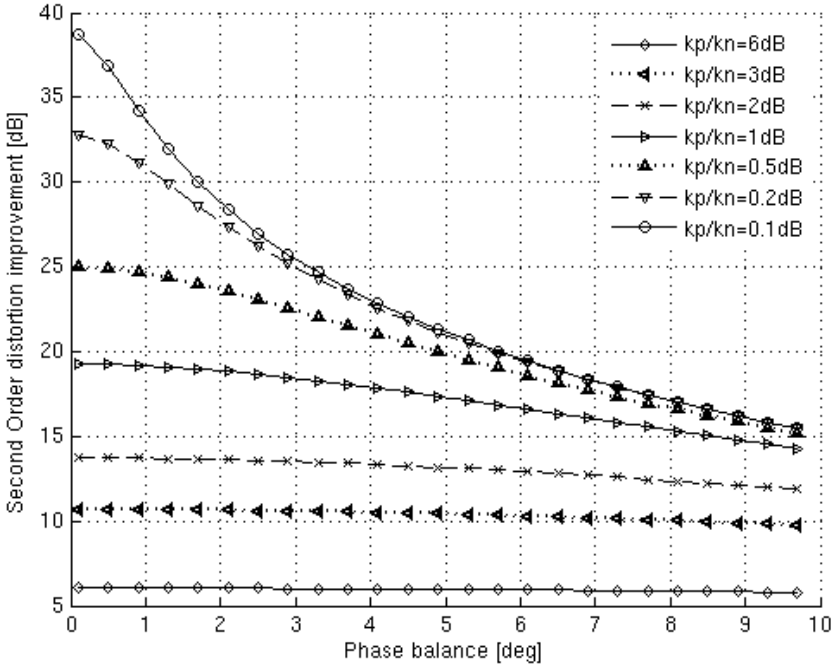


Fig 12. Impact des déséquilibres de gain et de phase sur la distorsion non-linéaire du second ordre

Par exemple, si 20 dB d'amélioration de non-linéarité sont recherchés, 5 degrés de déséquilibre de phase et 0,5 dB de déséquilibre de gain sont une combinaison acceptable.

La problématique du désappairage des canaux d'un CAN à entrelacement temporel est aussi revue dans un contexte de réception large bande, en liant le désappairage aux spécifications système du récepteur.

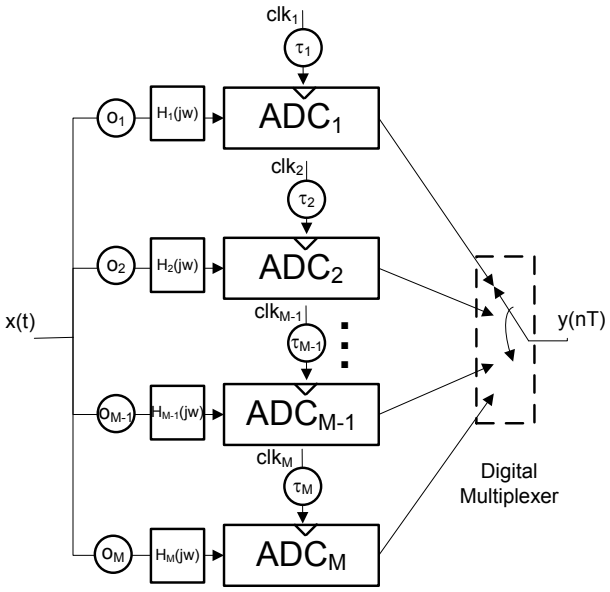


Fig 13. CAN à entrelacement temporal avec désappairage des canaux

Fig 14 montre un exemple d'un signal d'entrée multi-tons à large bande, échantillonné par un CAN à entrelacement temporel à quatre canaux, et un désappairage entre les horloges d'échantillonnage. Les tons d'entrée multiples sont

égaux et référencé à 0 dB, tandis que les trois images du signal d'entrée, causées par le désappairage d'horloge, sont fonction de la fréquence:

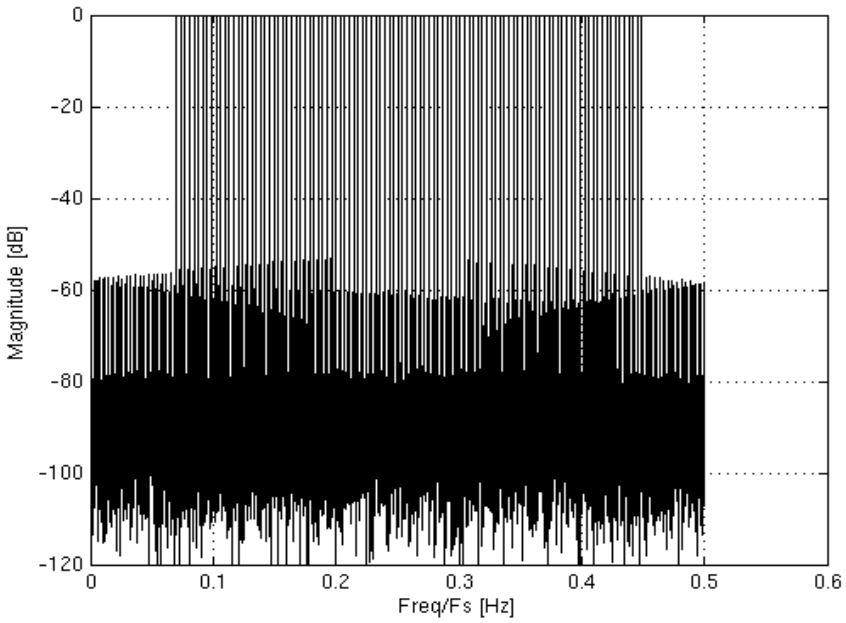


Fig 14. Numérisation d'un signal multi-tons large bande, avec un CAN à 4 canaux, et $\sigma_{skew}=3.5x10^{-4}xFs$

Le transfert de bruit de phase, de l'horloge vers le signal échantillonné, est revu:

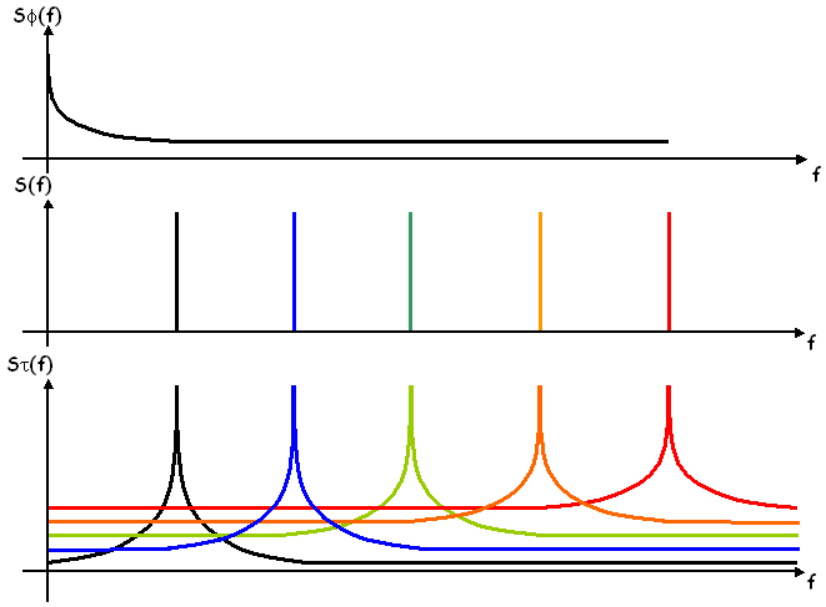


Fig 15. Convolution entre le spectre du bruit de phase de l'horloge et le spectre du signal d'entrée multi-tons

L'impact du bruit de phase est étudié dans ses différentes zones:

- Impact du bruit de phase dans la bande, sur une porteuse modulée en quadrature
- Impact du bruit de phase sur le mélange réciproque avec des brouilleurs proches ou lointains.

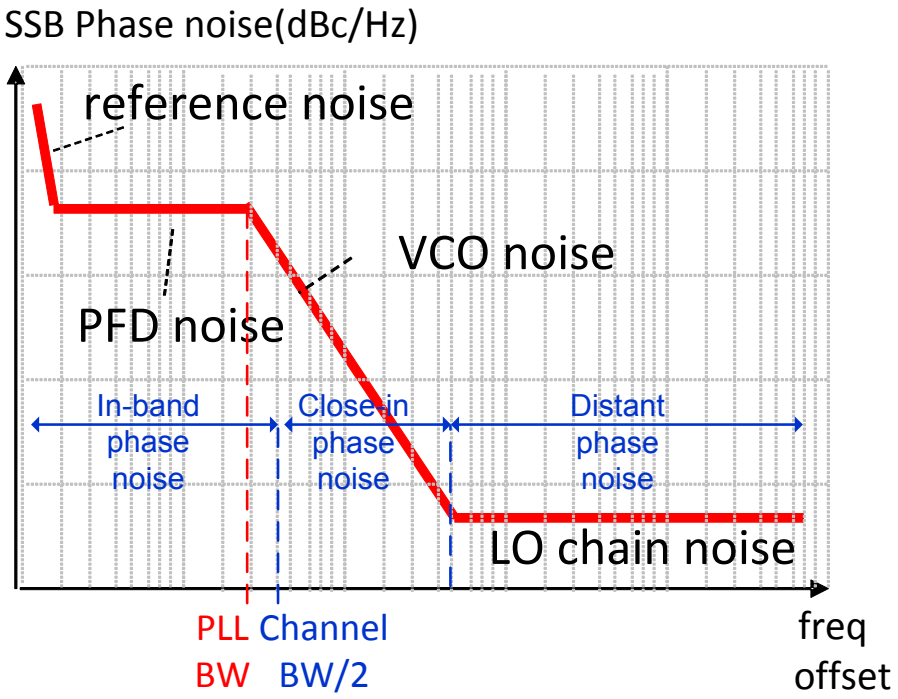


Fig 16. Profil typique de bruit de phase sur une horloge

Application à la réception multi-canal câble

Dans le chapitre 3, la théorie développée dans le chapitre 2 est appliquée à la conception au niveau système d'un récepteur câble multi-canaux utilisant la numérisation directe. Un conditionnement optimal du signal RF est mis en œuvre.

En premier lieu, le contexte applicatif est introduit :

La concurrence entre les opérateurs câble et les autres opérateurs Télécom est non seulement de fournir les meilleurs réseaux, capables de fournir le plus haut débit de données, mais aussi d'assurer la capacité de recevoir une grande quantité de données dans les équipements locaux du client, à faible coût et faible consommation d'énergie.

Comme l'augmentation de la qualité du signal sur les réseaux câblés nécessiterait un changement de l'infrastructure, et se traduirait par coût très élevé, l'augmentation du débit de données est réalisée par l'augmentation de la bande passante du signal. Cette augmentation est mise en œuvre par la transmission de plusieurs canaux RF en parallèle. Plus particulièrement, le marché demande la capacité de recevoir 1 Gbps par maison, ce qui nécessite la réception simultanée de 24 canaux RF.

La tendance pour une utilisation nomade de l'information au sein d'une maison, fait évoluer l'architecture de la maison d'un réseau de récepteurs distribués, basée sur les décodeurs, à une architecture centralisée (Fig 17), articulée autour d'une passerelle domestique.

Les données sont redistribuées de la passerelle vers les clients en utilisant un réseau local (Ethernet, Wifi, MoCA, PLC).

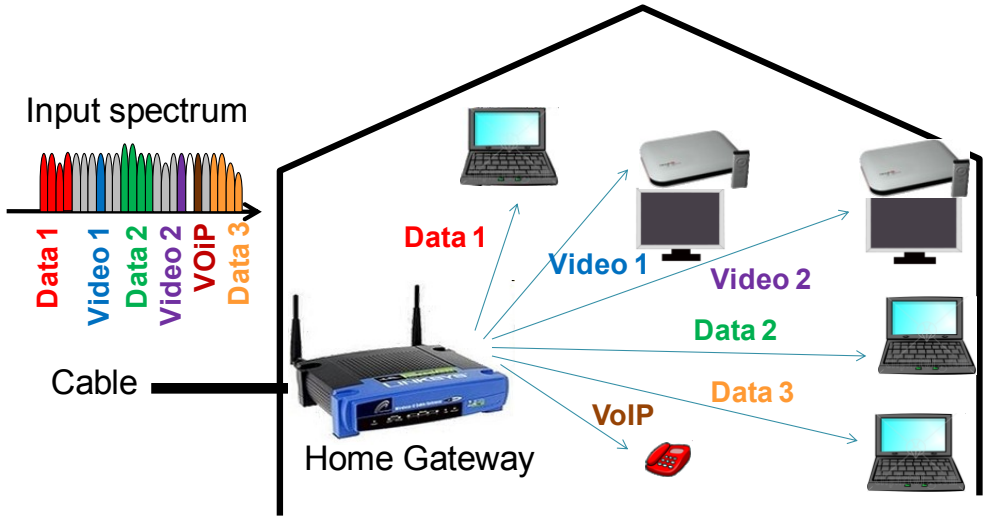


Fig 17. Architecture de récepteur centralisé, organisé autour d'une passerelle domestique

Il est donc nécessaire de construire un récepteur capable de capturer 24 canaux RF indépendants, sur l'ensemble du spectre des canaux câble (Fig 18).

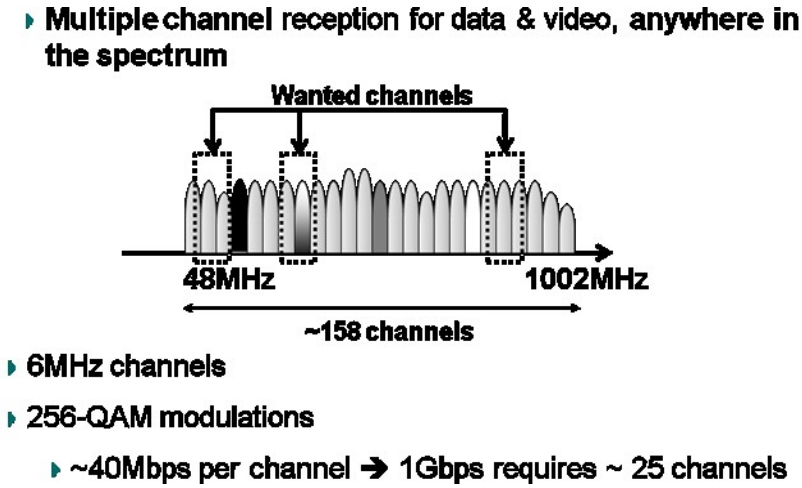


Fig 18. Spectre d'un signal de réseau cable typique

Les récepteurs RF câble courants (Fig 19) sont réalisés à partir d'une combinaison de récepteurs mono-canal et de récepteurs large bande.

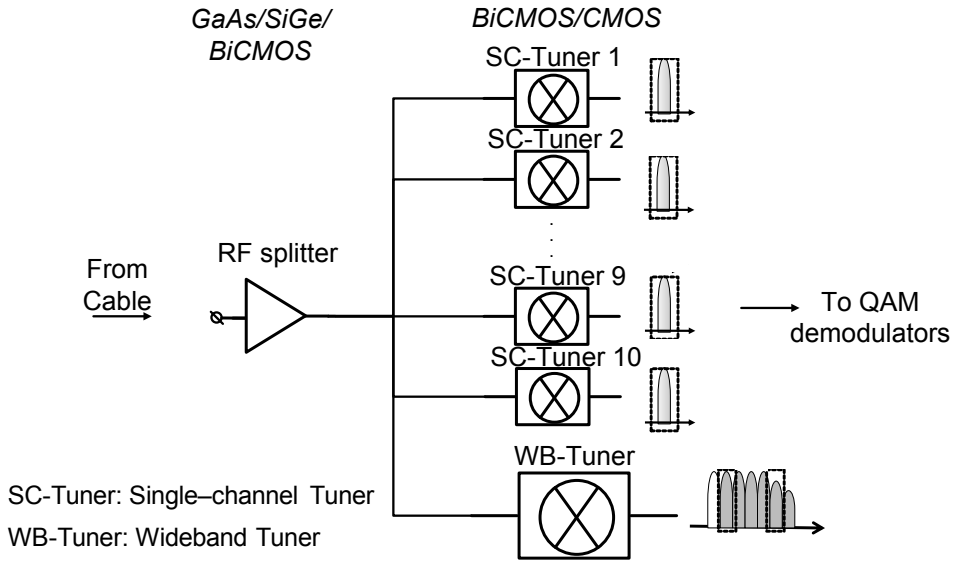


Fig 19. Récepteurs multi-canaux pour passerelle domestique

Les récepteurs large bande sont plus économiques et efficaces que les récepteurs mono-canal, mais limitent fortement les opérateurs câble, puisque les canaux RF tranmis sont contraints à être adjacents (dans une sous bande de 64MHz à 100MHz).

En utilisant des récepteurs mono-canal à l'état de l'art (moyenne de la puissance consommée dans [29], [33], [35]), Fig 20 montre que plus de 20 W seraient nécessaires pour mettre en œuvre le frontal RF d'une passerelle domestique à 24 canaux indépendants:

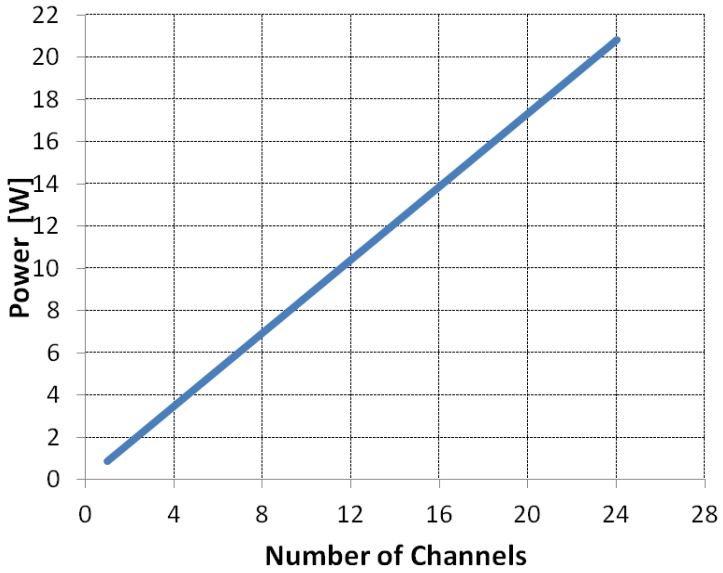


Fig 20. Puissance consommée par un frontal RF de passerelle domestique basée sur des récepteurs mono-canal

Cette analyse néglige la puissance supplémentaire rendue nécessaire par l'amplificateur de tête (division du signal d'entrée RF vers les multiples récepteurs).

Dans ce contexte, un frontal RF basé sur la numérisation directe (Fig 21) permettrait de réduire le matériel RF et analogique, et donc de diminuer le coût et la consommation d'énergie de la solution système.

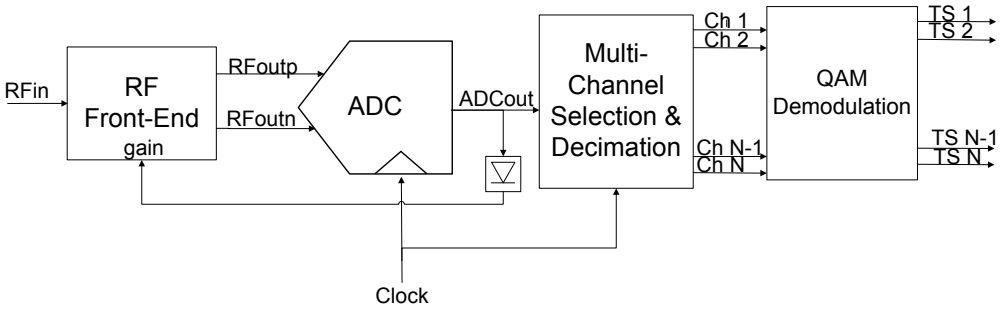


Fig 21. Récepteur à échantillonnage et numérisation directs

Fig 22 (en haut) illustre l'introduction d'un bruit blanc (quantification, thermique), causée par la conversion analogique-numérique, sur un signal RF incluant une atténuation des canaux à hautes fréquences: une très bonne performance est obtenue aux fréquences basses, grâce à forte amplitude des canaux, alors qu'une performance insuffisante est obtenue à des fréquences élevées en raison de la faible amplitude des canaux. La différence de performance (SNR) entre les canaux à basse et haute fréquence est égale à l'inclinaison du signal du câble (inclinaison = 10 dB dans TC2).

Fig 22 (en bas) montre l'effet positif qu'un égaliseur d'amplitude RF peut avoir: l'amplitude du signal est maintenant égalisée avant l'introduction de la source principale de bruit, la performance (SNR) est donc égalisée sur toute la bande de fréquences.

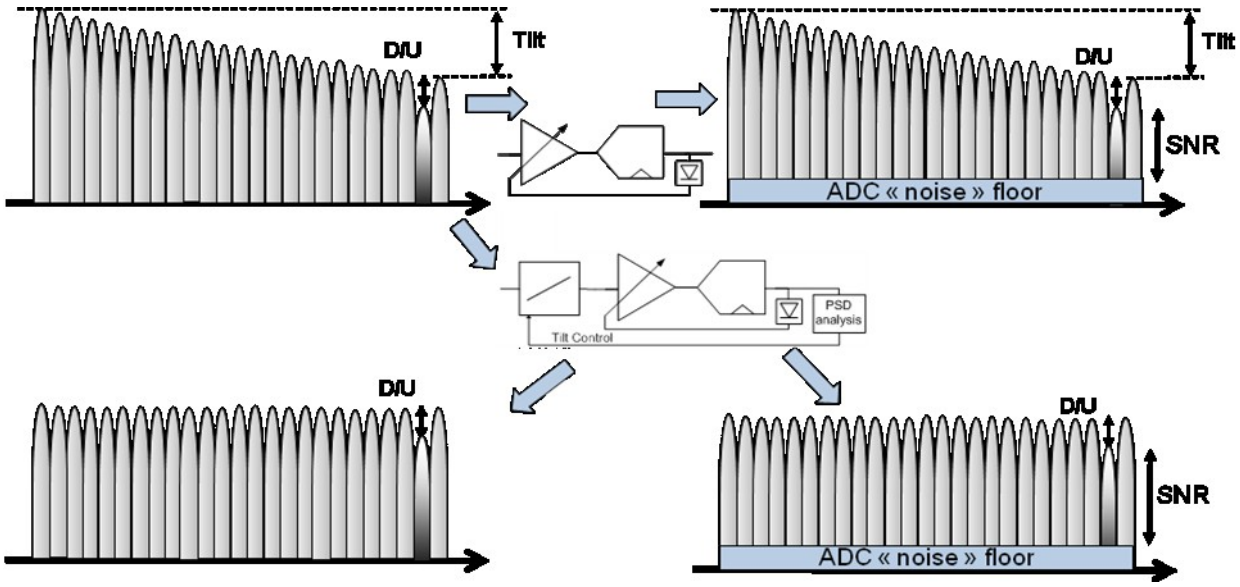


Fig 22. Récepteur à numérisation directe classique (haut), Récepteur avec égaliseur RF (bas)

Le gain de performance offert par un égaliseur RF est la différence (en dB) entre l'amplitude de canal à haute fréquence avec et sans égaliseur. Ceci est illustré sur Fig 23 (gauche) avec -10 dB d'inclinaison, et quantifié en fonction de l'inclinaison sur Fig 23 (droite).

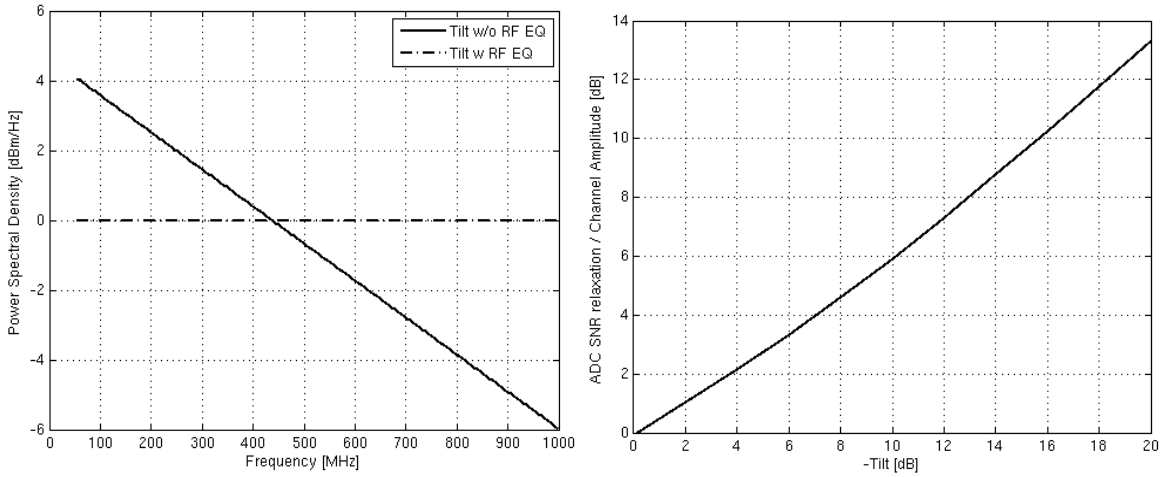


Fig 23. Amplitude des canaux en fonction de l'égalisation RF (gauche, -10dB d'inclinaison). Relâchement de la spécification du SNR d'un CAN grâce à un égaliseur RF (droite)

Les defaults majeurs des récepteurs à numérisation directe (distorsion non-linéaire, erreurs d'entrelacement temporal, et bruit de phase) sont simulés en utilisant une modélisation dans le domaine temporel, et comparés à la théorie.

Conception et mesures

Le chapitre 4 présente la conception et réalisation des fonctions de conditionnement de signal RF et du frontal à signaux mixtes. Les résultats de mesures du récepteur, aux niveaux bloc et système, sont mis en perspective dans un environnement large bande.

Le récepteur multi-canaux câble est réalisé par une approche en deux puces, afin de garantir une intégrité du signal optimale:

• Le frontal RF (RFFE) traite les signaux d'entrée asymétrique à faible amplitude, en utilisant un procédé propriétaire BiCMOS 0.25um [98] haute performance. Il intègre complètement les fonctions d'amplification, d'égalisation d'amplitude dans la bande 50-1002 MHz, de filtre anti-repliement et fournit un signal différentiel au circuit à signaux mixtes.

• Les frontal à signaux mixtes échantillonne le signal d'entrée différentiel, le quantifie, et intègre la sélection numérique de 24 canaux RF, à l'aide d'un procédé CMOS 65nm.

La solution combine un système de réception multi-canaux, un système de réception mono-canal, et un système d'émission multi-canaux (Fig 24).

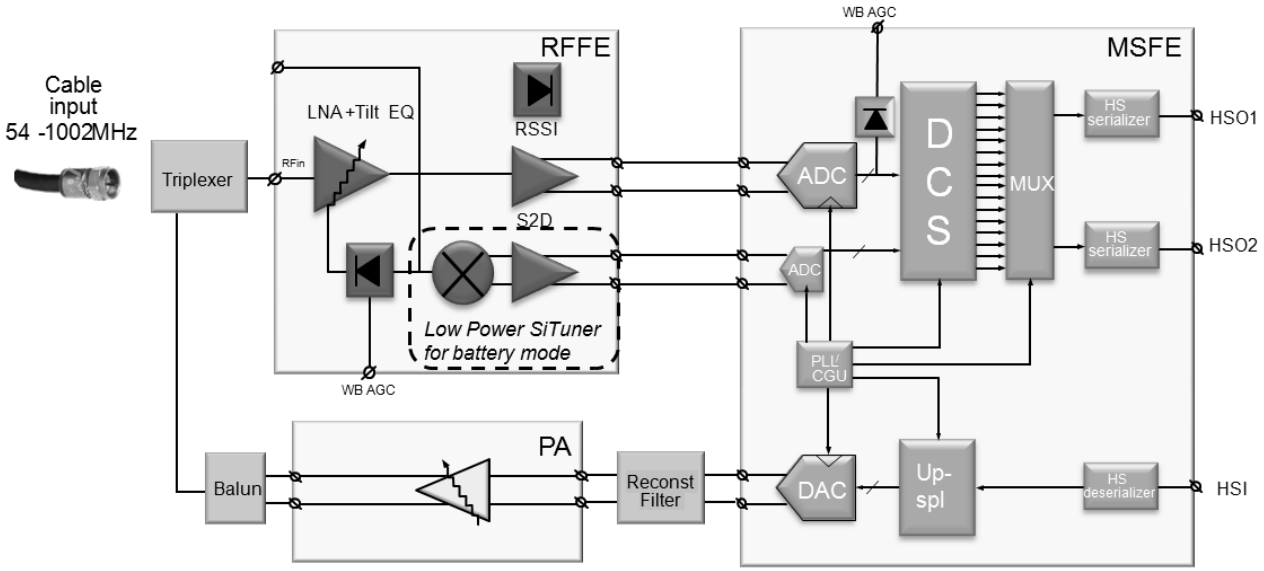


Fig 24. Schéma-bloc du récepteur multi-canaux câble

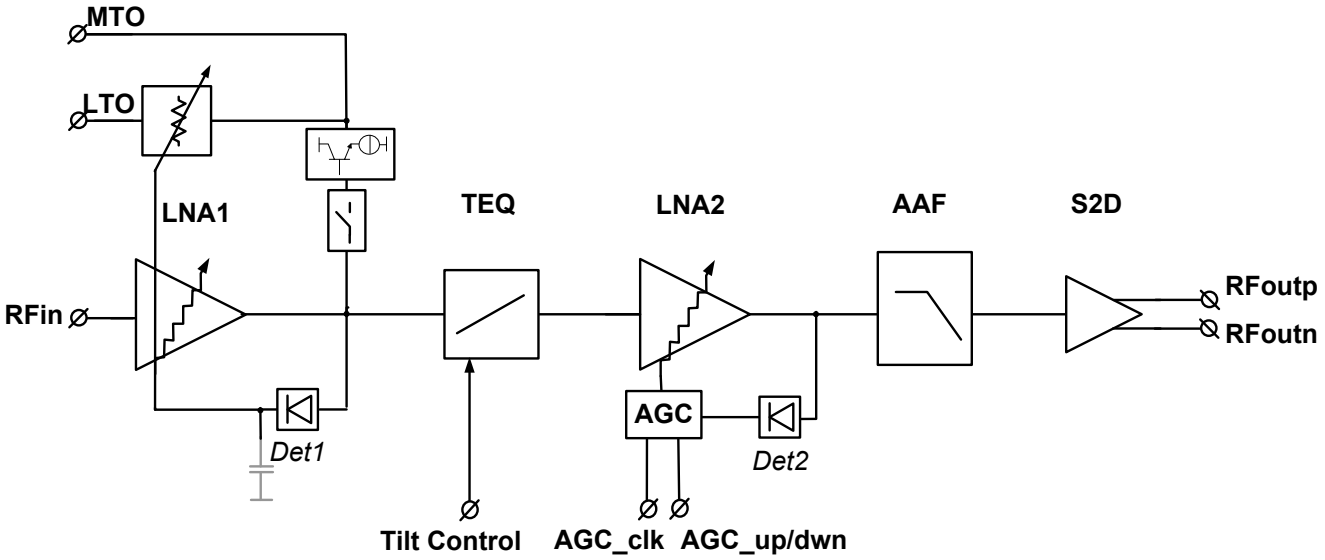


Fig 25. Schéma conceptuel du chemin de réception multi-canaux du frontal RF

Choix principaux:

• L'entrée et le chemin RF asymétriques ont été choisis afin d'éviter le coût d'un transformateur externe, et dans le but de réduire le coût des filtres internes (égaliseur RF, filtre anti-repliement), ce qui permet aussi de minimiser la consommation d'énergie.

• Comme l'égalisation n'est pas seulement bénéfique pour l'ADC, mais aussi pour les autres blocs RF, l'égaliseur RF a été placé aussi proche que possible de l'entrée du câble.

• Le bruit et la distorsion non-linéaire de tous les blocs situés entre le filtre anti-repliement et le CAN sont repliés dans la bande utile par l'opération d'échantillonnage. Ceci a motivé le choix de placer le filtre anti-repliement aussi proche que possible de l'entrée du CAN. La volonté de garantir une bonne adaptation d'impédance large bande

entre la sortie du RFFE et l'entrée du CAN a dicté de placer le filtre anti-repliement juste en amont du convertisseur asymétrique-différentiel.

Le premier bloc de la chaîne RF (Fig 26, [97]) est un amplificateur faible bruit (LNA1), qui présente une dynamique de gain de 18 dB, pour traiter des signaux d'entrée de -15 dBmV à +15 dBmV par canal. Le LNA comprend une boucle de contrôle de gain, afin de fournir le meilleur compromis NF / linéarité quel que soit le niveau d'entrée du câble. Les transitions de gain du LNA1 sont transparentes afin de ne pas perturber le démodulateur QAM. Ce LNA fournit aussi une recopie du signal RF pour les tuners supplémentaires (sorties MTO et LTO).

Après amplification de signal à un niveau de +35 dBmV, un égaliseur RF entièrement intégré corrige l'inclinaison du spectre du signal d'entrée sur la bande de fréquence utile. Sept configurations d'égalisation sont disponibles à partir de -10 dB jusqu'à +15 dB. Le 2ème LNA amplifie le signal après correction de l'inclinaison avec une dynamique de -12 dB à +15 dB, et un pas de 0,2 dB. Son gain est commandé pour une boucle de contrôle de gain doit le détecteur est situé, soit à la sortie du LNA2 (Det2 sur Fig 25), soit à la sortie du CAN (Fig 24).

Le filtre anti-repliement du 3ème ordre, elliptique, entièrement intégré, protège le récepteur contre les repliements potentiels, causés par du bruit ou la distorsion non linéaire hors bande utile. Le dernier étage réalise une conversion assymétrique-différentiel et une adaptation d'impédance entre le front-end RF et l'entrée différentielle de l'ADC.

Dans la topologie sélectionnée [102], représentée sur Fig 26, l'égaliseur entièrement intégré à inclinaison variable utilise une seule bobine d'inductance 5 nH, configurée dans un résonateur, soit série, soit parallèle, et égalise sur une largeur de bande de 1 GHz.

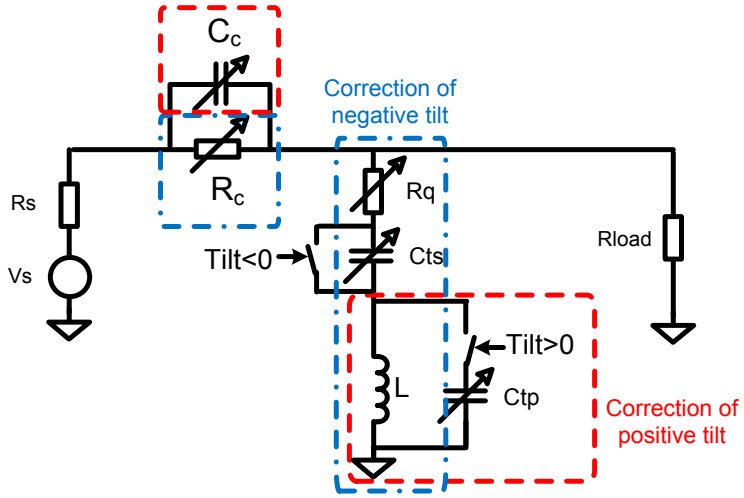


Fig 26. Topologie de l'égaliseur RF

Dans les deux configurations, le circuit LC résonne à 1,1 GHz. Lorsqu'il est configuré en parallèle (L, Ctp, Fig 27), l'égaliseur atténue les basses fréquences (comportement passe-haut). Lorsqu'il est configuré en série (L, Cts, Fig 28), l'égaliseur atténue les hautes fréquences (comportement passe-bas).

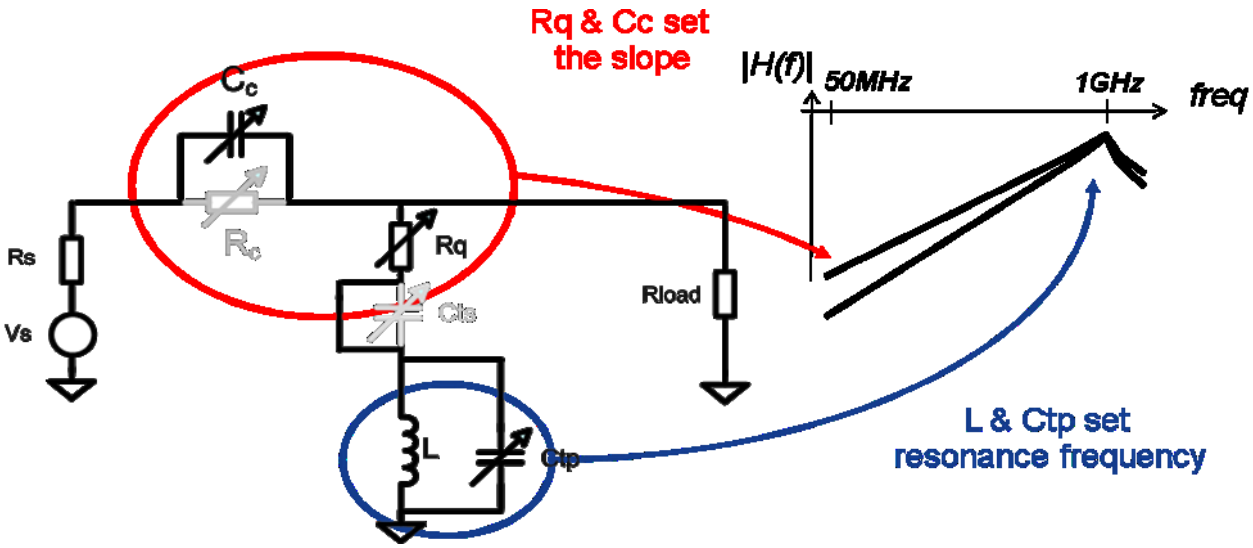


Fig 27. Egaliseur RF configuré dans un résonateur parallèle

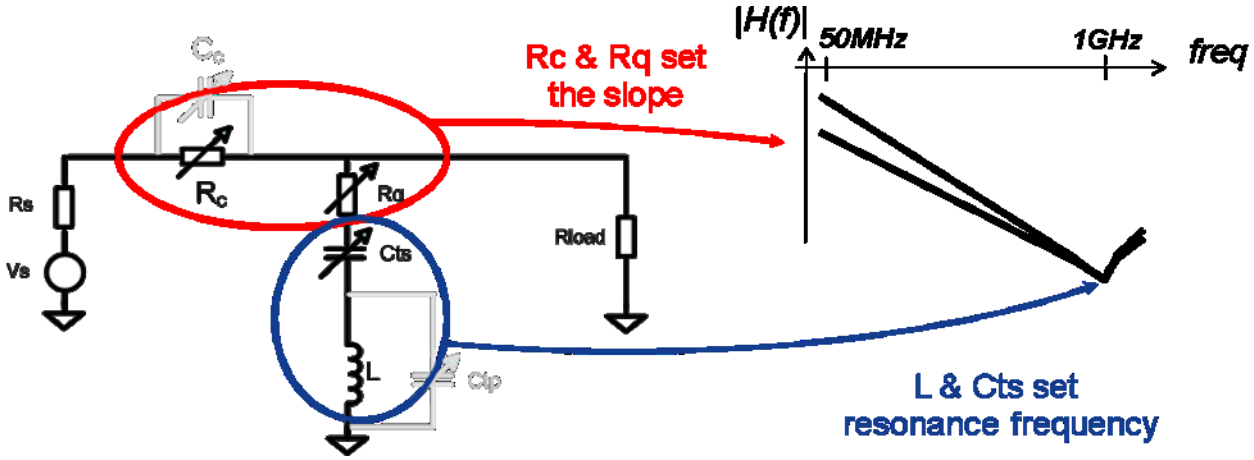


Fig 28. Egaliseur RF configuré dans un résonateur série

La programmabilité de l'inclinaison de l'égaliseur est obtenue en utilisant des composants variables (Rc, Cc, Rq, Cts et Ctp). À cette fin, des batteries de condensateurs et résistances ont été conçues.

Le gain du RFFE en fonction de la fréquence est indiqué sur Fig 29, qui montre les 7 inclinaisons de l'égaliseur, et l'atténuation du filtre anti-repliement.

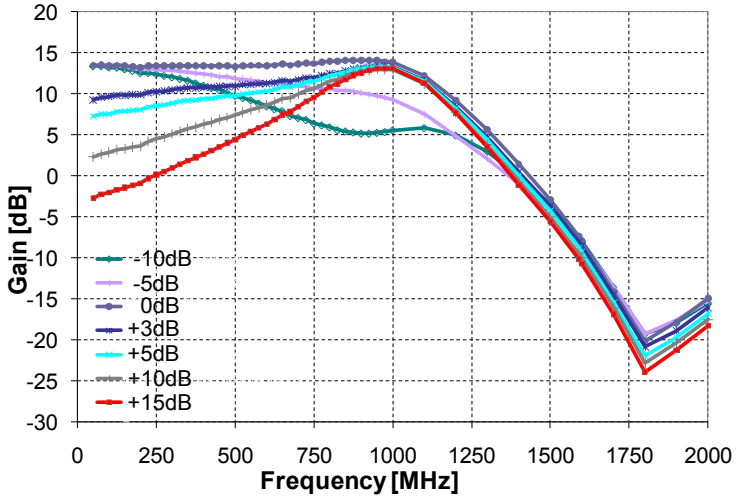


Fig 29. Mesure des fonctions de transfert du frontal RF pour plusieurs programmations d'égaliseur

Fig 30 (à gauche) indique le facteur de bruit du frontal RF. Le NF est inférieur à 4,3 dB, pour son gain maximum. Fig 30 (à droite) indique l'amplitude relative des produits de distorsion non-linéaire, du deuxième et troisième ordre, avec un signal d'entrée comprenant 158 sinusoides, chacune à +15 dBmV. Toutes les raies de distorsion non linéaire (CSO, CTB) sont meilleures que 58 dBc.

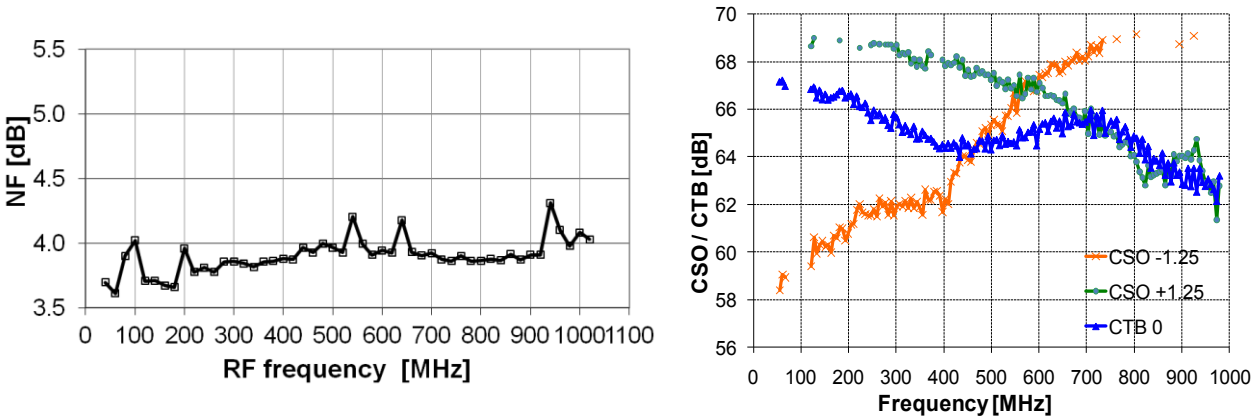


Fig 30. Facteur de bruit du frontal RF (gauche), et CSO/CTB (droite)

L'architecture de frontal à signaux mixtes (MSFE) est illustrée dans Fig 31. Il est similaire au démonstrateur technologique que nous avons présenté dans [103], mais est maintenant un produit qui comprend la réception simultanée de 24 canaux. Cela impose la nécessité d'un sérialiseur à grande vitesse afin de transférer des données vers un SoC ou FPGA avec une faible puissance et un nombre limité de broches.

Le signal différentiel est échantillonné par un CAN qui est reliée à la sélection de canal numérique (DCS) du filtre qui effectue la conversion en bande de base de chacun des canaux. Le DCS est en mesure de sélectionner simultanément et convertir les 24 canaux (6 ou 8 MHz) à un taux d'échantillonnage de 13,5 MS/s, en format complexe (IQ). Après filtrage et décimation, les 24 canaux sont envoyés vers le SoC/FPGA par deux liens séries 6 Gbps SATA III.

Le récepteur nécessite seulement un quartz externe pour servir de référence à la boucle à verrouillage de phase (PLL) intégrée.

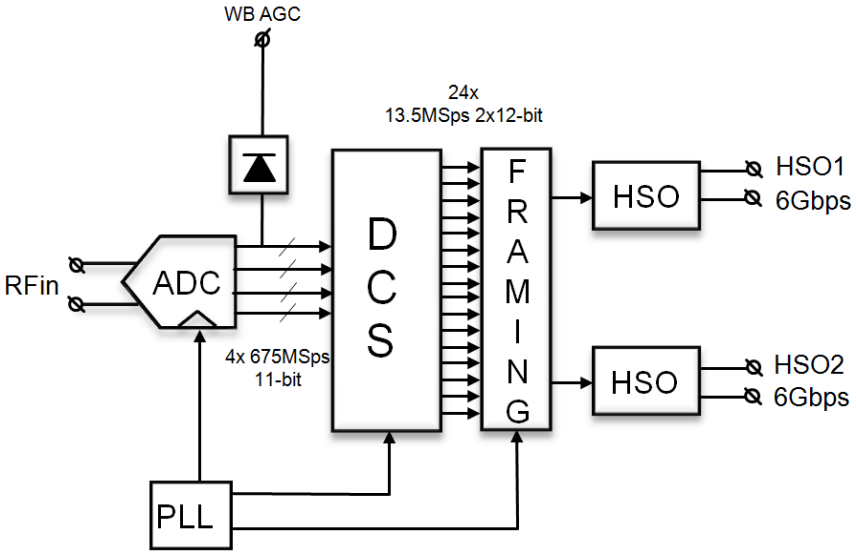


Fig 31. Schéma bloc du frontal à signaux mixtes

Une architecture de CAN à entrelacement temporel hiérarchique ([86], [87]) est utilisée en raison de son fort potentiel de parallélisme. Afin de surmonter les limites précisées en 1.3.5, seulement quatre échantillonneurs (TH) passifs sont entrelacées.

Comme le montre Fig 32, chaque échantillonneur est relié à 16 CAN SAR à base réduite pour un total combiné de 64 CAN unitaires, disposées en quatre quarts (QADC). Chaque échantillonneur conduit sa gamme QADC avec un interface multiplexé en boucle ouverte (Fig 33). Comme l'étage à gain en tension unitaire (buffer) est placé dans la boucle de conversion à approximations successives, sa distorsion non linéaire est expérimentée à la fois par le signal d'entrée et le signal de rétroaction du CNA. Comme le fonctionnement du convertisseur à approximations successives est basé sur la détection de passage à zéro du signal de différence, et comme les signaux d'entrée et du CNA sont pareillement déformés, il en résultera une décision correcte.

Les quatre séquenceurs déterminent l'ordre de randomisation et la séquence de hachage qui sont utilisés pour étaler la puissance de toutes les corrections résiduelles et des erreurs de gain.

La platitude du gain et la minimisation de la réflexion de signal sont assurées par une d'adaptation d'impédance large-bande à double terminaison entre les frontaux RF et mixtes. Une terminaison 100 Ω différentielle passive est montée en parallèle à l'entrée des échantillonneurs, à l'intérieur du frontal mixte. Les variations d'impédance dynamiques sont réduites au minimum en s'assurant que deux THS (sur quatre) sont toujours connectés au signal d'entrée. Ces mesures permettent de conduire le TH directement avec le RFFE, sans étage tampon à l'entrée du frontal mixte.

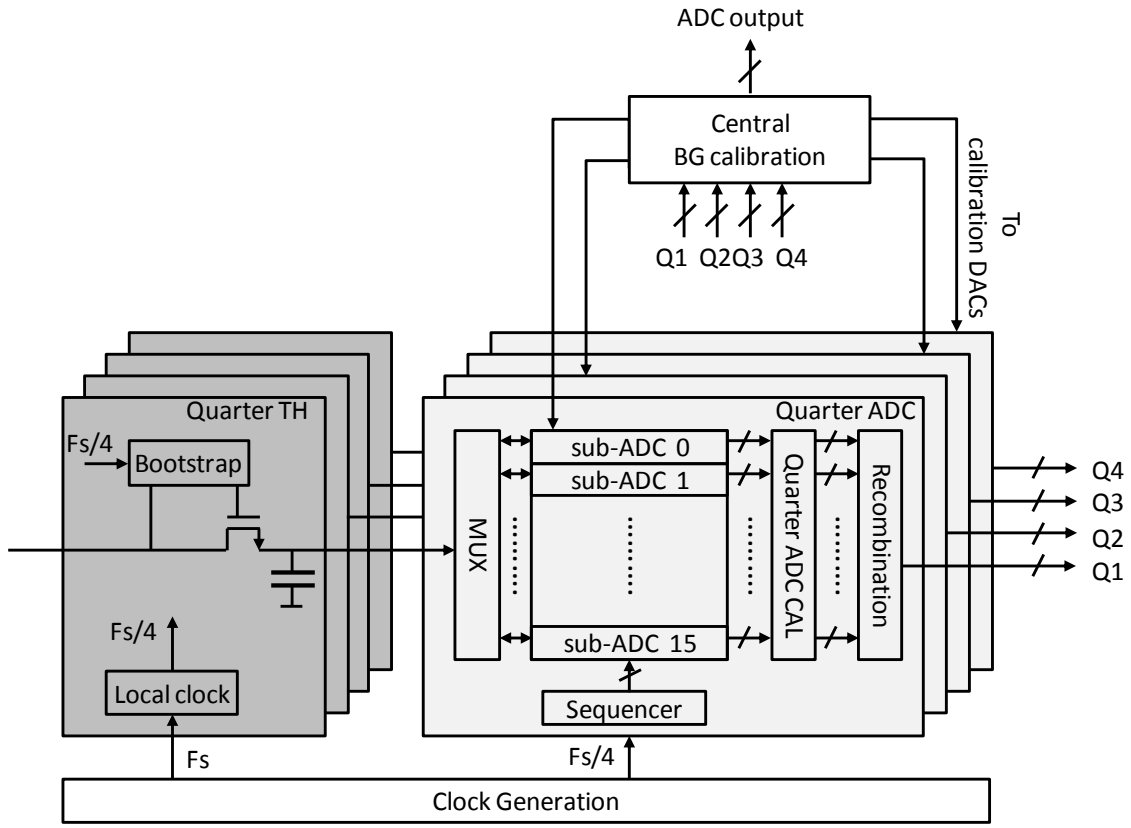


Fig 32. Schéma bloc du CAN

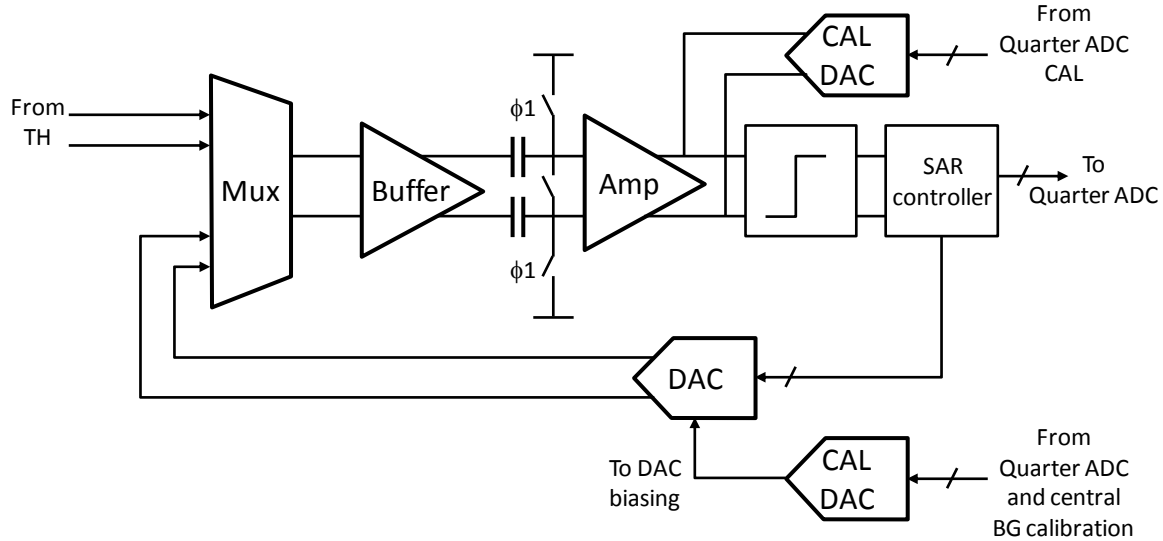


Fig 33. Architecture du convertisseur à approximations successives, et interface avec les échantillonneurs

La sélection de canaux mise en œuvre ([103], [104]) utilise une approche en deux étapes:
• Le spectre du signal d'entrée est divisé en 8 sous-bandes (A, B, ..., G, H sur Fig 34) par une fonction de séparateur de bande hiérarchique, basée sur une cascade (trois étages) de séparation de bande en deux sous-bandes. Comme ce séparateur de bande est sélectif, la fréquence d'échantillonnage peut être réduite progressivement, sans repliement conséquent. Cette fonction (cascade de trois étages) est instanciée une seule fois dans le circuit intégré.

• 24 sélecteurs numériques de canaux sont connectés à la sortie du séparateur de bandes: ils sont réalisés à partir d'un mélangeur numérique et d'un filtre de décimation qui réduit la fréquence d'échantillonnage de 375 MHz à 13,5 MHz.

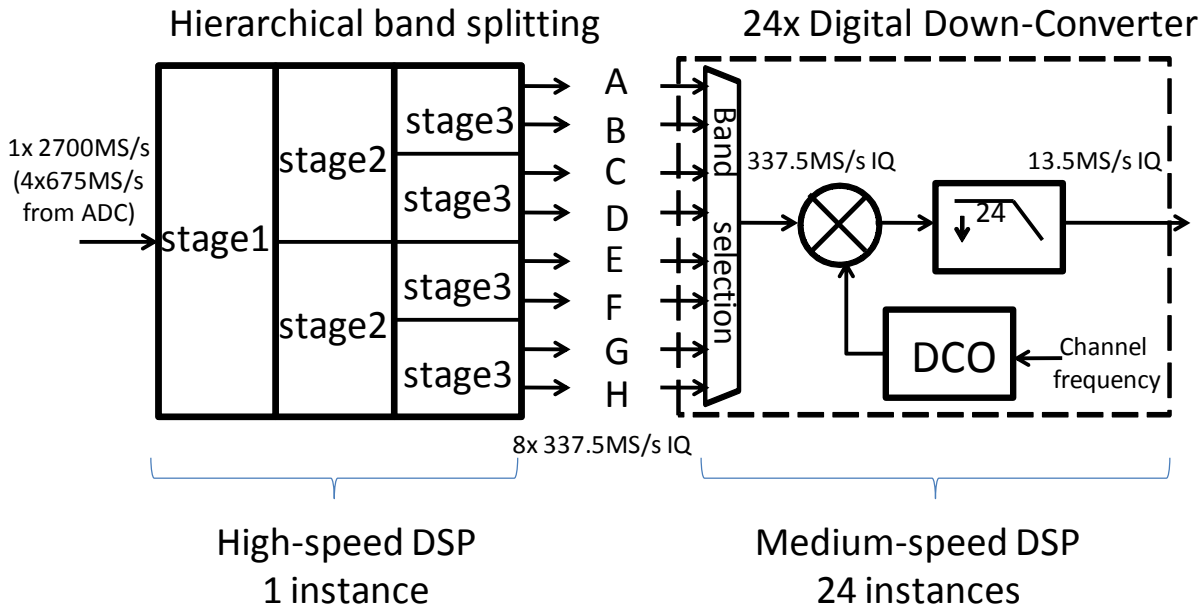


Fig 34. Sélecteur de canaux mis en œuvre

Table 1. Comparaison des récepteurs cable & TV

		Van Sinderen [32]	Tourret [33]	Stevenson [29]	Gupta [34]	Gatta [43]	Greenberg [35]	This work
Year		2003	2007	2007	2007	2009	2012	2012
Freq range	[MHz]	48-860	48-862	48-864	48-860	48-1000	40-1000	42-1002
Number of channels	[dB]	1	1	1	1	8	1	24
Channels independence		NA	NA	NA	NA	No	NA	Yes
Architecture		Low-IF	Low-IF	Dual-Conversion	Low-IF	Dual Low-IF	Low-IF	RF direct-sampling
NF	[dB]	7	5	8	7	6.5	3.8	5.5
CTB/CSO	[dB]		-57 / -57	-65 / -60	-53 / -115	-64 / -66		-62 / -59
IIP2 min/max	[dBm]				-22.4 / +36.5		+20 / +66	
IIP3 min/max	[dBm]	19 / 27			-13.8 / +17.5		-15 / +35	
LO integrated phase noise			0.5°RMS at 862MHz, 1kHz-4MHz		0.05°RMS to 0.8°RMS	0.2°RMS at 1GHz, 5kHz-10MHz	0.46°RMS at 855MHz	0.17°RMS at 1GHz, 5kHz-4MHz
Power	[mW]	1500	780	1500	750	1950	440	2370
Area	[mm2]	12.37	5.7 (total SIP: 9x9)	7.29	25	10mm2 + ref PLL	5.6	25
Technology		0.5um BiCMOS	0.25um BiCMOS	0.35um SiGe	0.18um CMOS	0.18um SiGe + 65nm CMOS	80nm CMOS	0.25um BiCMOS+ 65nm CMOS
Power / channel	[mW]	1500.0	780.0	1500.0	750.0	243.8	440.0	98.8
Area / channel	[mm2]	12.4	5.7	7.3	25.0	>1.25	5.6	1.0
Integration		LNA loop-through to analog IF	LNA loop-through to analog IF, using SIP	RF to analog IF, with ext. IF filters	RF to analog IF, using a digital IF selectivity	RF to DCS	RF to analog IF, using a digital IF selectivity	LNA loop-through to DCS, integrated RF filters

Ce travail est le premier à démontrer un récepteur RF à numérisation directe intégré. Il offre le plus grand nombre de canaux reçus, par rapport à l'état de l'art des récepteurs câble. Comme indiqué dans le tableau ci-dessus, ce travail est la solution la plus efficace en consommation de puissance et en coût par canal.

En plus de la puissance par canal indiquée dans le tableau 8, si 24 canaux devaient être reçus en utilisant les circuits référencés dans le tableau 8, d'autres amplificateurs RF seraient nécessaires pour séparer le signal d'entrée RF. Comme de nombreux circuits intégrés seraient nécessaires pour construire l'application, la surface de la carte, et son coût, augmenterait en proportion du nombre de canaux reçus. Une telle solution comprendrait de nombreux oscillateurs (au moins une par récepteur), ce qui pourrait donner lieu à de sérieux problèmes de coexistence (interactions entre oscillateurs). Ce travail démontre un des meilleurs NF, donc une des meilleures sensibilités, et une linéarité équivalente à l'état de l'art.

Notre solution offre la possibilité de recevoir des canaux à 24 fréquences totalement indépendantes. Comme il reçoit deux blocs de quatre canaux, le récepteur présenté dans [43] ne peut recevoir 8 canaux situés autour de deux fréquences RF différentes, ce qui réduit statistiquement l'efficacité spectrale que les opérateurs câble peuvent atteindre.

Conclusions & perspectives

L'objectif du travail effectué dans cette thèse de doctorat était d'étudier les récepteurs à numérisation directe, et de démontrer leur conception et leur intégration dans un produit électronique grand public, avec une performance (coût, puissance, taille, performance RF) compétitive. Dans le chapitre 2, une analyse au niveau système a permis d'identifier les principaux obstacles techniques à la conception d'un récepteur large bande à échantillonnage et numérisation RF directe. Les problématiques liées au conditionnement du signal, à l'échantillonnage et la conversion analogique-numérique, ont été modélisés analytiquement dans un contexte de réception large bande. Cette analyse théorique a été appliquée à la conception d'un produit récepteur multi-canaux RF (42MHz-1002MHz), basé sur l'échantillonnage et la numérisation directs RF (chapitre 3). L'architecture a été spécialement optimisée pour le contexte applicatif de passerelle domestique câble. Un frontal RF innovant a été mis en œuvre pour assouplir les exigences sur les performances du CAN.

Dans le chapitre 4, la conception des fonctions principales est présentée. Enfin, les résultats des mesures prouvent que le récepteur dépasse les exigences imposées par le standard, et permet une faible consommation d'énergie et un faible coût par canal.

Les principales contributions de cette thèse sont les suivants:

- Analyse et conception au niveau système des récepteurs à échantillonnage et numérisation directs RF
    - L'analyse théorique de la distorsion non-linéaire large-bande, pour les stratégies d'échantillonnage passe-bas et passe-bande
    - L'analyse théorique des défauts des convertisseurs analogique-numérique haute-vitesse (pureté horloge, bruit de quantification, erreurs d'entrelacement temporel, bruit dépendant du signal) dans un contexte de réception large bande
- Conception d'un conditionneur de signal RF optimisé pour une application, incluant:
    - Un égaliseur RF programmable multi-pente, utilisant une seule inductance, avec son algorithme de contrôle
    - Une boucle de contrôle de gain mixte combinant un détecteur RMS et un détecteur crête
    - Contribution à la réalisation d'un produit récepteur RF multi-canaux, à numérisation directe, meilleur que l'état de l'art en consommation d'énergie, coût (surface de silicium), et équivalent aux récepteurs existants sur les aspects performances RF.

Contents

List of abbreviations and symbols

ADC	Analog-to-digital converter
AM	Amplitude modulation
CCDF	Complementary cumulative density function
CSO	Composite second order broadband distortion
CT	Continuous-time
CTB	Composite triple beat broadband distortion
CTRX	Continuous-time receiver
dBmV	Voltage amplitude expressed in dB, and referenced to 1mV (X=20*log10(V/1mV)
dBuV	Amplitude expressed in dB, and referenced to 1uV (X=20*log10(V/1uV))
DSP	Digital signal processing
DT	Discrete-time
DTRX	Discrete-time receiver
F	Noise factor (linear scale)
HW	Hardware
IL	Implementation loss
IP2	2nd order intercept point
IP3	3rd order intercept point
LTO	Loop-Through Output
MSAGC	Mixed-signal automatic gain control loop
MSFE	Mixed-signal front-end
MTO	Multiple-tuner output
NCO	Numerically-controlled oscillator
NF	Noise figure (logarithmic scale)
OSR	Over sampling ratio
PA	Power amplifier
PAPR	Peak-to-average power ratio

PDF	Probability density function
QEF	Quasi-Error-Free (quality of reception in broadcast standards)
RFFE	RF front-end
S2D	Single-to-differential converter
STB	Set-top box
SW	Software
TD	Time-domain
TEQ	Tilt equalizer
TEQ	RF tilt equalizer
TH	Track-and-hold circuit
TI	Time-interleaved

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Introduction

Context

Digital communications have evolved to meet the demand of consumers for increasing access to Internet browsing, TV, Video on Demand, interactive games and social networking. This data rate increase is achieved by using advanced signal processing techniques, more complex modulations, and wider signal bandwidths. Therefore, high-performance receivers, able to capture wide-bandwidth signals, are required for high-end consumer communication, and infrastructure equipments. For instance, this includes Cable & Satellite home gateways, cellular infrastructure transceivers, white-space spectrum sensing.

As signal bandwidth continuously increase in these applications, the usage of narrowband receivers might become not power efficient. In addition, cost pressure requests low-cost multi-channel receivers to be more cost-effective than a multitude of narrowband receivers. Fig 1 shows a typical satellite receiver: an out-door unit translates the satellite band from the 10GHz range to 950MHz-2150MHz. As several 36 MHz-wide channels are required to be received in order to allow the user to perform simultaneously HD video watching or recording, a wideband receiver capturing the full 950MHz-2150MHz band could replace several 36 MHz-BW RF receivers.

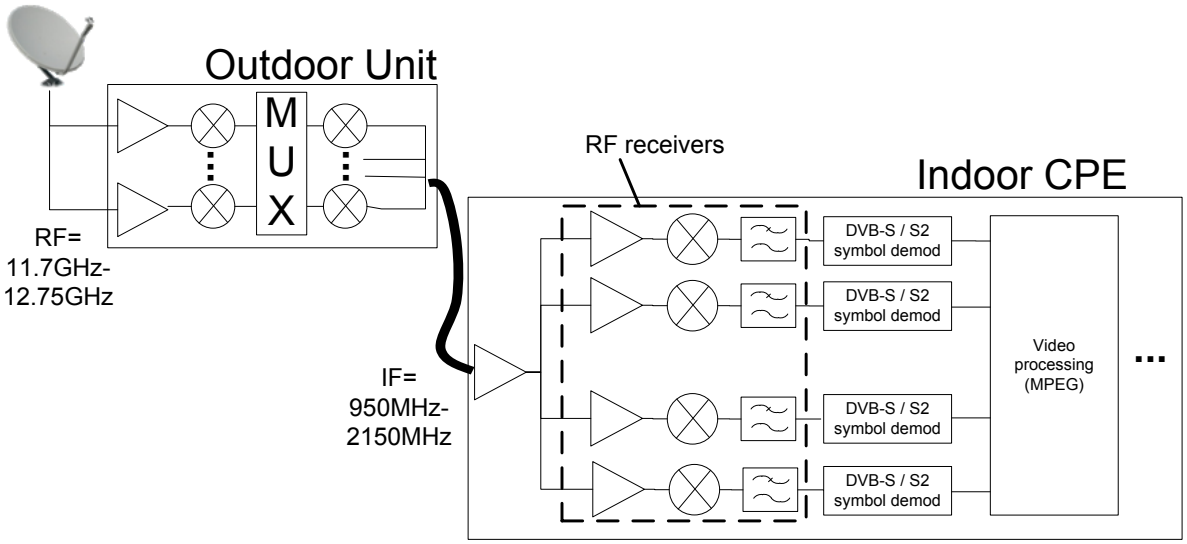


Fig 1. Satellite broadband multi-channel reception

In defense, radio-astronomy, space telecom applications which require multiple receivers, advances in CMOS processes could open the door to complex signal processing implementation. The use of these techniques is

typically not viable in wideband applications, since the use of parallel state-of-the-art wideband receivers would not be power and size/weight competitive. For instance, in S-band/L-band digital communication and radars applications, the versatility and performance advantages that digital beamforming (Fig 2, right) could bring, compared to analog beamforming (Fig 2, left), are not possible due to the lack of low-power low-size wideband receivers.

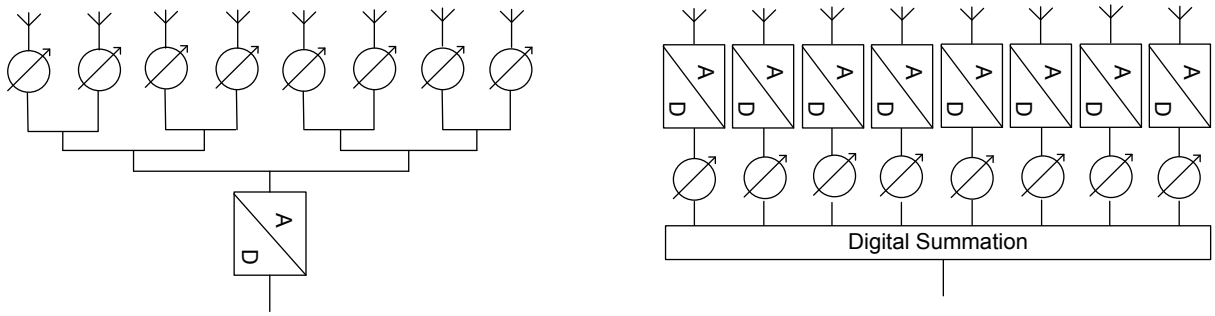


Fig 2. Left: Analog beamforming. Right: Digital beamforming

Identified research objectives

The research of highly integrated receivers, in the DC-3 GHz range, and capturing signal bandwidths of few hundreds of MHz is targeted in this work. Direct RF digitization receivers are attractive for these wideband applications, but several steps have to be taken into account in order to provide performing solutions.

The identified research activities that are required to tackle these challenges are:

- Architect direct RF digitization receivers at system-level from RF to DSP, considering broad-band aspects, and trades-off between cost, power consumption, RF performance and size
- Design high-performance low-power ADCs in a CMOS technology
- Design low-power high-speed Digital Channel Selection
- Design adequate RF signal conditioning that relaxes the ADC requirements
- Prove the full system performance from RF to baseband processing

Author contributions & thesis organization

This work presents the system-level design of direct RF sampling receivers, from theory to realization and measurements for a cable multi-channel receiver. This activity involved more than 20 people at NXP, including RF designers, analog and mixed-signal designers, digital designers, integrators, application engineers, software engineers, design & project leader, marketing. In addition, it is also the result of strong partnership with few architects working for several TOP-10 semiconductor companies and customers. The author acts as a Principal Engineer, System and IC Architect.

The main contributions of this thesis are:

- System-level analysis and design of direct RF sampling receivers
- Theoretical analysis of broadband non-linear distortion, for low-pass and band-pass sampling schemes
- Theoretical analysis of sampling and quantization (clock purity, time-interleaved errors, signal-dependent noise) in a broadband reception context

- Design of an application-optimized signal conditioner, including:
    - A single-inductance multi-slope programmable RF amplitude equalizer, together with its control algorithm
    - A mixed-signal AGC loop combining RMS and peak detection
- Design of an integrated direct RF digitization product, exceeding state-of-the-art power consumption, cost (silicon area), and equivalent or better RF performance than legacy silicon tuners

This thesis is organized as follows:

In chapter 1, signal processing techniques are reviewed, from RF mixing through sampling, to analog-to-digital conversion. The state-of-the-art of radio receivers is provided, motivating the focus on direct RF digitization architecture.

The system-level design framework for direct RF digitization receivers is provided in chapter 2, linking the communication system specifications to the radio receiver impairments, with a special focus on the broadband aspects of sampling, digitization, including broadband non-linear distortion, ADC time-interleaving non-idealities and clock purity.

In chapter 3, the theory developed in chapter 2 is applied to the system-level design of a direct RF digitization receiver product for multi-channel cable. An optimum RF signal conditioning is investigated.

Chapter 4 presents the block-level design of the RF signal conditioner and the mixed-signal front-end and also presents the system-level measurement results of the receiver in a broadband environment. This includes the work achieved by the whole team, so involves much more than the author contribution.

Finally, a general conclusion recapitulates the presented work and introduces future work orientations and perspectives.

CHAPTER 1.

RF receiver architecture state-of-the-art

This chapter introduces the principles of mixing, sampling, and quantization. It establishes the state-if-the-art of radio DC-3GHz receivers, using the following classification:

- Continuous-time receivers (Fig 1, left): they are based on an analog continuous-time mixer. The subsequent signal processing is also mainly achieved using continuous-time techniques, up to the ADC sample-and-hold.
- Discrete-time receivers (Fig 1, right): they are based on an early sampling circuit, which sometimes also performs a frequency translation. Analog discrete-time signal processing can be used in order to relax the ADC dynamic range. Alternatively, straight digitization might be performed.

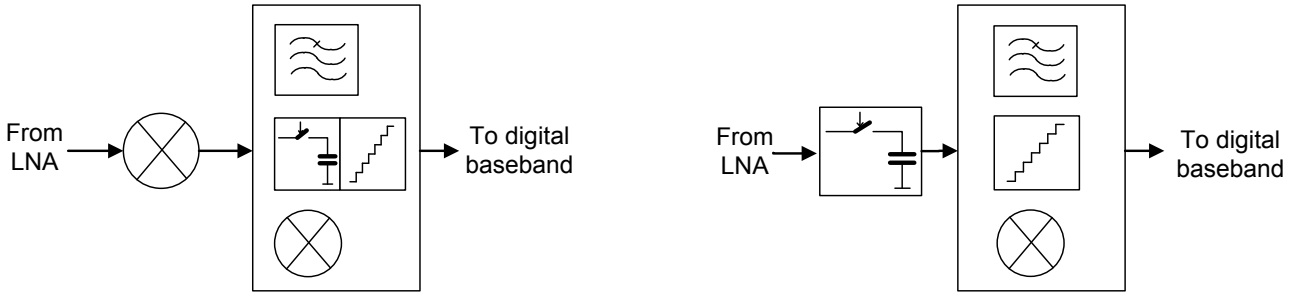


Fig 1. Left: continuous-time receiver (CTRX), right: discrete-time receiver (DTRX)

Most of the architecture choices are dictated by issues encountered in fundamental signal processing operations:

- Mixing
- Sampling
- Digitization

The next sections detail these three operations.

1.1 Mixing process

The usual way to receive a radio frequency signal is to down-convert it from radio frequencies to intermediate frequencies at which the subsequent signal processing functions can be implemented at acceptable power consumption and cost. This down-conversion process is realized by a continuous-time mixer, which down-converts a RF signal to an intermediate frequency F_{IF}.

$$F_{IF} = F_{RF} - F_{LO} \tag{1.1.}$$

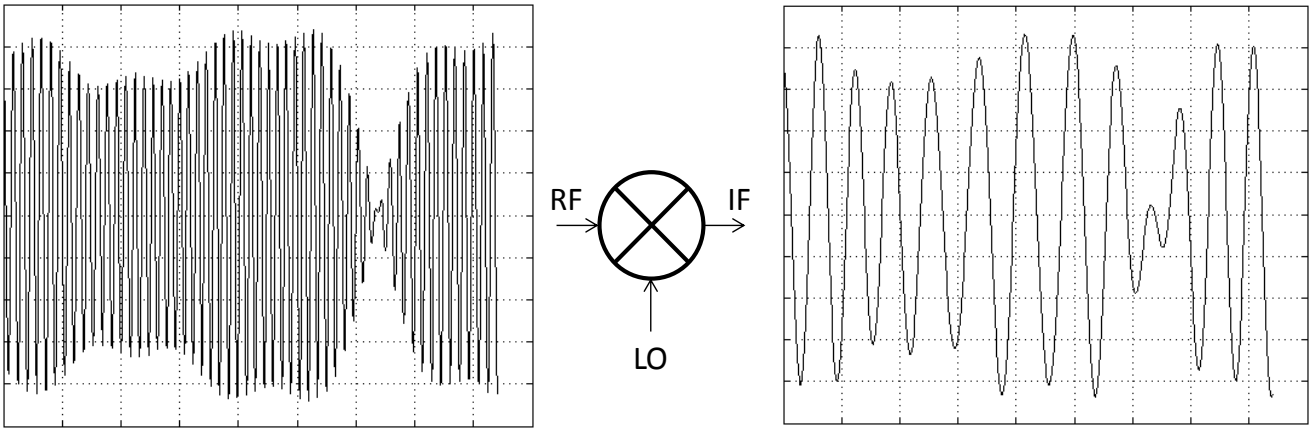


Fig 2. Frequency translation from RF to IF using a continuous-time mixer

A mixer is unable to discriminate positive from negative frequency beats. Therefore, signals lying both at $(F_{LO} - F_{IF})^{P_{tot\_dBuV}}$ and $(F_{LO} + F_{IF})$ are down-converted to the same intermediate frequency $F_{IF} = |F_{RF} - F_{LO}|$. As shown in Fig 3, such a situation leads to overlap of both RF frequencies to the same IF frequency.

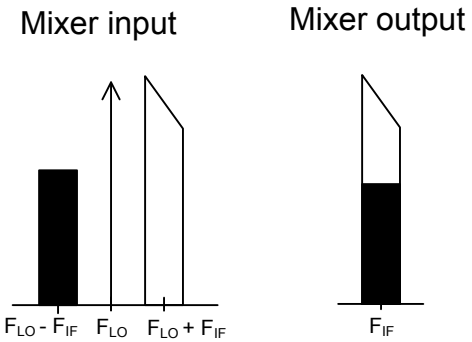


Fig 3. Image frequency in a down-conversion mixer

This is known as the image problem. This problem is exacerbated when the signal lying at the image frequency has stronger amplitude than the wanted signal, which can typically be the case in wireless communication systems environment.

Several solutions have been proposed to mitigate the image issue.

1.1.1 Image-reject filter

An alternative is to filter the RF image signal prior to the down-conversion process. The intermediate frequency choice implies a trade-off between image rejection and IF selectivity:

- A small difference between F_{RF} and F_{IMAGE} (low-IF) requires the use of a high-order RF image-reject filter, which turns into high cost & limited integration,
- A large difference between F_{RF} and F_{IMAGE} (high-IF) requires the use of a high-order and expensive IF filter,

1.1.2 Image-reject mixers (IRM):

Another alternative is to build a mixer structure that intrinsically rejects the image signal:

- Hartley structure: the complex signal processing involves an in-phase (I: 0°) and in-quadrature (Q: 90°) signal path that allows discrimination between positive and negative frequency beats (F_{LO}-F_{IF} and F_{LO}+F_{IF}). The 90° phase can be implemented using a passive polyphase filter, as shown in Fig 4 (right). However, designing a wideband 90° phase shift can involve a large number of RC-CR sections ([2])

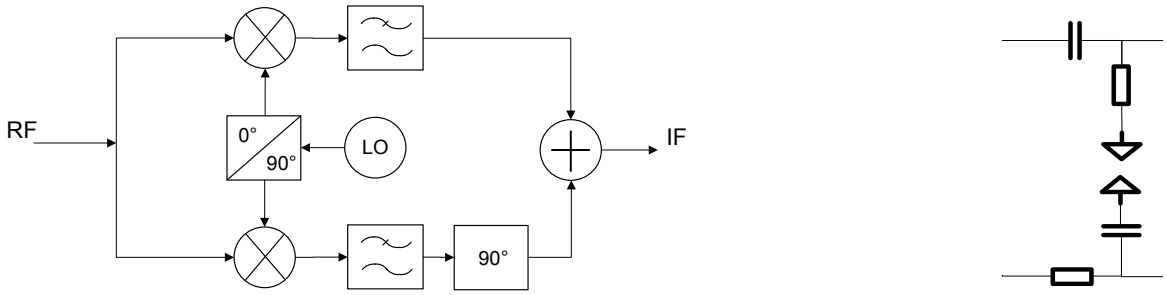


Fig 4. Hartley mixer structure (left), example of 90° phase shift realization (right)

- Weaver structure replaces the 90° phase shift by a second mixing stage.

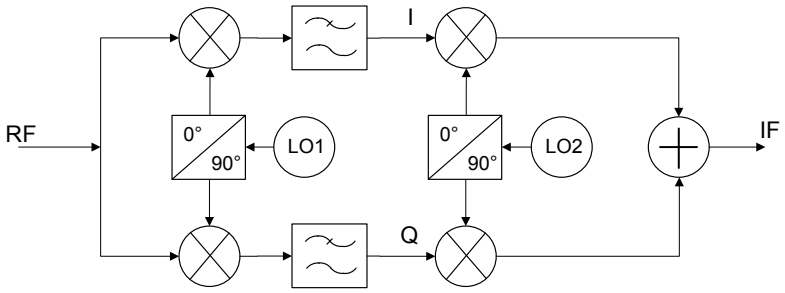


Fig 5. Weaver mixer structure

Because of amplitude and phase mismatch, I & Q (0° and 90°) signal path are in practice not exactly in quadrature. This places a limit on the image rejection ratio ([3]).

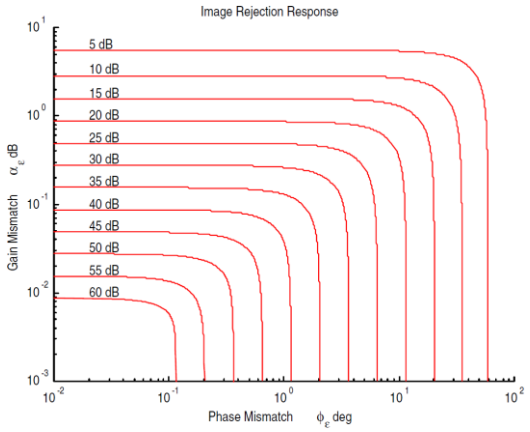


Fig 6. Image rejection ratio

For applications requiring a higher image rejection, double-quadrature structures using four mixers can be used ([2], [4]). Then, that image rejection depends only on the second order of quadrature inaccuracy in the LO and RF.

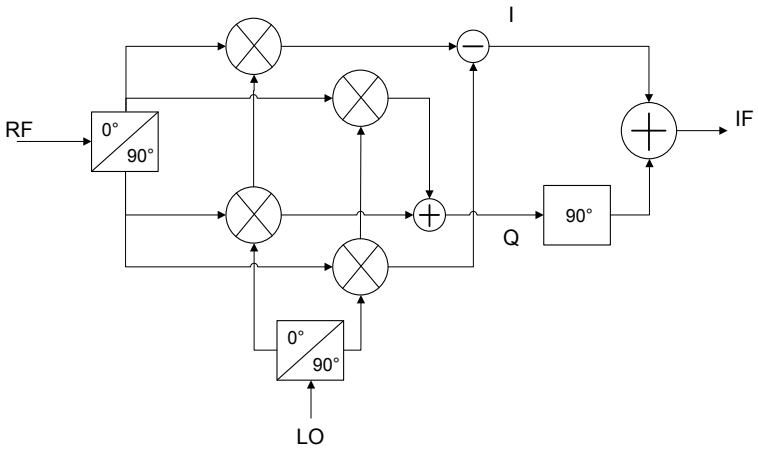


Fig 7. Double-quadrature mixer structure

Mixed-signal or DSP calibration techniques are also widely used to enhance the image-rejection performance of these mixers, often limited by components matching (LO signals, mixer switches…).

1.1.3 Mixing with LO harmonics

Switching mixers are used for their superior noise and linearity performance over fully linear multipliers. Consequently, the RF input signal is not multiplied with a pure sine wave but with a square wave. As the Fourier series of this square-wave LO is a sum of sine waves at integer multiple frequencies of F_{LO}, not only the wanted signal is down-converted but also potential interferers lying at $(N \cdot F_{LO} + F_{IF})$ are down-converted as well (Fig 8).

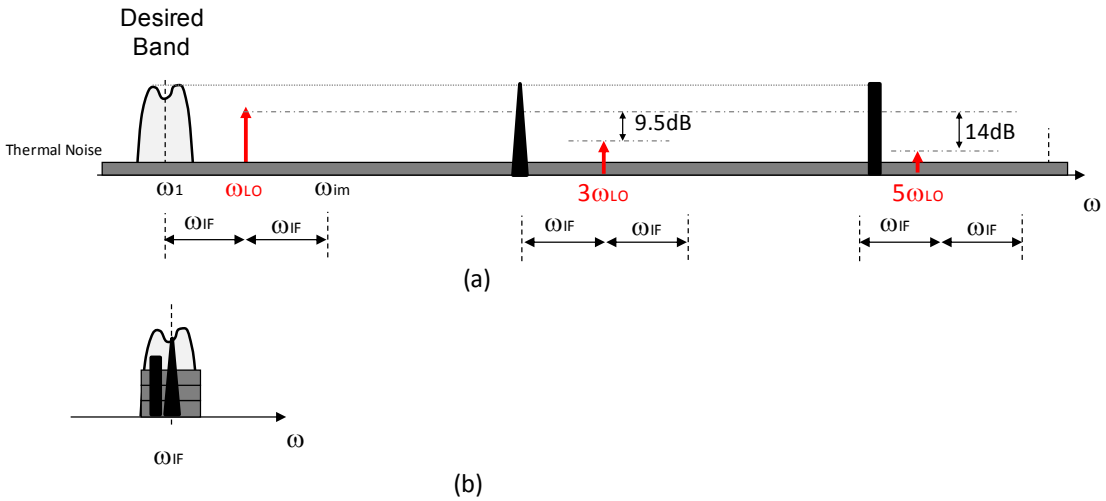


Fig 8. Mixing with LO harmonics

The LO harmonics amplitude, referred to the fundamental, follow the rule:

$$H_N = 20 \cdot \log_{10}(N) \tag{1.2.}$$

Where N is the harmonic order.

This limitation is not only relevant in broadband systems (multi-octave RF input band), but also in all applications that have to coexist with interferers whose frequencies are around the LO harmonics of the receiver.

This issue is exacerbated in the context of highly-integrated low-cost receivers where RF selectivity is preferably avoided.

Therefore mixer configurations that could avoid mixing with LO harmonics have been researched.

1.1.4 Harmonic-reject mixers (HRM)

In order to preserve the noise and linearity advantages of switching mixers over analog multipliers, harmonic-reject mixers have been built using combinations of switching mixers ([5]). Mixing with a pure sine wave is approached by summing several properly-scaled switching mixers outputs (Fig 9), which is realized when:

$$a1 = a3 = 1 \tag{1.3.}$$

$$a2 = \sqrt{2} \tag{1.4.}$$

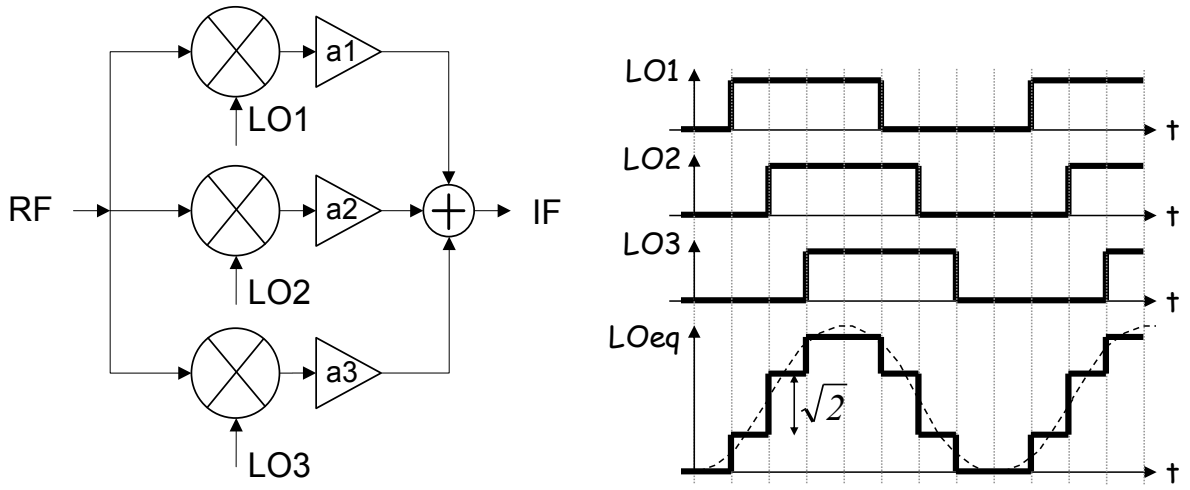
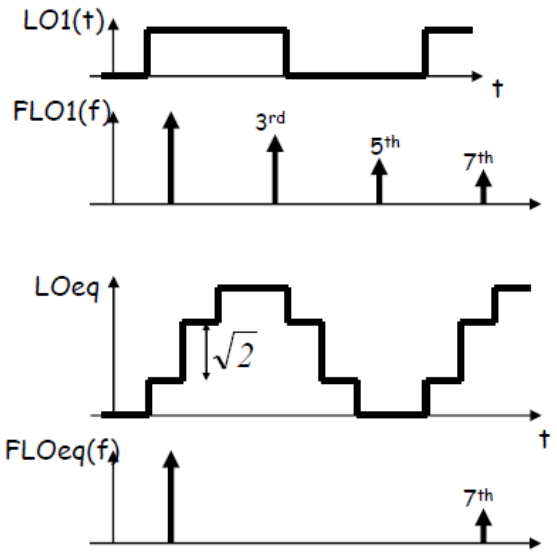


Fig 9. Harmonic-reject mixer

In the example of Fig 9, mixing of LO 3rd and 5th harmonics is ideally cancelled. Practically, layout and component matching (amplitude and phase errors) limit the harmonic rejection. This can be circumvented by using calibrations techniques ([6]), if a training signal or a calibration phase is available.

As several LO signal phases are required with high accuracy, the usage of HRM mixer places a tough constraint on the frequency synthesis strategy. In order to meet this phase accuracy, high VCO frequencies are typically required in order to allow for the different LO phases to be built from several outputs of a single frequency divider.

Despite the improvement that HRM brings, exceeding harmonic rejection higher than 50 dB typically requires the use of RF tracking filters, which increases cost, power and limits integration.



$$LO1(t)=\frac{\sqrt{2}}{\pi}\left\{\left[\cos(wt)-\sin(wt)\right]+\frac{1}{3}\left[\cos(3wt)+\sin(3wt)\right]\right.$$
$$\left.-\frac{1}{5}\left[\cos(5wt)-\sin(5wt)\right]+\ldots\right\}$$

$$LO2(t)=\frac{2}{\pi}\left\{\cos(wt)-\frac{1}{3}\cos(3wt)+\frac{1}{5}\cos(5wt)+\ldots\right\}$$

$$LO3(t)=\frac{\sqrt{2}}{\pi}\left\{\left[\cos(wt)+\sin(wt)\right]+\frac{1}{3}\left[\cos(3wt)-\sin(3wt)\right]\right.$$
$$\left.-\frac{1}{5}\left[\cos(5wt)+\sin(5wt)\right]+\ldots\right\}$$

$$HRM_3=\frac{1}{9}\left\{\left[1-\cos(3\theta)\cdot(1+\Delta)\right]^2+\left[(1+\Delta)\cdot\sin(3\theta)\right]\right\}$$

$$HRM_5=\frac{1}{25}\left\{\left[1-\cos(5\theta)\cdot(1+\Delta)\right]^2+\left[(1+\Delta)\cdot\sin(5\theta)\right]\right\}$$

Δ: gain mismatch,

θ: phase mismatch

Fig 10. Harmonic-reject response

1.2 Sampling process

1.2.1 Lowpass 1st order sampling

Sampling is the process of converting a continuous-time signal to a discrete-time signal. It is mathematically described in the time domain as a multiplication between the input signal and a Dirac comb.

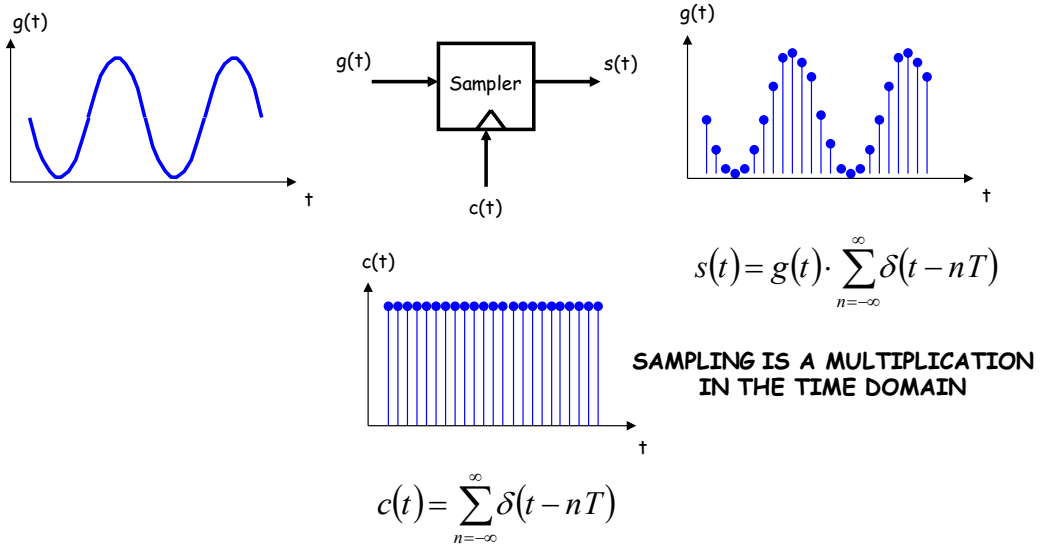


Fig 11. Sampling process

In the frequency domain, the sampling process is represented as a convolution between the input signal frequency spectrum and a Dirac comb frequency spectrum.

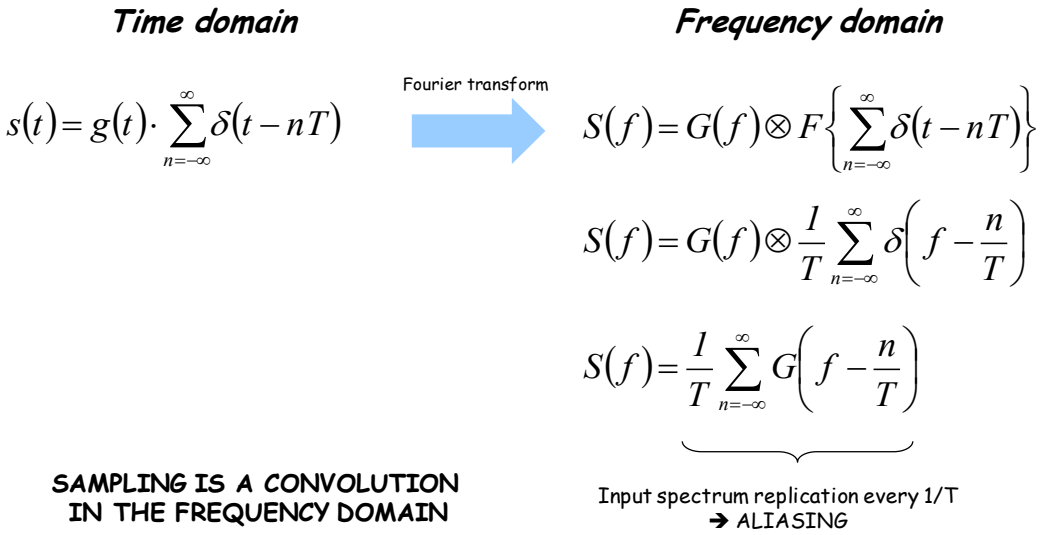


Fig 12. Sampling process: form time-domain to frequency domain

As the Fourier transform of a Dirac comb is also a Dirac comb in the frequency domain, this convolution product periodizes the spectrum of the input signal. If the Nyquist sampling theorem condition is fulfilled,

$$fs \geq 2 \cdot fin_{MAX} \tag{1.5.}$$

the output signal represents the input signal without any loss of information (Fig 13, left). In case Nyquist sampling condition is not fulfilled, aliasing occurs between the different copies (replica) of the input signal spectrum (Fig 13, right).

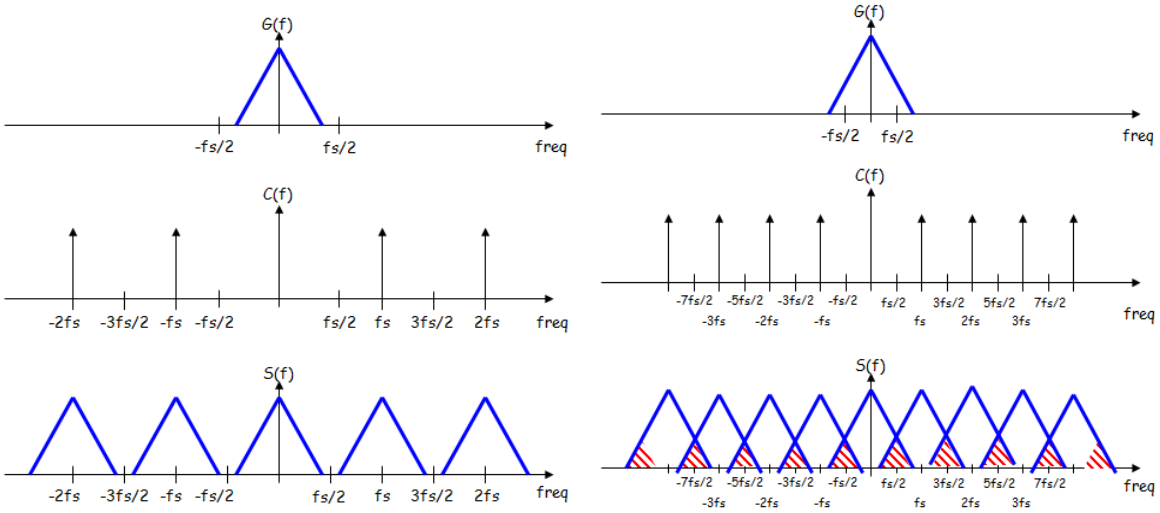


Fig 13. Sampling process in the frequency domain. Left: no aliasing, right: with aliasing

1.2.2 Bandpass 1st order sampling (sub-sampling)

When sampling a signal with a high F_{RF}/BW ratio (narrowband signal), using a sampling rate lower than twice the maximum input signal frequency is also a possible option (Fig 14):

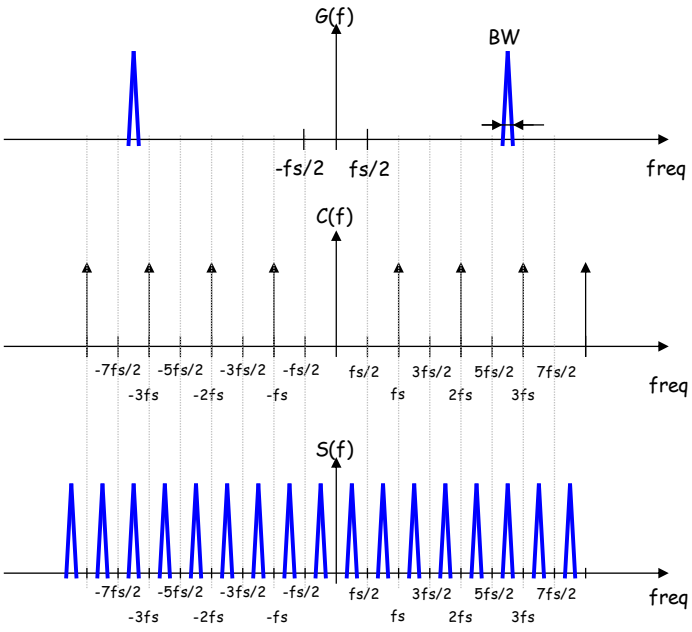


Fig 14. Bandpass sampling in the frequency domain

As it performs a down-conversion, this sampling technique can save a mixer stage on the RF front-end.

As in case of lowpass sampling, the input signal spectrum is periodized. This gives a bound on the sampling rate:

$$fs \geq 2 \cdot B$$

In addition, the relation-ship between the input signal centre frequency (fc), the input signal bandwidth (B) and the sampling rate (fs) must ensure the input signal energy to be confined across one single Nyquist zone.

The unvalid combinations of input signal centre frequency (fc), input signal bandwidth (B) and sampling rate (fs) are represented as shaded areas in Fig 15 ([8]):

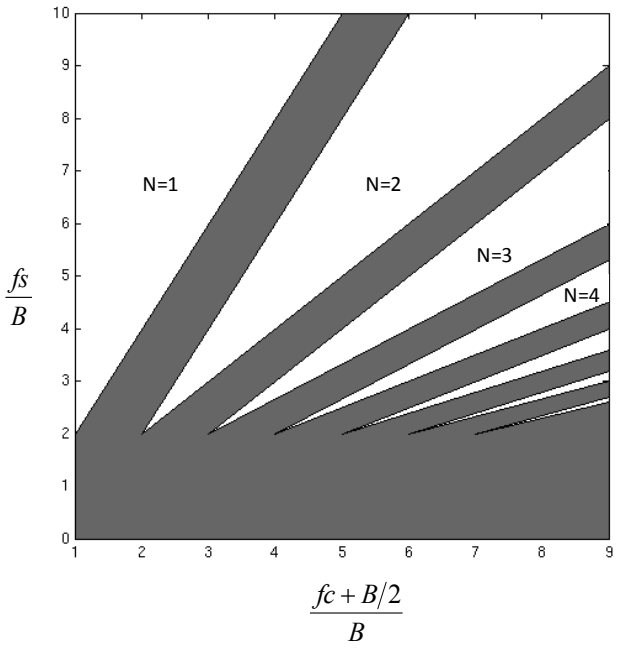


Fig 15. Valid sampling rates and band positions using bandpass sampling

Clearly, the few valid zones of sampling rates strongly limit the use of bandpass sampling. In addition, aliasing of wideband noise limits the receiver performance.

1.2.3 Nth-order sampling

Nth-order sampling ([7], [8]) removes the restrictions on the input signal band position for minimum-rate sampling: it has been demonstrated that no restriction exists for minimum-rate Nth-order sampling, for all even-values of N.

Obviously, the minimum sampling rate condition still needs to be fulfilled:

$$fs \geq 2 \cdot B \qquad (1.6.)$$

N-th order sampling technique makes use of several uniform sampling signals having specific delays one with respect to the others. The number of interleaved uniform sampling streams, N, defines the order of the sampling. The average sample rate is defined as the sum of the individual uniform sampling rates. The sampling is called "*periodically-non-uniform*" since the system alternates between several sampling rates, in a periodic manner.

The simplest implementation of Nth-order sampling, called second-order sampling (N=2), implements a quadrature sampling, and is explained on this section.

As shown in Fig 16, the input signal is being split into N sub-signals (N=2), A/D converted at fs/N (1/NT) with a specific delay $\Delta T = 1/4 \cdot fc$, and filtered through a digital interpolant (D(z)).

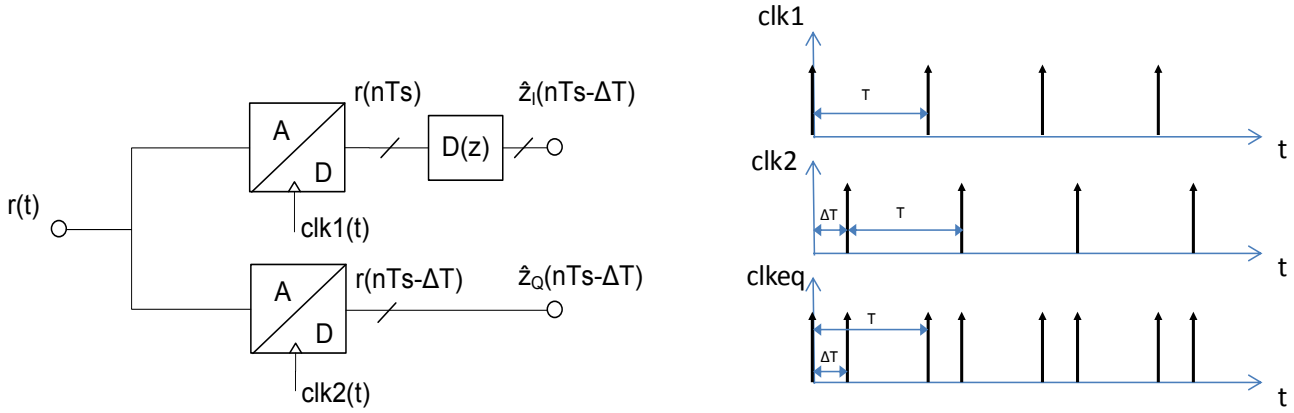


Fig 16. 2nd-order sampling. Left: block diagram, right: sampling streams

As described in [9], if a complex base-band signal (z(t)) is frequency-translated around an RF carrier (fc), the resulting bandpass signal (r(t)) can be expressed as:

$$r(t) = 2 \cdot \Re\left\{z(t) \cdot e^{j \cdot w_c \cdot t}\right\} \tag{1.7.}$$

The base-band signal can be decomposed into real and imaginary components:

$$z(t) = z_I(t) + j \cdot z_Q(t) \tag{1.8.}$$

Then,

$$r(t) = 2 \cdot z_I(t) \cdot \cos(w_c \cdot t) - 2 \cdot z_Q(t) \cdot \sin(w_c \cdot t) \tag{1.9.}$$

Choosing the sampling rate (fs) as:

$$fs = fc / r \tag{1.10.}$$

where r is an integer reflecting the sub-sampling ratio

And setting the time delay between the two paths in order to provide quadrature signals at the carrier frequency (90° phase-shift at f=fc):

$$\Delta T = 1 / 4 \cdot fc \tag{1.11.}$$

After some manipulations, the discrete-time signal at the output of the ADCs can be expressed as [9]:

$$r(nTs) = 2 \cdot z_I(nTs) = I'(n) \tag{1.12.}$$

$$r(nTs - \Delta T) = 2 \cdot z_Q(nTs - \Delta T) = Q'(n) \tag{1.13.}$$

$$I'(n) + j \cdot Q'(n) = r(nTs) + j \cdot r(nTs - \Delta T) = 2 \cdot z_I(nTs) + j \cdot 2 \cdot z_Q(nTs - \Delta T) \tag{1.14.}$$

Therefore, the complex discrete-time signal is closed to the complex baseband input signal, but is not a perfect reconstruction, since the timing offset (ΔT) creates an accurate 90° phase shift only at f=fc. For signal frequencies

which are different than fc, the time delay causes a phase shift which differs from 90°, and causes a finite image rejection ([9], Fig 17):

$$ir = \left| \frac{1 + e^{-2 \cdot \pi \cdot fd \cdot \Delta T}}{1 - e^{-2 \cdot \pi \cdot fd \cdot \Delta T}} \right|^2 \tag{1.15.}$$

With:

$$fd = f - fc \tag{1.16.}$$

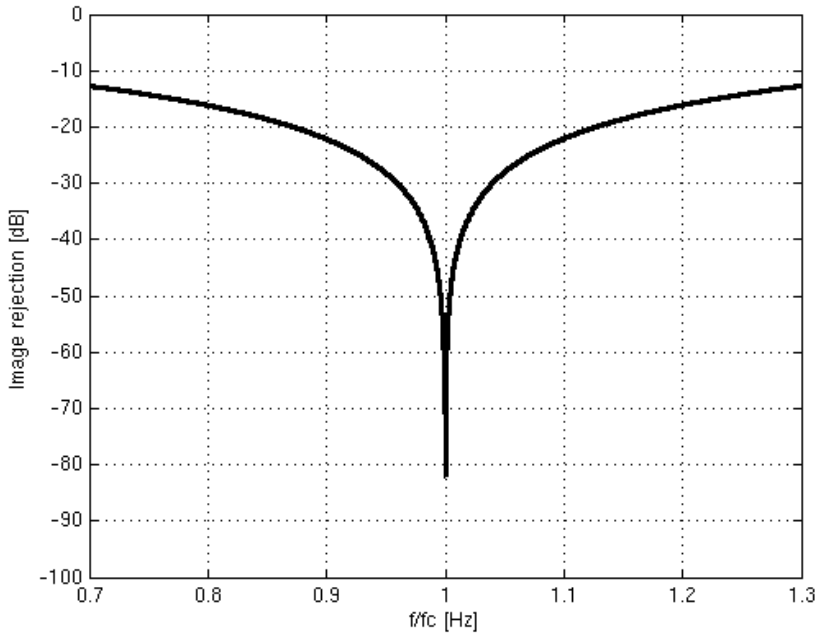


Fig 17. Narrowband image rejection with 2nd order sampling

A digital fractional-delay-filter ([9]) is required at the output of the real signal component, in order to time-align real and imaginary components, and ensure a high image rejection even in the presence of wideband input signals.

Another mean to realize N-th order sampling, is to replace the delays on the clock signal by some delays on the input signals. The additional difficulty, in the context of wideband reception, is to obtain constant and accurate delays across a wide bandwidth.

1.3 Analog-to-digital conversion

This section provides background and reference to core ADC technology.

Overall, ADC architectures can be classified depending on their ability to convert wideband signals with a high accuracy. Therefore, they can be represented in a speed-resolution plane.

This trade-off between speed and accuracy is often approached at architecture level: high-speed low-resolution ADCs typically convert a full byte-at-a-time, medium-speed medium-resolution ADCs convert a word-at-a-time, while low-speed high-resolution ADCs may convert a single bit-at-a-time.

1.3.1 Flash

Flash ADCs ([12]) make use of a bank of parallel comparators, that each evaluates if the input signal is greater or lower than a built-in reference signal.

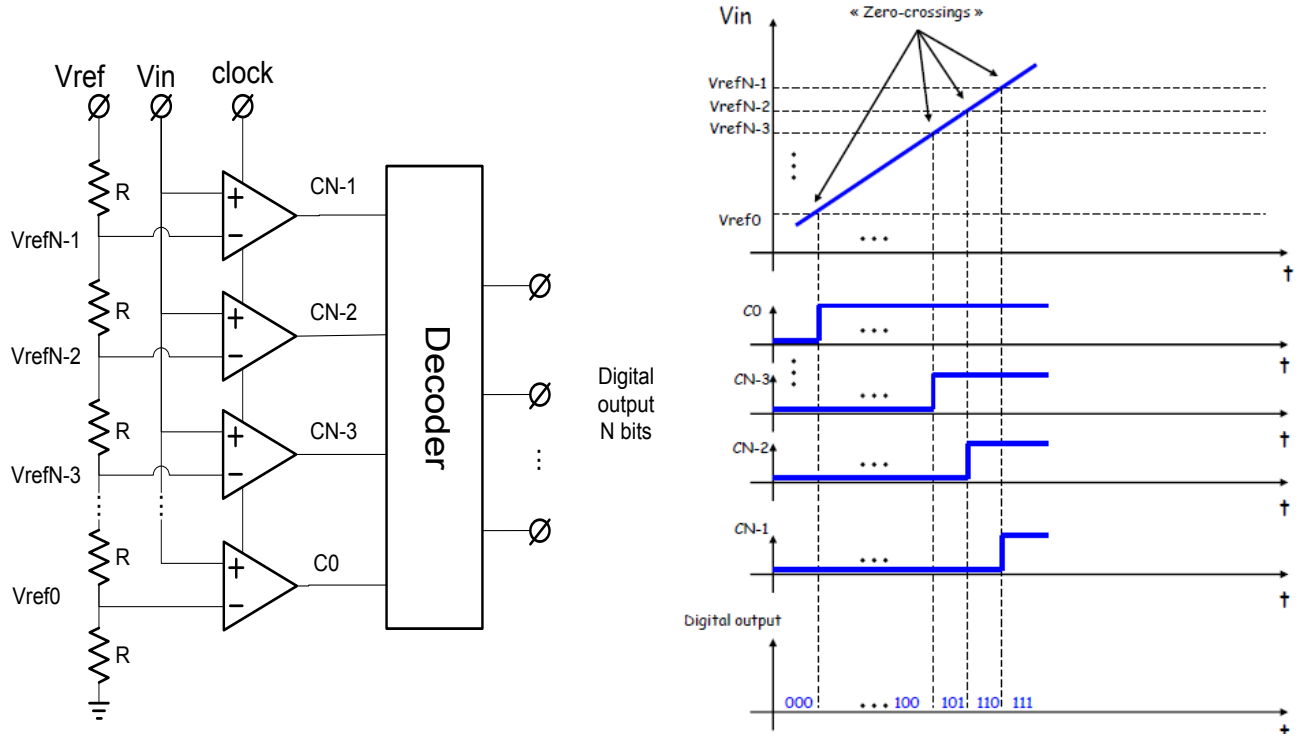


Fig 18. Flash ADC principle architecture

Therefore, through a single processing operation, flash ADCs convert the full analog signal into a digital representation (byte-at-a time), and are thus inherently very fast and low-latency.

They suffer from the high number of comparators (2^N-1) and reference voltages (2^N) which are required for building a N-bit ADC: these cause their area, input capacitance and power consumption to grow exponentially with the number of bits.

Several techniques have been developed for mitigating some of these limitations: input signal interpolation, input signal folding ([13], [14]), time-interpolation of comparators outputs ([15]). Still, Flash-family ADCs are generally limited to high-speed, low-resolution applications.

In [16], combination of input signal interpolation and folding allow building a dual 12-bit 1.8GSps ADC, which outputs can be externally combined to build a 3.6 GSps 12-b ADC. Still its 192-ball package and the 4.4 W power consumption limit its use in applications where cost and power are not the key drivers.

1.3.2 Pipeline

The general idea behind the pipeline family ([17]) is to split the conversion process into several cascaded sub-conversions (Fig 19).

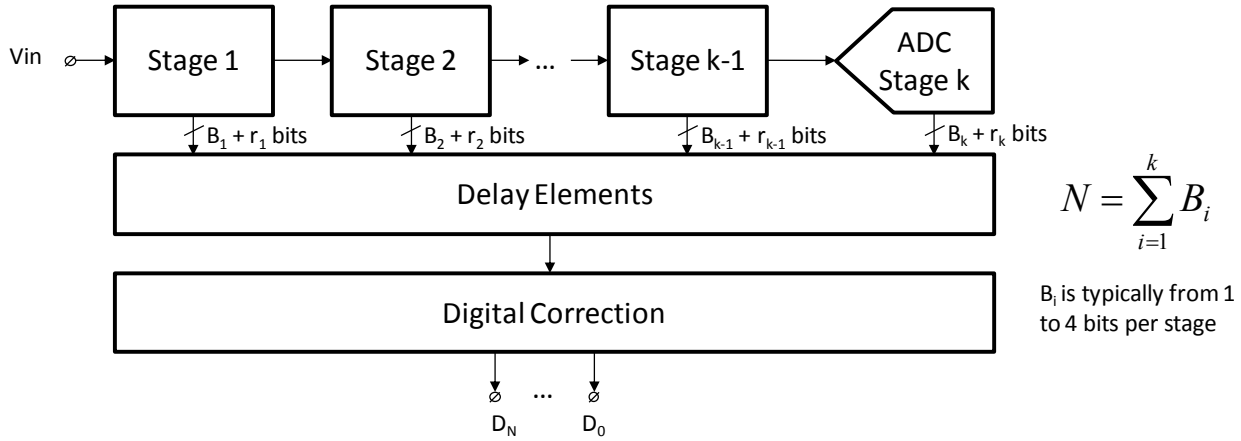


Fig 19. Sub-ranging / Multi-step / Pipeline ADCs principle architecture

Each pipeline stage (Fig 20) performs simultaneous sampling of the analog input signal (S/H), and coarse digitization, providing B_i+r_i bits (ADC). The digital signal is converted back to analog (DAC), and subtracted from the sampled analog input signal. This error signal represents the quantization error, and is amplified (G_i) for further processing through the next stage. This process is repeated for the following stages, until a sufficient resolution is achieved. Therefore, the converter resolved one word-at-a-time.

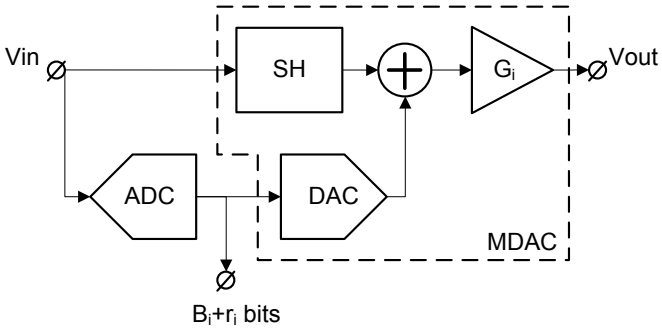


Fig 20. Pipeline sub-stage principle

The over-range technique (Fig 21) allows for some extra-range on the stages, in order to still provide a correct ADC output code, even in presence of errors in the individual stages. By doing so, the design of the individual stages is relaxed.

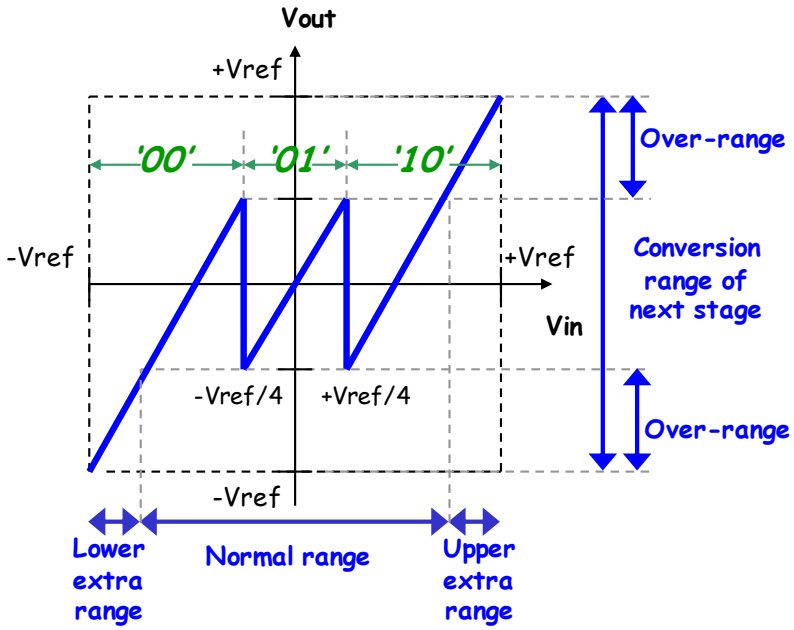


Fig 21. Pipeline ADCs conversion steps, without (left) and with (right) over-range

Maximum accuracy is requested on the first stage of the pipeline, since it must cope with the full input signal dynamic, while the required accuracy of the following stages is relaxed by the number of bits which have already been resolved up-front. This allows scaling down the area and power of stages through the pipeline, down to a limit where parasitic capacitors dominate.

As the total number of bits (N) is the sum of the useful bits provided by each stages:

$$N = \sum_{i=1}^{k} B_i \tag{1.17.}$$

Each stage necessitates L_i comparators:

$$L_i = 2^{B_i + r_i} \tag{1.18.}$$

Where B_i are the significant bits, and r_i bits are reserved for the over-range, with $r_i < B_i$

Assuming equal number of bits per stage and no over-range, the total number of comparators for a k-stage pipeline ADC with B_i bits per stage is:

$$L = \sum_{i=1}^{k} \left(2^{B_i} - 1\right) = k \cdot \left(2^{B_i} - 1\right) \tag{1.19.}$$

Therefore, neglecting hardware over-head due to over-range, a 12-bit ADC built upon a cascade of 12 1-bit sub-ADCs would require 12 comparators, while a flash ADC would require 4095 comparators.

Making use of switched-capacitors techniques, sampling, digital-to-analog conversion, subtraction and amplification can be implemented in a single "multiplying" DAC stage (Fig 22). This makes pipeline ADCs prone to integration

in CMOS processes.

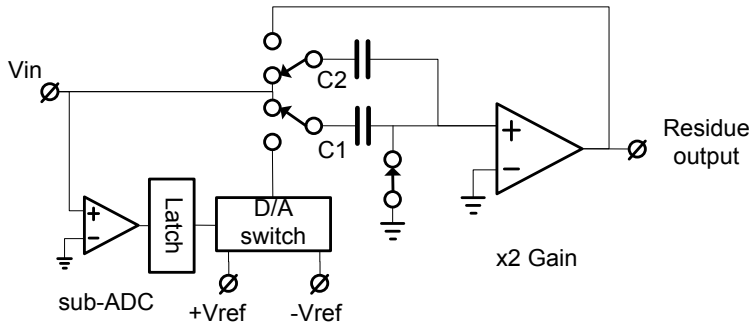


Fig 22. Pipeline stage switched-capacitor implementation

For a given resolution and speed, there is a trade-off between the number of stages and the resolution per stage. For medium-speed, medium-resolution applications (100 Msps, 10-bit), 1.5-bits per stage is a common practice. For high-resolution applications, a higher number of bits are typically resolved in the 1st stage, which challenges the amplifier (OTA) design.

The cascaded sub-conversion process allows dramatically reducing the number of comparators, therefore reaching higher resolution than flash ADCs (16-bit 125 MSps ADC, 385 mW in [18]).

As pipeline ADCs involve complex analog signal processing (sub-ADC, SC sub-DAC, OTA operating in close-loop) which needs linear settling time, they are more limited in speed than flash. Due to the cascade of multiple stages, they exhibit high latency, which can prohibit their use in control loops applications.

1.3.3 SAR

A Successive Approximation Register ADC ([19]) trades off speed for resolution: it converts the analog signal into a digital representation, gradually from MSB to LSB, using a single feedback DAC and comparator. Therefore, N conversion cycles are necessary for converting an analog signal into an N-bit digital representation. An N-bit SAR ADC, providing a new sample at Fs rate, needs to run internally at approximately NxFs.

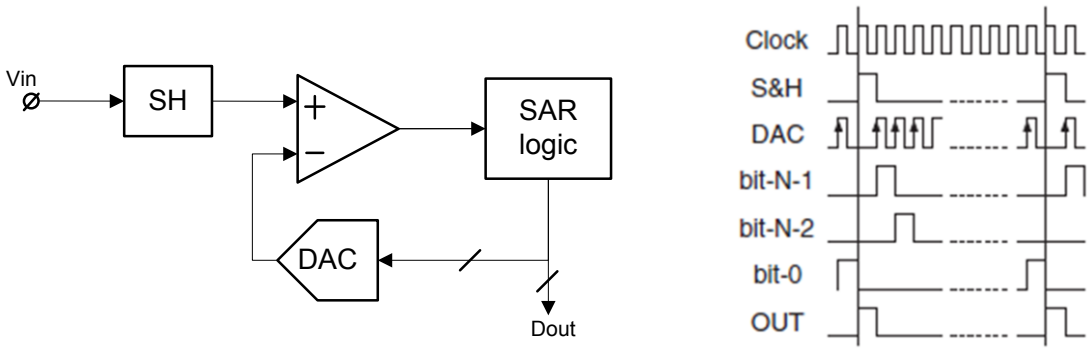


Fig 23. SAR ADC bloc diagram (left), and timing diagram (right)

As in pipeline ADCs, over-range (redundancy) is common practice for minimizing the impact of analog errors, (DAC settling), therefore allowing increase of the conversion speed. Operation of binary (radix-2) and redundant (reduced-radix) SARs are compared in Fig 24 ([20]):

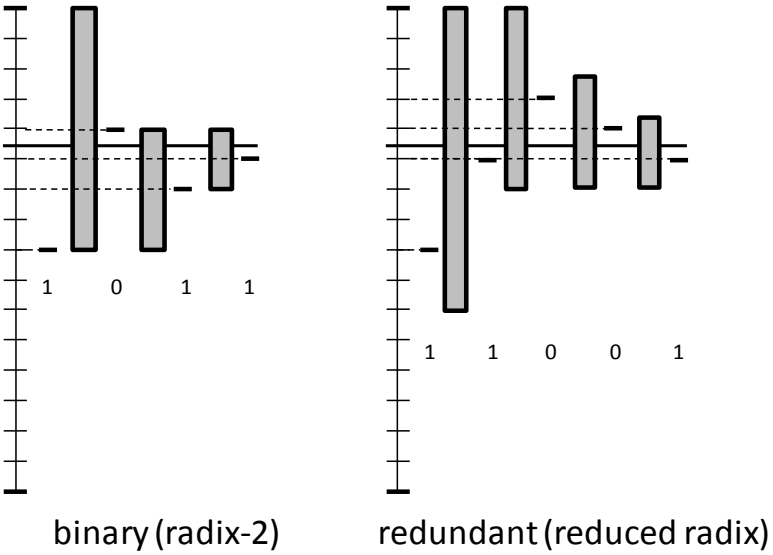


Fig 24. Operation of binary and redundant SAR ADCs

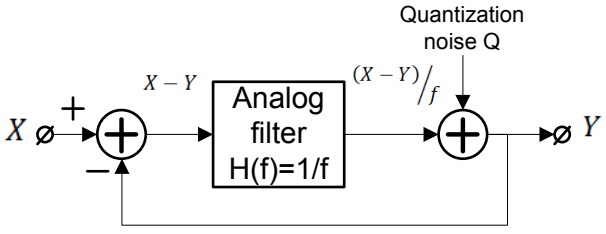
Capacitive-SAR implementation is prone to CMOS process, where the only remaining active analog block is the comparator.

SAR ADCs are adequate for high-resolution low-speed, and ultra-low-power applications ([21]).

1.3.4 Delta-sigma

Delta-sigma ADCs ([22]) trade off bandwidth for resolution, by using over-sampling and noise-shaping. They make use of high-speed low-resolution quantizers (for instance 1-bit), embedded in a delta-sigma loop. As a result of feedback, the input signal (x) and the output signal (y) are forced to nearly equal within the loop bandwidth. Consequently, most of the differences between input and output signals, i.e. quantization noise, are shaped outside of the loop bandwidth (i.e. toward high frequencies for a lowpass delta-sigma) (Fig 26).

As shown using a linear model (Fig 25), an integrator loop filter has a lowpass effect on the input signal ($H(f)=1/(f+1)$) while it high-pass filters the quantization noise ($H(f)=f/(f+1)$).



$$Y = \frac{1}{f}(X - Y) + Q$$

$$Y = \frac{X}{f+1} + \frac{Q \cdot f}{f+1}$$

signal term noise term

Fig 25. Delta-sigma ADC principle

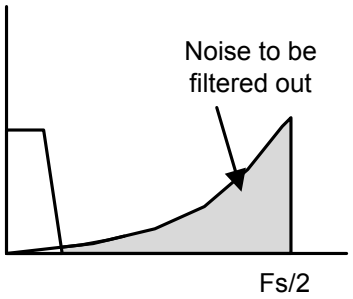


Fig 26. Oversampling and noise shaping

The combination of number of bits (N), over-sampling factor and order (L) determine the algorithmic performance (SQNR) of delta-sigma converters. The following equation ([23]) provides an SQNR estimate for single-loop topologies:

$$SQNR\max_{dB} = 6.02 \cdot N + 1.76 + (20 \cdot L + 10) \cdot \log_{10}(OSR) - 10 \cdot \log_{10}\left(\frac{\pi^{2 \cdot L}}{2 \cdot L + 1}\right) \quad (1.20.$$

Where, the over-sampling factor (OSR) is defined as:

$$OSR = \frac{fs}{2 \cdot BW} \quad (1.21.)$$

Practically, the loop filter order is limited to the order 5 ([24]) to 6, in order to manage stability. Multi-stage noise-shaping (MASH) can be used to overcome this limitation.

Numerous delta-sigma architectures are used ([25]), mainly characterized by

- The feedback filter technique: continuous-time, discrete-time
- The loop filter type: feed-back, feed-forward,
- The loop filter order
- The quantizer: single-bit, multi-bit
- The number of quantizers: single-loop, cascaded

Provided flexible loop and decimation filters, low-cost, low-power multi-mode sigma-delta ADCs can be realized ([24]).

As they make use of over-sampling, in order to reach high performance with loop filters of realistic orders, the maximum BW which can be quantized by delta-sigma converters is therefore lower than with a Nyquist-rate flash or pipeline ADC.

1.3.5 Time-interleaving

Time-interleaving technique ([26]) allows building high-speed ADCs at reasonable area and power consumption.

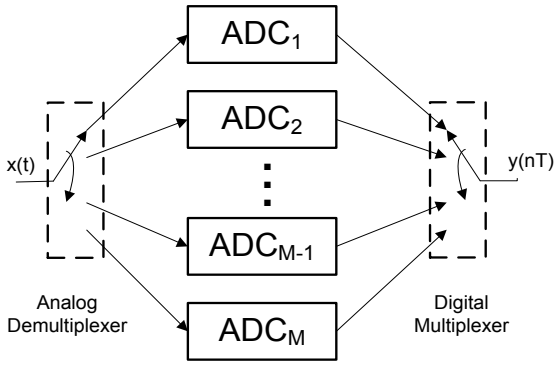


Fig 27. Time-interleaved ADC

Fig 27 shows a simplified block diagram of a time-interleaved ADC. It consists of M ADC's in parallel, an analog de-multiplexer at the input, and a digital multiplexer at the output. Each ADC operates at the overall sampling rate divided by M (Fs). During operation, the analog de-multiplexer selects each ADC in turn to process the input signal. The corresponding digital multiplexer selects the digital output of each ADC periodically and forms a high-speed ADC output. With interleaving, the overall sampling rate is MxFs, which is M times higher than the sampling rate of the ADC in each channel. The required die area and power dissipation are also increased by about a factor of M.

Unfortunately, performance of interleaved ADC's can be severely degraded by mismatches between the individual sub-channels, namely offset, gain, timing and transfer function mismatches. These mismatches create discrete spurs, and images of the input signal, on the output spectrum. Offset, gain and timing skew mismatches can be reduced using mixed-signal or digital calibration techniques.

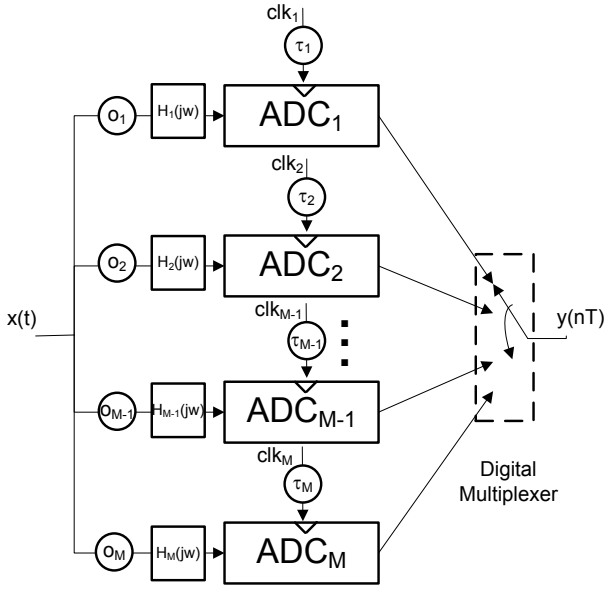


Fig 28. Time-interleaved ADC with channel mismatches

In addition, the S&H must be designed for an extended input signal bandwidth (xM), in order to benefit from the increased sampling rate (xM).

High-speed low-resolution ADCs can make extensive use of parallelism. For instance, [27] presents a 20 GSps 6-bit ADC using 80 sub-ADCs. A single input buffer drives the 80 THs, each one connected to an ADC. The ADC is based on a reduced-radix current-domain pipeline.

In [28], a 40GSps 6-bit ADC using 16 SAR ADCs is presented. In order to preserve the input bandwidth, the TH circuits are split into 2 banks of 8, driven through a 6-dB loss power splitter.

In high-resolution ADCs, as the TH input capacitance increases (dictated by KT/C noise), only few TH units can be parallelized in order to preserve the input BW and minimize BW mismatches. In addition, using few units reduces complexity so allows minimizing sampling clock time skew. If the speed requirement necessitates the use of many ADCs, some kind of TH hierarchy must be used, as conceptually shown in Fig 29. This does come at the disadvantage of adding noise and non-linearity of the additional buffer stages.

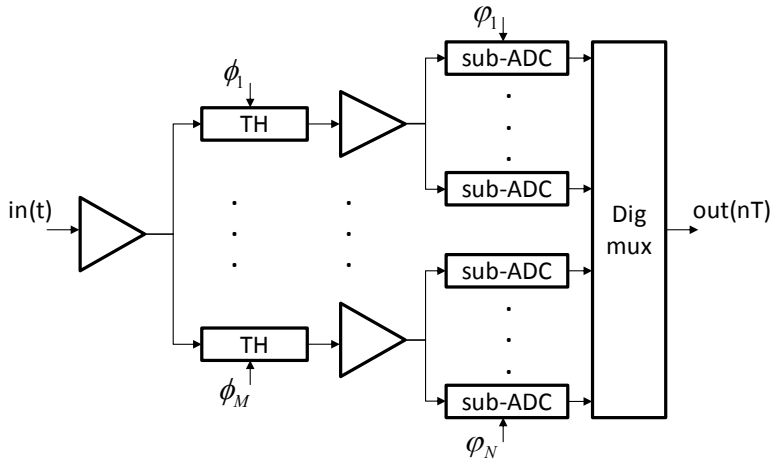


Fig 29. TH hierarchy

1.3.6 ADC state-of-the-art comparison & expected future trends

A survey collecting data from 1997 to 2012 is available in [10]. Reference [11] gives an insight into the distribution of the different architectures in a BW versus SNDR plane, and is used in Fig 30:

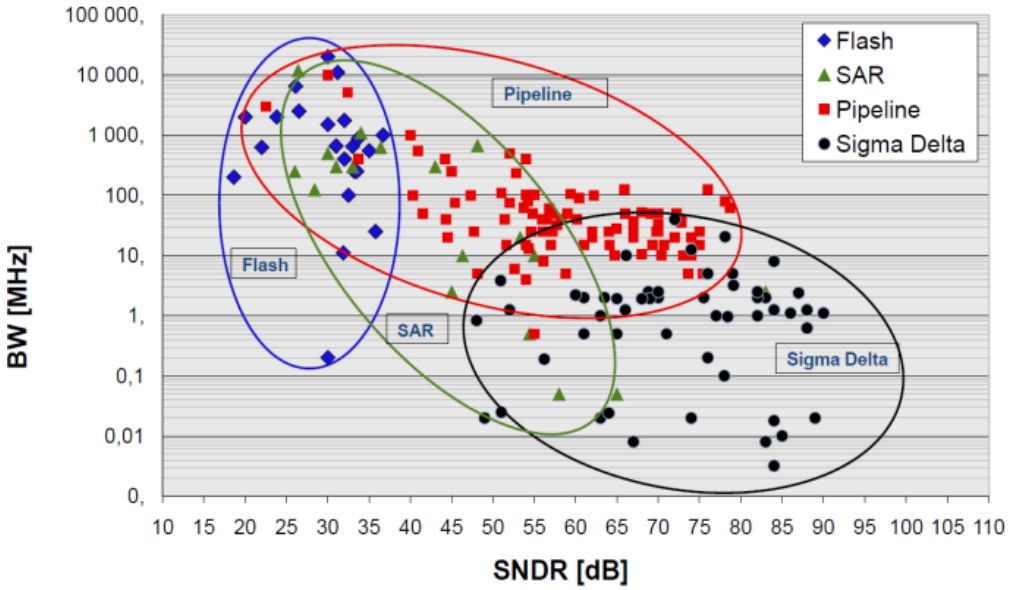


Fig 30. ADC state-of-the-art in a SNDR-BW plane

State-of-the-art shows that CMOS processes gate scaling facilitates the increase of sampling rate of data conversion

functions (ADCs, DACs).

From the other hand, downward scaling of supply voltage in CMOS processes, required to compensate for the reduced oxide thickness, exacerbates the design of high-dynamic-range data converters.

Obviously, modern CMOS processes allow massive integration of DSP functions, required for detecting and correcting analog impairments.

Therefore, we expect that future high-speed high-performance ADCs will extensively use:

- Over-sampling for trading resolution against sampling rate, in order to provide a low output noise-density,
- A mixture of mixed-signal techniques (chopping, randomization, shuffling, calibrations….) and fully digital techniques (equalization of time-interleaving errors, post-correction of non-linear distortion…), in order to offer a high spurious-free dynamic range. Full-digital calibrations become more and more power and area efficient.

1.4 Continuous-time receivers

1.4.1 Super-heterodyne

Super-heterodyne receiver has been invented by Armstrong in 1918 and is still used even if some changes have been made compared to the original architecture.

Fig 31 illustrates the concept with a dual super-heterodyne receiver. It includes a first bandpass RF filter which selects the desired RF band, and also acts as an image-reject filter for the first down-converter. The selected RF signal is amplified by a LNA, and down-converted to a first intermediate frequency (IF1). LO1 signal has to be tunable over the desired RF band. The IF1 is chosen high-enough in order to allow the RF filter to sufficiently attenuate the signal lying at the image frequency. After down-conversion, the signal is again image-filtered. Then, a second down-conversion operation is achieved, and the final channel selection is performed by the fixed channel filter, providing enough attenuation of adjacent channels prior to the subsequent processing in the demodulator. Thanks to the various degrees of freedom provided by the multiple frequency translations, both a good image rejection and a good channel selection can be achieved.

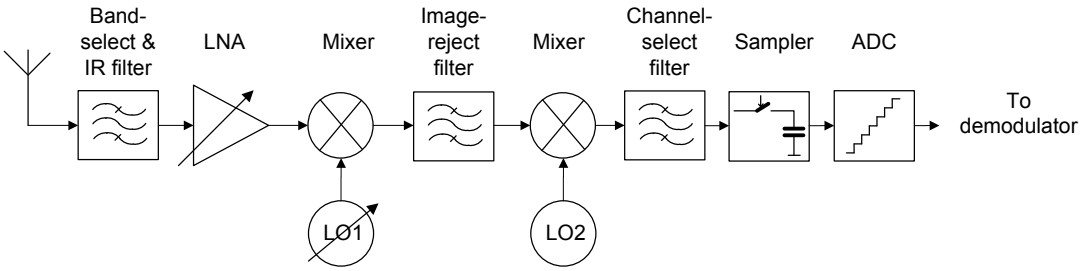


Fig 31. Dual Superheterodyne receiver

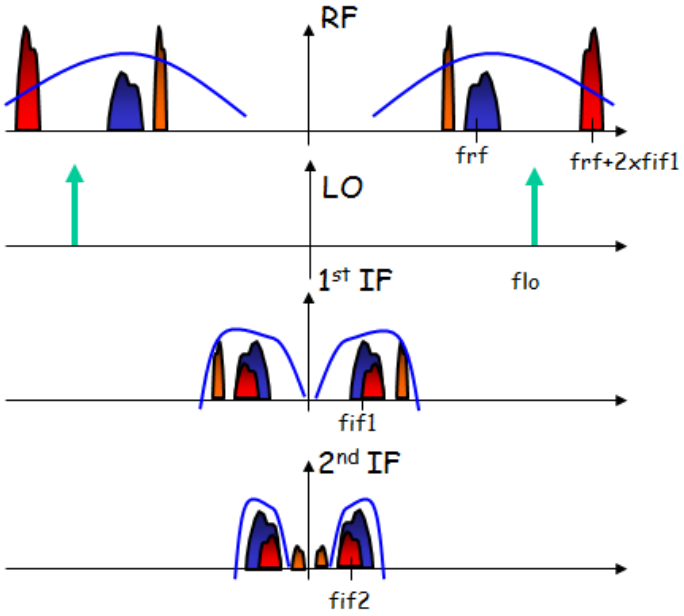


Fig 32. Signal processing operations in dual superheterodyne receiver

The first down-conversion stage is sometimes replaced by an up-converter: an example for TV reception using a dual-conversion approach is presented in [29].

As a matter of fact, super-heterodyne makes use of several high-Q filters, which are difficult-to-integrate. These filters are typically bulky, and require high-power drive capability. They are therefore not adequate for low-power,

highly-integrated and multi-standard receivers.

1.4.2 Homodyne

The homodyne receiver (also called Direct-conversion or Zero-IF) directly translates the RF signal to baseband without the use of any intermediate frequency. Therefore, only one RF bandpass filter is required. Frequency translation is achieved by a quadrature down-converter which creates a complex quadrature (I/Q) signal. As the signal is centered at DC, this avoids that the portion of signal located at negative frequencies folds on top of the signal located at positive frequencies. Channel selection is now performed by lowpass filters instead of bandpass filters in super-heterodyne. Baseband signal amplification and analog-to-digital conversion are applied to the selected channels.

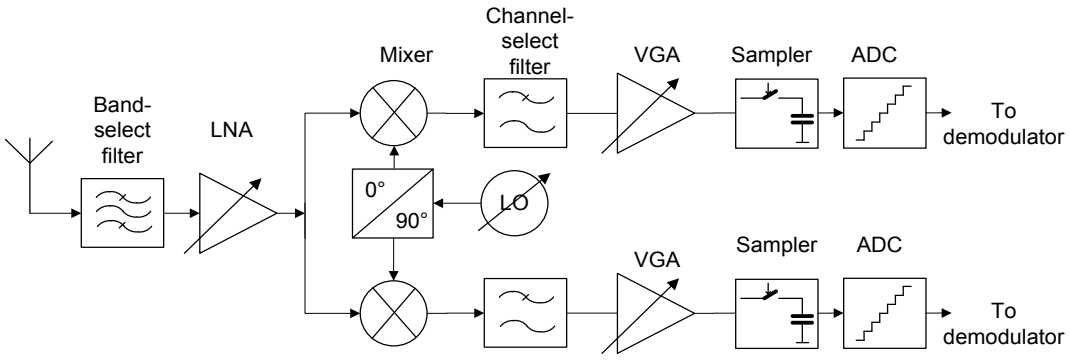


Fig 33. Homodyne receiver

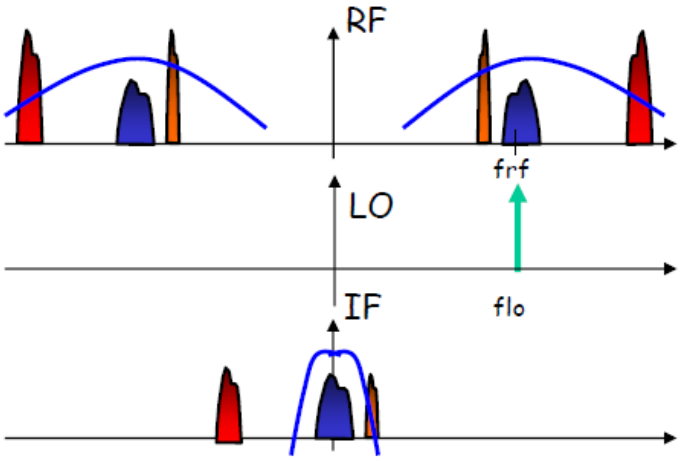


Fig 34. Signal processing operations in a homodyne receiver

However, homodyne receivers pose several design challenges ([30]):

The DC offset of the baseband path is superimposed on top of the down-converted channel. It is mainly generated by the LO leakage (LO port to RF port) which self-mixes, thereby creating a DC component in the signal chain that affects the receiver performance and can even cause saturation of the IF stages. Calibration loops are required to compensate for this DC offset.

Similar to DC offset, the flicker noise has high power at low frequencies that can be superimposed on top of the down-converted channels. Passive mixers, large-area MOS and periodic offset cancellation loops are used to

mitigate this effect.

I/Q imbalance (amplitude & phase) can degrade image rejection. Still, this image problem is reduced in a homodyne receiver since the image is one side of the received channel itself, as opposed to a heterodyne receiver where the channel lying at the image frequency can have much higher amplitude. In addition, I/Q digital calibration techniques can keep this effect under control ([31]).

In case the homodyne receiver is fed with two closed RF channels ($F_{RF1} = F_{RF2} + \varepsilon$), second-order non-linear distortion causes unwanted power at baseband ($f = \varepsilon$) at the mixer input. Again, feed-through from the RF port to the baseband port of the mixer creates overlapping of unwanted power on the wanted channel at baseband.

Despite these technical challenges, the monolithic integration of homodyne receivers allowed major break-through within the cellular phone industry ([34], [37]).

In addition, provided a broadband LNA (or multiple narrowband LNAs) and a flexible synthesizer [38], the homodyne receiver can be designed multi-band. If a flexible baseband filter is designed, the homodyne receiver can also address several communication standards.

An advanced implementation of a homodyne receiver for 900MHz cellular phone band is embedded in a 4th-order delta-sigma loop ([39]) as shown in Fig 35. The 1st stage of the delta-sigma prototype is transferred to RF using an up-mixer. In addition, an N-path frequency translation technique is used to build a filter at the first stage (gm1) output. This technique allows translating a low-Q lowpass filter prototype toward RF frequencies to become a high-Q RF bandpass filter, using only switches and capacitors ([40]).

The second stage is a CT quadrature mixer in the current mode. Baseband processing includes 3 CT integrator stages and 1-bit quantizer. As the frequency-translated RF delta-sigma feedback reduces in-band signals, while the N-path filter attenuates out-of-band interferers, both RF front-end and down-mixer are protected against in-band and out-of-band interferers, which improves the receiver linearity.

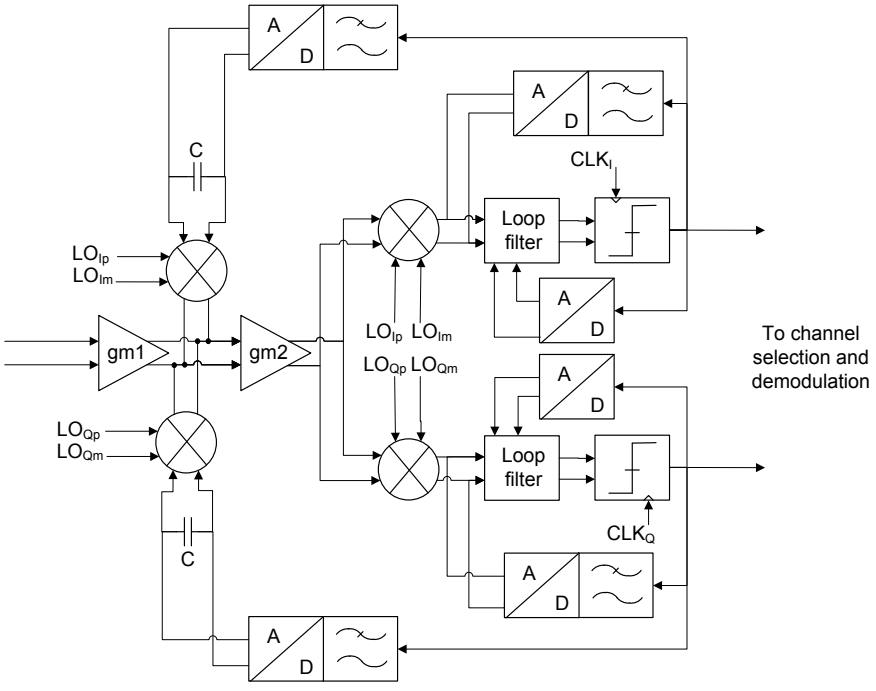


Fig 35. Direct conversion delta-sigma receiver

1.4.3 Low-IF

Low-IF is a trade-off between heterodyne and homodyne: the IF is slightly increased from DC to a frequency which

allows avoiding the DC and flicker noise issues of homodyne receivers. Therefore, low-IF keeps the high-integration and high flexibility properties of homodyne. The final translation from Low-IF to DC is performed in digital signal processing.

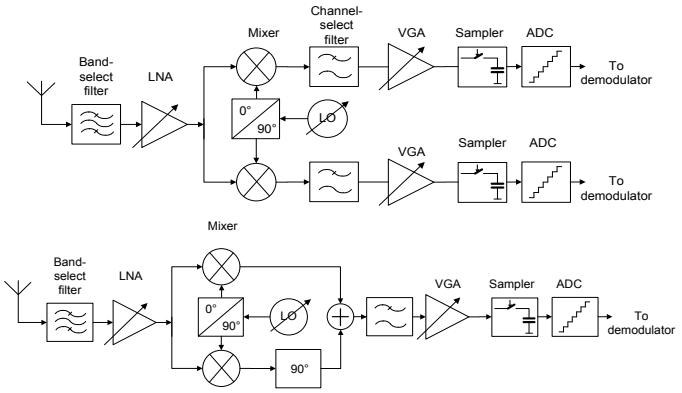


Fig 36. Low-IF receiver (left: complex baseband, right: real baseband)

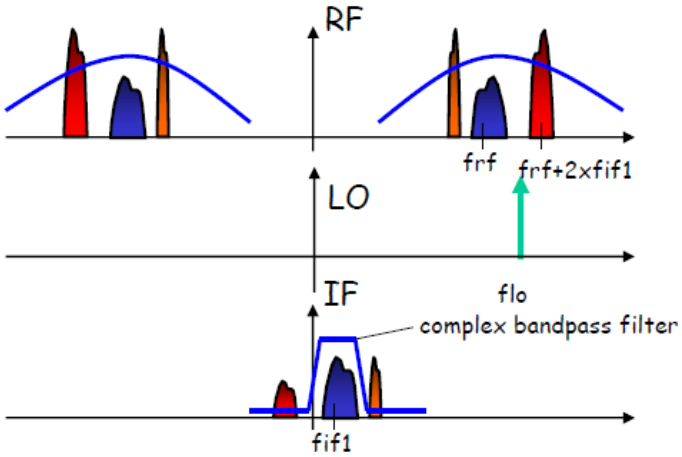


Fig 37. Signal processing operations in a low-IF receiver

However, the IF frequency shift has one drawback: as the channel lying at the image frequency can be much higher than the wanted channel, requirements on low-IF image rejection are much higher than on homodyne receivers. This issue can be alleviated by the use of a double-quadrature mixer. In case of digital I/Q signal path, this can also be mitigated using DSP techniques ([31]).

References [32],[33],[34] and [35] show broad-band low-IF implementations for high-performance cable and terrestrial TV receivers.

When wideband multiple-channel implementations of receivers are involved, homodyne and complex low-IF are equivalent, as the receiver can be viewed as homodyne only for the middle channel (ch3 in Fig 38) when the total number of channels is odd, while it is equivalent to a low-IF receiver for the other channels (ch1, ch2, ch4 and ch5 in Fig 38).

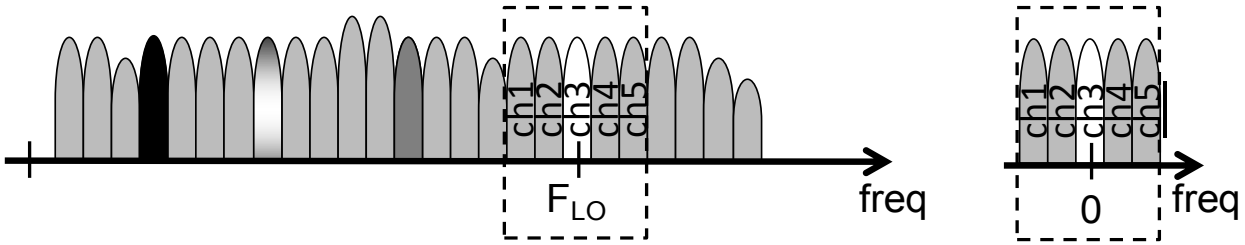


Fig 38. Multiple channels reception a complex low-IF / homodyne in a wideband RX. Left: RF signal. Right: IF signal

Partial integration of wideband multiple-channel homodyne/low-IF receivers are reported in the wireless infrastructure industry, while full-receiver integration is reported for cable modem applications:

- Reference [41] reports the IF main and diversity sections of a dual-channel GSM/EDGE. It integrates two IF amplifiers, two quadrature mixers for down-converting the 70-300 MHz IF1 to a zero-IF. Two I/Q 7th-order integrated anti-aliasing filters ensure 70dB of alias attenuation. Two double-speed 52MSPS 12-bit ADCs are shared between I/Q path, in order to minimize I/Q mismatch. Two digital front-ends correct DC-offset, perform the final frequency translation and the individual channels selection. Fabricated in a 0.35um BiCMOS process, it also includes the VCO/synthesizer, and consumes 1.5W.
- Up to 4 contiguous WCDMA channels are simultaneously received by an RF front-end in [42]. It operates over the RF band 1.7-2 GHz. It integrates a single-input LNA with differential output, a quadrature mixer, and an active 4th-order programmable LPF. It has been integrated in a 0.25um SiGe BiCMOS process, consumes 550 mW, and features a 2.2dB NF in high-gain mode (Av=51.5 dB) and low-IF output, together with a -10 dBm IIP3.
- Reference [43] demonstrates a 2x32 MHz-BW tuner able to receive 8 to 10 contiguous RF channels in the 42 -1002 MHz. It integrates in a 65nm CMOS process a variable-gain LNA, harmonic-reject mixer helped by an RF tracking filter, a 5th-order Butterworth anti-aliasing filter, a baseband VGA I/Q pair, a 11-bit 175 MSps ADC I/Q pair, a low-noise PLL, a digital offset-correction loop, a digital image-correction, and digital individual channel selection.

1.4.4 Digital-IF receiver

In digital IF receivers (Fig 39), a digital down-converter replaces the second down-conversion stage of a dual-heterodyne receiver. This is made possible by the digitization of the first IF, and complex digital down-converters. As the IF is relatively high, this configuration can be designed multi-standard, and has the potential to perform the simultaneous reception of multiple channels with a single receiver (with multiple parallel DDCs), therefore providing a low-power and low-cost implementation, without image rejection concern since the full analog path is real.

The main challenge is the analog-to-digital converter required performance [44]:

- Limited selectivity in the IF BPF leads to potential strong adjacent channels at the ADC input: this requests both low-noise and low distortion in the ADC
- The ADC input BW must be aligned with the IF signal BW, while its clock frequency must be at least twice.

A slightly different configuration allows relaxing part of the ADC requirements: if the IF signal BW is sufficiently low, IF sub-sampling can be performed in order to reducing the ADC clock frequency ([45]). This configuration is sometimes called IF-sampling, or IF-sub-sampling.

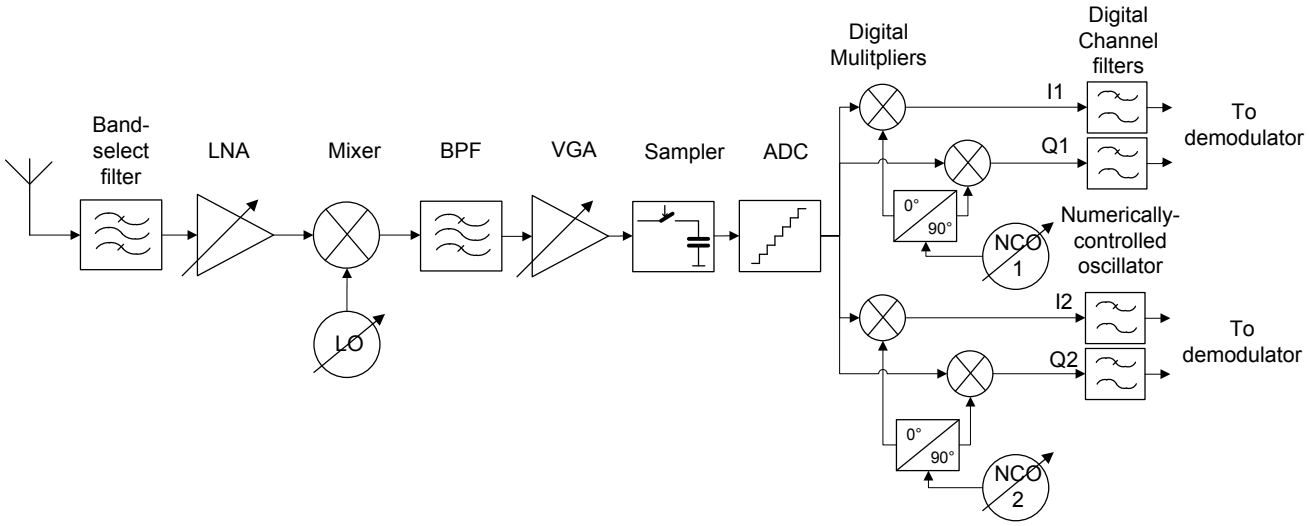


Fig 39. Digital-IF receiver

1.5 Discrete-time receivers

1.5.1 Discrete-time analog-processing receivers

RF DT analog-processing receivers make use of a sampler, instead of a CT mixer, at the LNA output. DT analog filter and down-sampler ([46]) are used to reduce the dynamic and the sampling rate requirements of the ADC, as CT filters do in a usual CT receiver.

Therefore, RF DT analog-processing receivers can be viewed as a DT implementation of a homodyne or low-IF CT receiver. Fig 40 provides a principle diagram of such a receiver ([47]): after external RF band selection, the LNA provides the RF signal to a quadrature sampler, which down-converts the RF signal to IF, provides anti-aliasing protection and sampling-rate reduction prior to analog-to-digital conversion. Channel selection is typically performed using DSP techniques.

The potential down-conversion of interferers with LO harmonics that is encountered in CT receivers is replaced by the aliasing of interferers due to sampling rate reduction in DT receivers.

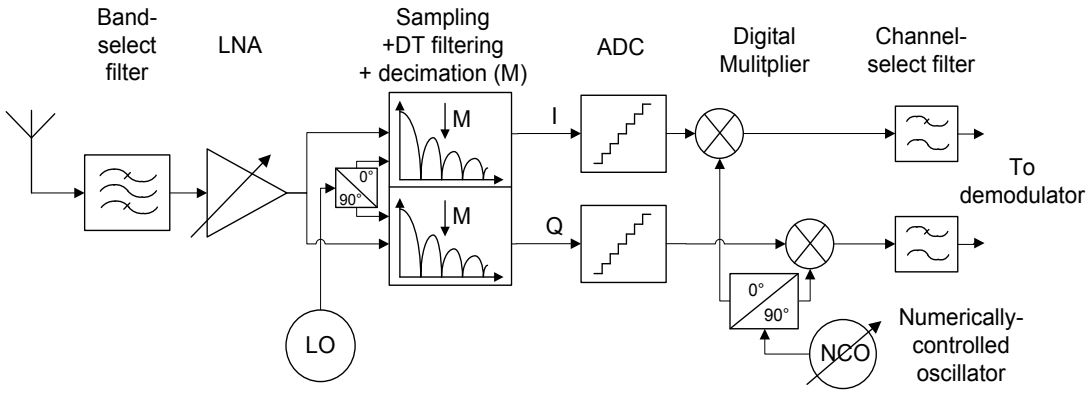


Fig 40. Discrete-time receiver principle diagram

In the first reported product implementation of RF DT analog-processing receiver ([46]), the front-end sampler makes use of sub-sampling in the 3rd Nyquist zone for performing a quadrature down-conversion to a low-IF. A combination of charge-domain FIR and IIR filters are used to perform anti-aliasing protection prior to sampling-rate reduction.

In the example of Fig 41 [48], a charge-domain FIR filter is realized by integrating N successive samples of the RF waveform on two switched equal capacitors. This moving average FIR filter (all-ones coefficients) places notches at multiple frequencies of fs/N.

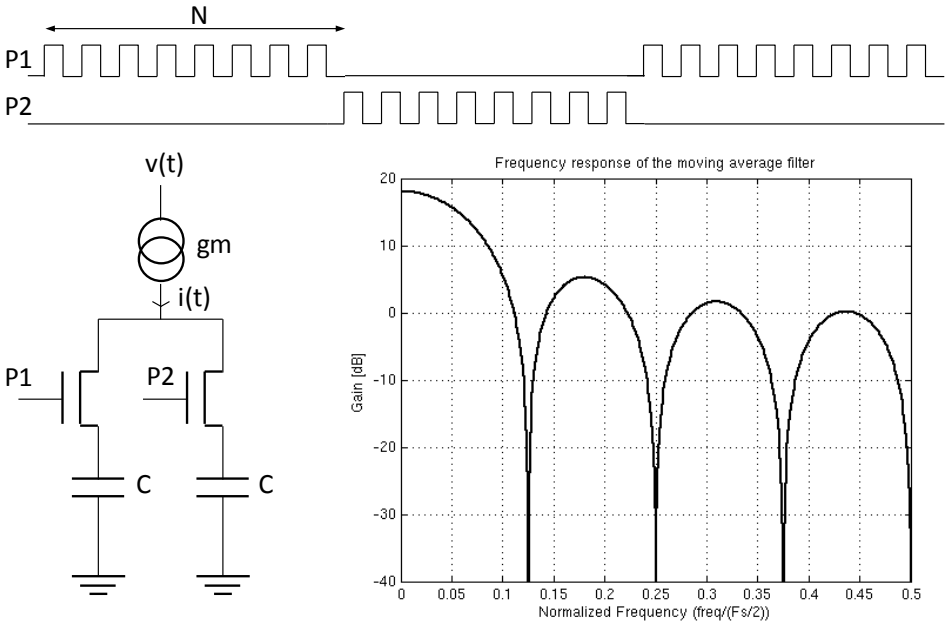


Fig 41. Example of analog FIR filter in the charge domain

The main obstacle for building wideband DT analog processing receivers is their intrinsic narrowband protection against aliasing: sinc-response FIR filter attenuates potential interferers only across the notches BW located around $k \cdot fs/N$. Non-decimated FIR filter forms allow cascading several filters prior to sampling-rate reduction, in order to increase the notches BW. Ref [49] / [50] reports 60dB / 90dB attenuation of interferers across 50 MHz / 10 MHz.

Besides discrete analog signal processing in the time-domain, research is also conducted on analog implementations of FFT ([51], [52]): in the context of software radio systems using OFDM, the move from DSP-based FFT to analog-based FFT allows filtering narrowband interferers prior to analog-to-digital conversion, which leads to a more robust receiver. In addition, analog implementations make high-speed low-power FFT possible: [52] demonstrates a 1GSps 8-points DT complex FFT consuming 25 mW in CMOS 0.13um.

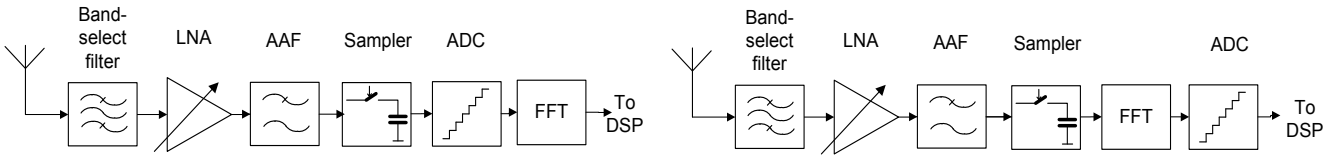


Fig 42. Move from DSP-based FFT (right) to analog-DT-based FFT (left)

1.5.2 Hybrid-Filter Bank (HFB) receiver

HFB receivers ([57]) decompose the RF input signal in the frequency domain, using an analog filter bank (analysis bank). The filtered RF signals are synchronously sub-sampled (Fs/M), quantized, interpolated, and recomposed using synthesis filter bank, for proper reconstruction of the wideband input signal. Despite the local aliasing, which occurs in each path, a perfect reconstruction can still be achieved if a specific relation-ship holds between analysis and synthesis filter banks.

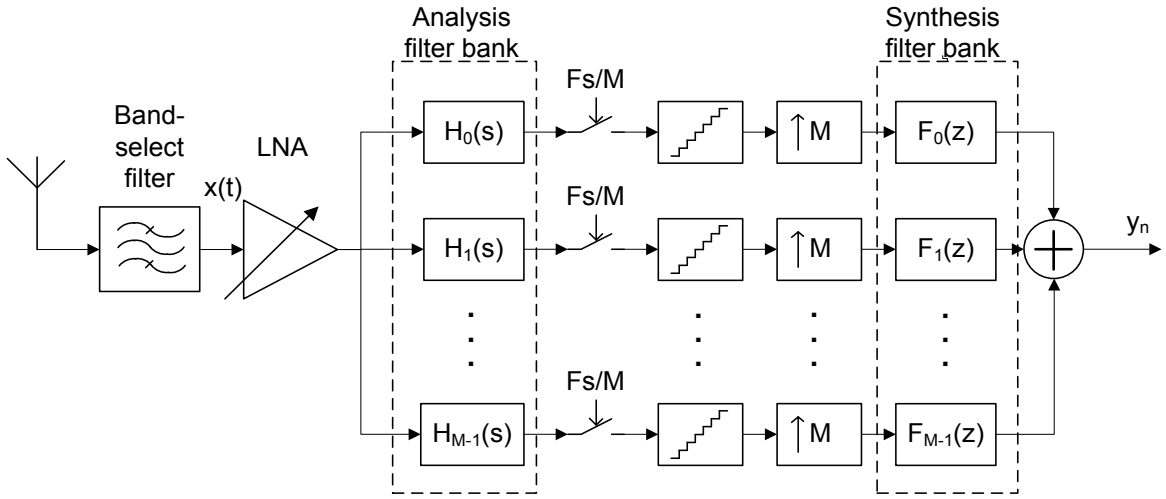


Fig 43. HBF receiver (left). Transfer functions of the analysis filter bank (right)

The system is called Hybrid since it makes use of both analog and digital filters.

HFB receivers are an active research topic since this configuration allows building a high-speed ADC from lower speed sub-ADCs, theoretically maintaining the sub-ADC performance over a higher sampling rate. Another interest is their ability to trade BW for performance in a versatile way. The software-controllable frequency-focusing capability ([58]) could be suitable for spectrum sensing in cognitive radio systems. In this context, programmable synthesis filter coefficients would allow HFB receivers to be either used as low-resolution broadband spectrum sensors or high-resolution narrowband receivers.

Different implementations of HFB use either CT or DT analog filters, potentially using CT or DT mixers for frequency translation of the filter transfer function. Work has been carried out to achieve quasi-perfect reconstruction while minimizing the analog filters complexity ([59]).

Their DT realization using charge-sampling filters are appropriate for integration in deep CMOS process nodes ([60]).

However, since practical implementations of analog filters are subject to manufacturing spreads and temperature drifts, their transfer functions deviate from the theoretical ones. Hence, the specific relation-ship which is necessary to be held between analog and digital filter banks for approaching perfect reconstruction is not fulfilled on a product environment. As performance of HFB receivers is highly sensitive to the analog filter transfer functions ([61], [62]), background calibration are required to solve this issue. This technical obstacle makes HFB receivers not used in commercial products yet.

1.5.3 Direct RF digitization receiver

Instead of using mixers, RF input signal band splitting, or discrete-time filtering for reducing speed and dynamic range requirements on the quantization process, direct-digitization receivers perform straight sampling and digitization of the wideband RF input signal with minimum analog hardware.

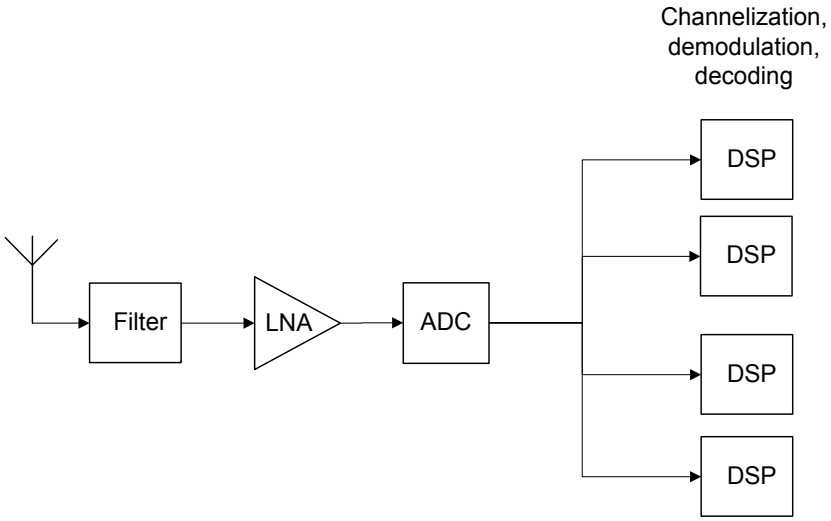


Fig 44. Multi-channel direct RF digitization receiver

Several forms of direct-digitization exist, depending on the ADC type:

- Filtering ADC
- Nyquist-rate

And on the sampling strategies:

- Lowpass sampling: B=[DC ; $fs/2$]
- Bandpass sampling: B=[$N \cdot fs/2$; $(N+1) \cdot fs/2$]

Fig 45 illustrates, in the frequency domain, the different nature lowpass/bandpass Nyquist-rate ADC, and bandpass sigma-delta ADC.

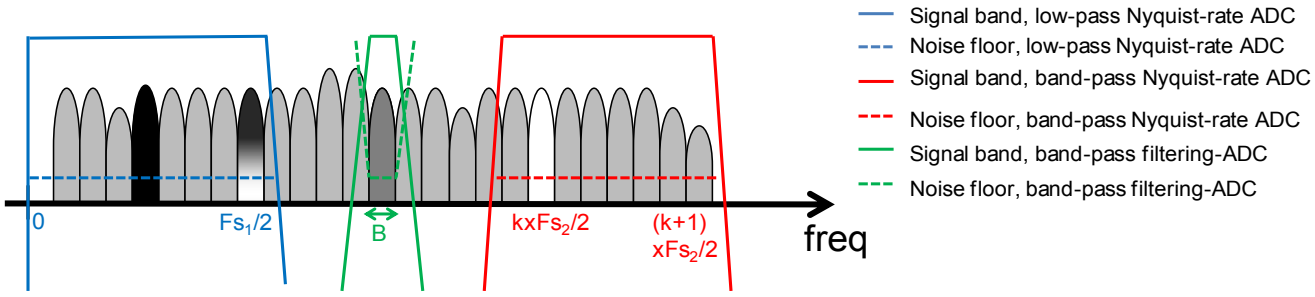


Fig 45. Direct-digitization receivers signal bands and noise floor

1.5.3.1 Bandpass direct RF digitization receiver using filtering ADCs

RF bandpass direct-digitization can be implemented using filtering ADCs: if the ΔΣ loop filter has a bandpass response, centered across the input signal band, the ΔΣ ADC samples and quantizes this input signal while rejecting out-of-band RF signals, and shaping the quantization noise outside of the filter pass-band.

This allows reaching low in-band quantization noise, even with low-order quantizers (single-bit for instance). Fig 46 illustrates the principle block diagram of bandpass ΔΣ ADCs.

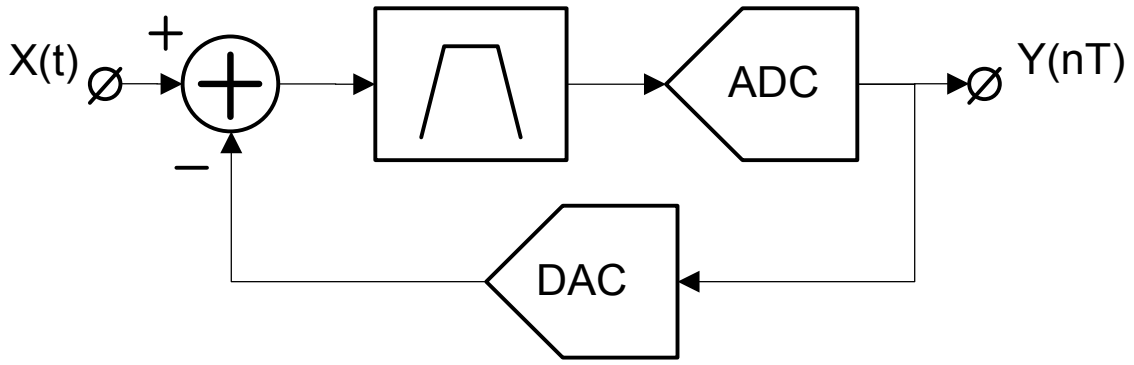


Fig 46. Direct digitization receiver based on bandpass filtering ADC

Capture bandwidths up to ~100MHz have been reported for RF carriers ~2 GHz for CMOS and SiGe processes ([64] provides a complete comparison).

If the system has to cope with a wide range of input RF frequencies, the ΔΣ must be designed flexible, as no RF mixer is used. This flexibility can be reached at the cost of a tunable RF bandpass loop filter. For instance, [65] demonstrates a tunable 6th-order feedback RF ΔΣ ADC with DR=74 dB and BW=150 MHz, using a combination of one RC and two LC resonators to cover the DC-to-1 GHz RF input band. The converter necessitates the use of two external inductances, and exhibit large performance variations across the RF band due to the switching between the three filters.

For applications that necessitate the simultaneous reception of multiple radio bands, a parallel combination of filtering ADCs with complementary transfer functions can be designed. Reference [63] realizes a 9GHz-13GHz digitizer using four bandpass delta-sigma ADCs designed with a superconductor material.

1.5.3.2 Lowpass direct RF digitization receiver using Nyquist ADCs

Instead of using a filtering ADC embedding a loop filter and a low-order quantizer, sampling and quantization of an RF signal without filtering can be achieved. As the solution does not benefit from noise-shaping, a higher-order quantizer must be used, in order to reach the same level of performance as a filtering ADC. This architecture is prone to acquisition of very high-bandwidth signals.

Very few realizations have been reported. In [53], a high-linearity software radio for HF band [0 to 31 MHz] is realized. It uses a cascade of 7th and 9th order elliptic lowpass anti-aliasing filters, GaAs FET-based attenuator, GaAs MMIC amplifier, and 14-b 65MSps ADC. The ADC non-linearity power is re-distributed across the Nyquist bandwidth using a narrowband dithering technique ([54]). The full receiver approaches the performance of high-quality super-heterodyne receivers. Still, the carrier frequency, and the processed signal bandwidth are limited. In addition, the solution is not integrated and makes uses of RF blocks in expensive technologies.

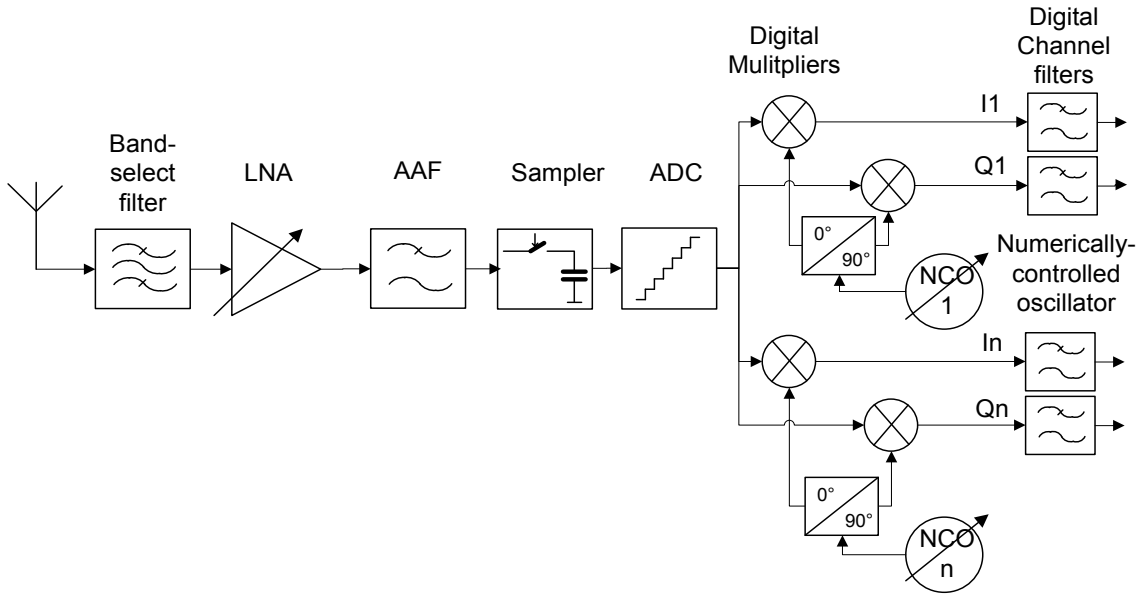


Fig 47. Direct digitization receiver based on Nyquist ADC

1.5.3.3 Bandpass direct RF digitization receiver using Nyquist ADCs

As shown in section 1.2.2, a bandpass RF input signal can be directly sub-sampled by a low-rate ADC, without any analog mixer in the signal path. In the case of bandpass signal reception, sub-sampling allows relaxing the ADC sampling rate and reducing the speed of the required digital signal processing, compared to lowpass sampling.

These advantages do not come for free. In order to mitigate aliasing, a high-Q RF anti-aliasing filter is required for attenuating RF front-end noise and out-of-band interferers. Still, the ADC sampling rate must be carefully chosen (see 1.2.2). In addition, the aliasing of wideband jitter that occurs during the sampling process (see 2.2.8.2) puts a tough requirement on the clock signal quality.

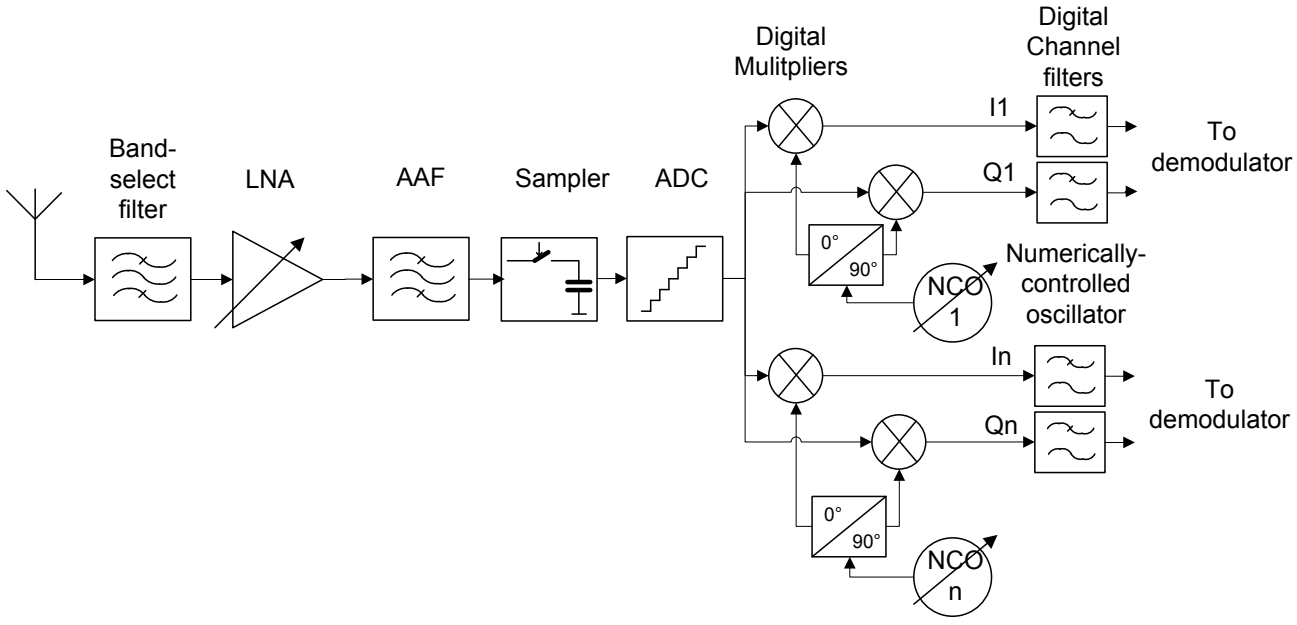


Fig 48. RF sub-sampling receiver

RF sub-sampling receivers have been experimented for Global Navigation Satellite System (GNSS) applications

([55]): [56] reports the simultaneous reception of two 20MHz-wide signals located into two adjacent Nyquist bands (GPS signal at F_{RF1}=1227.6 MHz, GLONASS signal at F_{RF2}=1575.42 MHz), with a sub-sampling frequency of 91.956 MHz.

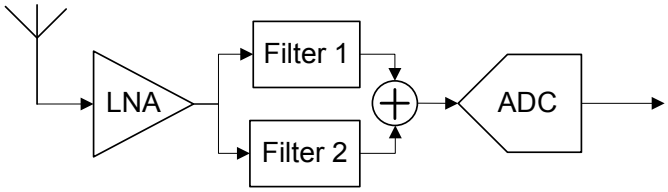


Fig 49. Multiband GNSS sub-sampling receiver front-end

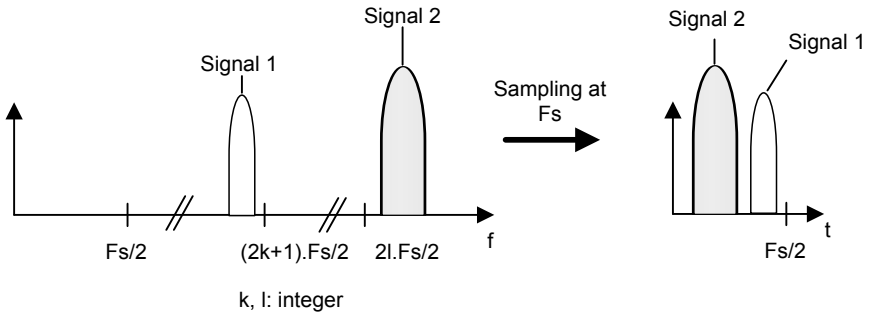


Fig 50. Multi-band GNSS RF spectrum (left). Spectrum after sampling (right)

This illustrates how a single sampling action performs two different frequency translations. Still, the required RF pre-filters limit the receiver's flexibility.

1.5.4 Summary & work orientation

For applications that require the reception of one narrowband channel, homodyne, low-IF and discrete-time receiver architectures are the most adequate architectures (cost, size, power).

For applications that require the selection of a moderate bandwidth signal, it is expected that digital-IF, wideband LIF or homodyne are the most adequate architectures (cost, size, power).

In the context of DC-3 GHz radios necessitating the reception of several RF channels across a 1GHz RF band, a mixer-based solution would require several parallel receivers, each one capturing a specific sub-band. A possible implementation uses a complex mixer and sampling and digitization of analytical signals.

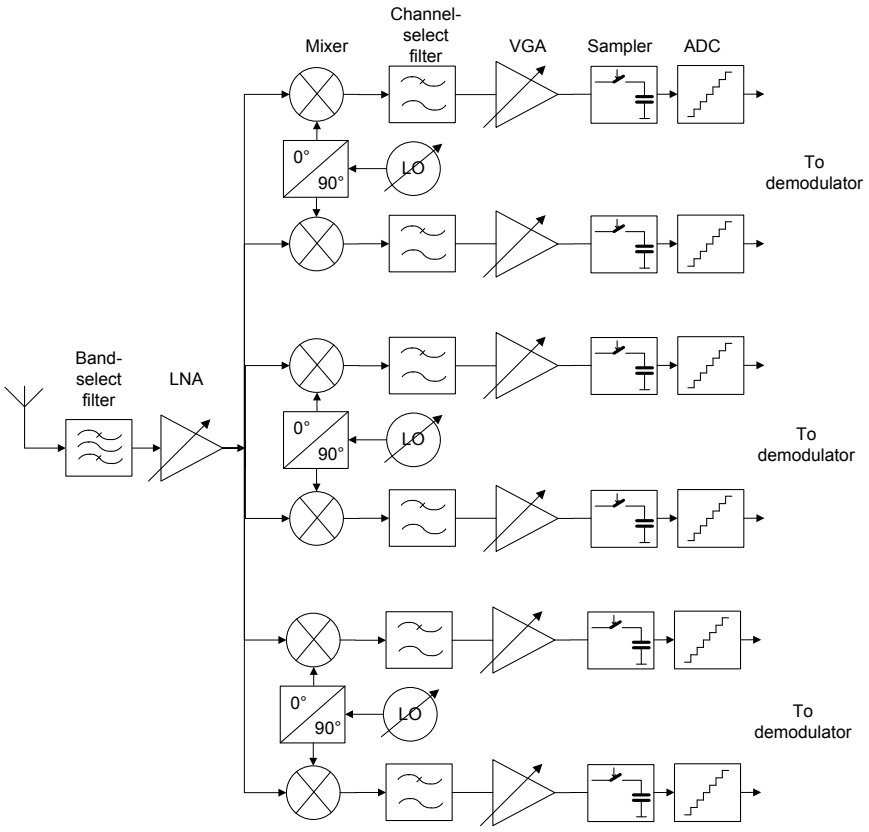


Fig 51. Sub-band splitting with analytic signals and down-conversion

As studied in [66] for applications in the DC-1GHz range, using analytical signals, a sub-band decomposition with analog down-conversion concept seems to require a higher die area, while not significantly providing a power-consumption advantage, compared to direct RF sampling receivers. In addition, this sub-band decomposition puts a bound on the maximum channel bandwidth that can be captured. The architecture is therefore limited to the reception of multiple narrowband channels, and should be seen as a way to extend the bandwidth and dynamic range of the sub-ADCs.

Direct-digitization receivers have the potential to provide very high-bandwidth reception, at low power and low size in several kinds of applications:

- **"High-density" applications:**

These applications have the following property:

$$\frac{\sum_{k=1}^{N} BW_k}{F_{RF\max} - F_{RF\min}} >> 0 \qquad (1.22.)$$

Where BW_k is the bandwidth of each individual channel that is required to be received, N is the average number of channels required to be received over time.

$F_{RF\max}$ & $F_{RF\min}$: bounds of the RF band.

They can typically be multi-channel applications with a high number of channels, or UWB applications. Here, direct RF sampling also has the uniqueness of allowing digital signal processing over the full-band RF signal.

- **"Multi-octave" applications:**

In these applications, RF mixers pose serious challenges and strongly influences the receive architecture, due to mixing with LO harmonics. Direct RF sampling simplifies the architecture and alleviates these issues.

Direct-digitization features several additional advantages, compared to the other receiver architectures, which come with the early digitization:

- Tunability: any RF signal within the ADC input bandwidth (or at least within one Nyquist zone) can be processed, as no narrowband filter is used. The Digital Channel selection can be made tunable, especially in advanced CMOS technologies
- Flexibility: as the full RF signal band is available in a digital format, additional signal processing techniques, that are not possible with analog receivers, can be applied to direct-digitization receivers
    - Full-band FFT (spectrum sensing in Cognitive Radio, Spectrum observation in military applications, ultra-wideband communications)
    - Linear-phase filtering (channel selection for communication systems receivers)
    - Digital corrections
    - Post-correction of wideband non-linear distortion
- Re-configurability: as the radio is mostly limited to an ADC and digital signal processing, applications using FPGAs allow building standard-agnostic & multi-band radios that are re-configurable by software (Mitola Software Radio)
- Low size / weight and low power consumption: if a wide RF signal bandwidth is required to be received, and as most of the analog processing (RF & IF) is eliminated, an integrated direct-digitization receiver has the ability to provide the smallest, lightest, and lowest-power receiver (wideband multiple element radios: beamforming systems, space telecom re-multiplexers).
- Reliability: since many analog blocks, which are subject to production variations, are replaced by more stable digital signal processing, the receiver reliability is improved.

Next chapter dives into the system design aspects of direct RF digitization receivers.

CHAPTER 2.

System-level design framework for direct RF digitization receivers

In this chapter, a system-level design framework is developed for direct RF digitization receivers.

In the first section, the main system-level requirements and signal characteristics, linked to the RF receiver, are reviewed in the context of communication systems.

In the second section, the direct digitization receiver components and their impairments are studied in details in a broadband context:

- Receiver noise contributions are analysed, taking into account RF front-end thermal noise, and ADC quantization, thermal and clipping noise. A model is proposed to assess the impact of signal-dependent noise on system performance.
- Non-linear distortion in a broadband system is examined, allowing studying the impact of the sampling strategy (lowpass, bandpass) on system performance.
- Impact of ADC time-interleaving channel mismatches is also studied, providing closed-form expression that allows mismatch specification in a broadband environment.
- Transfer of phase noise, from the clock signal to the sampled signal, including in-band, close-in, and distant phase noise regions, are put in equations. This allows taking into account phase noise impact on quadrature modulations, as well as reciprocal mixing with adjacent channels or interferers.

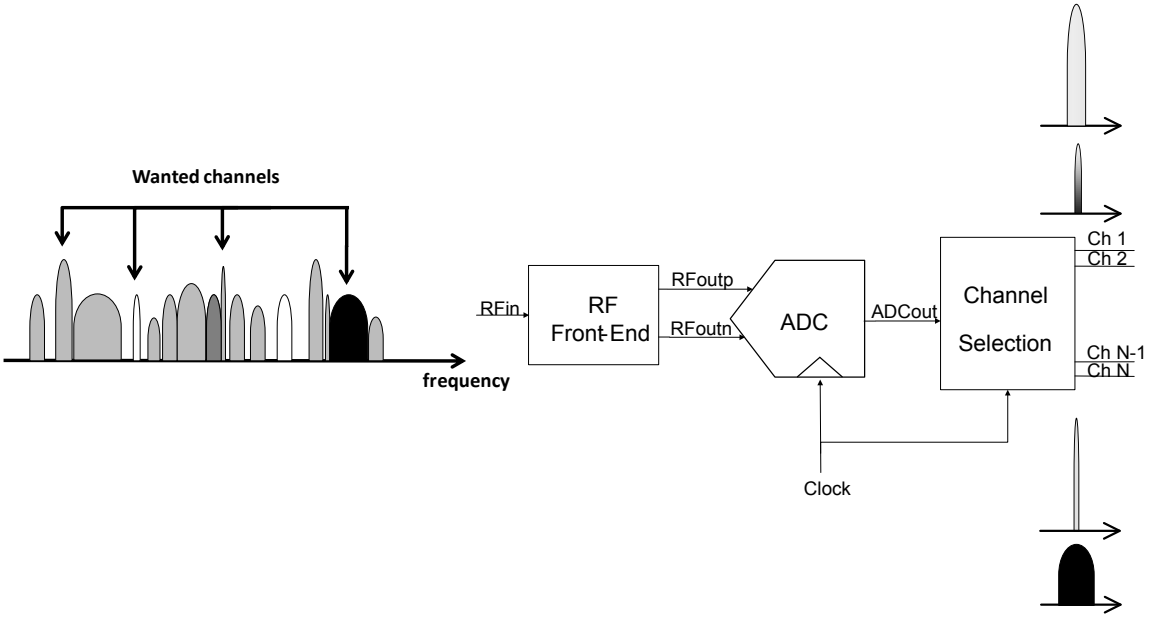


Fig 1. Direct RF digitization receiver

2.1 System-level aspects

In this section a generic communication system is considered. The main relevant characteristics of this communication system that influence the receiver are highlighted.

2.1.1 Signal characteristics

2.1.1.1 Signal distribution

Digital modulation has revolutionized RF communications. Both cellular and broadcast industries have moved from analog to digital modulation. This move causes higher peaks in the signals that can lead to higher distortion, unless it is accounted for in the design of the receiver sub-blocks (amplifiers, mixers, ADCs).

The complementary cumulated density function (CCDF) is an excellent tool for assessing the peak-to-average power ratio (PAPR) of a signal. As described in [74], and shown in Fig 2, CCDF is the complement of the integrated probability density function (PDF) of a signal.

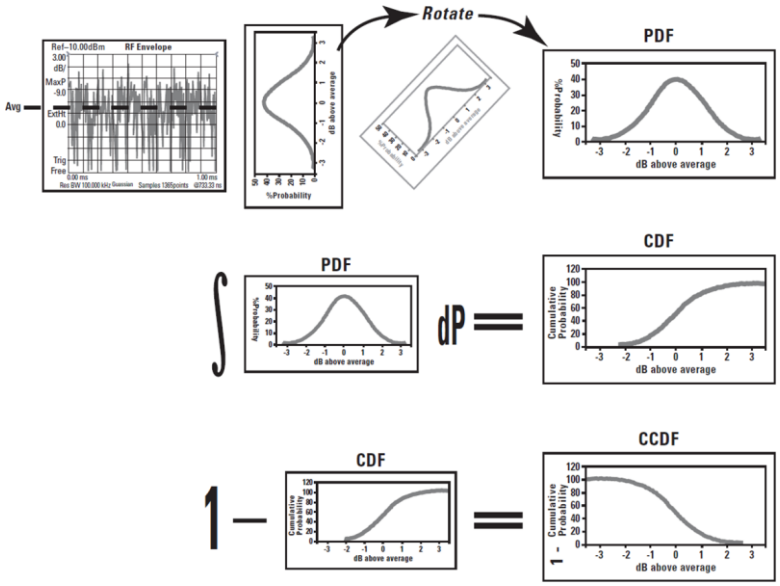


Fig 2. Mathematical origin of the CCDF

CCDF represents the probability (y axis) that the signal power is higher than the average signal power, by a certain amount of dB (x axis). For instance PAPR=10dB, at an assumed probability, indicates that the peak power is higher than the average power by 10dB.

CCDF curves strongly depend upon several system parameters:

- Number of carriers: multi-carrier modulations (for instance OFDM) increase peaks compared to single-carrier modulations
- Type and order of modulation: high-level modulation increase peaks
- Roll-off factor of root-raised-cosine filter: low roll-offs increase peaks

As shown in Fig 3, if a sufficiently high number of channels are used, the distribution of multi-CWs and multi-QAM signals tend to follow a Gaussian law.

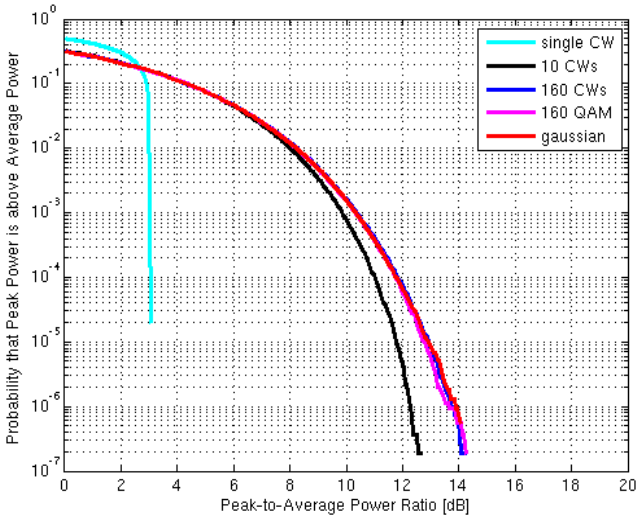


Fig 3. Multi-QAM / Gaussian signals distribution

This agrees with the central limit theorem. In probability theory, the central limit theorem states conditions under which the mean of a sufficiently large number of independent random variables, each with finite mean and variance, will be approximately normally distributed.

In addition, when a large number of channels are added, the initial per-channel distribution (/modulation) does not affect the composite signal distribution.

Therefore, and for the sake of simplicity, a signal with multiple tones is extensively used through this thesis to emulate a signal with multiple digitally-modulated channels.

2.1.2 BER and Es/N0

The starting point of a receiver design is the minimum Bit Error Rate which is required by the system. This BER depends on the integrity targeted by the application. Fig 4 illustrates the required Es/N0 as a function of the required BER, for several modulations. Es/N0 is homogeneous to a signal-to-noise ratio, and is defined across the signal BW.

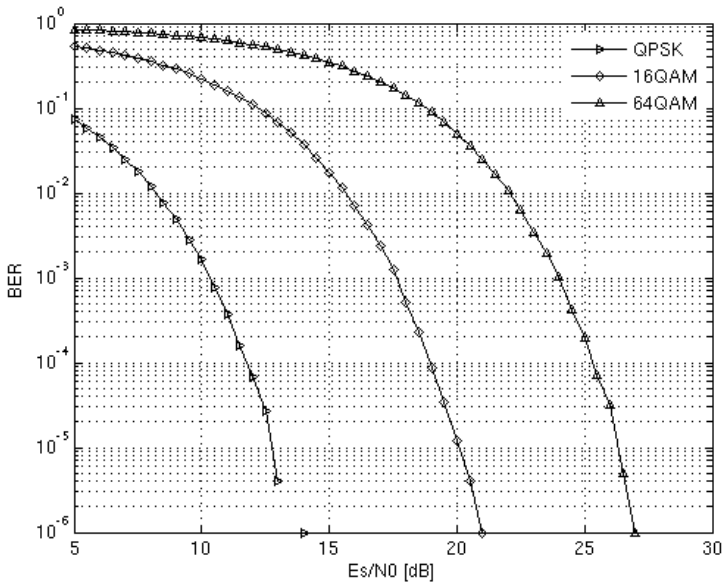


Fig 4. BER versus Es/N0 for several QAM modulations

2.1.3 Sensitivity test

It is the minimum level at the receiver input, at which the receiver must be able to perform with the specified BER.

2.1.4 Adjacent & blocker test

When a communication system has several users, and the channel conditions between users are different, the adjacent and non-adjacent channels can typically be much greater than the wanted channel, especially in wireless communications. In addition, coexistence of several communication systems over the same communication channel leads to strong out-of-band blocker requirements (Fig 5). In this situation, the receiver must be able to provide a sufficiently low equivalent NF despite the additional unwanted power.

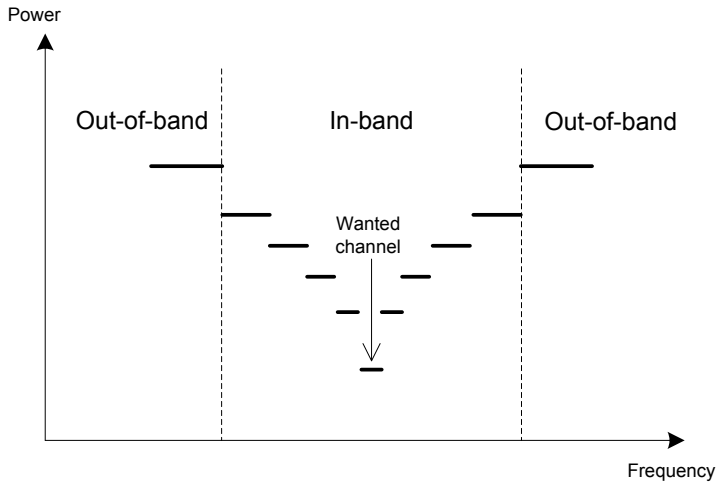


Fig 5. Example of adjacent & blocker test

This concern is exacerbated in the context of broad-band receivers with a limited amount of RF filtering.

2.1.5 Intermodulation & broadband non-linearity test

Third and higher-order mixing of the two interfering RF signals can produce an interfering signal in the band of the desired channel. Intermodulation is a measure of the capability of the receiver to receive a wanted signal on its assigned channel frequency in the presence of two interfering signals which have a specific frequency (Fig 6, left). In the context of broadband receivers, the receiver also has some constraints under a multiple channel input spectra (Fig 6, right). In an extreme case of fully occupied spectrum with similar-amplitude channels, the non-linearity power density tends to be white.

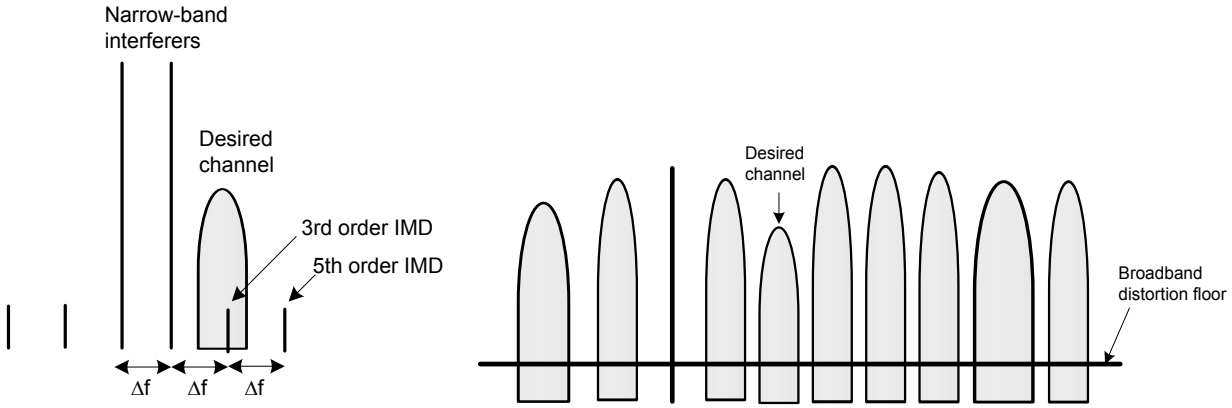


Fig 6. Intermodulation test (left), broadband non-linearity test (right)

2.1.6 Summary

This section shows the main signal characteristic that are relevant for the receiver:

- Signal distributions (PDF, CCDF)
- Minimum Signal-to-Noise ratio which is required at the baseband demodulator input.

The principal tests that are applied to a broadband receiver have been reviewed:

- Sensitivity
- Blocker and adjacent test
- Intermodulation test
- Broadband multiple-channel test

2.2 Receiver system-level design

2.2.1 Equivalent noise figure

A maximum equivalent noise figure (Fig 7) required to be handled by the full receiver is determined in this section. This figure of merit does not only include thermal noise, but all impairments added in the receiver, and is very useful for doing a 1st order assessment of the receiver design challenge.

In these calculations, we assume that the receiver input impedance is ideally matched to the source impedance (Rin=Rs).

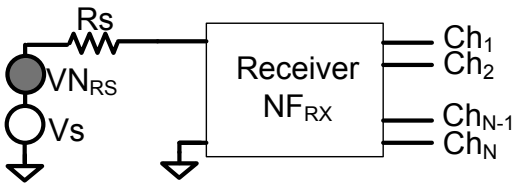


Fig 7. Full receiver and its equivalent Noise Figure

In most communication systems, the non-ideal communication channel already limits the receiver input signal quality. This is typically modeled by an additive noise at the receiver input (SNRin).

The noise generated in the source resistance is also included here in this input SNR (SNR_{in}), but not in the receiver signal-to-noise (SNR_{RX}). The SNR requirement on the receiver alone can be expressed as a function of the input SNR limitation and the output SNR (SNR_{out}) dictated by BER specification:

$$SNR_{RX}\,\min = -10\cdot\log_{10}\left(10^{-SNRout/10} - 10^{-SNRin/10}\right) \tag{2.1.}$$

Assuming an ideal input impedance matching, the input-referred noise voltage added by the receiver, and integrated over the noise bandwidth is:

$$Vn_{RX} = \sqrt{4\cdot K\cdot T\cdot Rs\cdot NBW\cdot\left(F_{RX}-1\right)}\cdot\frac{Rin}{Rs+Rin} = \sqrt{K\cdot T\cdot Rs\cdot NBW\cdot\left(F_{RX}-1\right)} \tag{2.2.}$$

Where F_{RX} is the receiver noise factor (linear scale), and NBW is the equivalent noise bandwidth.

The input-referred receiver SNR can be expressed as:

$$snr_{RX} = \frac{RFinWant}{Vn_{Rx}} \tag{2.3.}$$

And in dBs:

$$SNR_{RX} = RFinWant_{dBmV} - 20 \cdot \log 10 \left(\sqrt{K \cdot T \cdot Rs \cdot NBW \cdot \left(10^{(NF_{RX})/10} - 1 \right)} \Big/ 1e-3 \right) \quad (2.4.)$$

The required receiver noise figure can thus be expressed as:

$$NF_{RX} = 10 \cdot \log_{10} \left(1 + \frac{1e-6 \cdot 10^{(RFinWant_{dBmV} - SNR_{RX})/10}}{K \cdot T \cdot Rs \cdot NBW} \right) \quad (2.5.)$$

The derivation of the equivalent noise figure is illustrated by a level diagram in Fig 8, where the input SNR limitation ($SNRin$) and the receiver output SNR ($SNRout$) are also shown for completeness:

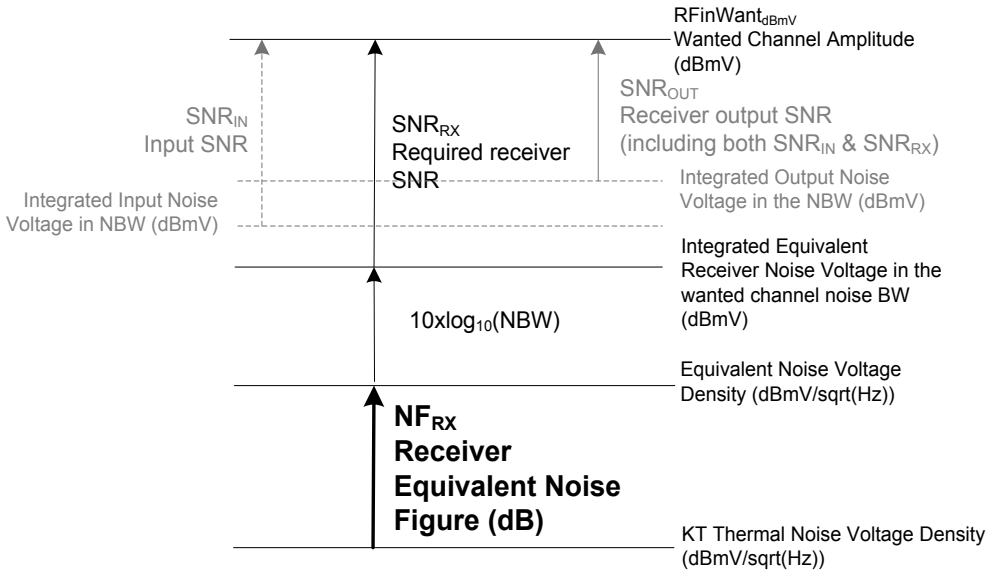


Fig 8. Required Equivalent Noise Figure level diagram

The minimum NF of the receiver can be computed in the case where the wanted channel amplitude is set to its minimum (sensitivity test).

In real-life, as a direct-RF receiver is essentially broad-band, it should not only provide the required NF in the presence of the low-level wanted channel, but also maintain a low NF despite the presence of strong unwanted channels.

2.2.2 Receiver implementation loss

Implementation loss (IL) characterizes the required loss of system performance due to impairments in the receiver.

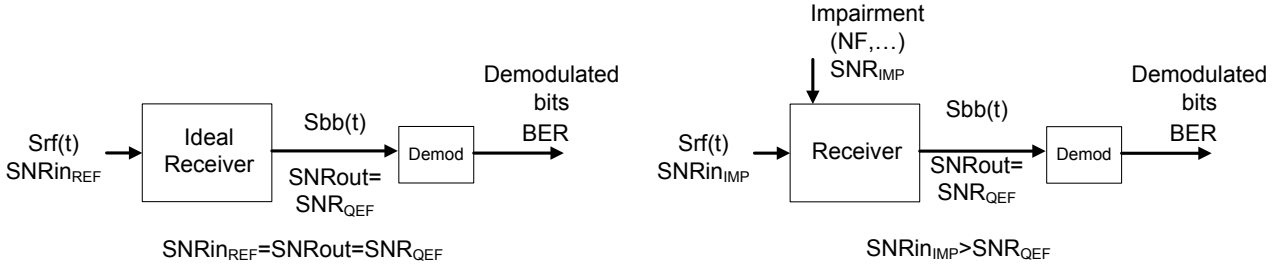


Fig 9. Receiver model for implementation loss characterization. Left: ideal receiver. Right: receiver with one impairment

In Fig 9, the left part shows an ideal receiver. In this case, the input SNR ($SNRin$) can be decreased down to $SNRin_{QEF}$, while still achieving a suitable BER.

On the right side of Fig 9, an impairment of the receiver is considered, and it already limits the SNR at the level of SNR_{IMP}. An increase of the input SNR ($SNRin_{IMP}$) is required in order for the system to still maintain a QEF reception.

In such a context, the implementation loss is defined as the required increase of input SNR, due to a non-ideality in the receiver:

$$IL_{IMP} = SNRin_{IMP} - SNRin_{REF} \tag{2.6.}$$

It can be expressed as:

$$IL_{IMP} = -10 \cdot \log_{10}\left(10^{-SNRin_{REF}/10} - 10^{-SNR_{IMP}/10}\right) - SNRin_{REF} \tag{2.7.}$$

Fig 10 illustrates that:

- 3dB IL is caused by an impairment whose SNR is 3dB above the minimum SNR for QEF reception.
- 0.5dB IL is caused by an impairment whose SNR is 10dB above the minimum SNR for QEF reception.
- 0.1dB IL is caused by an impairment whose SNR is 16.4dB above the minimum SNR for QEF reception.

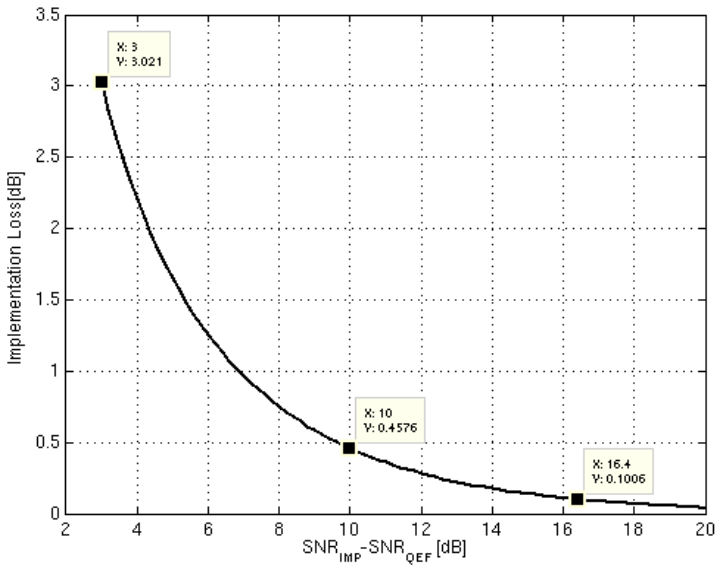


Fig 10. Implementation Loss against delta SNR

2.2.3 Noise analysis

2.2.3.1 Quantization noise

Since the quantization process (Fig 11) approximates a continuous-amplitude signal (x) to a discrete-amplitude signal (y), it introduces a quantization error. This error is, by definition:

$$e_q[n] = y[n] - x[n] \tag{2.8.}$$

$$-\Delta/2 \le e_q[n] \le \Delta/2 \tag{2.9.}$$

Where Δ is the step size of the quantizer.

The input signals, output signals and quantization errors are illustrated in Fig 11 , both in case of a ramp and sine wave input signals:

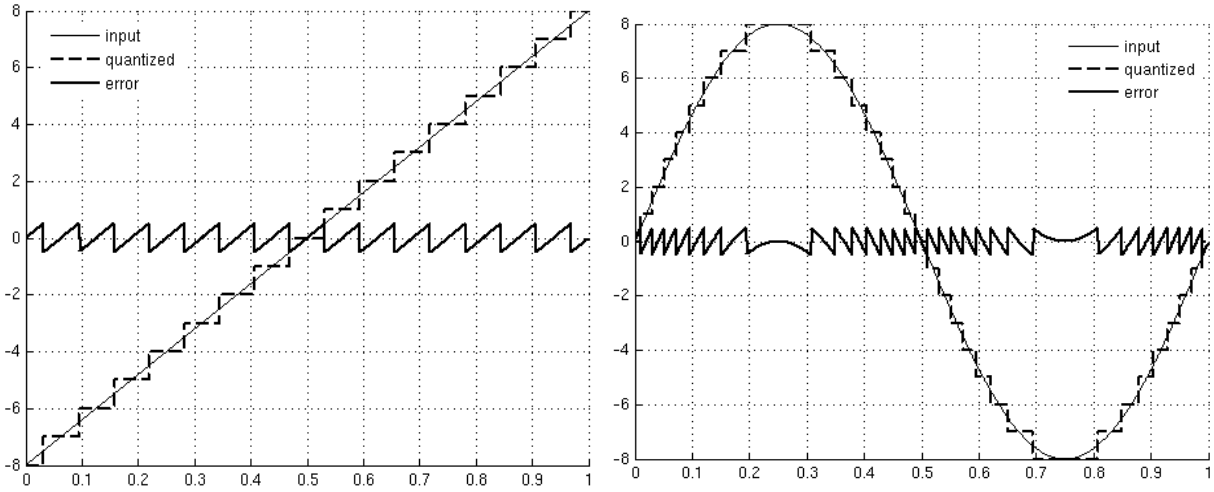


Fig 11. Quantization error with a ramp signal (left), and a sine wave signal (right)
Fig 12.

This quantization error can easily be calculated for a ramp input signal:

$$e_q = \frac{\Delta}{T} \cdot t \tag{2.10.}$$

The average power of this signal is its integral over one period:

$$\overline{e_q^{\,2}} = \frac{1}{T} \cdot \int_{-T/2}^{T/2} e_q^{\,2}(t) \cdot dt = \frac{\Delta^2}{12} \tag{2.11.}$$

A useful model of a quantizer is depicted in Fig 13:

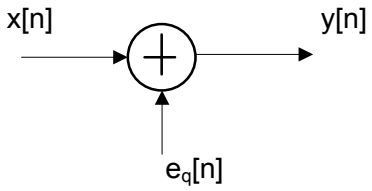


Fig 13. Additive noise model of a quantizer

The model is exact if e[n] is known. However, in most cases, e[n] is not known, because of input signal complexity, and a *statistical model* based on Fig 13 must be adopted. In such a case, the following properties are assumed for the quantization noise ([75]):

- Uniform distribution of amplitudes over one quantization interval. [76] determines the conditions under which the PDF of quantization noise is exactly uniform, and shows that this assumption is very accurate for Gaussian signals whose RMS amplitude are:

$$\sigma_{sig} \geq 0.7 \cdot \Delta \tag{2.12.}$$

The quantization error distribution is illustrated in Fig 14 for a Gaussian input signal: the PDF of quantization noise can be constructed by cutting the input signal PDF into strips, stacking and adding them, which results in a uniform distribution.

- Wide-sense-stationary process and white PSD
- No correlation with the input signal
- $\overline{e_q^{\,2}} = \frac{\Delta^2}{12}$

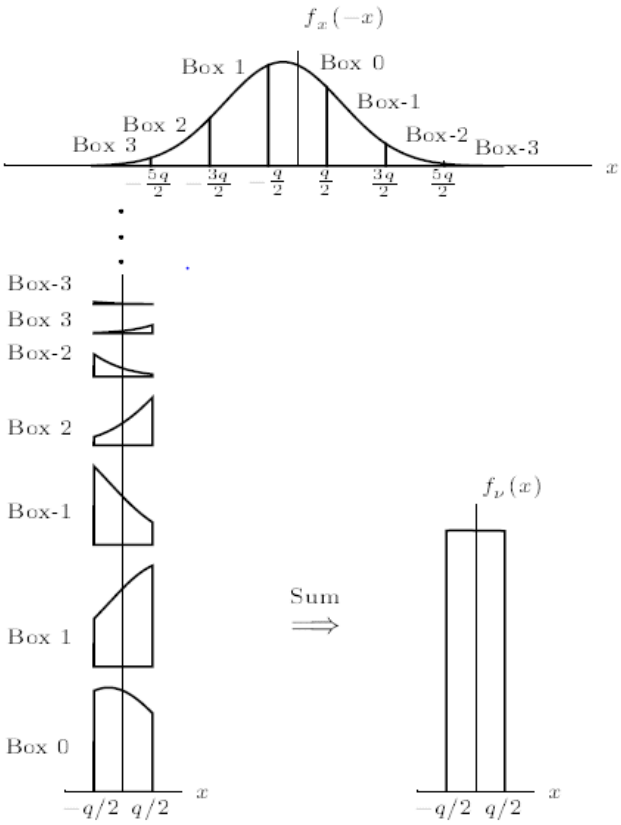


Fig 14. Construction of the PDF of quantization noise

In practice, these assumptions hold reasonably well under several conditions:

- The signal must hit a large number of quantization steps
- The signal must be "sufficiently active"
- The signal must be sufficiently small in order to avoid significant clipping

This is the case in direct-RF-sampling receivers for communication systems, as modulated RF signals are being processed, and gain control loops ensure a nearly full-scale signal at the ADC input, with low amount of clipping.

2.2.3.2 ADC Thermal noise

Thermal noise is often higher than quantization noise and limits the performance of ADCs. This noise is added during the process of sampling (KT/C noise), and during the analog process of quantization (pre-amplifiers noise,

comparators noise). This noise sources are Gaussian-distributed and have a white Power Spectral Density.

2.2.3.3 Over-sampling ratio

Fig 15 illustrates the acquisition of a communication system channel. The converter is said to be in an over-sampling situation if $fs/2 > BW$.

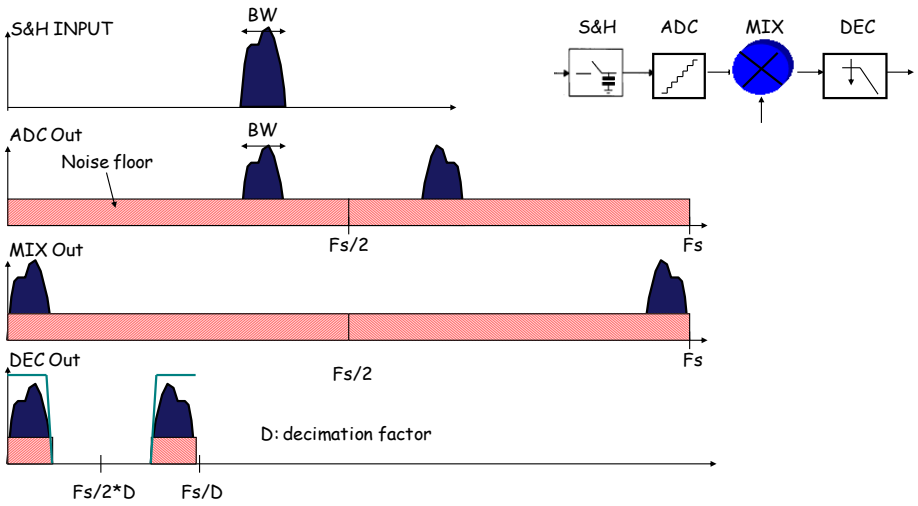


Fig 15. Over-Sampling Factor

In such a case, only a fraction of the total ADC noise lies below and corrupts the wanted channel. In a classical receiver, the digitized channel is then down-converted and selected.

The oversampling ratio (OSR) represents the SNR improvement, compared to the Nyquist-bandwidth SNR, resulting from the action of over-sampling a signal, and can be expressed as:

$$OSR = 10 \cdot \log_{10}\left(\frac{Fs}{2 \cdot BW}\right) \tag{2.13.}$$

In case of a direct-RF-sampling receiver with channel BW of 0.5 MHz, and ADC sampling rate of 1 GHz, the over-sampling factor provides a SNR improvement of 30 dB.

2.2.3.4 ADC clipping noise and optimum loading factor

The ADC will not only add thermal and quantization noises, but also hard-limiting clipping noise if it is driven too close to its full-scale. This section shows the impact of clipping, and provides guidance for choosing the optimum loading factor.

The loading factor ([81]) defines how close an ADC is driven from its full-scale, and is the ratio between the peak voltage of a full-scale sine wave, and the RMS of the composite input signal (σ).

$$LF = 20 \cdot \log_{10}\left(\frac{\sigma}{FS/2}\right) \tag{2.14.}$$

Fig 16 shows the quantization error within both the normal quantization region and the clipping region:

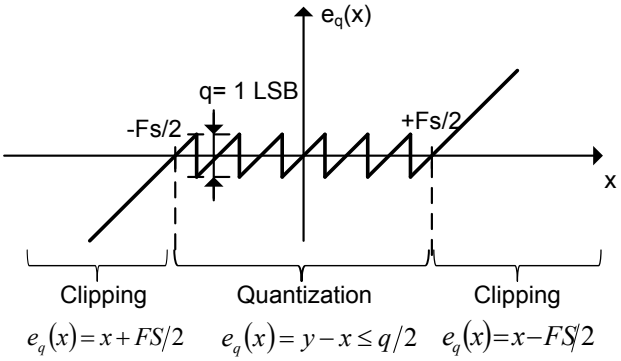


Fig 16. Ideal quantizer errors

The quantization error power can be written as:

$$Nq = \frac{q^2}{12} = \frac{\left(FS/2^N\right)^2}{12} = \frac{FS^2}{3 \cdot 2^{2 \cdot N+2}} \tag{2.15.}$$

The clipping error power is by definition:

$$Nc = \int_{-\infty}^{+\infty} e^2(x) \cdot P(x) \cdot dx \tag{2.16.}$$

With:

$$e(x) = x - FS/2 \tag{2.17.}$$

for $x > Fs/2$,

Assuming an input signal with a normal distribution, its probability density function is:

$$P(x) = \frac{1}{\sigma\sqrt{2\pi}} \cdot e^{-x^2/2\sigma^2} \tag{2.18.}$$

Then,

$$Nc = \frac{1}{\sigma\sqrt{2\pi}} \int_{FS/2}^{+\infty} (x - FS/2)^2 \cdot e^{-x^2/2\sigma^2} \cdot dx \tag{2.19.}$$

As demonstrated in [81], this can be expressed as:

$$Nc = 2\sigma^2\left(k^2+1\right)\left(1 - \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{k} e^{-t^2/2} \cdot dt\right) - k\sigma^2\sqrt{\frac{2}{\pi}} e^{-k^2/2} \tag{2.20.}$$

Where the remaining integral can be expressed as a function of the *erf* function:

$$\frac{1}{\sqrt{2\pi}}\int_{-\infty}^{k} e^{-t^2/2}\cdot dt = \frac{1}{2}\cdot\left(1+erf\left(\frac{k}{\sqrt{2}}\right)\right) \tag{2.21.}$$

The *erf* itself can easily be numerically evaluated with classical simulation tools.

Then, the total noise power Nt is:

$$Nt = Nq + Nc \tag{2.22.}$$

Noise Power Ratio (NPR, [81], [82]) is a metric used for evaluating the wideband performance of data converters, typically in Frequency Division Multiplexed (FDM) communication systems. It allows reflecting the true SNDR that the converter can deliver, including the effects of quantization, clipping noise, non-linear distortion and clock jitter.

In the present situation, it allows evaluating the combination of quantization noise and clipping noise for a wideband Gaussian signal, and is defined as:

$$NPR = 10\cdot\log_{10}\left(\frac{\sigma^2}{Nt}\right) \tag{2.23.}$$

NPR can be plotted as a function of the loading factor, for various ADC resolutions, and assuming an input signal which occupies the full Nyquist band [DC; Fs/2]:

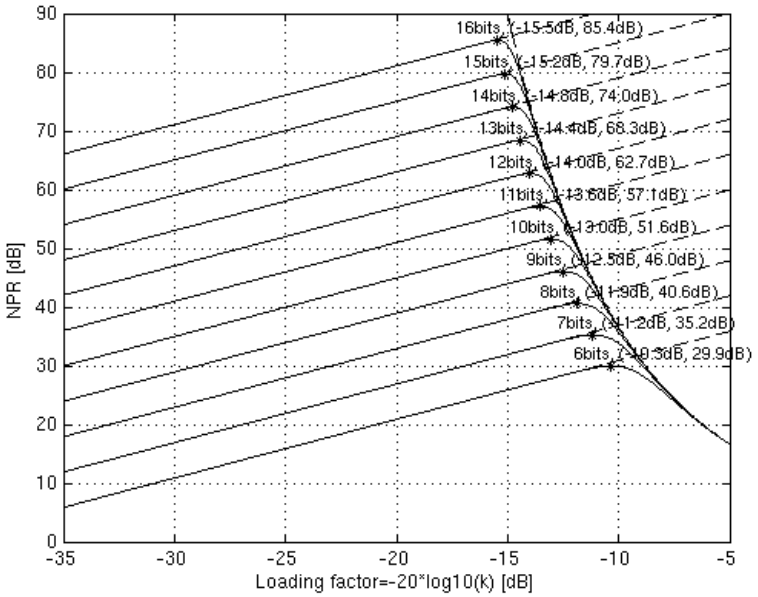


Fig 17. Noise Power Ratio & optimum loading factor for different ADC resolutions (Gaussian signal)

From low to the optimum loading factors, the system is limited by quantization/thermal noise. In this case, the sensitivity of NPR to loading factor is quite low (1 dB NPR loss for 1 dB signal reduction)

On the other hand, from the optimum to higher loading factors, the system is limited by clipping noise. In such a situation, NPR is highly sensitive to loading factor.

Given this high sensitivity, it is generally required for the ADC to be driven slightly below the optimum loading factor. The design of the front-end Automatic Control Loop (AGC) can be critical, depending on the dynamics of the communication channel and the potential RF interferers.

It is worth noting that the optimum loading factor depends on the ADC resolution. Indeed, in order to provide an

optimum total noise performance, the clipping noise must be scaled at the level of the quantization noise, which directly depends on the ADC resolution.

A high resolution ADC has a small quantization error: the clipping noise by itself must be low in order not to dominate the total noise level. On the other hand, a low resolution ADC has a relatively big quantization error: the clipping noise can be quite high, while still being below the thermal noise.

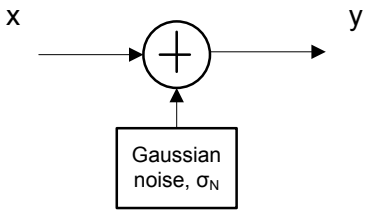
2.2.3.1 Impact of signal-dependent noise

Noise floor of practical Nyquist ADCs is typically higher at large signal compared to small-signal. This degradation of performance near the ADC full-scale can be due to:

- Increase of thermal noise, caused, for instance, by a degraded rejection of the noise generated in current sources used in differential structures
- High-order non-linear distortion

If this degradation is neglected, and the ADC noise performance (SNR) is specified at lower loading factors, impact on system performance is unknown. Alternatively, the ADC performance can be over-specified at full-scale, in order to have safe margin on system performance. As ADCs are the bottleneck in direct RF digitization receivers, neither of the two approaches is satisfactory. We are therefore seeking for an analytical method to determine the impact of ADC noise degradation at large signals.

The proposed approach is to model this phenomenon by a Gaussian noise, whose amplitude is signal-dependent. The proposed model is illustrated in Fig 18:



$$\sigma_N(x)=f(x)$$

Fig 18. Model for signal-dependent noise amplitude

The signal dependence can be modelled by a polynomial fit. Therefore, the Gaussian noise RMS amplitude can be expressed as a function of the input signal amplitude:

$$\sigma_N(x)=\sum_{k=1}^{L}\alpha_k\cdot x^k \tag{2.24.}$$

The average noise RMS amplitude is, by definition:

$$\overline{\sigma_N}^2=\int_{-FS/2}^{FS/2}\sigma_N{}^2(x)\cdot P(x)\cdot dx \tag{2.25.}$$

Where P(x) is the input signal PDF.

The integral can be numerically calculated for various signal distributions. The ADC SNR can then be calculated as a function of the average noise RMS amplitude and the input signal RMS amplitude:

$$SNR = 20 \cdot \log_{10}\left(\frac{\sigma_{IN}}{\sigma_N}\right) \tag{2.26.}$$

Data converters are commonly simulated and measured with a sine wave input test signal, which PDF can be expressed as:

$$P(x) = \frac{1}{\pi \cdot \sqrt{A^2 - x^2}}, -A < x < A \tag{2.27.}$$

Where A is the sine wave peak voltage.

In such a case, the average noise RMS amplitude can be expressed as:

$$\overline{\sigma_N}^2 = \int_{-FS/2}^{FS/2} \left(\sum_{k=1}^{L} \alpha_k \cdot x^k\right)^2 \cdot \frac{1}{\pi \cdot \sqrt{A^2 - x^2}} \cdot dx \tag{2.28.}$$

As motivated in 2.1.1.1, while sine waves are a typical lab signal, real-life signals are more likely to follow a Gaussian distribution, which PDF is:

$$P(x) = \frac{1}{\sigma_{IN}\sqrt{2\pi}} \cdot e^{-x^2/2\sigma_{IN}^2} \tag{2.29.}$$

Where σ_{IN} is the input signal RMS amplitude.

In this situation, the average noise RMS amplitude can be expressed as:

$$\overline{\sigma_N}^2 = \frac{1}{\sigma_{IN}\sqrt{2\pi}} \int_{-FS/2}^{FS/2} \left(\sum_{k=1}^{L} \alpha_k \cdot x^k\right)^2 \cdot e^{-x^2/2\sigma_{IN}^2} \cdot dx \tag{2.30.}$$

Fig 19 and Fig 20 illustrate the performance of an ADC having a degraded noise floor at high signal levels, both for a sine wave and Gaussian input signals. The assumed noise degradation follows a square law:

$$\sigma_N(x) = \alpha_0 + \alpha_2 \cdot x^2 \tag{2.31.}$$

For illustrating the impact of the noise degradation on ADC performance, signal-dependent noise amplitude is plotted against signal amplitude in Fig 19 (right y-axis), for several noise floor degradations.

Comparing both signal distributions, it is already clear on Fig 19 (left y-axis), that because of the low probability at high signal amplitudes, a Gaussian signal should be less sensitive to signal-dependent noise than a sine wave input signal.

In Fig 20, the proposed theory is used for calculating the theoretical ADC output SNR, for both input signal PDFs.

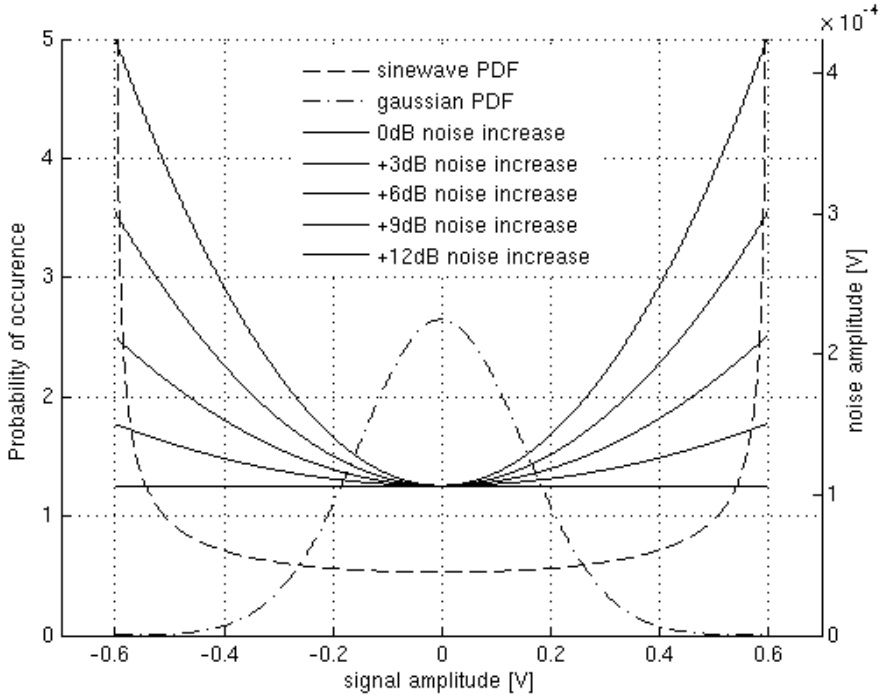


Fig 19. Input signal Probability Density Function (sine wave, Gaussian), and signal-dependent noise amplitude

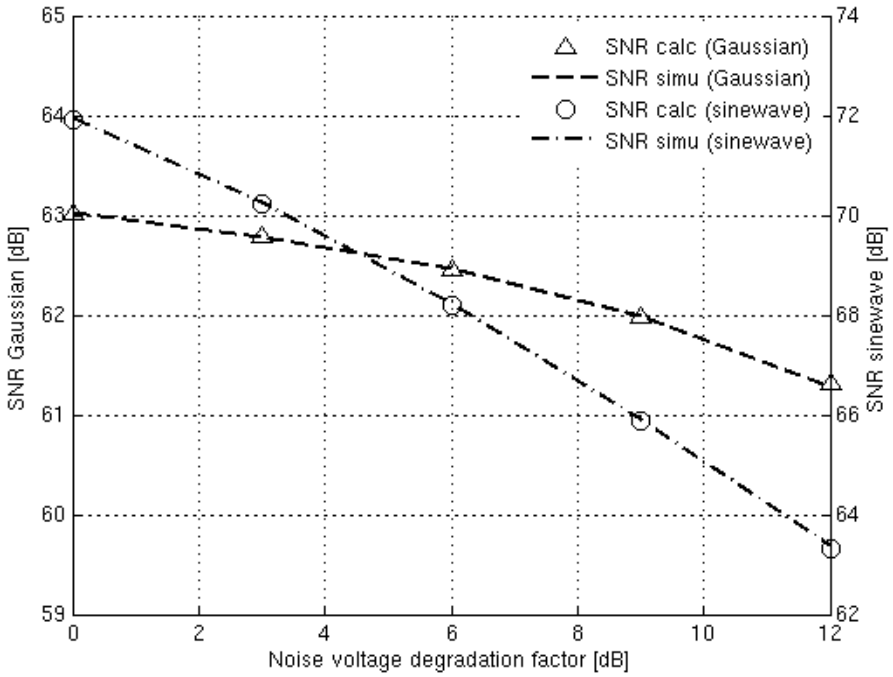


Fig 20. Calculated & simulated Signal-to-Noise versus large-signal noise degradation (left: sine wave; right: Gaussian)

Clearly, the noise floor degradation for large input signals much less impacts Gaussian signals than sine waves. Indeed for 12-dB noise floor degradation at full-scale, assuming a second-order dependency, the ADC performance for a Gaussian signal is only degraded by 1.7 dB with -12-dB loading factor (LF). In comparison, the SNR of the sine wave is degraded by 8.6 dB.

Therefore, for systems in which Gaussian signals are processed, design effort should be put on reducing small-signal

noise, while the allowable noise degradation for high-level signals can easily be evaluated using the developed theory.

This analysis can well be adapted to various input signal distributions and noise degradation profiles, depending on the application context. In addition, the analysis and its conclusions are also valid for RF and IF analog blocks.

2.2.3.2 ADC Noise Figure

Calculating the ADC noise figure is useful for system-level design. As for RF circuits, the noise factor of an ADC, F, is simply defined as the ratio of the total effective input noise power of the ADC to the amount of that noise power caused by the source resistance alone [83]. NF can be derived from the ADC full-scale voltage, input impedance, SNR (dBFS) & clock frequency parameters.

The SNR used in the formula should be extrapolated from simulations/measurements carried out at the optimum application-specific ADC loading factor, rather than with a classical full-scale sine wave test signal.

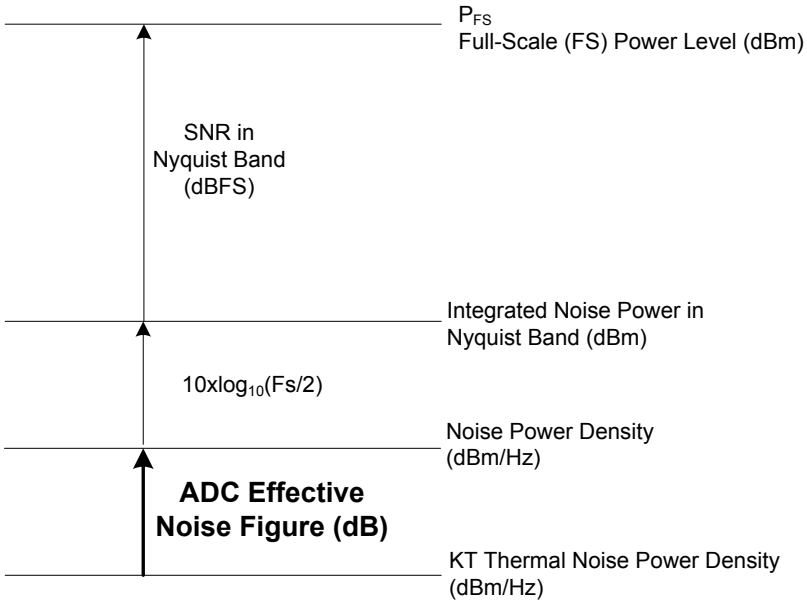


Fig 21. ADC noise figure calculation

$$NF = P_{FS(dBm)} - SNR_{(dBFS)} - 10 \cdot \log 10(Fs/2) - (K \cdot T)_{dBm/Hz} \quad (2.32.)$$

Therefore:

- Improving an ADC SNR by 6 dB results in a 6-dB NF improvement
- Increasing an ADC sampling rate by a factor 2 (without degrading the SNR) results in a 3-dB NF improvement

Fig 22 illustrates the ADC Noise Figure as a function of ADC SNR and sampling rate, for a 100Ω input impedance:

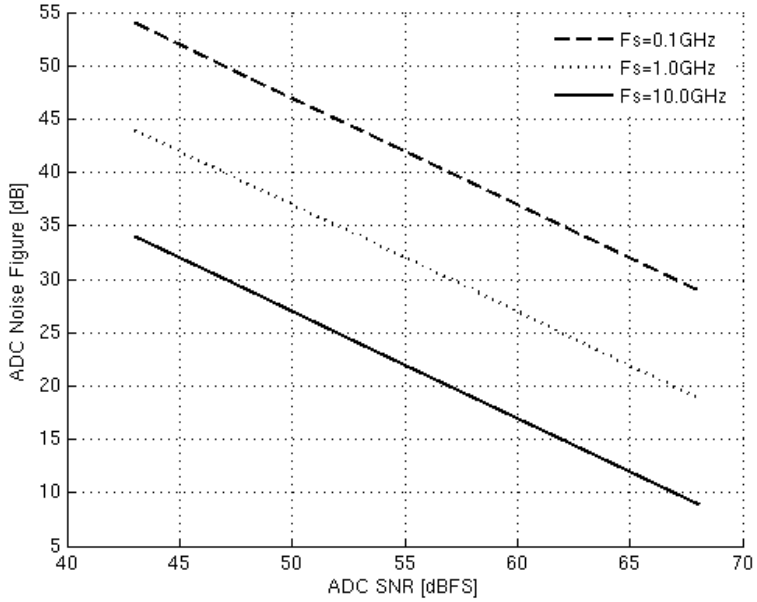


Fig 22. ADC noise figure for different SNR and sampling rates

2.2.3.3 RFFE gain range

The receiver requires an RF front-end (RFFE) for providing the adequate gain to the input signal prior to the noisy analog-to-digital conversion.

The RF front-end loaded voltage gain is defined as:

$$Gv_{RFFE} = RFout_{dBmV} / RFin_{dBmV} \tag{2.33.}$$

Where $RFout$ is the RF front-end output signal, and the ADC input signal. As detailed in 2.2.3.4, the RF front-end should load the ADC to its optimum loading factor in order to maximize the use of the ADC dynamic range.

In such a situation, RFFE gain can be written:

$$Gv_{RFFE} = \left(FS\_ADC_{dBmV} - LF_{dB}\right) - RFin_{dBmV} \tag{2.34.}$$

Where

$$FS\_ADC_{dBmV} = 20 \cdot \log_{10}\left(FS\_ADC/2 \cdot 1e-3\right) \tag{2.35.}$$

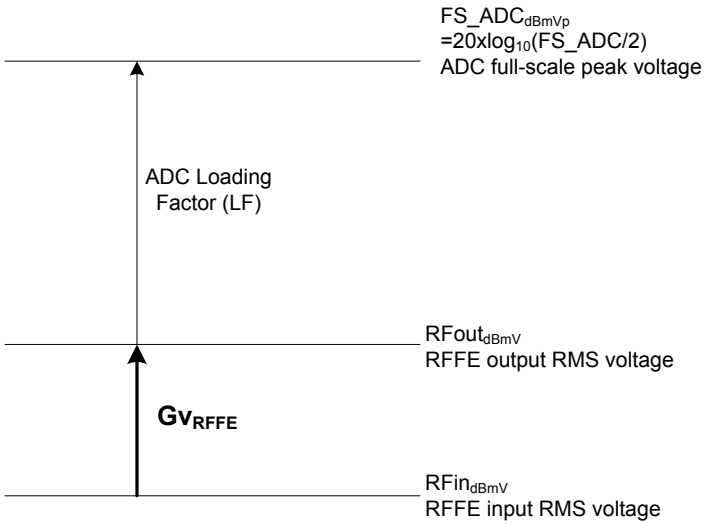


Fig 23. Level Diagram

2.2.3.4 Cascaded Noise & impact of RFFE gain flatness

The cascaded noise figure of the full receiver is influenced by the individual gains and noise floors. The cascaded noise factor ([83]) can be expressed as:

$$F_{RX}(f) = F_{RFFE}(f) + \frac{F_{ADC\_DSP}(f) - 1}{Gp_{RFFE}(f)} \tag{2.36.}$$

Where F_{RFFE} is the RFFE noise factor, Gp_{RFFE} is the RFFE power gain, and F_{ADC_DSP} is the noise factor of the A/D converter and digital channel selection.

It is clear that an optimum RFFE has a low noise figure and a high gain for reducing the impact of the ADC noise.

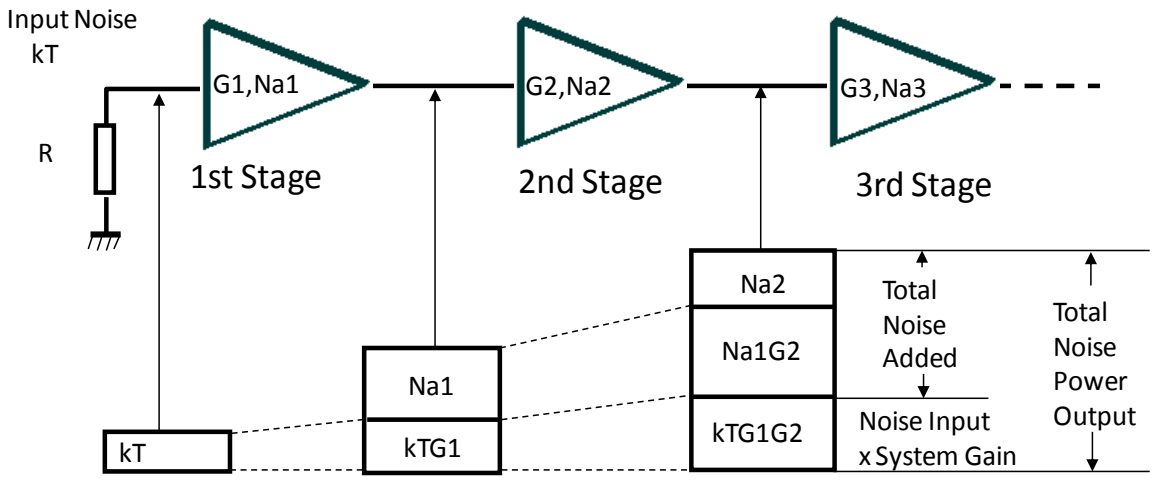


Fig 24. Friis formula

ADC/DSP noise factor can be expressed as a function of the full receiver noise factor, the RFFE noise factor and power gain:

$$F_{ADC\_DSP}(f) = 1 + (F_{RX}(f) - F_{RFFE}(f)) \cdot Gp_{RFFE}(f) \tag{2.37.}$$

Or

$$F_{RFFE}(f) = F_{RX}(f) - \frac{F_{ADC\_DSP}(f) - 1}{Gp_{RFFE}(f)} \tag{2.38.}$$

To illustrate the possible design trade-offs, Fig 25 shows the receiver NF for two different input test conditions:

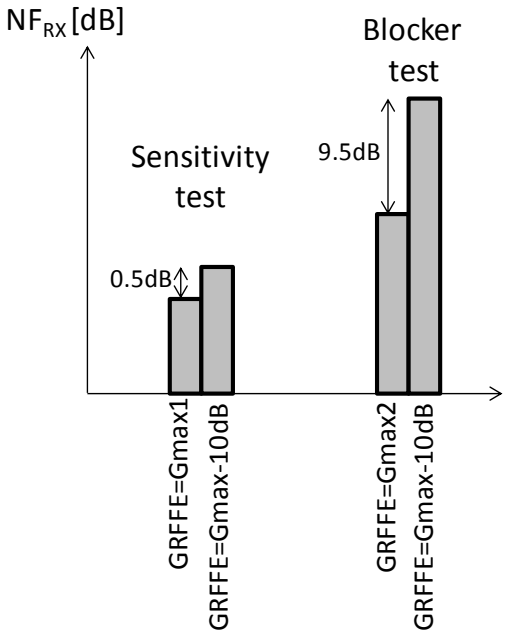


Fig 25. Cascaded Receiver NF, for sensitivity test and blocker test, for different RFFE gains

Sensitivity test: a low-amplitude single channel is provided to the receiver. The RFFE is at a very high gain, thus largely dominates the receiver noise figure. Therefore, decreasing the RFFE gain only has a minor impact on the receiver NF. It is not required in this situation that the RFFE drives the ADC to its full-scale. Minimizing the maximum gain of LNAs reduces stability and non-linear distortion issues usually encountered with the design of very high gain LNAs.

Blocker test: a high-amplitude blocker desensitizes the receiver while it also processes a medium amplitude wanted channel. In this case, RFFE gain is medium to low, thus ADC NF largely dominates the receiver NF. Therefore, RFFE gain reduction strongly impacts the receiver NF (1 dB NF increase per dB gain reduction in the worst case). It is therefore crucial in such a case to drive the ADC to its optimum loading factor.

It is also very clear, from the analysis above, that any frequency-dependence on the RFFE NF, gain or ADC NF adversely impacts the full-receiver NF. For instance, for input signal levels under which the ADC NF is the major noise limitations (high-level signals), a typical 1st order lowpass RFFE frequency response increases the receiver NF with a high-pass frequency response (Fig 26):

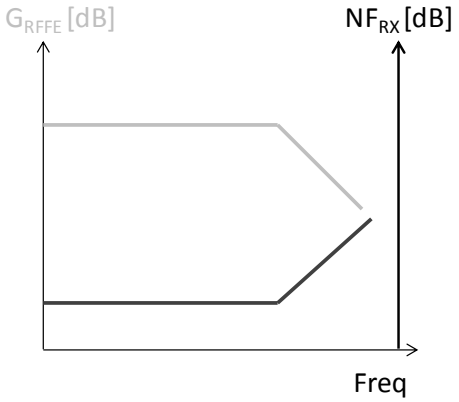


Fig 26. Cascaded Receiver NF, with lowpass RFFE gain, for ADC dominating the RX noise

2.2.3.5 Summary

ADC thermal noise, quantization noise, clipping noise, noise figure, and optimum ADC loading factor have been reviewed.

The performance degradation caused by large-signal signal-dependent noise of an ADC has been developed for sine wave and Gaussian signals. It has been demonstrated that important degradation of ADC noise floor at large input signals have a low impact on system performance, when Gaussian signals are being processed.

The impact of ADC noise, RFFE frequency-dependent gain & NF were studied in the context of the receiver cascaded noise figure.

2.2.4 Non-linear distortion

Fig 27 shows the receiver model used for assessing the impact of the sampling strategy on the main receiver blocks:

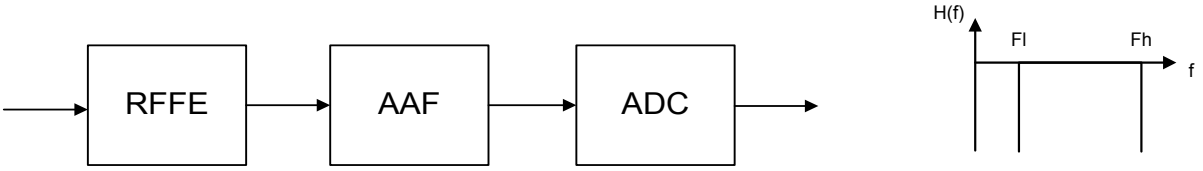


Fig 27. Simplified receiver model for non-linear distortion (left), AAF transfer function (right)

An ideal AAF is assumed, having a unity gain across the received Nyquist zone, and a zero gain in the other Nyquist zones:

$$H(f)=1,\ F_L<f<F_H$$

$$H(f)=0,\ f<F_L,\ f<F_H$$

$$F_L=(n-1)\cdot Fs/2,\ F_H=n\cdot Fs/2,$$

n: Nyquist zone index

Assuming a memory-less system, and using a Taylor series development, both RFFE and ADC non-linearities can be modeled as:

$$y(t)=\sum_{k=0}^{\infty}\alpha_k\cdot x^k(t) \tag{2.39.}$$

Limiting the analysis to 2nd and 3rd order non-linear distortion:

$$y = \alpha_1 \cdot x + \alpha_2 \cdot x^2 + \alpha_3 \cdot x^3 \tag{2.40.}$$

2.2.4.1 Non-linear distortion in a narrowband system

In narrowband wireless system reception, the input signal level to the antenna is generally dominated by one or few "blockers". A typical challenging condition is the test with 2 interferers depicted in Fig 28 (left):

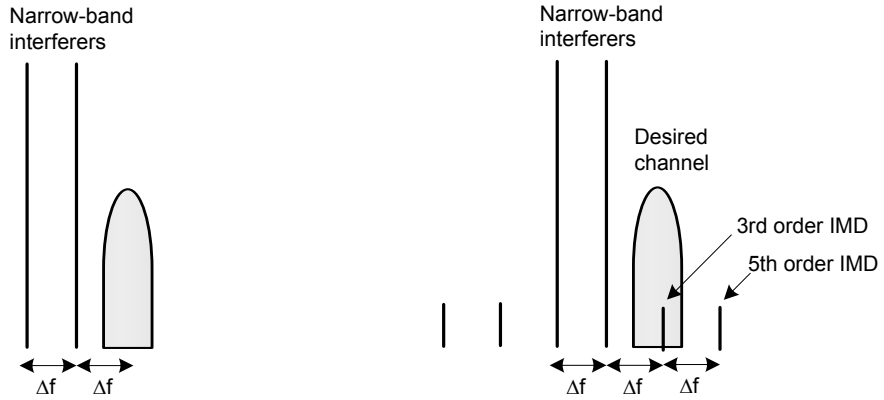


Fig 28. Third-order Intermodulation test – Input signal (left), RF Sampling ADC output signal (right)

The front-end output signal also contains odd and even intermodulation products. In the context of a narrowband wireless system reception, the nearby 3rd order intermodulation products (Fig 28) pose severe constraints on the RF & analog front-end design.

The resulting 3rd order intermodulation tone amplitude can be calculated. For this purpose, the power of the modulated channel in Fig 28 is temporarily neglected, and the Taylor series is limited to the 3rd order:

$$y(t) = \alpha_1 \cdot x(t) + \alpha_2 \cdot x^2(t) + \alpha_3 \cdot x^3(t) \tag{2.41.}$$

$$\begin{aligned} y(t) = & \left[\alpha_1 \cdot A_1 + \frac{3}{4} \cdot \alpha_3 \cdot A_1^{\,3} + \frac{3}{4} \cdot \alpha_3 \cdot A_1 \cdot A_2^{\,2} \right] \cdot \cos(w_1 \cdot t) \\ & + \left[\alpha_1 \cdot A_2 + \frac{3}{4} \cdot \alpha_3 \cdot A_2^{\,3} + \frac{3}{4} \cdot \alpha_3 \cdot A_2 \cdot A_1^{\,2} \right] \cdot \cos(w_2 \cdot t) \\ & + \alpha_2 \cdot A_1 \cdot A_2 \cdot \left[\cos((w_1 + w_2) \cdot t) + \cos((w_1 - w_2) \cdot t) \right] \\ & + \frac{3 \cdot \alpha_3 \cdot A_1^{\,2} \cdot A_2}{4} \left[\cos((2 \cdot w_1 + w_2) \cdot t) + \cos((2 \cdot w_1 - w_2) \cdot t) \right] \\ & + \frac{3 \cdot \alpha_3 \cdot A_2^{\,2} \cdot A_1}{4} \left[\cos((2 \cdot w_2 + w_1) \cdot t) + \cos((2 \cdot w_2 - w_1) \cdot t) \right] \end{aligned} \tag{2.42.}$$

Assuming that the two adjacent channels have equal amplitude (A), the 3rd order intermodulation distance (IMD3) can be expressed as:

$$IMD3 = \frac{3 \cdot \alpha_3}{4 \cdot \alpha_1} \cdot A^2 \tag{2.43.}$$

The maximum value of the 3rd order polynomial coefficient can therefore be calculated depending on the application context. In case of a single-carrier modulation, with adjacent channels of equal amplitude:

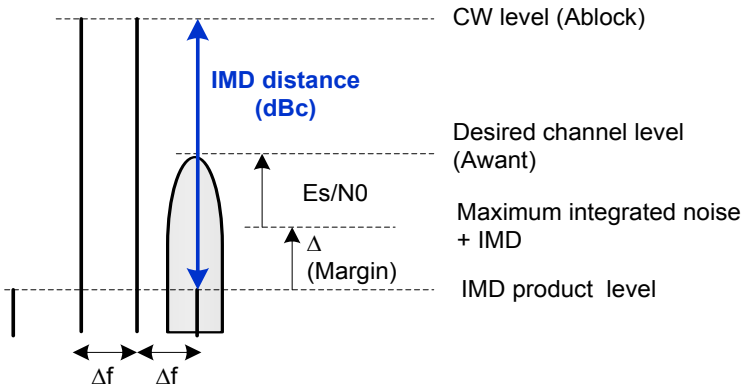


Fig 29. Third-order Intermodulation requirement

$$IMD3 \geq Ablock - (Awant + Es/N0 - \Delta) \tag{2.44.}$$

Which can alternatively be translated in a 3rd order intercept point (IP3):

$$A_{IP3} = \sqrt{\frac{4 \cdot \alpha_1}{3 \cdot \alpha_3}} \tag{2.45.}$$

In case of cascaded sub-blocks (several cascaded LNAs in the RFFE, ADC), the phase relation-ship between the intermodulation products added in each block has to be taken into account. This is difficult to predict before being in the full design process. In order to establish requirements prior to the design phase, the worst-case situation should be assumed, in which all intermodulation products are in-phase. This results into an addition of intermodulation products in voltage.

2.2.5 Non-linear distortion in a broadband system

In broadband receivers, the composite RF input signal may include many channels. These channels have pretty equal amplitudes in wired or wireless line-of-sight systems (cable, satellite), and quite different amplitudes in non-line-of sight wireless applications (cellular radios).

The next section introduces composite non-linear distortion, inspects the influence of lowpass and bandpass sampling on RFFE non-linear distortion, and establishes a link to more usual IP2/IP3 metrics.

2.2.5.1 Composite distortion products identification

Considering an input signal x(t) consisting of N continuous waves:

$$x(t) = \sum_{i=1}^{N} A_i \cdot \cos(w_i \cdot t + \varphi_i) \tag{2.46.}$$

$$y(t)=\alpha_1\cdot\left(\sum_{i=1}^{N}A_i\cdot\cos(w_i\cdot t+\varphi_i)\right)+\alpha_2\cdot\left(\sum_{i=1}^{N}A_i\cdot\cos(w_i\cdot t+\varphi_i)\right)^2+\alpha_3\cdot\left(\sum_{i=1}^{N}A_i\cdot\cos(w_i\cdot t+\varphi_i)\right)^3 \quad (2.47.)$$

After some trigonometric manipulation, y(t) can be expressed as:

$$y(t)=y_1(t)+y_2(t)+y_3(t) \quad (2.48.)$$

With,

$$y2(t)=\frac{\alpha_2}{2}+y2_{HD2}(t)+y2_{IMDp}(t)+y2_{IMD2m}(t) \quad (2.49.)$$

$$y3=y3_{HD3}+y3_{IMD3m}+y3_{IMD3p}+y3_{TBm}+y3_{TBp} \quad (2.50.)$$

Each term can be expressed as:

Fundamental:

$$y1(t)=\alpha_1\cdot\sum_{i=1}^{N}A_i\cdot\cos(w_i\cdot t+\varphi_i)+\frac{3\cdot\alpha_3}{2}\sum_{i=1}^{N}\sum_{j\neq i}\cdot\left(A_i\cdot A_j\cdot\cos(w_j\cdot t)+\varphi_j\right) \quad (2.51.)$$

2nd order harmonic distortion:

$$y2_{HD2}(t)=\frac{\alpha_2}{2}\cdot\sum_{i=1}^{N}A_i^2\cdot\cos(2\cdot w_i\cdot t+2\cdot\varphi_i) \quad (2.52.)$$

2nd order intermodulation (w_i+w_j):

$$y2_{IMD2p}(t)=\alpha_2\cdot\sum_{1\le i<j\le N}A_i\cdot A_j\cdot\cos(w_i\cdot t+w_j\cdot t+\varphi_i+\varphi_j) \quad (2.53.)$$

2nd order intermodulation (w_i-w_j):

$$y2_{IMD2m}(t)=\alpha_2\cdot\sum_{1\le i<j\le N}A_i\cdot A_j\cdot\cos(w_i\cdot t-w_j\cdot t+\varphi_i-\varphi_j) \quad (2.54.)$$

3rd order harmonic distortion:

$$y3_{HD3}(t)=\alpha_3\cdot\sum_{i=1}^{N}(A_i\cdot\cos(w_i\cdot t+\varphi_i))^3 \quad (2.55.)$$

3rd order intermodulation $(2\cdot w_i-w_j)$:

$$y3_{IMD3m}(t)=\frac{3\cdot\alpha_3}{4}\cdot\sum_{i=1}^{N}\sum_{j\neq i}A_i^2\cdot A_j\cdot\cos(2\cdot w_i\cdot t-w_j\cdot t+2\cdot\varphi_i-\varphi_j) \quad (2.56.)$$

3rd order intermodulation $\left(2 \cdot w_i + w_j\right)$:

$$y3_{IMD3p}(t) = \frac{3 \cdot \alpha_3}{4} \cdot \sum_{i=1}^{N} \sum_{j \neq i} A_i^{\,2} \cdot A_j \cdot \cos\left(2 \cdot w_i \cdot t + w_j \cdot t + 2 \cdot \varphi_i + \varphi_j\right) \tag{2.57.}$$

3rd order triple beat $\left(w_i - w_j + w_k\right)$:

$$y3_{TBmp}(t) = \frac{6 \cdot \alpha_3}{4} \cdot \sum_{1 \le i < j \le k < N} A_i \cdot A_j \cdot A_k \cos(w_i \cdot t - w_j \cdot t + w_k \cdot t + \varphi_i - \varphi_j + \varphi_k) \tag{2.58.}$$

3rd order triple beat $\left(w_i + w_j + w_k\right)$:

$$y3_{TBpp}(t) = \frac{6 \cdot \alpha_3}{4} \cdot \sum_{1 \le i < j \le k < N} A_i \cdot A_j \cdot A_k \cos(w_i \cdot t + w_j \cdot t + w_k \cdot t + \varphi_i + \varphi_j + \varphi_k) \tag{2.59.}$$

3rd order triple beat $\left(w_i - w_j - w_k\right)$:

$$y3_{TBmm}(t) = \frac{6 \cdot \alpha_3}{4} \cdot \sum_{1 \le i < j \le k < N} A_i \cdot A_j \cdot A_k \cos(w_i \cdot t - w_j \cdot t - w_k \cdot t + \varphi_i - \varphi_j - \varphi_k) \tag{2.60.}$$

3rd order triple beat $\left(w_i + w_j - w_k\right)$:

$$y3_{TBpm}(t) = \frac{6 \cdot \alpha_3}{4} \cdot \sum_{1 \le i < j \le k < N} A_i \cdot A_j \cdot A_k \cos(w_i \cdot t + w_j \cdot t - w_k \cdot t + \varphi_i + \varphi_j - \varphi_k) \tag{2.61.}$$

Because of the multiple tone combinations in each term derived above, and assuming a constant channel spacing, many intermodulation products fall on top of each other.

Indeed, the number of distortion beats per frequency can be computed. The result of this analysis agrees with reference [84].

Fig 30 shows the number of the different beats across frequency, prior to aliasing operation, for a lowpass sampling receiver, i.e. for input signal frequencies within the interval [0; Fs/2]:

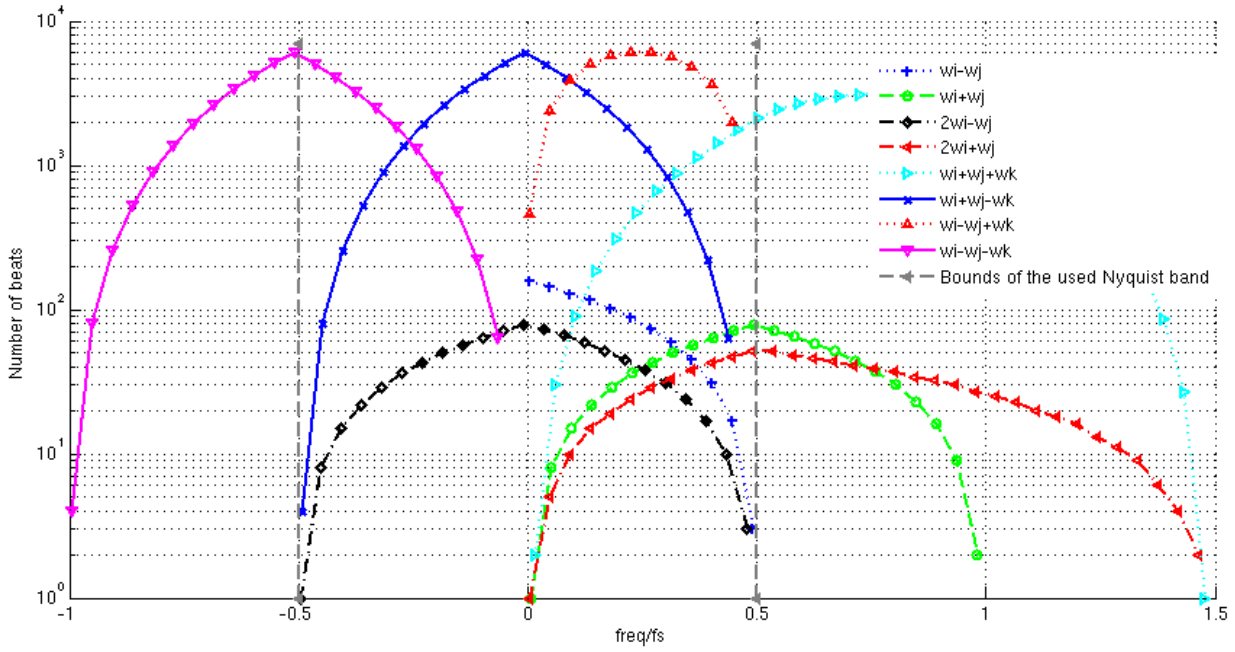


Fig 30. Number of beats across frequency, sampling in 1st Nyquist band, 158 tones equally distant tones

Non-linear distortion has several noticeable characteristics within the interval $[0; fs/2]$:

- 2nd order beats:
  - 2nd order harmonic distortion beats $(2 \cdot w_{i,j})$ are very few (N beats)
  - $(w_i - w_j)$ beats are dominant near DC
  - $(w_i + w_j)$ beats are dominant at the high side of the 1st Nyquist band
- 3rd order beats:
  - 3rd order harmonic distortion beats $(3 \cdot w_{i,j})$ are very few (N beats)
  - Triple beats $(w_i \pm w_j \pm w_k)$ are dominant

For both non-linear distortion orders, a large portion of the non-linear distortion falls within the Nyquist band of interest

Fig 31 shows the non-linear distortion beats for a bandpass 4th-Nyquist-band sampling strategy, i.e. for input signal frequencies in the interval $[3 \cdot fs/2; 4 \cdot fs/2]$:

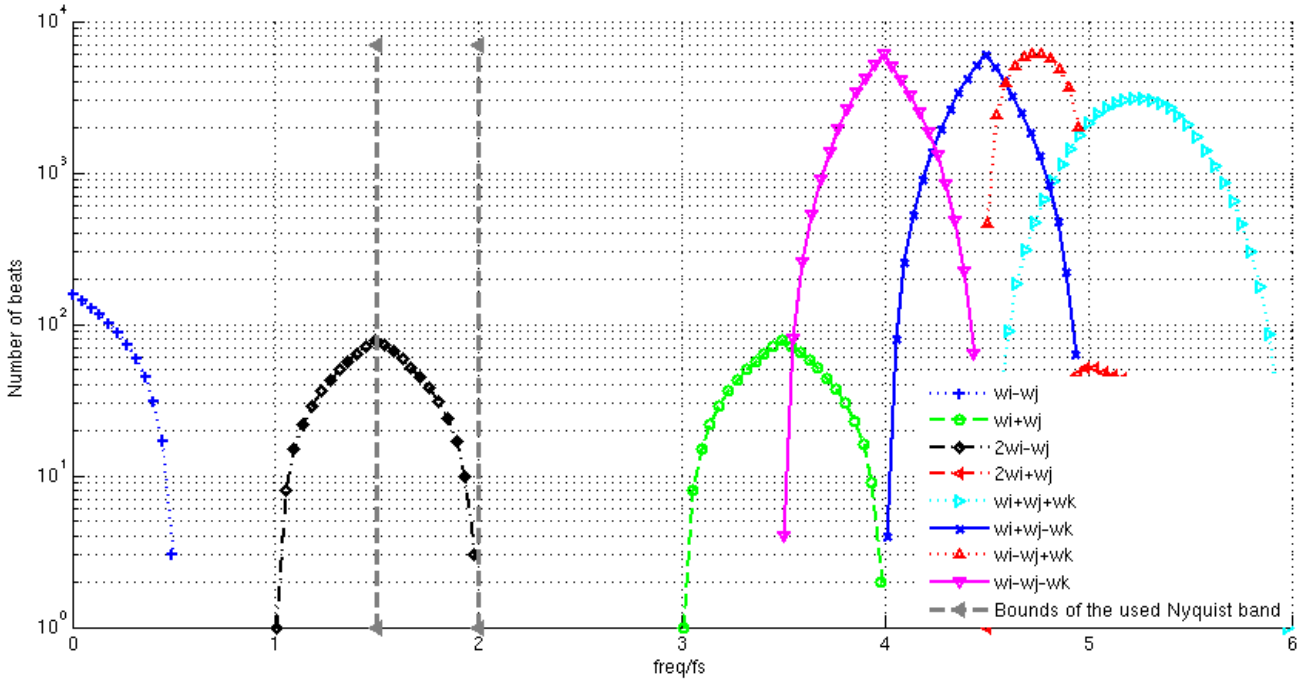


Fig 31. Number of beats across frequency, sampling in 4th Nyquist band, 158 equally distant tones

The sampled 4th-Nyquist-band is clearly much less impacted by the RFFE non-linear distortion than in the previous case of the 1st-Nyquist-band sampling (Fig 31):

- 2nd order beats:
  - 2nd order harmonic distortion beats $(2 \cdot w_{i,j})$ and intermodulation products $(w_i \pm w_j)$ fall out-of-band
- 3rd order:
  - Triple beats $(w_i \pm w_j \pm w_k)$ and $(2 \cdot w_i + w_j)$ intermodulation products also fall out-of-band
  - $(2 \cdot w_i - w_j)$ intermodulation products are the only beats that fall in-band

Fig 32 provides an overview of the sampling strategy impact on non-linear distortion, by reporting the RFFE out-of-band non-linearity that an AAF can potentially attenuate for the Nyquist zones from one to four:

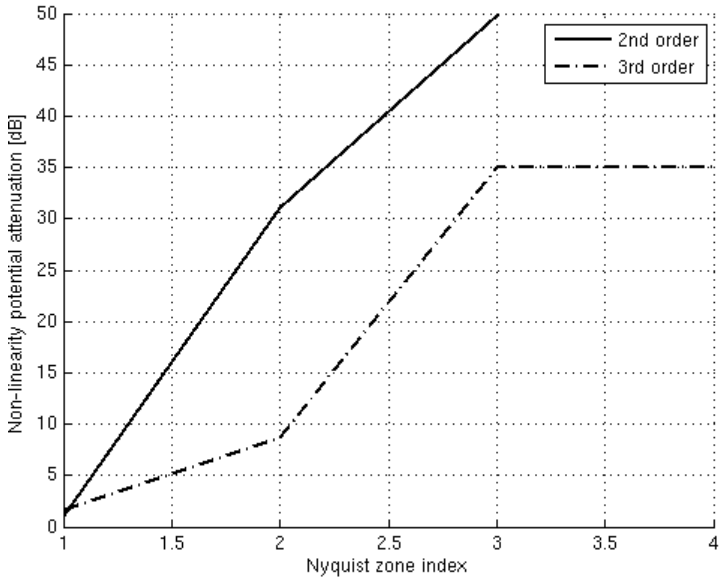


Fig 32. Non-linear distortion potential improvement factor, depending on the sampling strategy

While most of the RFFE distortion beats fall within the zone of interest with a lowpass sampling strategy (only 2dB attenuation of 2nd and 3rd order distortion), a bandpass sampling strategy allows the AAF to filter out some parts of the RFFE non-linear distortion products, quite independently of the received Nyquist zone, for Nyquist zones greater than two.

However, it should be kept in mind that:

- RFFE non-linear distortion won't practically be strictly limited to the order three, and will therefore exhibit a wider spectrum. Still, low-order harmonics typically dominate non-linear distortion.
- ADC non-linear distortion is aliased in-band independently of the sampling strategy,

2.2.5.2 Composite Triple Beat (CTB) link with 3rd order intercept point (IP3)

This section explicitly links CTB and IP3, in case of 1st Nyquist zone sampling. The same methodology can be used for doing so in any Nyquist zone.

Because of their high number, the dominant beats are $(w_i \pm w_j \pm w_k)$:

$$y3_{TBpp}(t) = \frac{6 \cdot \alpha_3}{4} \cdot \sum_{1 \le i < j \le k < N} A_i \cdot A_j \cdot A_k \cos(3 \cdot w_1 \cdot t + (i + j + k - 3) \cdot \Delta w \cdot t + \varphi_i + \varphi_j + \varphi_k) \tag{2.62.}$$

The developed result can be either analytically or numerically solved, depending on the input signal complexity.

An interesting outcome is the case of equal signal amplitudes.

In such a situation, each composite triple beat amplitude is:

$$A_{beat} = Ain^3 \cdot \frac{6 \cdot \alpha_3}{4} \tag{2.63.}$$

Each fundamental amplitude is:

$$A_{fund} = Ain \cdot \alpha_1 \tag{2.64.}$$

The ratio between individual beat amplitude and fundamental amplitude is:

$$ctb_{beat} = \frac{\frac{6 \cdot \alpha_3}{4} \cdot Ain^3}{\alpha_1 \cdot Ain} = \frac{6 \cdot \alpha_3}{4 \cdot \alpha_1} \cdot Ain^2 \quad (2.65.)$$

As the 3rd-order intercept point is:

$$ip3 = \sqrt{\frac{4 \cdot \alpha_1}{3 \cdot \alpha_3}} \quad (2.66.)$$

Each CTB beat can be expressed as:

$$ctb_{beat} = \frac{2 \cdot Ain^2}{ip3^2} \quad (2.67.)$$

Composite triple beat will be the addition of multiple beats. Considering random-phased CWs, beats will add in power (and not in voltage):

$$ctb = \frac{2 \cdot Ain^2 \cdot \sqrt{Nbeats}}{ip3^2} \quad (2.68.)$$

In a logarithmic scale:

$$CTB = 2 \cdot (Ain_{dBuV} - IP3_{dBuV}) + 20 \cdot \log_{10}(2) + 10 \cdot \log_{10}(Nbeats) \quad (2.69.)$$

With:

$$N_{beat} \leq \frac{N_{ch}^{\ 2}}{4} \quad (2.70.)$$

The RF front-end IP3 specification can be expressed as:

$$IP3_{dBuV} = \frac{1}{2} \cdot (2 \cdot Ain_{dBuV} + 20 \cdot \log_{10}(2) + 10 \cdot \log_{10}(Nbeats) - CTB) \quad (2.71.)$$

This result agrees with the result provided in reference [85].

2.2.5.3 Composite Second Order (CSO) link with 2nd order intercept point (IP2)

This section explicitly links CSO and IP2, in case of 1st Nyquist zone sampling. The same methodology can be used for doing so in any Nyquist zone. Because of their high number, the dominant beats are the $(w_i \pm w_j)$:

$$y2_{IMD2m}(t) = \alpha_2 \cdot \sum_{1 \leq i < j \leq N} A_i \cdot A_j \cdot \cos((i-j) \cdot \Delta w \cdot t + \varphi_i - \varphi_j) \quad (2.72.)$$

$$y2_{IMD2p}(t) = \alpha_2 \cdot \sum_{1 \leq i < j \leq N} A_i \cdot A_j \cdot \cos(2 \cdot w_1 \cdot t + (i+j-2) \cdot \Delta w \cdot t + \varphi_i + \varphi_j) \quad (2.73.)$$

If all amplitudes are equal, each CSO beat has an amplitude $= \alpha_2 \cdot Ain^2$. Each fundamental has amplitude of $\alpha_1 \cdot Ain$.

$$cso_{beat} = \frac{\alpha_2 \cdot Ain^2}{\alpha_1 \cdot Ain} = \frac{\alpha_2}{\alpha_1} \cdot Ain \tag{2.74.}$$

$$ip2 = \frac{\alpha_1}{\alpha_2} \tag{2.75.}$$

$$cso_{beat} = \frac{Ain}{ip2} \tag{2.76.}$$

As for CTB, composite second order beats will be the sum of multiple beats. Considering random-phased CWs, beats will add in power (and not in voltage).

$$cso = \frac{Ain \cdot \sqrt{Nbeats}}{ip2} \tag{2.77.}$$

In log domain:

$$CSO = (Ain_{dBuV} - IP2_{dBuV}) + 10 \cdot \log_{10}(Nbeats) \tag{2.78.}$$

With $Nbeats \leq N$.

This result agrees with reference [85].

The RF front-end IP2 specification can be expressed as:

$$IP2_{dBuV} = Ain_{dBuV} + 10 \cdot \log_{10}(Nbeats) - CSO \tag{2.79.}$$

This analysis allows specifying the required IP2/IP3 for reaching a targeted level of composite non-linear distortion (CSO/CTB) in case of a flat input signal consisting of continuous waves. However, the theory can be also be used with digitally-modulated channels. In such a case, the number of distortion beats will be strictly similar than with continuous waves. Instead of causing discrete beats, non-linear distortion will cause wideband beats, which will be perceived nearly as white noise by the baseband demodulator.

2.2.5.4 Impact of RFFE gain & phase unbalance

The RF front-end converts the single-ended RF input to a differential output RF signal. However, a practical RF front-end does not provide perfectly balanced outputs. As shown in [78], the main consequence is a non ideal cancellation of the 2nd order non-linear distortion of the TH. The analysis provided below links 2nd order non-linear distortion to the combined gain / phase balances.

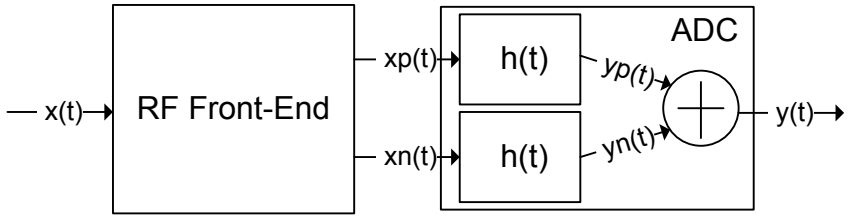


Fig 33. RF Front-End to Sample-And-Hold interface

$$x_{in}(t) = A_{in} \cdot \cos(w_{in} \cdot t + \varphi_{in}) \tag{2.80.}$$

$$x_p(t) = A_{in} \cdot k_p \cdot \cos(w_{in} \cdot t + \varphi_{in} + \Delta\varphi/2) \tag{2.81.}$$

$$x_n(t) = -A_{in} \cdot k_n \cdot \cos(w_{in} \cdot t + \varphi_{in} - \Delta\varphi/2) \tag{2.82.}$$

$$y_p(t) = h(x_p(t)) \tag{2.83.}$$

And:

$$y_n(t) = h(x_n(t)) \tag{2.84.}$$

With:

$$h(t) = a_0 + a_1 \cdot x(t) + a_2 \cdot x^2(t) + a_3 \cdot x^3(t) \tag{2.85.}$$

$$y_p(t) = a_0 + a_1 \cdot x_p(t) + a_2 \cdot x_p{}^2(t) + a_3 \cdot x_p{}^3(t) \tag{2.86.}$$

$$y_n(t) = a_0 + a_1 \cdot x_n(t) + a_2 \cdot x_n{}^2(t) + a_3 \cdot x_n{}^3(t) \tag{2.87.}$$

$$y(t) = a_1 \cdot [x_p(t) - x_n(t)] + a_2 \cdot [x_p{}^2(t) - x_n{}^2(t)] + a_3 \cdot [x_p{}^3(t) - x_n{}^3(t)] \tag{2.88.}$$

$$y(t) = y_1(t) + y_2(t) + y_3(t) \tag{2.89.}$$

After some manipulation, y1 can be written as:

$$y_1(t) = a_1 \cdot A_{in} \cdot \left[\sqrt{\left(\cos\left(\Delta\varphi / 2 \right) \cdot \left(k_p + k_n \right) \right)^2 + \left(\sin\left(\Delta\varphi / 2 \right) \cdot \left(k_p - k_n \right) \right)^2} \cdot \cos\left(w_{in} \cdot t + \varphi_{in} + \varphi_1 \right) \right. \tag{2.90.}$$

Where $\varphi 1$ depends on $\Delta\varphi$, k_p and k_n.

$y2$ can be expressed as:

$$y_2(t) = a_2 \cdot \frac{A_{in}^2}{2} \cdot \left[\left(k_p^{\,2} - k_n^{\,2} \right) + \sqrt{\left(\left(k_p^{\,2} - k_n^{\,2} \right) \cdot \cos(\Delta\varphi) \right)^2 + \left(\left(k_p^{\,2} + k_n^{\,2} \right) \cdot \sin(\Delta\varphi) \right)^2} \cos\left(2 \cdot w_{in} \cdot t + 2 \cdot \varphi_{in} + \varphi_2 \right) \right] \tag{2.91.}$$

Where φ_2 depends on $\Delta\varphi$, k_p and k_n ..

As a comparison, the 2nd order harmonic distortion of a single-ended structure is:

$$hd2_{single} = \frac{a_2 \cdot A_{in}}{2 \cdot a_1} \tag{2.92.}$$

The improvement factor of 2nd order non-linear-distortion (HD2, IMD2 or CSO) from a single-ended to a differential structure with non-ideal gain and phase balance can be written as:

$$\frac{hd2_{diff}}{hd2_{single}} = \sqrt{\frac{\left(\cos\left(\Delta\varphi / 2 \right) \cdot \left(k_p + k_n \right) \right)^2 + \left(\sin\left(\Delta\varphi / 2 \right) \cdot \left(k_p - k_n \right) \right)^2}{\left(\left(k_p^{\,2} - k_n^{\,2} \right) \cdot \cos(\Delta\varphi) \right)^2 + \left(\left(k_p^{\,2} + k_n^{\,2} \right) \cdot \sin(\Delta\varphi) \right)^2}} \tag{2.93.}$$

This 2nd order non-linear distortion improvement can be plotted as a function of gain & phase balance:

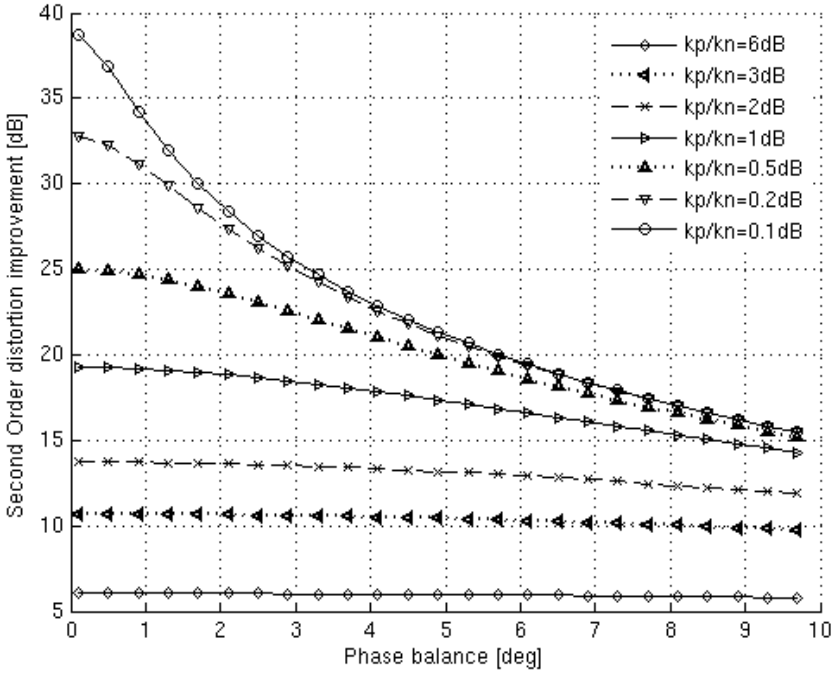


Fig 34. Gain and phase unbalance impact on 2nd order non-linear distortion

For instance, if 20dB of 2nd order non-linearity improvement is targeted, 5 deg of phase imbalance and 0.5 dB of gain imbalance are an acceptable combination.

2.2.5.5 Summary

Behaviour of non-linear distortion of RF front-ends & S&H/ADCs have been explicitly described both in case of narrowband and broadband input signals.

IP2 & IP3 specification have been linked to non-linear distortion performance (IMD, CSO, CTB)

The impact of RFFE non-linear distortion is influenced by the sampling strategy:

- 1st Nyquist band sampling: most of the non-linear distortion beats fall within the 1st Nyquist band, and can therefore not be filtered out
- Nth Nyquist band sampling (N>1): offers the ability to use an AAF for filtering out RFFE non-linear distortion products

The combined impact of limited RFFE gain & phase matching on second-order non-linear distortion has been quantified.

2.2.6 Aliasing

Taking a lowpass sampler as an example, considering the reception of the blue signal in Fig 35 (top), aliasing occurs from two sources:

- Broadband noise (red signal in Fig 35) from many Nyquist zones of the ADC is aliased to the 1st Nyquist zone after sampling
- An interferer located in another Nyquist zone (orange signal in the 2nd Nyquist zone in Fig 35) is aliased back to the 1st Nyquist zone after sampling

To mitigate this effect, an anti-aliasing lowpass filter (green curve in Fig 35, right) is required to provide sufficient

attenuation of broadband noise, non-linear distortion, and interferers (Fig 35, right):

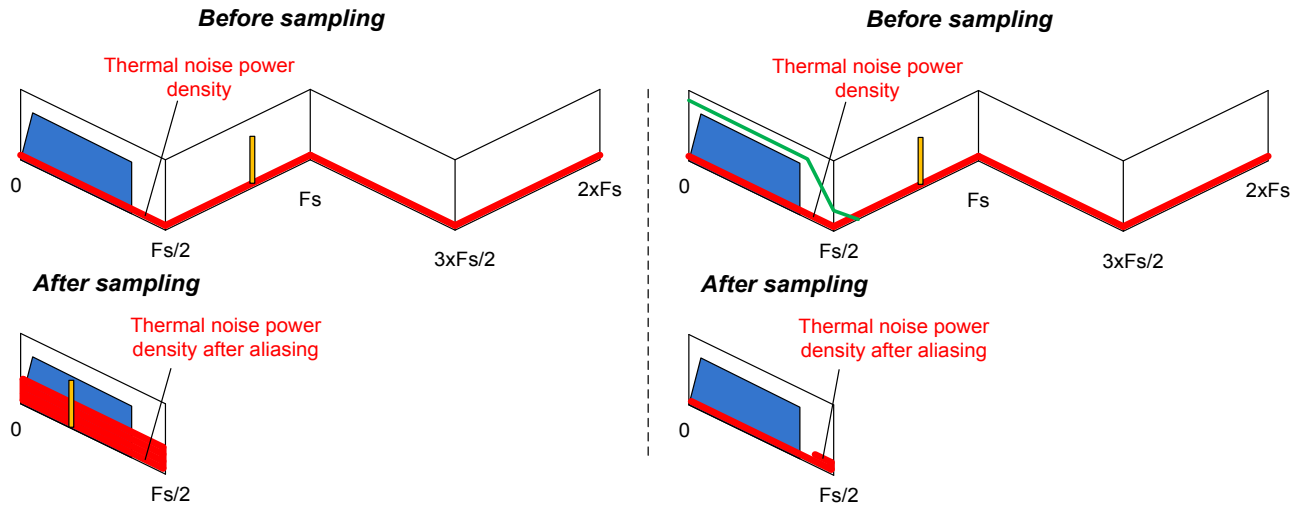


Fig 35. Aliasing of broadband noise and interferers. Left: without AAF, right: with AAF

The increase of noise floor caused by aliasing is a function of the number of Nyquist bands that are being aliased (N_{NYQ}).

$$\Gamma_{AlNoise} = 10 \cdot \log_{10}\left(N_{NYQ}\right) \tag{2.94.}$$

With

$$N_{NYQ} = ceil\left(\frac{NBW}{Fs/2}\right) \tag{2.95.}$$

2.2.7 Time-Interleaved ADC

Considering communication systems with RF frequency in the range of hundreds of MHz or few GHz, very high speed ADC and high dynamic-range ADCs are required, which are often implemented using the time-interleaved technique.

Unfortunately, the performance of interleaved ADC's is sensitive to mismatches between the individual sub-channels ([88]). The effect of these mismatches on a RF direct sampling receiver is detailed on the next sections, and illustrated by taking a four-time interleaving ADC as an example; and assuming Gaussian-distributed channel mismatches.

2.2.7.1 Offset mismatch

A time-interleaved ADC with offset mismatches is shown in Fig 36:

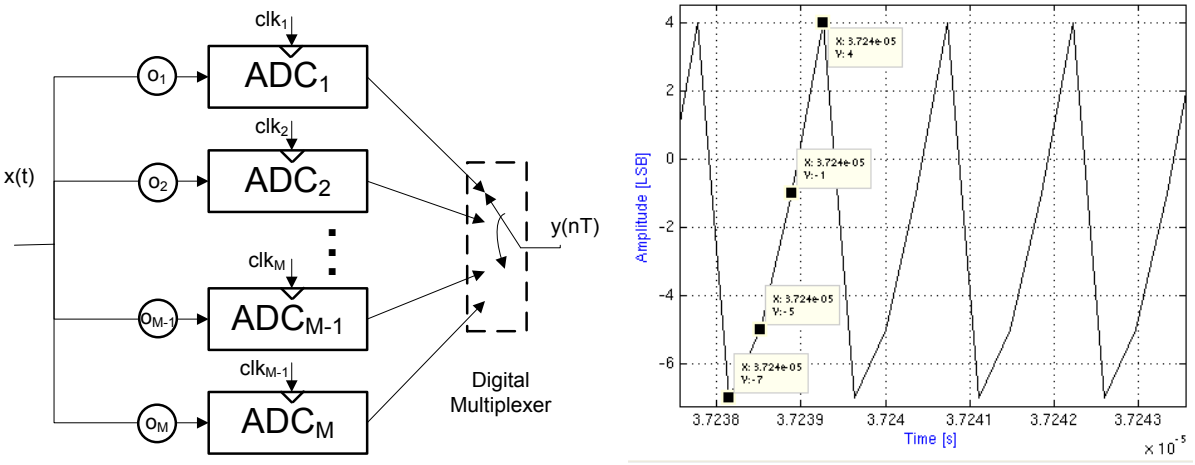


Fig 36. Time-interleaved ADC with offset mismatch (left), time-domain response with four channels & no input signal (right)

Indeed, the time-domain error signal is circularly equal to the individual channel offsets.

The impact of these offsets can be explicitly calculated in the frequency domain:

$$Y(j\Omega)=\frac{1}{M\cdot Ts}\cdot\sum_{k=-\infty}^{+\infty}X\left(j\cdot(\Omega-k\cdot\Omega s)\right)+\frac{1}{M\cdot Ts}\cdot\sum_{k=-\infty}^{+\infty}\delta\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\cdot\sum_{l=0}^{M-1}o_l\cdot 2\pi\cdot e^{-j\cdot k\cdot l\cdot\frac{2\pi}{M}} \quad (2.96.)$$

Where

Ωs : sampling pulsation

M : number of channels

o_l : individual offsets

Sub-channel offset mismatches cause additive tones at integer multiples of the sub-channel sampling rate. Therefore, the output signal is the sum of the sampled input signal and (M-1) spurs at $k\cdot fs/M$. Each spur's amplitude is a vectorial sum of the individual ADC offsets.

For instance, a four-time interleaved ADC would have an output spectrum as shown in Fig 37:

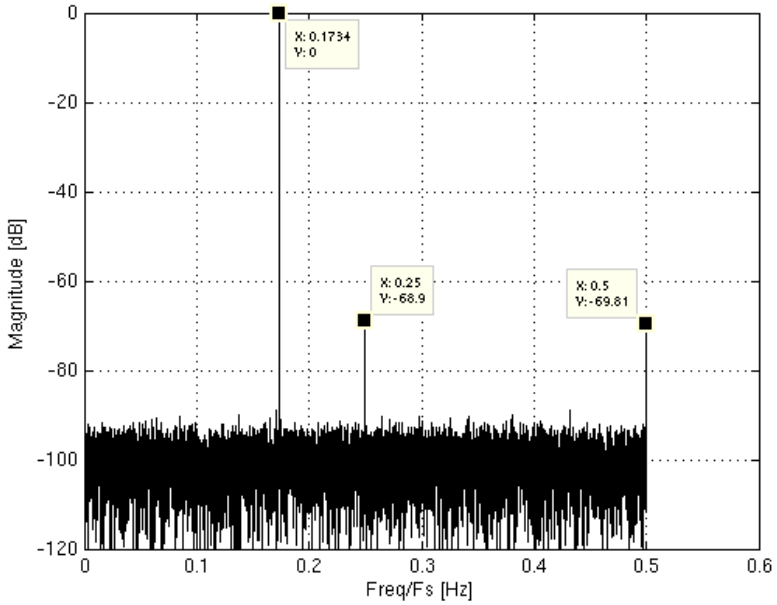


Fig 37. Offset spurs in an ADC with an interleaving factor of four, input=sine wave at 0.1734xFs, σ_{offset}=130µVrms

Two spurs are visible over the full Nyquist band:

- $fs/4$, $=3\cdot fs/4$
- $fs/2$

The $fs/2$ offset spur is generally not relevant, since it falls outside of the useful band. However, when receiving a channel which center frequency is $fs/4$, the signal-independent $fs/4$ offset spur must be low enough to ensure that the receiver still provides a high quality output signal. The offset spur specification can be elaborated against the system specifications (Es/N0 or C/I, loading factor, D/Utot, allocated IL) (Fig 38):

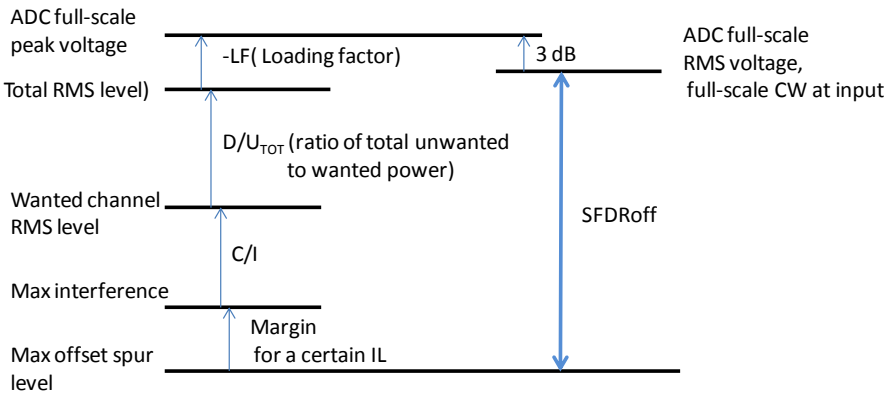


Fig 38. Specification for offset mismatch caused SFDR

The offset spur Nyquist SNR limitation can also be linked to the offset mismatch standard deviation (σ_{off}), independently of the number of parallel channels:

$$SNR_{Nyq} = 20\cdot\log 10\left(\frac{Aw}{\sigma_{off}}\right) \tag{2.97.}$$

In case of a full-scale CW input signal, this can be re-written:

$$SNR_{Nyq} = 20 \cdot \log 10\left(\frac{FS\_Vpp}{2 \cdot \sqrt{2} \cdot \sigma_{off}}\right) \tag{2.98.}$$

The link between SFDR and SNR_{Nyq} depends on the number of spurs, so depends on the number of channels. In a four-time interleaved system, offset-mismatch causes discrete $(M-1)$=3 spurs in total, among which 2 $(M-2)$ fall at $fs/4$. Therefore:

$$SFDR_{Fs/4} = 20 \cdot \log 10\left(\frac{FS\_Vpp}{2 \cdot \sqrt{2} \cdot \sigma_{off}}\right) + 10 \cdot \log_{10}\left(\frac{M-1}{M-2}\right) \tag{2.99.}$$

2.2.7.2 DC gain mismatch

A time-interleaved ADC with gain mismatches is shown in Fig 39:

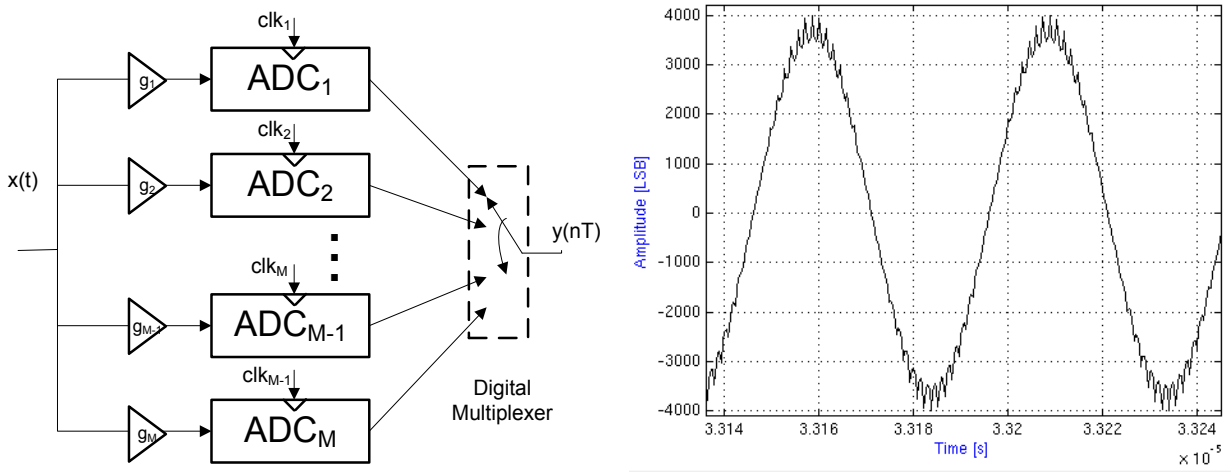


Fig 39. Time-interleaved ADC with gain mismatch (left), time-domain response with four channels & a sine wave input signal (right)

The ADC output signal is amplitude-modulated by the channel gain errors.

The impact of these gain mismatches can be explicitly calculated in the frequency domain:

$$Y(j\Omega) = \frac{1}{M \cdot Ts} \cdot \sum_{l=0}^{M-1} \sum_{k=-\infty}^{+\infty} g_l \cdot X_l\left(j \cdot \left(\Omega - k \cdot \frac{\Omega s}{M}\right)\right) \cdot e^{-j \cdot k \cdot l \cdot \frac{2\pi}{M}} \tag{2.100.}$$

Where

Ωs : sampling pulsation

M : number of channels

g_l : individual gains

Channel gain mismatch causes the input spectrum to be duplicated around multiple of Fs/M, with amplitudes that depend on the vectorial sum of the gain errors. In the case of ideally matched channels; these aliases perfectly cancel each other. This is not the case with a limited matching between all channels. In such a case, the vectorial sum of the individual ADC gains defines the spurs amplitude.

For instance, a four-time interleaved ADC would have an output spectrum as shown in Fig 40 in case the input signal is a single sine wave:

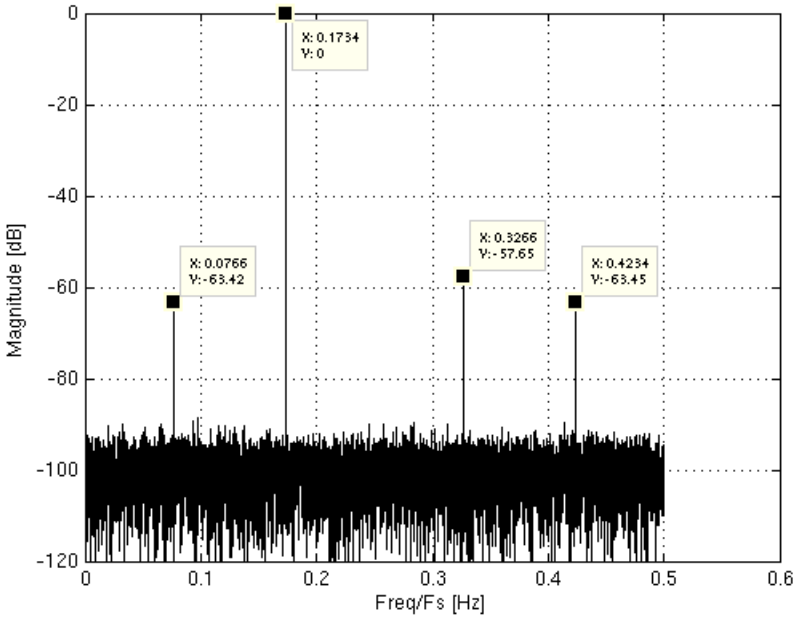


Fig 40. Gain spurs in an ADC with an interleaving factor of four, input=sine wave at 0.1734xFs, $\sigma_{gain}=0.5x10^{-3}$

Three spurs are visible over the full Nyquist band:

- $Fin + fs/4$,
- $Fin + 2 \cdot fs/4$ after aliasing,
- $Fin + 3 \cdot fs/4$ after aliasing.

In case of the reception of a multi-tone signal, the amplitude of the individual tones are reduced compared to the full-scale sine wave of Fig 40. Indeed, the amplitude of the aliases reduces as well, providing an equivalent SFDR in both situations. These aliases cause wideband "noise" in the case of wideband modulated input signals.

The full-rate ADC output signal can be expressed as:

$$out(k \cdot T) = (1 + gain(k \cdot T)) \cdot in(k \cdot T) \tag{2.101.}$$

gain: random variable with standard deviation is σ_{gain}.

For an input signal that consists on a wanted channel only, the SNR is:

$$SNR_{Nyq} = 20 \cdot \log 10\left(\frac{1}{\sigma_{gain}}\right) \tag{2.102.}$$

For wideband input, gain mismatch causes wideband "noise". Assuming this "noise" is uniformly distributed over Nyquist frequency band, SNR can be estimated quite accurately with:

$$SNR_{Nyq} = 20 \cdot \log_{10}\left(\frac{Pw}{Ptot \cdot \sigma_{gain}}\right) \tag{2.103.}$$

This can be interpolated to the SNR within a wanted channel BW:

$$SNR_{ChBW} = D/Ptot\_dB - 20\cdot\log_{10}(\sigma_{gain}) + 10\cdot\log_{10}\left(\frac{Fs}{2\cdot NBW}\right) \quad (2.104.)$$

Therefore, gain spur specification can be elaborated against the system specifications, considering the targeted Es/N0 and the IL allocated for this impairment:

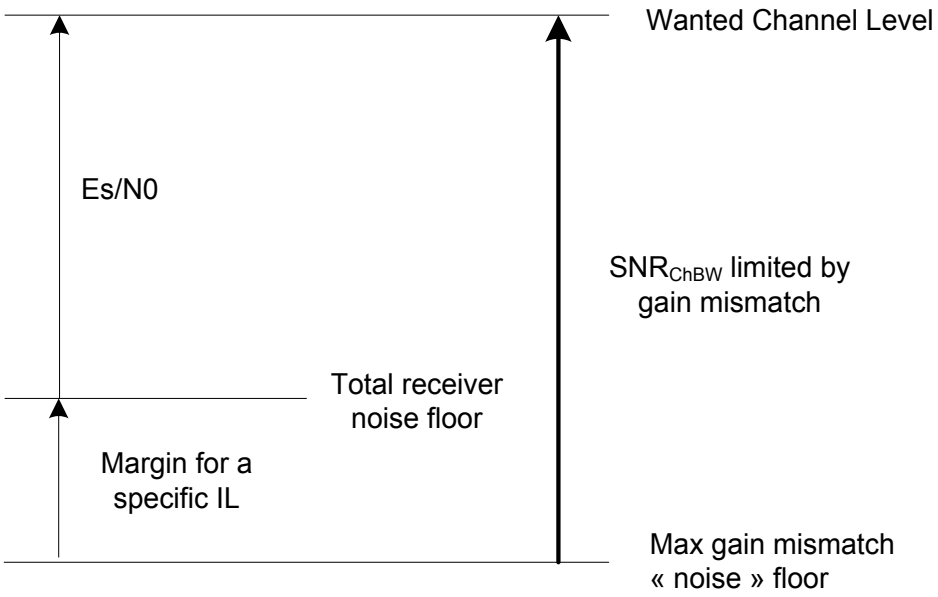


Fig 41. Specification for gain mismatch caused SNR

2.2.7.3 Sampling time skew

A time-interleaved ADC also suffers from time skew mismatch, as shown in Fig 42:

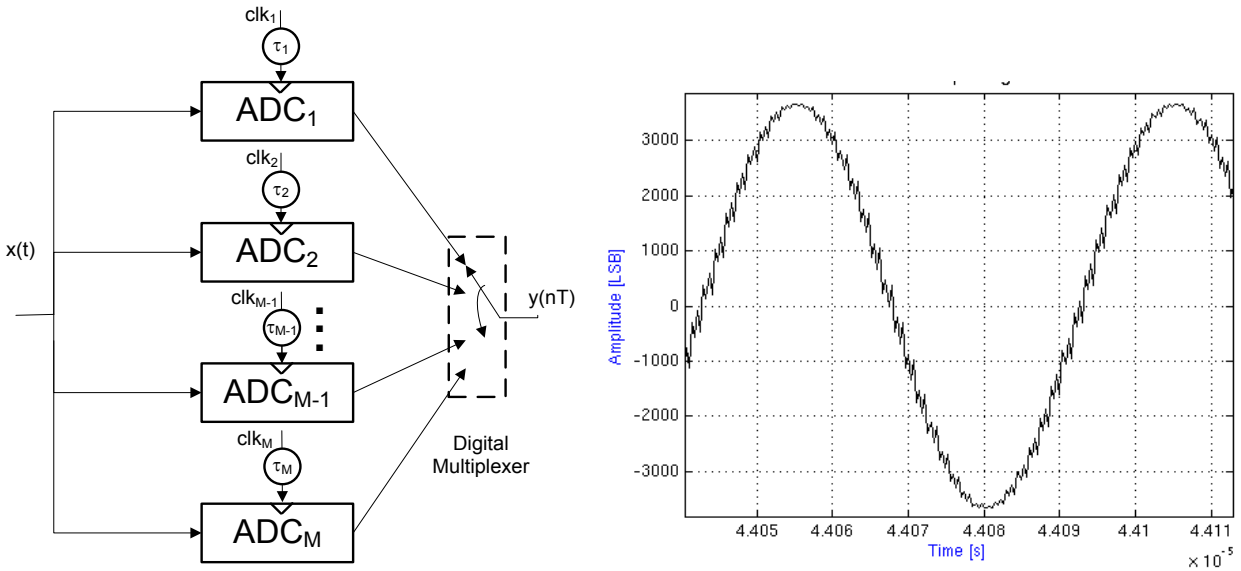


Fig 42. Time-interleaved ADC with time skew mismatch

Time skew mismatch is due to imperfectly equal signal/clock lines, differences on the sub-channel clock buffers or

on the sampling switches. This sampling time error can be seen as a phase modulation of the input signal.

The frequency domain output of a time-interleaved converter with time skew can be expressed as:

$$Y(j\Omega)=\frac{1}{M\cdot Ts}\cdot\sum_{k=-\infty}^{+\infty}X\left(j\cdot\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\right)\cdot\sum_{l=0}^{M-1}e^{-j\cdot k\cdot l\cdot\frac{2\pi}{M}}\cdot e^{-j\cdot\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\cdot\Delta t_l} \quad (2.105.)$$

Ωs : sampling pulsation

M : number of channels

Δt_l : individual time skews

The input spectrum is therefore duplicated around multiple of Fs/M, where the images amplitude depends on the vectorial sum of the timing errors (last exponential term).

Time skew produces images at the same frequencies as DC gain mismatch does. The images amplitudes are proportional to the input signal frequency for time skew errors, when they are independent of the input signal frequency for DC gain errors.

Seeking for simpler expressions that allow Signal-to-Noise calculations, we can write:

$$out(k\cdot T)=in(k\cdot T+skew(k\cdot T)) \quad (2.106.)$$

Assuming small time skew errors, we can write the sampled signal as the wanted signal plus an error, which is a linear function of input signal variation and time error (1st term of Taylor series):

$$s_\tau(k)\approx s(k\tau)+\Delta t(k\tau)\cdot\frac{\partial}{\partial t}s(t)_{|k\tau} \quad (2.107.)$$

$$out(k\cdot T)\approx in(k\cdot T)+skew(k\cdot T)\cdot\frac{\partial}{\partial t}in(t)\Big|_{k\cdot T} \quad (2.108.)$$

$skew$: random variable which standard deviation= σ_{skew} .

Thus, it is clear that the error depends on the total input signal derivative, so amplitude & frequency.

For input signal consisting of a single channel, Signal-to-Noise Ratio in Nyquist band can be calculated as:

$$SNR_{Nyq}=20\cdot\log_{10}(\sigma_{skew}\cdot w_w) \quad (2.109.)$$

Considering a multi-tone input signal with random phases:

$$in(t)=\sum_{i=1}^{N}Ai\cdot\sin(wi\cdot t+\varphi i) \quad (2.110.)$$

As the time skew images are frequency-dependent, the SNR, limited by time skew, over a channel BW, cannot be expressed simply. However, its mean value, calculated as the SNR per channel, averaged across a Nyquist band can be simply calculated as:

$$SNR_{ChBW} = 20 \cdot \log_{10}\left(\frac{Aw}{\sigma_{skew} \cdot \sqrt{\sum_{i=1}^{N}(Ai \cdot wi)^2}}\right) + 10 \cdot \log_{10}\left(\frac{Fs}{2 \cdot NBW}\right) \quad (2.111.)$$

Fig 43 shows an example of a broadband multi-tone input signal, sampled with four channels and time skew mismatch. The input multiple tones are equal and referenced at 0 dB, while the three input signal images, caused by time-skew, are frequency-dependent:

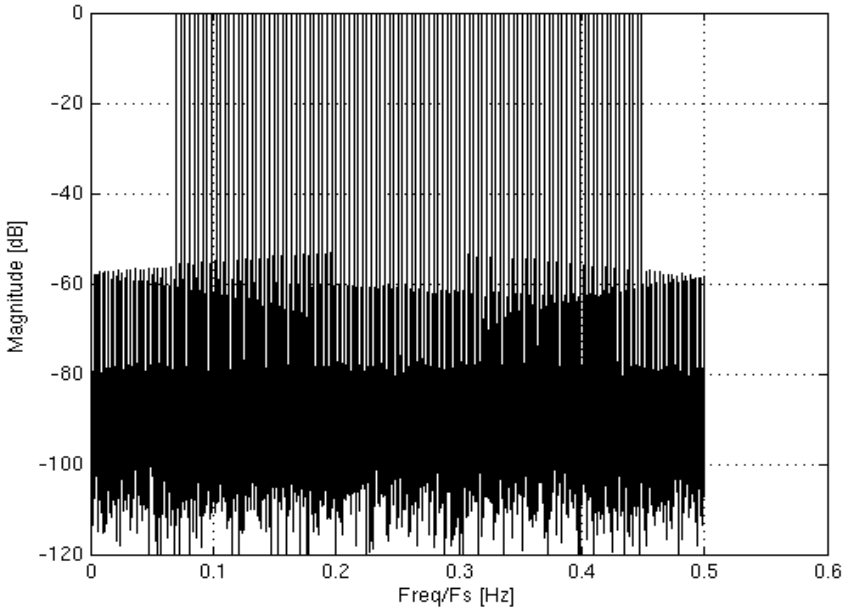


Fig 43. Multi-tone broadband signal digitization with σ_{skew}=3.5x10^{-4}xFs

Finally, time skew spur specification can be elaborated against the system specifications, considering the targeted Es/N0 and the IL allocated for this impairment, exactly as shown for gain mismatch in Fig 41.

2.2.7.4 Transfer function mismatch

In addition to offset mismatch, gain mismatch & time skews, time-interleaved ADC also suffer from Sample-And-Hold transfer function mismatch (Fig 44).

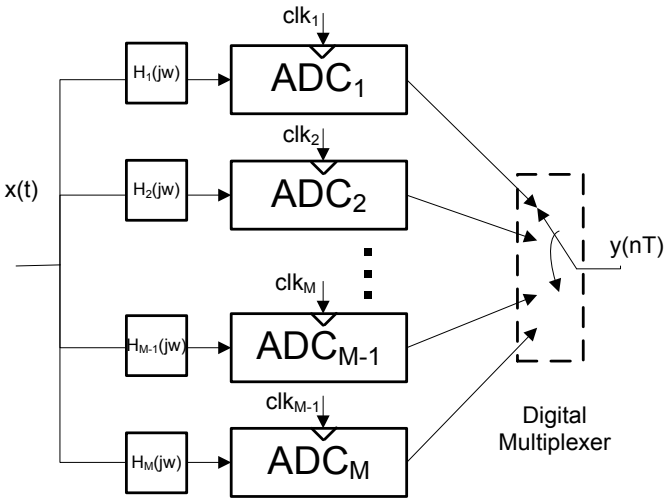


Fig 44. Time-interleaved ADC with transfer function mismatch

After some manipulation, the frequency-domain output of a time-interleaved ADC suffering from transfer function mismatch can be expressed as:

$$Y(j\Omega)=\frac{1}{M\cdot Ts}\cdot\sum_{k=-\infty}^{+\infty}X\left(j\cdot\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\right)\cdot\sum_{l=0}^{M-1}\left|H_l\left(j\cdot\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\right)\right|\cdot e^{-j\cdot k\cdot l\cdot\frac{2\pi}{M}}\cdot e^{-j\cdot\left(\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\cdot\Delta t_l-\theta_l\left(j\cdot\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\right)\right)} \quad (2.112.)$$

$$\theta_l(j\Omega)=\arctan\left(\frac{\Omega}{\Omega c_l}\right) \quad (2.113.)$$

Where Ωc_l are the TH cut-off pulsations of the different channels (1st order assumption).

For $\Omega c_l >> \Omega$, this can be approached by a limited series development:

$$\theta_l(j\Omega)\approx\frac{\Omega}{\Omega c_l} \quad (2.114.)$$

$$Y(j\Omega)\approx\frac{1}{M\cdot Ts}\cdot\sum_{k=-\infty}^{+\infty}X\left(j\cdot\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\right)\cdot\sum_{l=0}^{M-1}\left|H_l\left(j\cdot\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\right)\right|\cdot e^{-j\cdot k\cdot l\cdot\frac{2\pi}{M}}\cdot e^{-j\cdot\left(\left(\Omega-k\cdot\frac{\Omega s}{M}\right)\cdot\Delta t_l-\left(\frac{\Omega-k\cdot\frac{\Omega s}{M}}{\Omega c_l}\right)\right)} \quad (2.115.)$$

The dominant source of mismatch is the difference in phase between THs. Therefore we split the phase into common (mean) phase and phase deviation. Phase deviation can be written as:

$$\Delta\theta_l(j\Omega)=\frac{\Omega}{\Omega c_l}-\frac{\Omega}{\overline{\Omega c}}=\Omega\cdot\frac{\overline{\Omega c}-\Omega c_l}{\Omega c_l\cdot\overline{\Omega c}} \quad (2.116.)$$

$$\Omega c_l = \overline{\Omega c} + \Delta\Omega c_l \tag{2.117.}$$

(Mean cut-off pulsation, cut-off pulsation mismatch)

$$\Delta\theta_l(j\Omega) \approx \Omega \cdot \frac{\Delta\Omega c_l}{\overline{\Omega c}^2} \tag{2.118.}$$

Therefore, if both phase mismatch and time skew mismatch are allowed to equally degrade performance:

$$\Delta\theta_l(j\Omega) \leq \Delta t_l \cdot \Omega \tag{2.119.}$$

$$\Omega \cdot \frac{\Delta\Omega c_l}{\overline{\Omega c}^2} \leq \Delta t_l \cdot \Omega \tag{2.120.}$$

$$\frac{\Delta\Omega c_l}{\overline{\Omega c}} \leq \Delta t_l \cdot \overline{\Omega c} \tag{2.121.}$$

Or, written in relative variations of cut-off frequencies:

$$\frac{\Delta Fc_l}{\overline{Fc}} \leq 2\pi \cdot \Delta t_l \cdot \overline{Fc} \tag{2.122.}$$

Where Fc is the mean cut-off frequency (Hz),

Δt_l is the time skew (seconds),

ΔFc_l is the cut-off frequency absolute deviation (Hz).

For instance, if 0.3 ps time skew standard deviation was specified, with a 6 GHz TH, 1.1% bandwidth mismatch is required.

2.2.7.5 Statistical behavior of the channel mismatches

Channel mismatches are subject to manufacturing variations. Those induce variations on the ADC SDR & SFDR from sample to sample. A properly manufactured IC will have to meet a certain performance with a targeted confidence interval. The study, which is provided in [89] demonstrates that the probability density functions of SNR & SFDR caused by offset mismatch, gain mismatch and time-skew follow a Chi-square law. Fig 45 plots an example of SNR distribution for a time-interleaved ADC with two, four and eight channels, assuming Gaussian-distributed random mismatches:

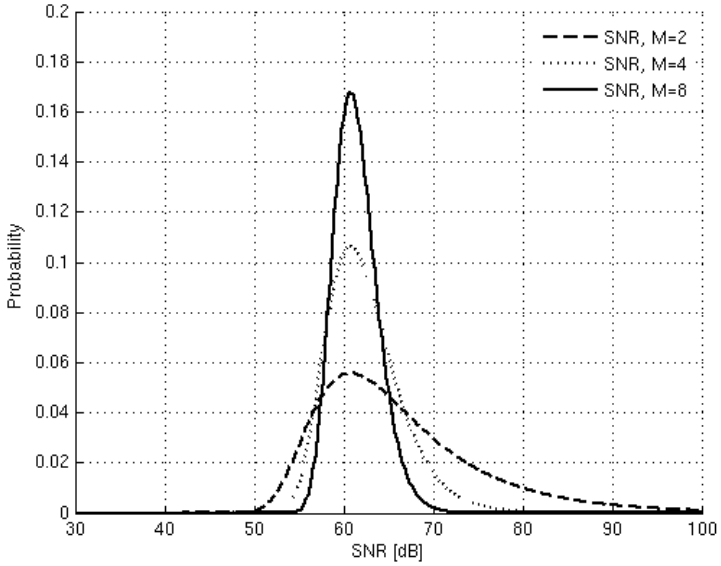


Fig 45. Statistical simulation of SNR induced by offset mismatch in a two/four/eight-channel time-interleaved ADC

A low number of sub-channels causes a high SNR spread. The theoretical statistical distribution (PDF) of SNR is confirmed by the simulation results shown in Fig 46, for respectively offset, gain and time skew mismatches:

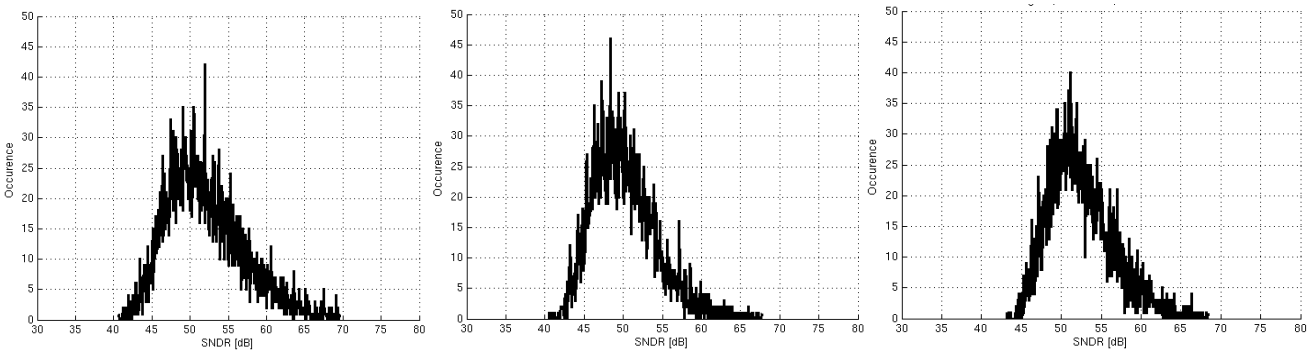


Fig 46. SNDR distribution for offset, gain & time-skew mismatches, four channels, 5000 trials

The SNR/SFDR specification developed in 2.2.7.1, 2.2.7.2, 2.2.7.3 and 2.2.7.4 were calculated for the average SNR/SFDR, which is the peak of the PDF curve in Fig 45 & Fig 46.

Yield analysis can be easily done by calculating the SFDR/SNR cumulated density function (CDF, F). This is achieved by integrating the SFDR/SNR probability density function (PDF, P).

$$F(x) = \int_{-\infty}^{x} P(t)dt \tag{2.123.}$$

In this way, it is possible to design for a specific yield.

2.2.7.1 Summary

Time-interleaved ADCs channel mismatches (offset, gain, time-skew and transfer function) have been analyzed and specified for a communication system receiver, taking into account a broadband environment.

Gain, time skew and transfer function mismatches cause signal images in the time-interleaved ADC output spectrum, and might be low in case of a broadband signal, if the input signal approaches a constant PSD.

As offset mismatch cause a signal-independent spur on the ADC output spectrum, it might be harmful when receiving a broadband input signal.

The statistical aspects of channel mismatches have also been reviewed, showing the necessity to specify channel mismatches with margin in order to guarantee a sufficient SFDR, over a high number of samples.

2.2.8 Sampling clock requirements

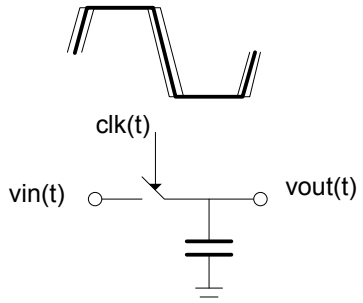


Fig 47. Sampling with a non-ideal clock

During sampling process, input and clock signals are multiplied in the time-domain. Therefore, clock phase noise spectrum is convolved with ADC input signal spectrum, and phase noise is transferred from the ADC clock to the output signal.

The developed theory starts from [90] and adapts it for a multi-channel signal.

s : input signal (to be sampled)

$s\tau$: sampled version of s(t),

Δt : small absolute jitter,

$\Delta s\tau$: Error signal

$$s_\tau(k) = s(k\tau + \Delta t(k\tau)) \tag{2.124.}$$

Assuming that time jitter is small, we can write the sampled signal as the sum of the wanted signal and an error term, which is a linear function of input signal variation and time error (1st term of Taylor series)

$$s_\tau(k) \approx s(k\tau) + \Delta t(k\tau) \cdot \frac{\partial}{\partial t} s(t)_{|k\tau} \tag{2.125.}$$

Then, error term can be written as:

$$\Delta s\tau(k) = s(k\tau + \Delta t(k\tau)) - s(k\tau) \tag{2.126.}$$
$$\Delta s\tau(k) \approx \Delta t(k\tau) \cdot \frac{\partial}{\partial t} s(t)_{|k\tau}$$

Taking the Discrete-time Fourier transform:

$$TF(\Delta s\tau(k)) \approx TF(\Delta t(k\tau)) \otimes TF\left(\frac{\partial}{\partial t} s(t)_{|k\tau}\right) \tag{2.127.}$$

Then, considering an input signal composed by a sum of channels:

$$s(t) = \sum_{i=1}^{i\max} s_i(t) \tag{2.128.}$$

The error term Fourier transform can be written as:

$$TF(\Delta s\tau(k)) \approx TF(\Delta t(k\tau)) \otimes TF\left(\frac{\partial}{\partial t}\sum_{i=1}^{i\max} s_i(t)_{|k\tau}\right) \tag{2.129.}$$

Using the distributive property of derivative operation, Fourier transform and convolution operators:

$$TF(\Delta s\tau(k)) \approx \sum_{i=1}^{i\max}\left\{TF(\Delta t(k\tau)) \otimes TF\left(\frac{\partial}{\partial t} s_i(t)_{|k\tau}\right)\right\} \tag{2.130.}$$

If we assume that each channel can be modeled by a sine wave, then input signal is:

$$s(t) = \sum_{i=1}^{i\max} A_i \cdot \sin(w_i \cdot t + \varphi_i) \tag{2.131.}$$

The error term Fourier transform is:

$$TF(\Delta s\tau(k)) \approx \sum_{i=1}^{i\max} TF(\Delta t(k\tau)) \otimes A_i \cdot w_i \cdot TF(\cos(wi \cdot k\tau)) \tag{2.132.}$$

$$TF(\Delta s\tau(k)) \approx \sum_{i=1}^{i\max} TF(\Delta t(k\tau)) \otimes A_i \cdot w_i \cdot TF\left(\frac{e^{(j\cdot wi\cdot k\cdot\tau)} + e^{(-j\cdot wi\cdot k\cdot\tau)}}{2}\right) \tag{2.133.}$$

$$TF(\Delta s\tau(k)) \approx \sum_{i=1}^{i\max} TF(\Delta t(k\tau)) \otimes A_i \cdot w_i \cdot \left\{\frac{\delta(f - f_i) + \delta(f + f_i)}{2}\right\} \tag{2.134.}$$

This shows that clock phase noise is convolved with every carrier of the input spectrum (Fig 48). This convolution product transfers the clock noise spectrum around each channel, weighted by "amplitude times frequency" product. Therefore, more phase noise is transferred to high-frequency signals than to low frequency signals. Ultimately, the different noise floors add in power.

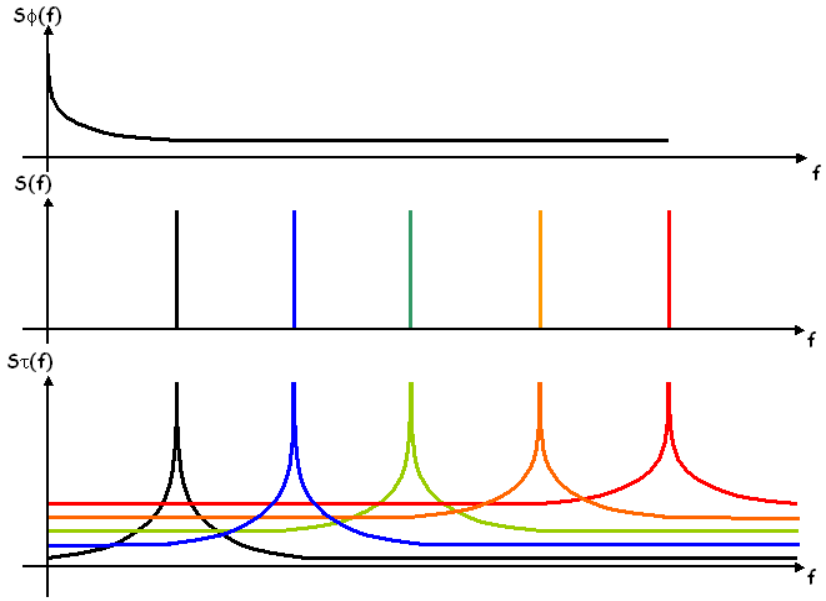


Fig 48. Clock phase noise convolved with multiple carriers input spectrum

Sϕ(f) is the phase noise density, S(f) is the input spectrum, Sτ(f) is the sampled signal spectrum.

Assuming an integer N PLL, the phase noise model, which follows ([91]) can be used as an approximation (Fig 49):

- Low frequency part: phase noise is typically limited by the reference phase noise (crystal oscillator),
- Within the PLL BW, phase noise is typically limited by the phase/frequency detector,
- For frequencies above PLL BW, phase noise density is limited by the VCO phase noise
- For very large frequency offsets, the LO chain (dividers, buffers) dominate the constant noise floor.

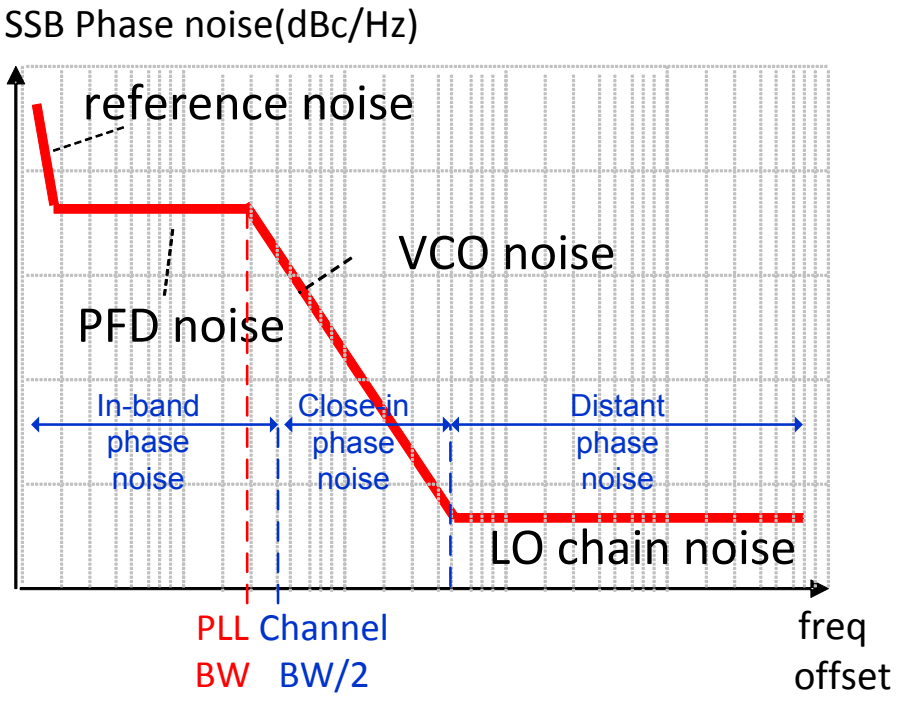


Fig 49. Typical clock phase noise profile

Next sections will provide guidance for specifying the phase noise in these different regions.

2.2.8.1 In-band Phase Noise

Modern single-carrier systems use amplitude & phase modulations. In these complex digital modulations, data symbol represented by the coordinate pair (ak, bk) are transmitted.

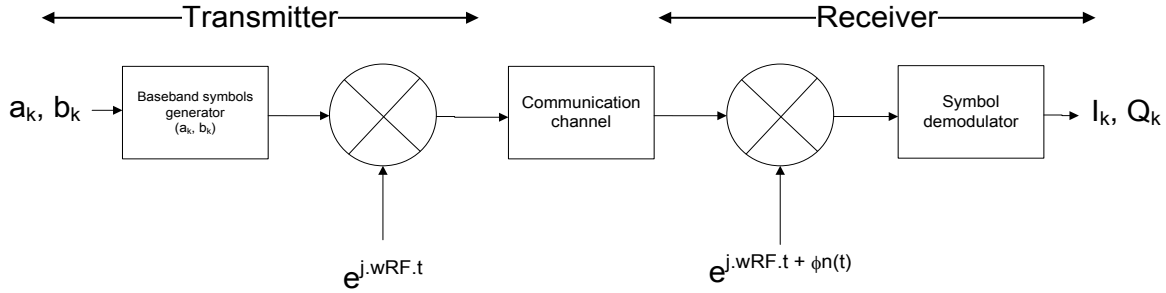


Fig 50. Communication system with phase noise in the receiver

After down-conversion by a receiver, the baseband I & Q signals can be written as:

$$I_k = \Re\left\{\left(a_k + j \cdot b_k\right) \cdot e^{j \cdot \varphi_n}\right\} \tag{2.135.}$$

$$Q_k = \Im\left\{\left(a_k + j \cdot b_k\right) \cdot e^{j \cdot \varphi_n}\right\} \tag{2.136.}$$

$$I_k = a_k \cdot \cos\left(\varphi_n\right) - b_k \cdot \sin\left(\varphi_n\right) \tag{2.137.}$$

$$Q_k = a_k \cdot \sin(\varphi_n) - b_k \cdot \cos(\varphi_n) \tag{2.138.}$$

$$\begin{bmatrix} I_k \\ Q_k \end{bmatrix} = \begin{bmatrix} \cos(\varphi_n) & -\sin(\varphi_n) \\ \sin(\varphi_n) & \cos(\varphi_n) \end{bmatrix} \cdot \begin{bmatrix} a_k \\ b_k \end{bmatrix} \tag{2.139.}$$

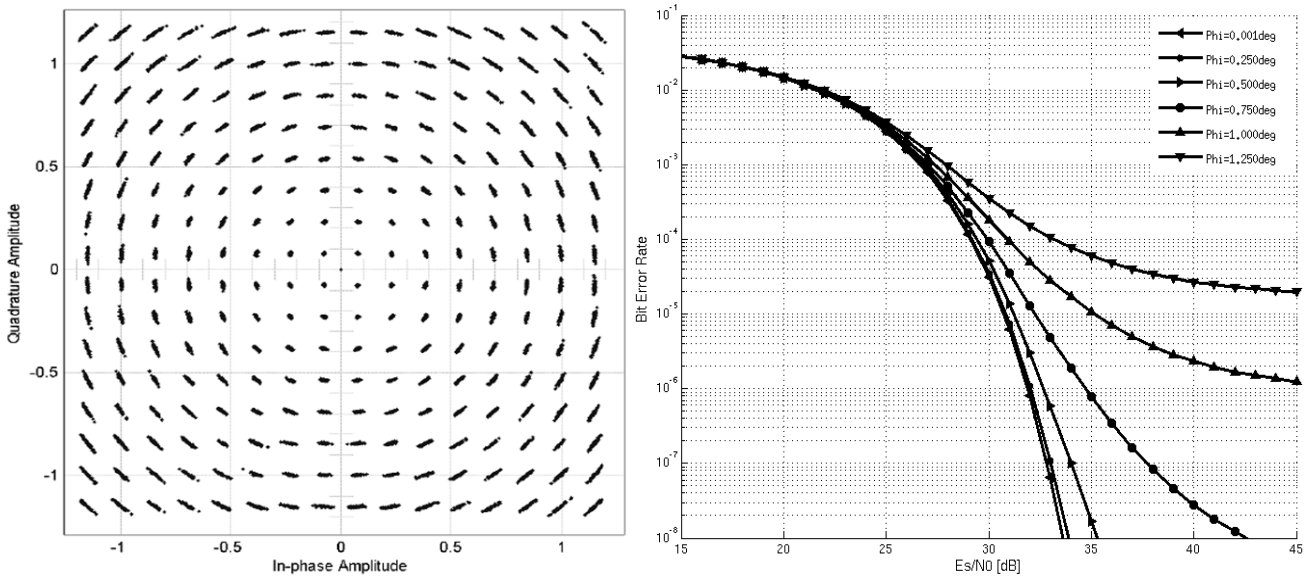


Fig 51. In-band phase noise effect on a complex modulation (left), and on BER (right)

Fig 51 (left) shows the cross-talk between I and Q components caused by in-band phase noise. The BER degradation caused by this cross-talk is calculated for a 256-QAM modulation using the demonstration of [92], and is plotted in Fig 51 (right).

Using the following relation-ship between integrated phase noise and SSB phase noise, in-band SSB phase noise can be specified:

$$\Delta\theta_{RMS}, \deg = \frac{180 \cdot \sqrt{\int_{f1}^{f2} L(f)df}}{\pi} \tag{2.140.}$$

$f1, f2$: limits of digital baseband clock recovery loop

$L(f)$: Single Side Band phase noise

Phase noise transfer from clock [dBc] to A/D output [dBc] can be found to follow the rule [93]:

$$Noise\_ADout = Noise\_clk + 20 \cdot \log 10\left(\frac{fsignal}{fclk}\right) \tag{2.141.}$$

Phase noise is transferred from clock to A/D output with is a scaling factor proportional to the ratio between $fsignal$ and $fclk$.

The same scaling factor also applies for the transfer of integrated phase jitter.

Finally, integrated phase jitter can be converted to integrated time jitter using the following:

$$\sigma_{tjit} = \sigma_{IPN} \cdot \frac{Tclk}{360} = \frac{\sigma_{IPN}}{Fclk \cdot 360} \tag{2.142.}$$

This impact of in-band phase noise in case of OFDM modulations is very well detailed in [92].

2.2.8.2 Reciprocal sampling

As presented in section 2.1.4, unfiltered nearby interferers or blockers can also be part of the RF input signal.

As illustrated in Fig 48, clock phase noise is convolved with each of these individual blockers. If the difference in frequency between the wanted channel and the blockers is lower than the frequency at which the PLL enters the "distant phase noise" zone, the receiver noise floor can be drastically degraded. Fig 52 illustrates the reciprocal sampling process in the presence of an N+/-1, N+/-2 and N+/-3 blockers.

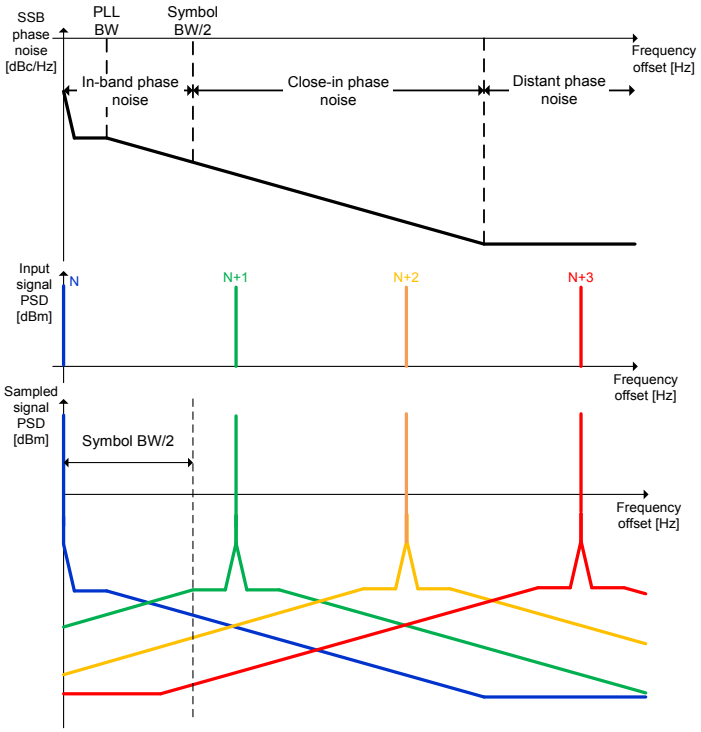


Fig 52. Reciprocal sampling process

Clearly, in case of blockers with equal amplitude, the closer from the wanted channel the blocker is, the worst the situation is with respect to reciprocal sampling. As illustrated in 2.1.4, a typical wireless system specifies the blockers amplitude to decrease when the frequency offset reduces.

Close-in phase noise region

The integrated noise floor due to phase noise in the presence of a blocker can be calculated and simplified assuming phase noise flatness across a single channel BW:

$$Pn_{\text{int}} = Pbl \cdot \int_{foff-BW/2}^{foff+BW/2} Sn(f) \cdot \left(\frac{Fbl}{Fadc}\right)^2 \cdot df \approx Pbl \cdot Sn(f) \cdot \left(\frac{Fbl}{Fadc}\right)^2 \cdot BW \tag{2.143.}$$

$$Pn_{\underset{dBm}{\text{int}}} \approx Pbl_{dBm} + Sn_{dBc/Hz} + 20 \cdot \log_{10}\left(\frac{Fbl}{Fadc}\right) + 10 \cdot \log_{10}(BW) \quad (2.144.)$$

Where $Sn(f)$ ($Sn_{dBc/Hz}$) is the clock signal phase noise density.

Where:

$$20 \cdot \log_{10}\left(\frac{Fbl}{Fadc}\right) \quad (2.145.)$$

is the phase noise transfer factor from [93].

In order to be able to specify close-in phase noise density, Fig 53 directly links it to the targeted SNR ($SNR_{RecSamp}$):

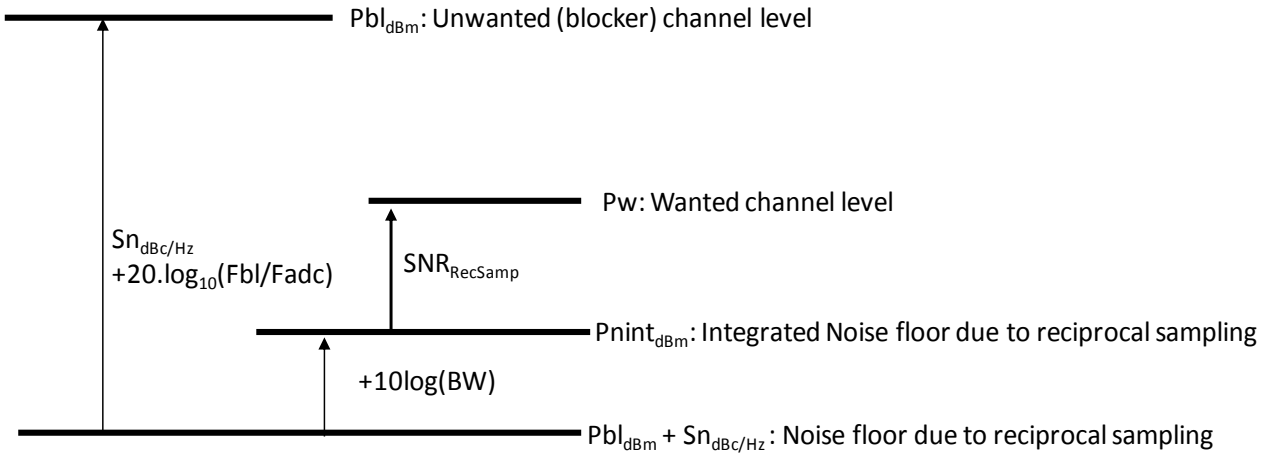


Fig 53. Reciprocal Sampling – Link between phase noise density and SNR

Wideband phase noise region

Wideband phase noise specification must take into account whole input spectrum shape. In case of a multi-tone input signal (amplitude: Ai, frequency: Fi), the Nyquist-BW SNR limited by wideband phase noise can be approximated as [95]:

$$SNR_{Nyq} = -10 \cdot \log 10\left(\frac{(2 \cdot \pi \cdot \sigma jit)^2 \cdot \sum_{i=1}^{N} Ai^2 \cdot Fi^2}{Awant^2}\right) \quad (2.146.)$$

Where σjit is the integrated time jitter (integration of wideband distant phase noise).

Assuming a flat distant phase noise, the SNR within one channel BW is improved by the over-sampling factor:

$$SNR_{ChBW} = -10 \cdot \log_{10}\left(\frac{(2 \cdot \pi \cdot \sigma jit)^2 \cdot \sum_{i=1}^{N} Ai^2 \cdot Fi^2}{Awant^2}\right) + 10 \cdot \log_{10}\left(\frac{Fclk}{2 \cdot ChBW}\right) \quad (2.147.)$$

$$D/U = 20\log_{10}(Ai/Aw)$$

In case of equal unwanted tones and D/U being the difference in dB between wanted and each unwanted channel level, this can be simplified to:

$$SNR_{ChBW} = -10\cdot\log_{10}\left(10^{\frac{-D/U}{10}}\cdot(2\cdot\pi\cdot\sigma jit)^2\cdot\sum_{i=1}^{N}Fi^2\right)+10\cdot\log_{10}\left(\frac{Fclk}{2\cdot ChBW}\right) \quad (2.148.$$

In addition, wideband noise of the sampling clock over the multiple Nyquist zones is aliased within a single A/D Nyquist zone ([93], Fig 54):

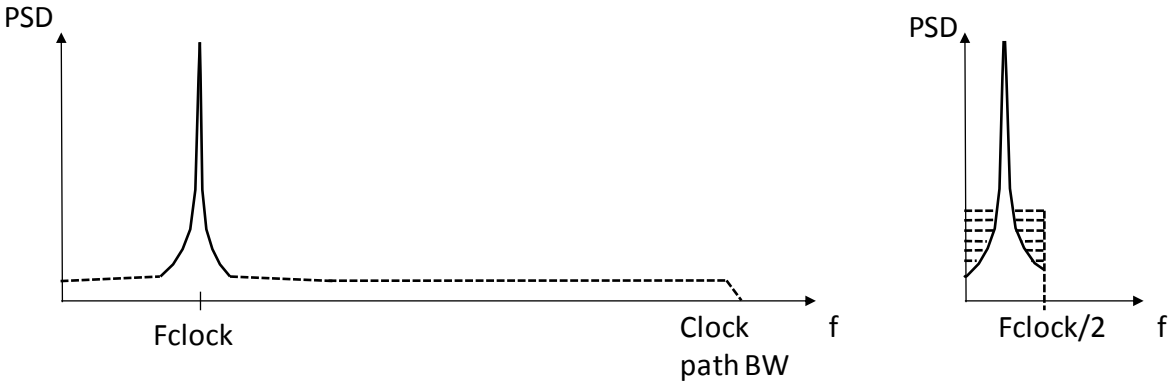


Fig 54. left: clock PSD, right: wideband clock phase noise PSD transfered to the sampled signal (inclusing aliasing)

This can result in a significant accumulation of the noise and a significant reduction of SNR (in dB), which can be taken into account by a degradation factor ([93]):

$$ClkBWFactor = 10\cdot\log_{10}\left(\frac{BWclk}{\frac{Fs}{2}}\right) \quad (2.149.)$$

It can be seen that the higher the clock buffers bandwidth (compared to clock frequency), the higher the degradation factor. Such a high bandwidth is likely to be required for getting sharp edges to switch off S&H switches.

2.2.8.1 Summary

The effect of phase has been studied in the context of medium-bandwidth channels. The transfer of phase noise, from the clock signal to the complex broadband signal has been calculated. For the analysis, phase noise spectrum has been split into three regions:

- In-band phase noise: the phase noise gives rise to crosstalk between I & Q components of complex modulations. This degrades the minimum SNR under which a demodulator can still deliver an acceptable BER.
- Close-in phase noise: the phase noise spectrum density, which is typically still high at low frequency offset, convolves with potentially strong adjacent channels. This reciprocal mixing adds noise inside the wanted channel BW.
- Distant phase noise: large BW clock path cause aliasing of phase noise. Because of the large conversion bandwidth, a large number of interferers can altogether increase the noise level within the wanted channel

BW, through the reciprocal sampling process.

2.2.9 Digital channel selection

After digitization of the whole RF input signal, digital channel selection (DCS) selects the individual RF channels that are of interest in the application.

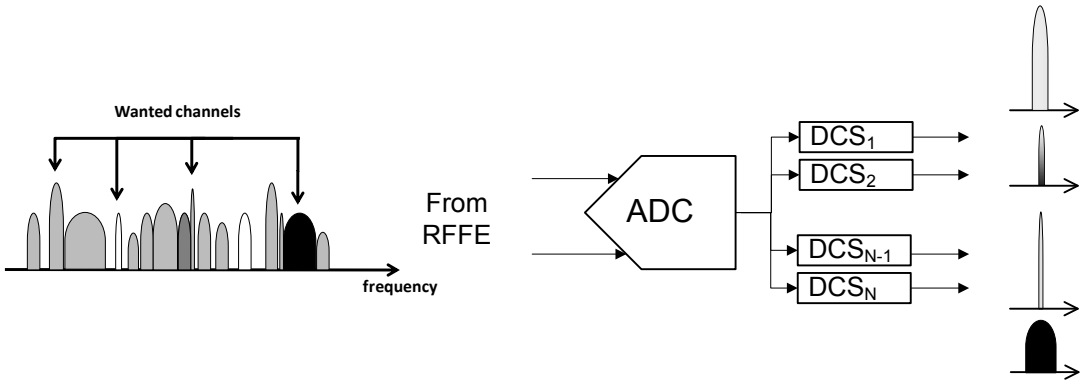


Fig 55. Digital Channel Selection

The different signal processing operations that are used in a general DCS are shown in Fig 56:

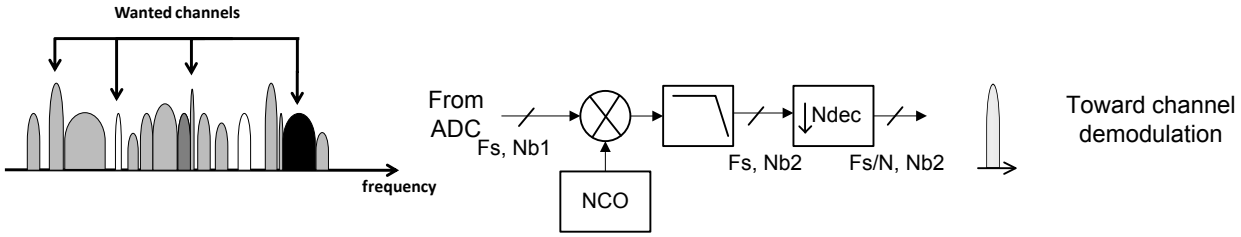


Fig 56. Signal Processing involved in Digital Channel Selection

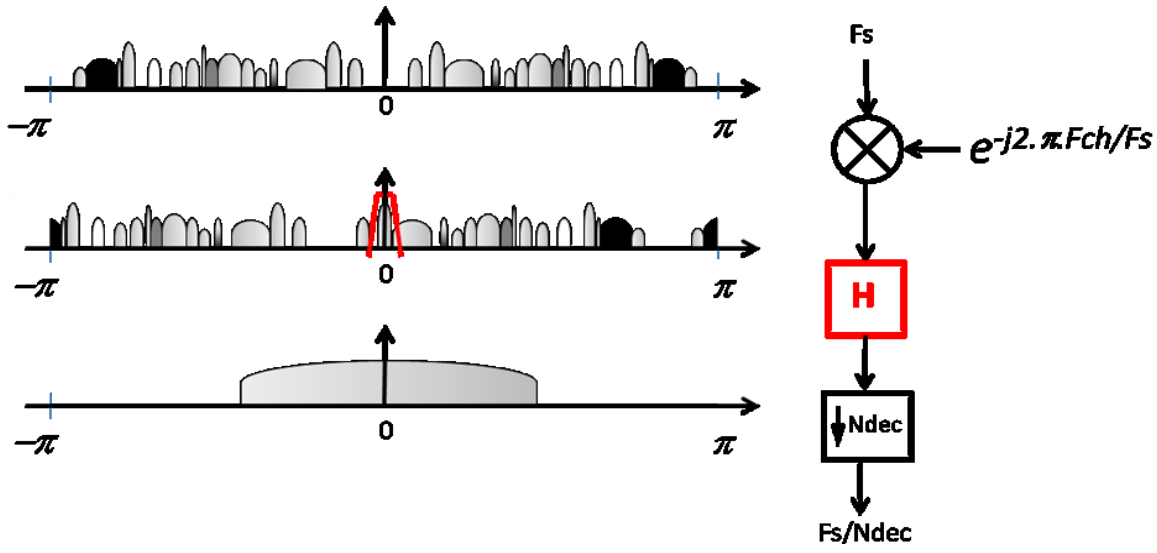


Fig 57. Digital Channel Selection process in the frequency domain

Frequency translation: translate the wanted channels to DC, using a Numerically Controlled Oscillator

Filtering: rejects the unwanted channels. The filter transfer function (H) specification is driven by several parameters:

- Gain flatness in the pass-band. Generally driven by the type of modulation, and the demodulator amplitude equalization capability.
- Phase linearity in the pass-band. Generally driven by the type of modulation, and the demodulator phase equalization capability. For instance, this might drive the choice of a FIR filter instead of an IIR filter.
- Attenuation of unwanted channels prior to sampling rate reduction, to mitigate the impact of aliasing.
- Attenuation of unwanted channels prior to signal path width reduction, to mitigate quantization noise.

Down-sampling: achieves a sampling rate reduction prior to symbol to bits conversion (channel demodulation).

High-sampling rate ADC implies a high-speed DCS, which, in case of multiple channel selection, causes high power consumption, large area, and high level of interference.

Many techniques exist for decreasing power and area of DSP blocks. Among them:

- Multi-rate DSP:
- Poly-phase implementation of decimation and interpolation filters
- CIC (Cascaded Integrator-Comb Filter) of decimation and interpolation filters
- Frequency translation:
- CORDIC algorithm ([96])

Despite these techniques, a power-and-area-efficient implementation seeks for minimum signal path width and sampling rate. In order to do so while still getting a sufficient performance, it is crucial to understand the fundamental limitations of these digital front-end designs.

Effects of coefficient quantization in FIR systems are well described in [75]. In this work, the impacts of signal path width and decimation factors on signal quality are studied, considering the general DCS depicted in Fig 56, and assuming an ideally-accurate digital down-converter.

2.2.9.1 Quantization noise

For quantization noise purpose, the diagram of Fig 56 can be simplified to Fig 58:

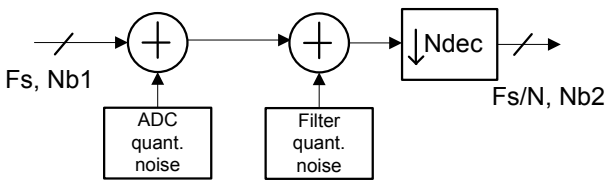


Fig 58. Noise model of a Digital Channel Selection unit

As seen in 2.2.3.4, ADC loading factor (lf), full-scale voltage (FS), and input signal RMS amplitude (σ) have the following relation-ship:

$$lf = 10^{LF/20} = \frac{\sigma}{FS/2} \tag{2.150.}$$

The integrated ADC quantization noise error can be expressed as a function of the ADC full-scale voltage and number of bits ($Nb1$):

$$\sigma_{ADC} = \frac{V_{LSB}}{\sqrt{12}} = \frac{FS \cdot 2^{-Nb1+1}}{\sqrt{12}} \tag{2.151.}$$

The ADC output noise density (Fig 59-a) can be expressed as (in V/sqrt(Hz)):

$$N_{ADC} = \frac{FS \cdot 2^{-Nb1+1}}{\sqrt{12}} \cdot \frac{1}{\sqrt{Fs/2}} = \frac{FS \cdot 2^{-Nb1+1}}{\sqrt{6 \cdot Fs}} \tag{2.152.}$$

Assuming a brick-wall digital filter with the following characteristics (Fig 59-b):

- cut-off frequency, $fc \le \frac{Fs \cdot Ndec}{2}$
- pass-gain gain = 1,
- out-of-band gain= ε, with $\varepsilon \approx 0$

As illustrated in Fig 59-c, while the signal is processed through the digital filter, the ADC output noise density is unchanged within the signal pass-band, but filtered out-of-band. Therefore,

$$N_{ADC,[0;NBW]} = \frac{FS \cdot 2^{-Nb1+1}}{\sqrt{6 \cdot Fs}} \tag{2.153.}$$

$$N_{ADC,[NBW;Fs/2]} \approx 0 \tag{2.154.}$$

The digital filter also introduces additional quantization noise, which density is a consequence of signal path width and sampling rate (Fig 59-c):

$$N_{DSP} = \frac{FS \cdot 2^{-Nb2+1}}{\sqrt{6 \cdot Fs}} \tag{2.155.}$$

Therefore, after down-sampling (sampling rate reduction by a factor $Ndec$), while ADC noise keeps unchanged within the signal BW, DSP noise increases due to aliasing (Fig 59-d). The individual integrated noises, over the channel BW (NBW) can be expressed:

$$\sigma_{ADC,[0;NBW]} = FS \cdot 2^{-Nb1+1} \cdot \sqrt{\frac{NBW}{6 \cdot Fs}} \tag{2.156.}$$

$$\sigma_{DSP,[0;NBW]} = FS \cdot 2^{-Nb2+1} \cdot \sqrt{\frac{NBW \cdot Ndec}{6 \cdot Fs}} \tag{2.157.}$$

As they are uncorrelated, the RMS amplitude of their sum is:

$$\sigma_{TOT,[0;NBW]} = \sqrt{\left(2^{-2 \cdot Nb1+2} + Ndec \cdot 2^{-2 \cdot Nb2+2}\right) \cdot \frac{NBW}{6 \cdot Fs}} \cdot FS \tag{2.158.}$$

Equivalently, the output signal-to-noise ratio can be written:

$$snr = \frac{\sigma_{SoutDec}}{\sigma_{NoutDec}} = \frac{lf \cdot \sqrt{6 \cdot Fs}}{\sqrt{NBW \cdot \left(2^{-2 \cdot Nb1+2} + Ndec \cdot 2^{-2 \cdot Nb2+2}\right)}} \tag{2.159.}$$

2.2.9.1 Summary

- For every signal path reduction by 1 bit, the DCS SNR is degraded by a factor 2.
- The DCS output noise floor increases with the square root of the decimation factor.
- In case Nb1=Nb2, and without decimation, SNR is degraded by a factor $\sqrt{2}$ compared to the noise the ADC output.

Therefore, in order to limit performance degradation due to DSP quantization:

- The number of bits through the DCS typically needs to be higher than at the ADC output,
- The number of bits needs to grow through DCS for compensating the bandwidth reduction caused by decimation.
- If digital filters provide sufficient rejection of interferers (>6 dB), a digital AGC loop can be a suitable solution for limiting the number of bits through the DCS path.

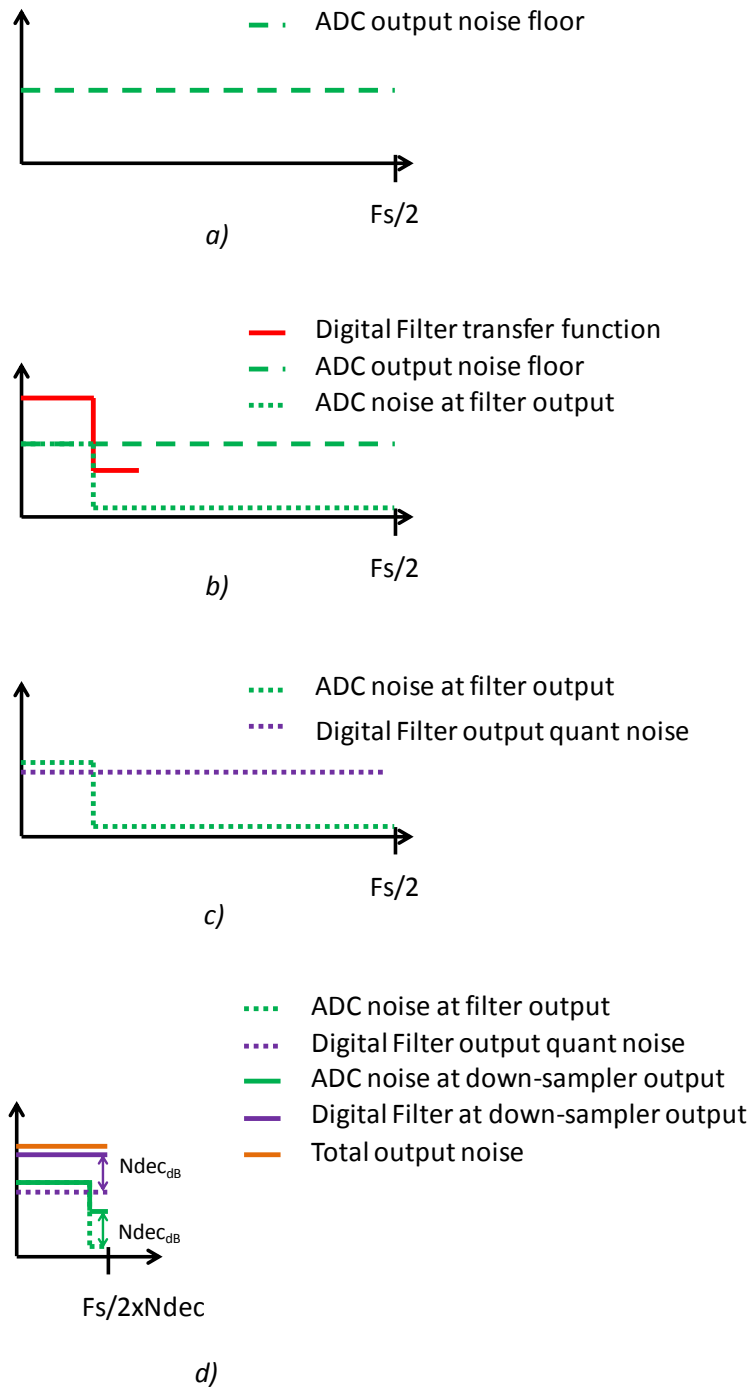


Fig 59. Impact of DSP filters and down-sampling on ADC and DSP noises

CHAPTER 3.

Application to the system design of a multi-channel cable receiver

In this chapter, the theory developed in chapter 2 is used for the system-level design of a multi-channel cable receiver. It provides an overview of the cable reception requirements, a translation of the system-level requirements to the RF receiver specifications, and presents a signal conditioning technique for relaxing the direct RF digitization receiver requirements.

3.1 Overview of the cable reception

Competition among cable operators and Telco providers is not only to provide the best networks that are capable of providing the highest data rates, but also to ensure the ability to receive huge amount of data in customer's premises equipments, at low cost and low power consumption.

Since increasing the signal quality over the cable networks is not cost-effective, increasing the data rate translates into increasing the signal bandwidth, which is implemented by transmitting several bonded RF channels. There is a wish for providing 1 Gbps per home, which necessitates the simultaneous reception of 24 RF channels.

The trend for nomadic use of the information within a home, transforms the home receiver architecture from a distributed, STBs-based, to a centralized architecture (Fig 1), articulated around a home gateway. Data is re-distributed from the gateway to clients, using either WLAN (Wifi), MoCA or PLC as a communication pipe.

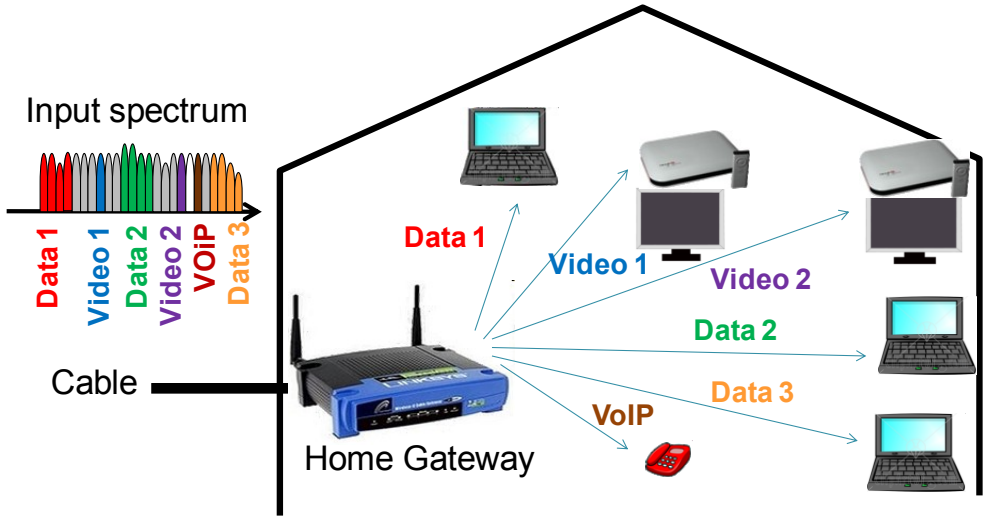


Fig 1. Centralized receiver architecture, articulated around a Home Gateway

It is therefore required to build a receiver able to capture 24 6MHz-wide channels across the cable spectrum (Fig 2).

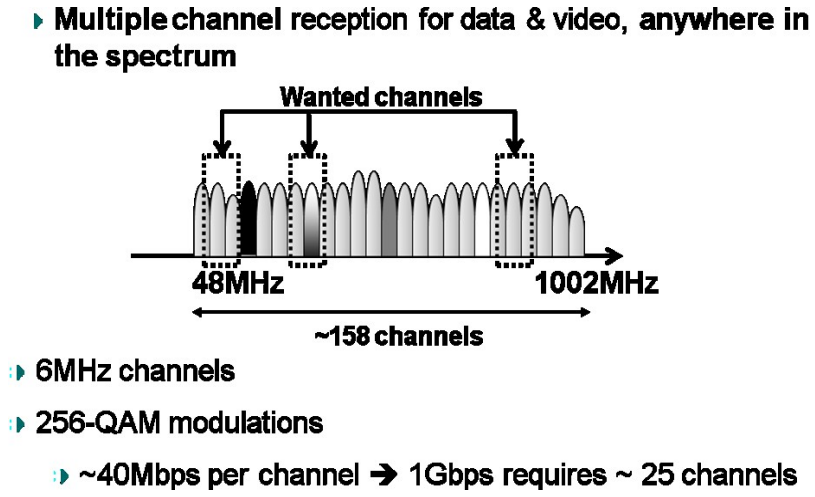


Fig 2. Typical spectrum of a digital cable network

RF front-end of current cable receivers (Fig 3) are made from a combination of single-channel tuners and wideband tuners.

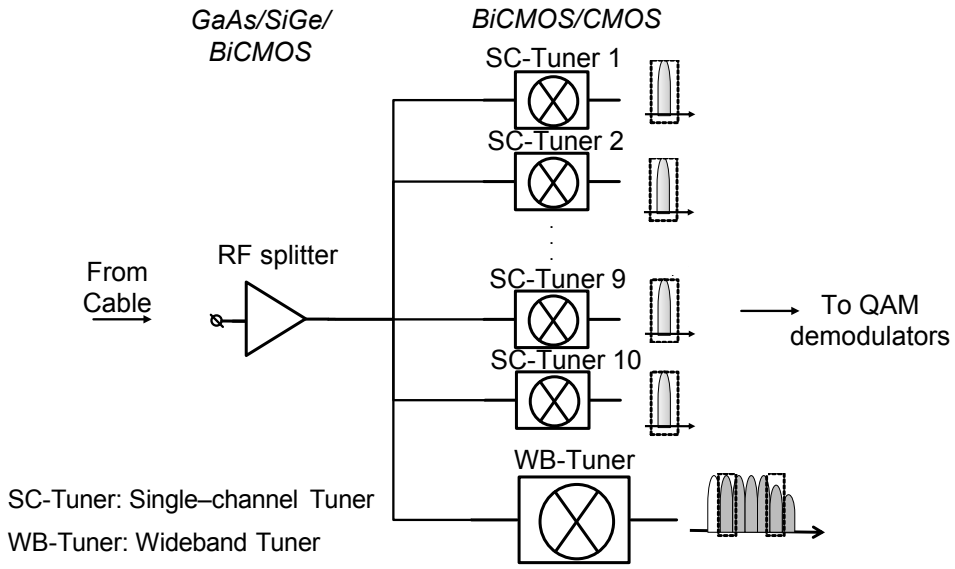


Fig 3. Silicon-Tuner-based Home Gateway front-end

Wideband tuners are more cost and power effective than single-channel tuners, but strongly limit the cable operator flexibility, since the RF channels they receive are constrained to be adjacent.

Using state-of-the-art single-channel tuner technology (average of the power consumed in [29], [33], [35]), Fig 4 shows that more than 20 W would be required for the RF receiver front-end of a multi-channel home gateway:

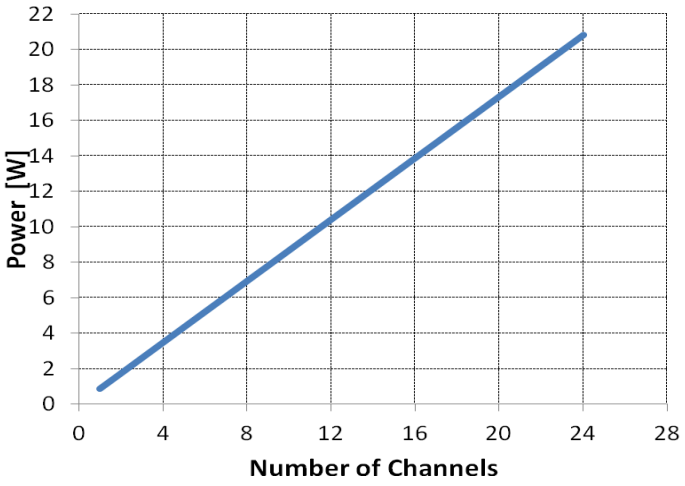


Fig 4. Power consumption of a Silicon-Tuner-based Home Gateway front-end

This analysis neglects the additional power that would be involved for splitting the input RF signal towards the multiple receivers.

Therefore, there is a strong interest for building power and cost-efficient cable receivers, able to capture a large number of independent RF channels.

In this context, a Home Gateway receiver front-end making use of a direct-sampling (Fig 5) would reduce the RF and analog hardware, and could therefore decrease the system solution cost & power consumption.

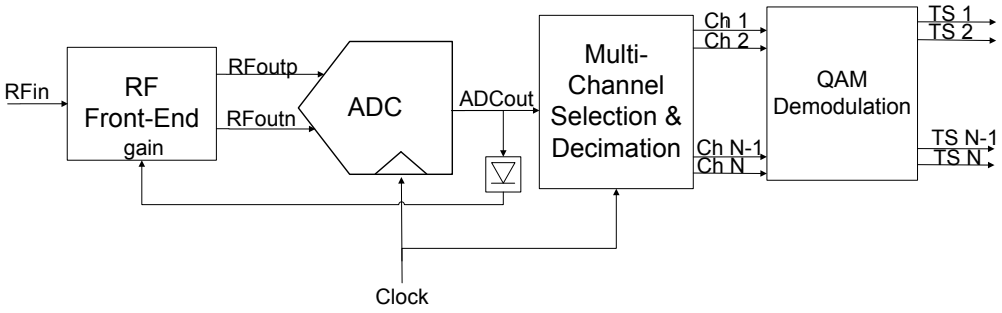


Fig 5. Direct-RF Sampling Home Gateway receiver

In addition, this highly-digitized architecture has several advantages over the mixer-based silicon tuners:

- Agility: allows for a completely flexible plan for the cable operators
- No RF mixer: no image rejection a harmonic rejection issues.
- No group delay variation: digital channel selection can be realized with linear-phase filters (FIR).
- Scalability: increasing the number of channels can be made without re-designing the RF & analog front-end. Only re-scaling the digital channel selection block is required.

3.2 Cable reception key specifications

3.2.1 Standardized requirements

Cable transmission makes use of 64-QAM and 256-QAM. Fig 6 shows the BER as a function of Es/N0 for different modulations including 64-QAM & 256-QAM

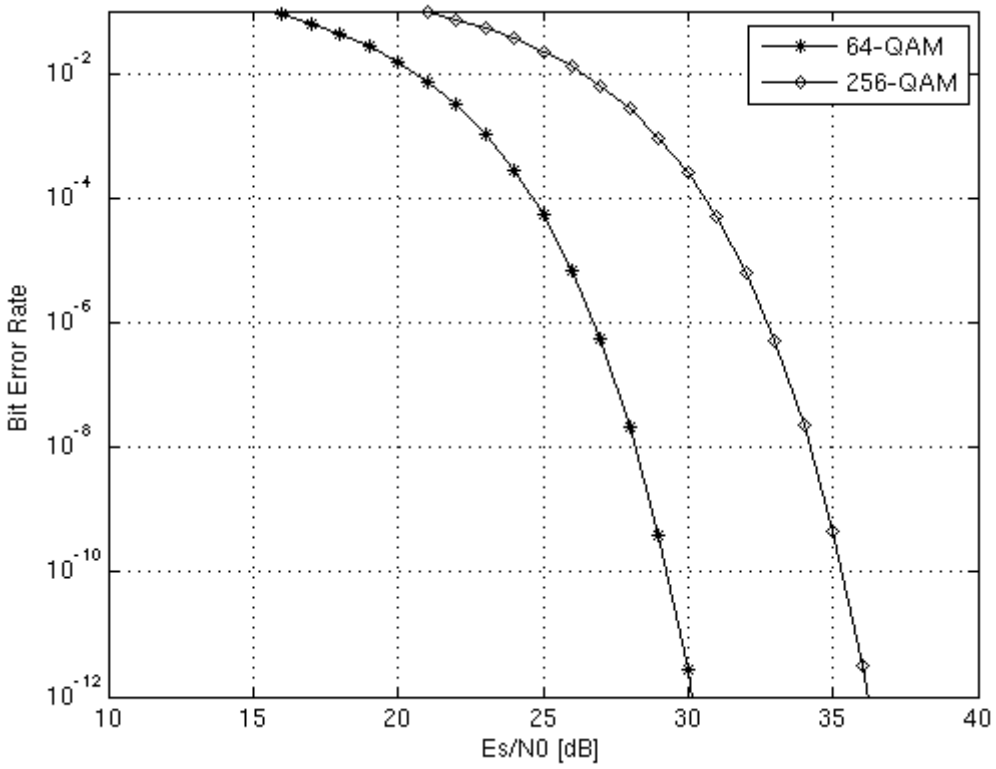


Fig 6. BER as a function of Signal-to-Noise Ratio

ITU.J83-B [67] standard allows for a residual post-FEC BER $\leq 1x10^{-11}$. The (128, 122, t = 3) Reed-Solomon coding request a pre-FEC BER $\leq 7x10^{-5}$ for getting this quasi-error-free performance level. Thanks to the additional treillis coding, a signal-to-noise ratio Es/N0 $\geq$ 28 dB is requested for 256-QAM.

DVB-C [68] targets a residual post-FEC BER $\leq 1x10^{-11}$. DVB-C FEC has a corrective capacity from $2x10^{-4}$ to $1x10^{-11}$. A signal-to-noise ratio Es/N0 $\geq$ 29.7 dB is required for receiving 256-QAM signals at quasi-error-free performance level.

The main characteristics of the RF signals transmitted over cable, and of the received signals quality are synthesized in Table 2, for different standards (DOCSIS/ EuroDOCSIS [69], [70], SCTE40 [71],).

Table 2. Down-stream cable signals characteristics

Parameter	Condition	ITUJ83.B	DVB-C	DOCSIS	SCTE40	EuroDOCSIS	Unit
Parent specification				ITUJ83.B	ITUJ83.B	DVB-C	
RF channels Freq range				108-1002	54-864	47-862	MHz
Min level per channel	64QAM			-15	-15	-17	dBmV
Min level per channel	256QAM			-15	-12	-13	dBmV
Max level per channel	64QAM			+15	+15	+13	dBmV
Max level per channel	256QAM			+15	+15	+17	dBmV
Total input power				+33		+33	dBmV
Channel bandwidth				6	6	7/8	MHz
C/(N+I)	64QAM, at tuner input				27		dB
C/(N+I)	256QAM, at tuner input				33		dB
CSO	at tuner input				-53		dBc
CTB	at tuner input				-53		dBc
Symbol rate	64QAM			5.06	5.06	6.952	Msymb/s
Symbol rate	256QAM			5.36	5.36	6.952	Msymb/s
Es/N0	required at tuner output for quasi-error-free reception with 256QAM	28	29.7				dB
BER performance	at the receiver, Post-FEC	3.00E-11	1.00E-11	1.00E-08		1.00E-08	
D/U	64QAM wanted channel			-10	-21		dB
D/U	256QAM wanted channel			-10	-11		dB
Input Return Loss	5M-1002MHz band, 75 ohms ref			>6		>6	dB
Tuner spurious emission				<-50			dBmV
Seasonal & diurnal level variation						8	dB
Tilt						+/-12	dB

DVB-C2 is the 2nd generation cable standard for Europe ([72]). DVB-C2 is not emphasized on this thesis, since the first deployment proposals which have been made, result in equivalent RF requirements as DVB-C.

3.2.2 Worst-case field test conditions

3.2.2.1 Down-stream cable test conditions

The following test conditions (Table 3 & Fig 7) are practically used by cable operators to assess the robustness of receivers. They are the heritage of a strong know-how, and deep analysis of worst-case field tests. They are used extensively though this document for specifying the receiver in order to get the right level of performance. They put more constraints on the receiver than the specified conditions provided in the previous section.

Table 3. Down-stream cable signals test patterns

Test Pattern Name	NickName	M	LvlWant @ 1GHz	Fwant	D/U with low frequency channel amplitude	D/U with high frequency channel amplitude	D/U with adjacent channel amplitude	Tilt	SNRin	Post-FEC BER	Es/N0
			[dBmv]	[MHz]	[dB]	[dB]	[dB]	[dB]	[dB]		[dB]
TP1	Sensi	256	-15	54-->1002					33	7.00E-05	28
TP2	Flat	256	-15-->+5	54-->1002	-10	-10	-10	0	33	7.00E-05	28
TP3	Tilt	256	-15-->+7	54-->1002	-10	-10	-10	-10	33	7.00E-05	28
TP4	Flat+Step	256	-15-->+5	54-->1002	-6	0	-16	0	33/30	7.00E-05	28
TP5	Flat+Step+Tilt	256	-15-->0	54-->1002	-6	0	-16	-10	33/30	7.00E-05	28

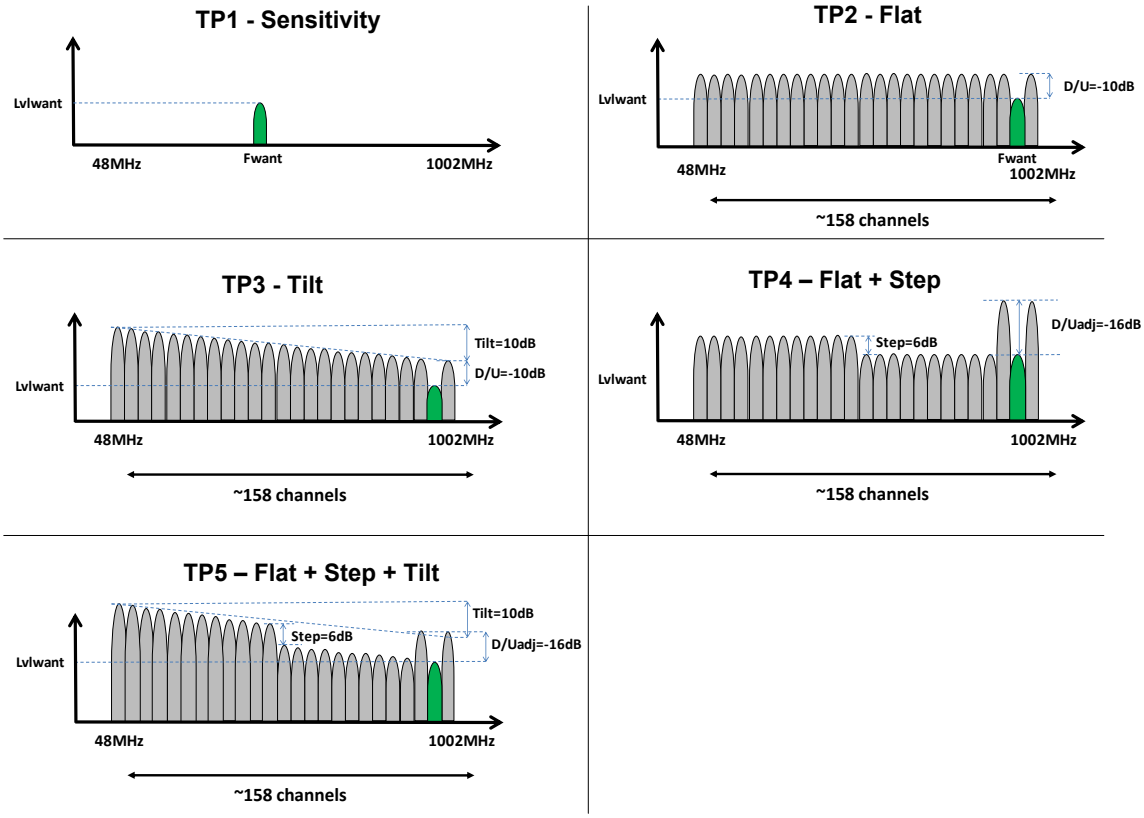


Fig 7. Cable reception Test Patterns

3.2.2.2 Coexistence with MoCA

MoCA ([73]) is a standard adopted by the Multimedia Over Coax Alliance, which defines interface specifications for a digital transport system for multimedia content over coaxial cable. It can delivers up to 500 Mbps MAC rate between 2 connected nodes. MoCA deployment requests low investment in US since 90% of the houses are already cabled.

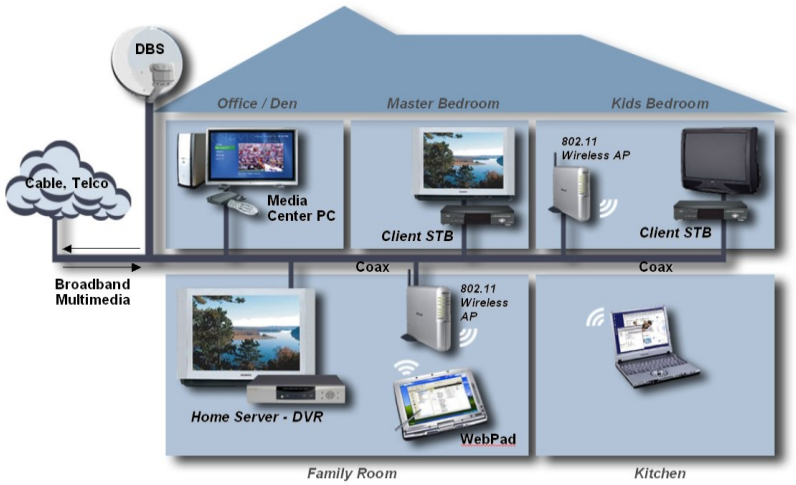


Fig 8. Home networking using MoCA

MoCA makes use of Discrete Multi-tone modulation in 50MHz/100MHz wide channels and occupies RF bands located just above the cable band (Fig 9):

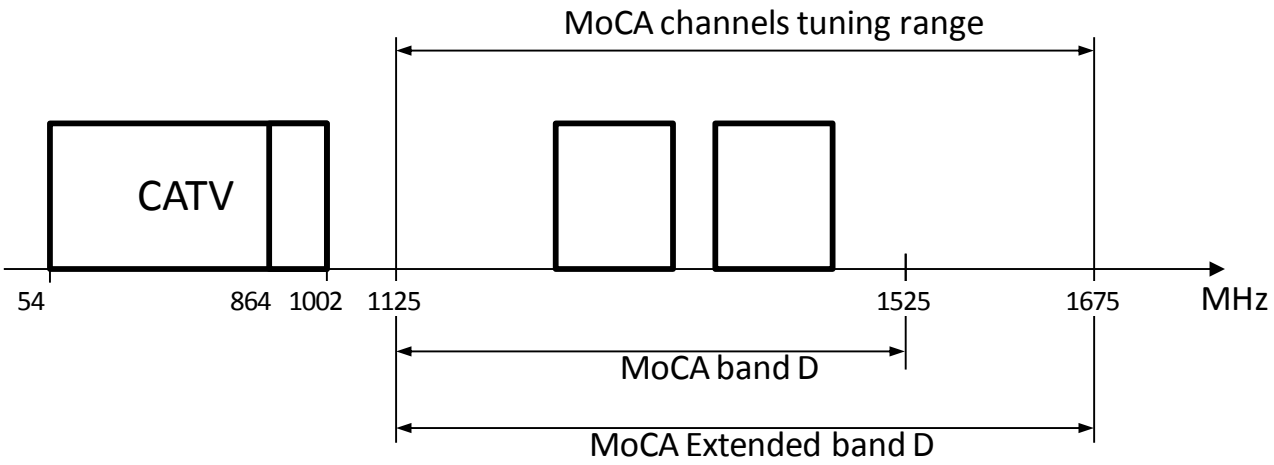


Fig 9. MoCA frequency plan

The maximum power off a transmitter is specified to be +8 dBm. The maximum power per MoCA channel perceived by a cable modem is commonly agreed to be +2 dBm. A triplexer (3-port filter) is commonly used to split the different signals (CATV D/S band, CATV U/S band, MoCA band) at the home gateway input. Still, part of the MoCA power is present at cable receiver input, due to limited attenuation of the triplexer. A realistic order of magnitude for the triplexer attenuation of MoCA is 40 dB. This brings the MoCA level at -38 dBm=+11 dBmV max at the 75Ω receiver input.

The design of the RF receiver must ensure a good reception despite the presence of a potential MoCA signal.

3.3 System design of cable multi-channel receiver

This section applies the theoretical background of chapter 2 to the system-level design cable reception. The main architecture choices are argued, and the main block specifications are calculated from the cable standards/test cases.

3.3.1 ADC sampling rate

The ADC of the direct RF sampling receiver must digitize a 1 GHz-BW signal which dictates a minimum sampling rate of 2 GHz. An additional concern is the coexistence with MoCA signals, as shown in Fig 10. The minimum sampling rate which avoids destructive aliasing can be expressed as:

$$Fs > F\max_{DS} + F\max_{MoCA}$$

Fulfilling this condition allows to greatly relaxing the anti-aliasing filter requirements.

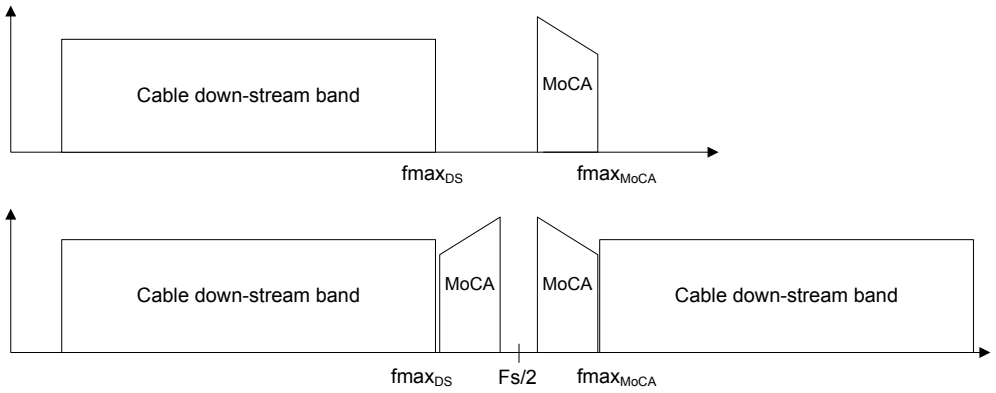


Fig 10. Aliasing of MoCA signals

Table 4. Min sampling frequency versus MoCA revision

MoCA revision	Max. MoCA Frequency	Min. Sampling rate
	[MHz]	[MHz]
1.0	1575	2577
2.0	1675	2677

This leads us to the choice of a 2.7GHz sampling frequency.

3.3.2 System-level design strategy for cable reception

Cable is an application where a large number of channels (~158) coexist on the same medium, using a FDD multiplexing technique. Hence, the ratio between wanted channel level and total input signal level is quite high. Since no aggressive RF filter can be used because the full cable band is being digitized, this leads to a highly challenging requirement on the ADC SNR.

However, the cable PSD is fairly flat, since differences in amplitude between the various channels are moderate (compared to wireless communication systems). This causes a flat non-linear distortion profile as well. In addition, the maximum input level can also been considered as medium (93 dBuV with CF=15 dB, which corresponds to a peak voltage of 0.3 Vpeak). Therefore, this leads to moderate non-linear distortion requirements on the RFFE &

ADC.

In addition, DSP techniques for equalizing time-interleaved errors and cancelling non-linear distortion errors are active research subject, while no techniques exist for cancelling broadband thermal noise.

Because of this rationale, most of the impairment budget is allocated to the ADC noise. The impairment distribution is detailed in Table 5.

SNRin refers to the SNR limitation due to the cable transmitters and network, Es/N0 is the minimum required output receiver SNR, which allows a symbol demodulation with an acceptable BER.

Preserving as much room as possible for the RFFE+ADC noise, an implementation loss (IL) is allocated to each impairment,

- RFFE+ADC+DCS noise (thermal, quantization, clipping),
- RFFE+ADC non-linear distortion (2^{nd} + 3^{rd} order),
- ADC time-interleaved mismatches (offsets, gain and time-skews),
- PLL in-band, close-in and distant phase noise,

Finally the performance provided by a receiver meeting these IL specifications is calculated (Total RX)

Table 5. Receiver impairments distribution for cable reception

				RFFE + ADC			ADC Time-interleaved errors			PLL phase noise			
SNRin	Es/N0			NOISE	CSO	CTB	TI-OFF	TI-GAIN	TI-SKEW	PN-INBAND	PN-CLOSEIN	PN-DISTANT	TOTAL RX
[dB]	[dB]	SNR	[dB]	31	45.0	45.0	45.0	45.0	45.0	45.0	45.0	45.0	28.1
33.0	28.0	IL	[dB]	3.0	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	

The minimum receiver SNR (thermal noise + quantization noise) is 31 dB, while the other impairments (non-linear distortion, ADC time-interleaved errors, PLL phase noise) have for now been equally distributed at 45dB, to ensure a total output SNR ≥ 28 dB, as requested by TP2.

3.3.3 Noise analysis

Using the theory explained in the previous chapter, the Noise Figure, which is required by the receiver is calculated for the different test conditions (NF_{RX} column in Table 6), at min/max levels and min/max frequencies.

The RFFE maximum voltage gain (Gv_{RFFE} column in Table 6), that ensures negligible clipping on the ADC, is calculated from the ADC full-scale and the total RF input level.

The next step is to make a first-order model about the RFFE noise figure: broadband tuners typically show a NF in the 3-6 dB range, at maximum gain. It is expected that our RFFE can be on the same NF range than broadband cable/terrestrial tuners. NF degradation, at low gain values, is also taken into account in our RFFE noise model (Fig 11), which is based on simulation of a 3-stage LNA cascade. RFFE NF model (NF_{RFFE} column in Table 6) is 5 dB for gains above 30 dB, and increases with a 2^{nd} order polynomial law up to 24 dB at 0 dB gain.

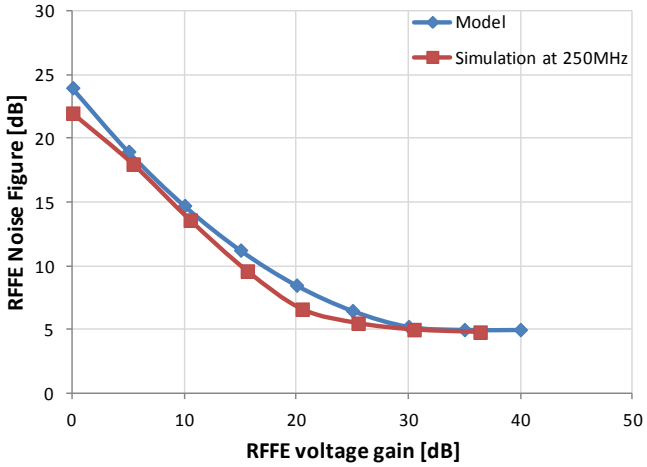


Fig 11. RFFE assumed NF versus voltage gain

The maximum ADC NF that satisfies the full receiver NF (NF_{ADC} column in Table 6) can be calculated as explained in 2.2.3.4.

Finally, the required ADC Nyquist SNR (SNR_{ADC} column in Table 6) can be deduced following 2.2.3.2 & 2.2.3.4.

Table 6. Receiver Noise Figure, and RFFE ADC requirements for meeting cable reception test conditions

Test Pattern Name	NickName	LvlWant	Fwant	Total level	SNRin	Es/N0	SNR_{RX}	IL_{NOISE}	SNR_{NOISE}	**NF_{RX}**	Gv_{RFFE} max	**NF_{RFFE}**	NF_{ADC}	**SNR_{ADC}**
		[dBmv]	[MHz]	[dBmV]	[dB]	[dB]	[dB]	[dB]		**[dB]**	[dB]	**[dB]**	[dB]	**[dB]**
TP1	Sensi	-15	1002	-15	33	28	29.7	3.0	31.0	**12.2**	56.6	**5.0**	66.6	**22.9**
TP2	Flat	-15	1002	+17	33	28	29.7	3.0	31.0	**12.2**	24.6	**6.6**	34.1	**55.4**
TP2	Flat	+5	1002	+37	33	28	29.7	3.0	31.0	**31.9**	4.6	**19.4**	35.0	**54.5**
TP3	Tilt	-5	54	+22.3	33	28	29.7	3.0	31.0	**22.0**	19.3	**8.9**	39.8	**49.7**
TP3	Tilt	-15	1002	+22.3	33	28	29.7	3.0	31.0	**12.2**	19.3	**8.9**	27.5	**61.9**
TP3	Tilt	+7	54	+34.3	33	28	29.7	3.0	31.0	**33.9**	7.3	**17.0**	39.9	**49.6**
TP3	Tilt	-3	1002	+34.3	33	28	29.7	3.0	31.0	**24.0**	7.3	**17.0**	29.0	**60.5**
TP4	Flat+Step	-15	1002	+11.5	33	28	29.7	3.0	31.0	**12.2**	30.1	**5.2**	40.0	**49.4**
TP4	Flat+Step	+5	1002	+31.5	30	28	32.3	3.0	31.0	**31.9**	10.1	**14.7**	40.7	**48.8**
TP5	Flat+Step+Tilt	-5	54	+17.6	33	28	29.7	3.0	31.0	**22.0**	24.0	**6.8**	44.5	**44.9**
TP5	Flat+Step+Tilt	-15	1002	+17.6	33	28	29.7	3.0	31.0	**12.2**	24.0	**6.8**	33.4	**56.1**
TP5	Flat+Step+Tilt	10	54	+32.6	30	28	32.3	3.0	31.0	**36.9**	9.0	**15.6**	44.6	**44.9**
TP5	Flat+Step+Tilt	0	1002	+32.6	30	28	32.3	3.0	31.0	**26.9**	9.0	**15.6**	34.3	**55.2**

Few conclusions can be drawn from the results of Table 6. The tests can be classified in the decreasing order of difficulty:

- TP3 & TP5 (Tilt, Tilt+Step) are the most stringent tests:
  - Because of the cable tilt, reception of high-frequency channels requires a 2.7 GSps ADC with 62 dB Nyquist SNR
  - RFFE noise is negligible compared to ADC noise: $NF_{RFFE} << NF_{RX} \rightarrow F_{RX} \approx 1 + \frac{(F_{ADC} - 1)}{Gp_{RFFE}}$
- TP2 (Flat) is the 3rd most difficult test:
  - It requests an ADC with ~55 dB Nyquist SNR, independently of the channel frequency

- RFFE noise is much lower than ADC noise

- TP1 (sensitivity) is the easiest test.

The toughest ADC specification (SNR>62 dB) is due to the tilt on the cable. This SNR specification is very challenging when associated with a 2.7 GS/s (1.3). Therefore, it would be highly desirable to reduce this requirement.

3.3.4 RF tilt equalizer impact on noise

Fig 12 (top) illustrates the introduction of white noise (quantization, thermal), caused by A/D conversion, on a tilted RF signal: very good performance is achieved at low frequency thanks to strong-amplitude channels, when poor performance is achieved at high frequencies due to weak-amplitude channels. The difference in performance (SNR) between low and high-frequency channels is equal to the cable tilt (Tilt=10 dB in TC2).

Fig 12 (bottom) shows the positive effect that a TEQ (RF tilt equalizer) can have: as the signal amplitude is now equalized prior to the main noise source introduction, the performance (SNR) is now flat against frequency.

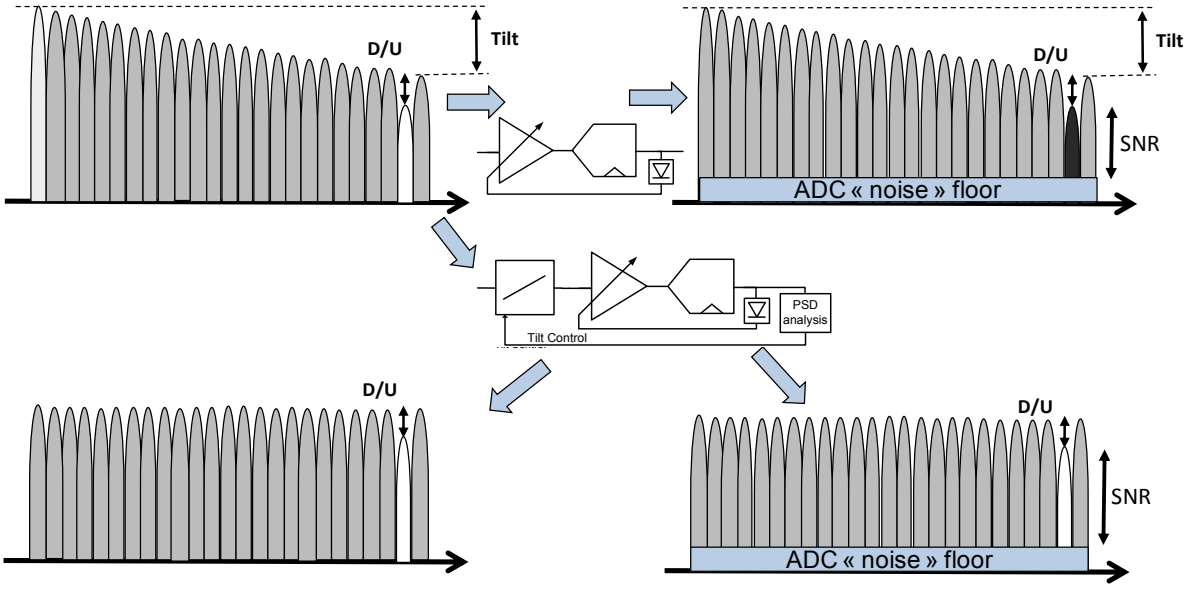


Fig 12. Receiver without Tilt Equalizer (top), Receiver with Tilt Equalizer (bottom)

In case of a constant-over-frequency input signal, its RMS can be expressed as:

$$\sigma in_{Flat}^{\ 2} = \int_{f\min}^{f\max} vdens_{Flat}^{\ 2} \cdot df = vdens_{Flat}^{\ 2} \cdot \int_{f\min}^{f\max} df = vdens_{Flat}^{\ 2} \cdot [f\max - f\min] \quad (3.1.)$$

The RMS amplitude of a tilted signal, in case of a linear-in-dB tilt, can be expressed as:

$$\sigma in_{Tilt}^{\ 2} = \int_{f\min}^{f\max} vdens_{Tilt}^{\ 2} \cdot df \quad (3.2.)$$

With

$$vdens_{Tilt}(f) = 10^{\frac{\alpha \cdot f + \beta}{20}} \quad (3.3.)$$

Where α is the tilt slope, and β is the voltage spectral density at fmin.

Because of the AGC loop that ensures optimum loading of the ADC, both RMS amplitudes of composite flat (with TEQ) and composite tilted signals (without TEQ) are equal at the ADC input.

$$\sigma in_{Tilt}^{\ 2} = \sigma in_{Flat}^{\ 2} \quad (3.4.)$$

The gain in SNR performance offered by a TEQ is the difference (in dB) between high-frequency channel amplitude with and without TEQ. This is illustrated in Fig 13 (left) with -10 dB tilt example, and quantified as a function of the tilt amplitude in Fig 13 (right).

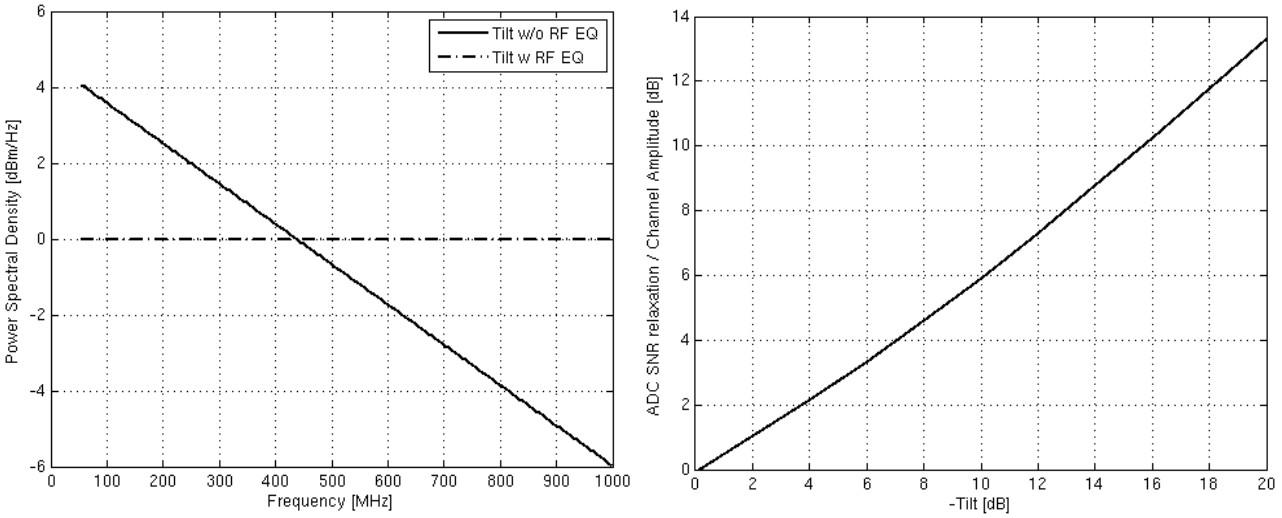


Fig 13. Channels amplitude w/wo RF tilt equalizer (left, -10dB tilt), ADC SNR relaxation with an RF tilt equalizer (right)

Therefore, the use of a TEQ can relax the ADC SNR requirement by 6 dB if -10 dB tilt is applied (1 bit relaxation on ENOB), or 13 dB if -20 dB is applied (>2 bits relaxation on ENOB), assuming an ideal RFFE, clock, DSP, and perfect TEQ transfer functions

Alternatively, with a constant ADC SNR, a TEQ can improve high-frequency channel SNR by 6 dB when -10 dB tilt is applied, 13 dB when -20 dB tilt is applied.

The different test patterns can be revisited including a TEQ with the following properties:

- Variable-slope (from 0 dB to 20 dB, continuously): the TEQ perfectly cancels the cable tilt for each condition (0 dB in TP1, TP2, TP4; +10 dB in TP3 & TP5).
- Passive network: it reduces the strong channels.
- 0 dB of loss is assumed at high frequencies.
- Located in front of the RFFE, with NF=0 dB (no noise)

In such a case, TP3 become identical to TP2, TP5 becomes identical to TP4.

The most stringent test condition (with respect to ADC noise) becomes TP2, because it has the maximum difference (in dB) between wanted channel level (-15 dBmV) and total input signal level (+17 dBmV). TP2 requests:

SNR_{ADC}>=55.4 dB with Fclk=2.7 GS/s.

This specification is still very tough and ahead of the current state-of-the-art. Therefore, the system design strategy should push the other impairment low enough so that they only contribute for a small part in the receiver equivalent NF. In this way, the final SNR_{ADC} will be close from the estimate made on this section.

TP2 is used through the next section as the worst-case scenario.

3.3.5 RFFE Gain range

Flat test conditions (TP2 & TP4)

Referring to Table 6, the required RFFE gain range that is required for passing the different flat test patterns:

4 dB < Gv_{RFFE_FLAT} <=30 dB

Sensitivity test condition (TP1)

The RFFE gain, which is required in Table 6 for driving the ADC to its full-scale under the sensitivity test, should not be taken as a real constraint. As the ADC noise specification is dictated by the most difficult test conditions, SNR_{ADC} will be >50 dB. In such a case, the receiver NF is limited by the RFFE NF ($F_{RX} \approx F_{RFFE}$) under the sensitivity test. Still, RFFE gain can be reduced while still meeting the specification with comfortable margin. Fig 14 shows the receiver NF dependence on RFFE voltage gain, assuming an ADC with 54.5 dB SNR:

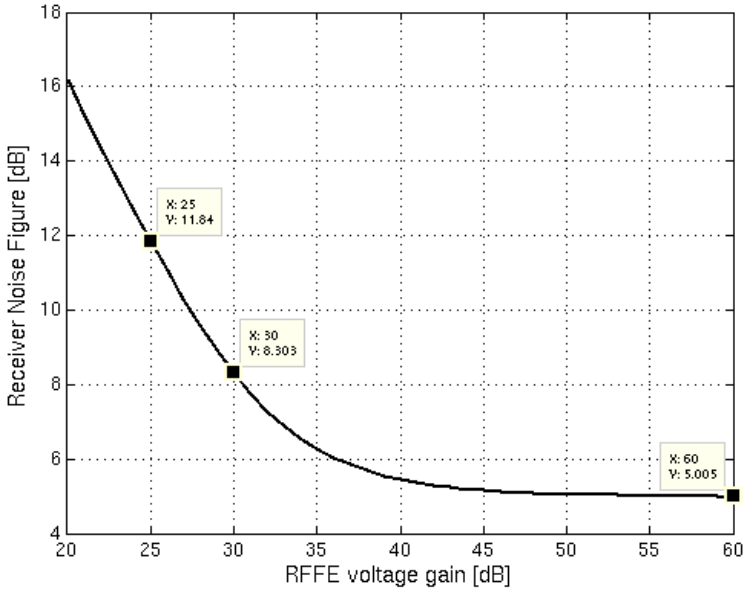


Fig 14. RFFE gain impact on Noise Figure

An RFFE gain around 30 dB is sufficient for meeting the receiver NF that is required (NF_{RX}<12.2 dB) to pass the sensitivity test with a safe margin. In this case, the ADC is driven well below its full-scale voltage.

Tilted test condition (TP3 & TP5)

In case TP3 is passed through an ideal equalizer (0 dB loss), the amplitude of the low-frequency channels are attenuated and become as low as the amplitude of the high-frequency channels. Therefore, after ideal RF tilt equalizer, TP3 becomes similar to TP2, and no additional gain is necessary in theory.

Practically, a passive RF equalizer will probably exhibit several dB losses (2-3 dB). The RFFE maximum gain should

include these losses.

4 dB <= G_{VRFFE} <= 33 dB

The AGC loop, required to control the RFFE gain against amplitude variations on the cable, will be detailed in CHAPTER 4.

3.3.6 Non-linear distortion analysis

The receiver is making use of a lowpass 1st order sampling strategy. Therefore, most of the RFFE non-linear distortion tones fall in-band.

The receiver non-linear distortion specification must be elaborated at maximum input power (TP2 with +15 dBmV/tone). In such a case, both CSO and CTB must contribute a SNR>45 dB. As the wanted channel is 10 dB below the other channels, CSO>54 dB & CTB>54 dB. Using the theory developed in 2.2.5.2 & 2.2.5.3, the required IIP2 and IIP3 can be found to be:

IIP2>=92 dBmV, IIP3>65.5 dBmV

A time-domain simulation with several trials and random phases allows checking the theoretical link between IP3/IP2 and CTB/CSO. With TP2 conditions (Flat test pattern) with 158 tones at +15 dBmV, IIP2=92 dBmV, IIP3=65 dBmV, the resulting 2nd and 3rd order broadband distortions are (Fig 15, left), which matches theory within 1 dB:

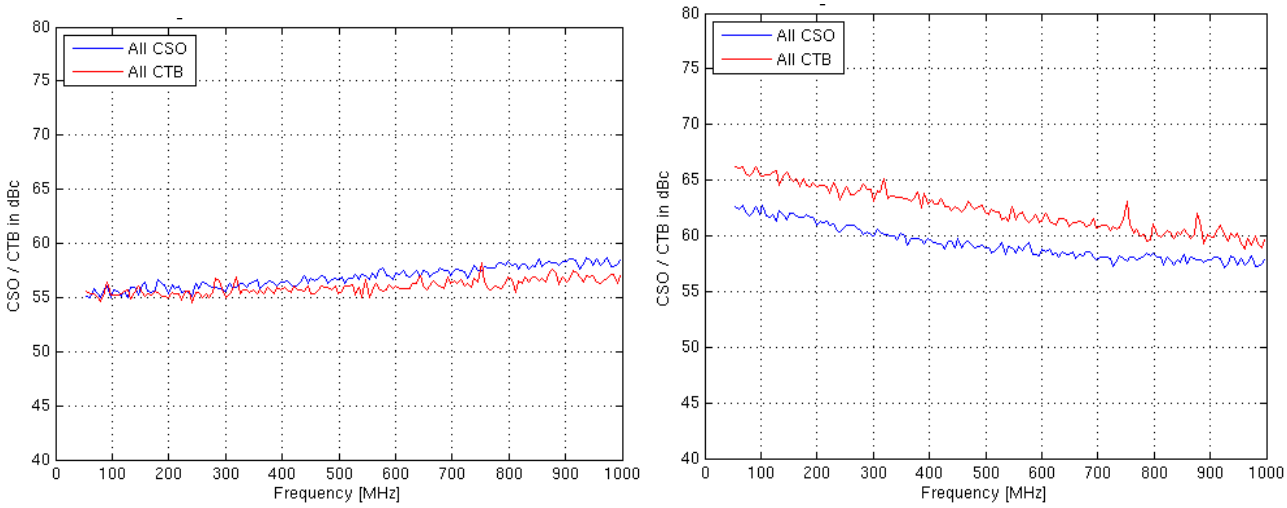


Fig 15. 2nd and 3rd order non-linear distortion with TP2, 158 tones, +15dBmV/tone

The reported CSO and CTB are referenced to the +15 dBmV tones.

Fig 15 (right) reports a non-linear distortion time-domain simulation with TP3. As -10 dB tilt is applied to the cable, the receiver input signal has a lower power than with TP1. That is the reason for the better distortion results.

3.3.7 Anti-aliasing filter

3.3.7.1 Anti-aliasing filter specification

The RFFE should protect the receiver from any unwanted signal that is generated inside the cable network (thermal noise, non-linear distortion).

For instance, the noise floor could be severely degraded by aliasing of wideband input noise. This degradation factor can be expressed as a function of AAF noise bandwidth (AAF_{BW}) and sampling clock frequency (Fs).

$$\Gamma_{AlNoise} = 10 \cdot \log_{10}\left(\frac{AAF_{BW}}{2 \cdot Fs}\right), \text{ for } Fs > AAF_{BW} \tag{3.5.}$$

This case can be illustrated with Test Pattern 4 at high levels (Lvlwant=+15 dBmV): the input signal-to-noise ratio is SNRin=30 dB, when the required output SNR Es/N0 ≥ 28 dB.

If the AAF noise bandwidth equals to Fs, the noise degradation is 3 dB, so the output SNR (SNRout) is already limited to 27 dB, which is already lower than the required Es/N0.

Allowing the aliasing to cause a maximum degradation of the input SNR (SNRin) of 0.1 dB, the required anti-aliasing attenuation must be:

Stop band attenuation<-16.4 dB at the aliasing frequency, which is:

$$Falias = Fadc - Fcable_{MAX} \tag{3.6.}$$

with $Fadc$ =2700 MHz, $Fcable_{MAX}$ =1002 Mz, $Falias$ =1698 MHz

Additionally, any RF wireless signal (above 1698 MHz) which might be coupled into the cable, non-linear distortion generated in the network or inside the RFFE itself, will also benefit from this attenuation.

3.3.7.2 Anti-aliasing filter characteristics choice

As the filter should minimize the attenuation of down-stream cable channels, while maximizing attenuation at 1698 MHz, a filter prototype with steep transfer function is seeked. For these requirements, Elliptic approximation is well suited, as it provides the best falloff rate in the transition band. Still the in-band ripple must be minimized.

The filter requirements are:

In-band ripple<=0.2 dB

Stop-band ripple<=-20 dB

Fig 16 shows the transfer function modulus for different elliptic filter orders, together with the required specification:

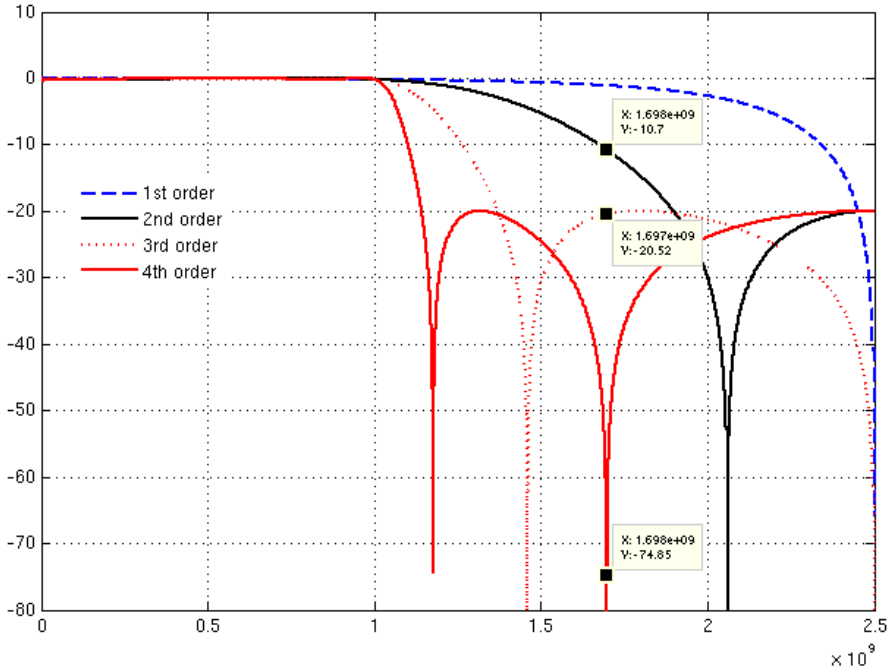


Fig 16. Transfer function modulus of Elliptic filter for several orders

A 3rd order elliptic filter can meet our specification with safe margin.

3.3.8 Time-Interleaved ADC specification

As fully detailed in [86], the converter TH has been chosen to be four-time interleaved (Fig 17), in order to reduce the speed of the individual THs by four. As discussed in section 1.3.5, this allows preserving a relatively low input capacitance, so a high input signal BW, keeping manageable the system complexity, hence the time-interleaving gain and clock mismatches.

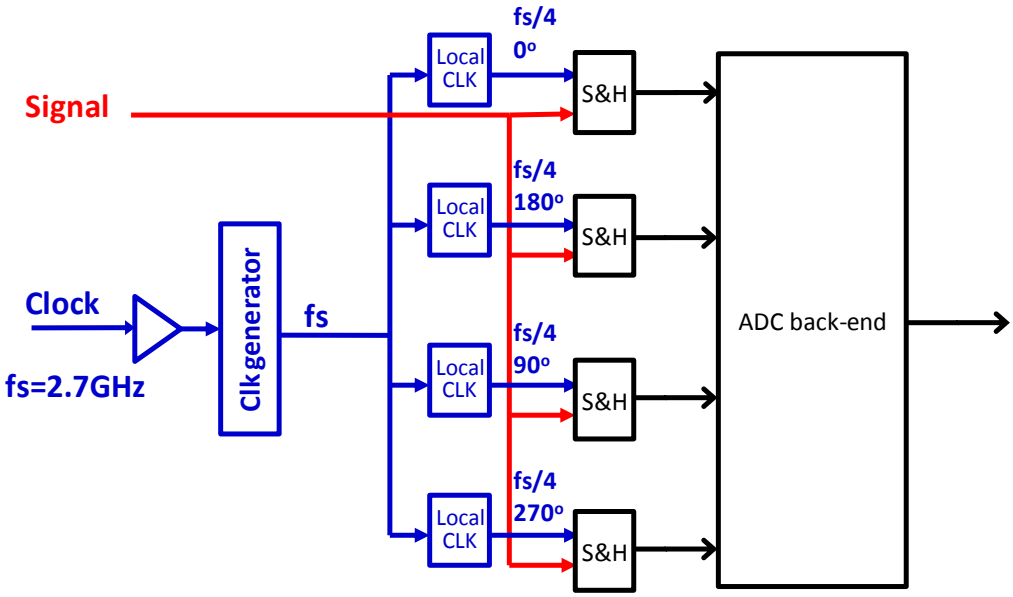


Fig 17. ADC high-level architecture

The next sections calculate the channel matching requirements, and compare the theory to the results of a time-domain simulation model.

3.3.8.1 TH Offset-mismatch specification

In case an RF channel around Fs/4 needs to be received, the offset mismatch standard deviation needs to be low enough: using the method explained in 2.2.7.1, the offset-mismatch SFDR can be specified in order to have an SNR channel contribution ≤ 45 dB (as specified in Table 5). For this purpose, the Nyquist-SFDR caused by offset mismatch must be ≥ 88 dB.

The required offset mismatch standard deviation, which provides an average Nyquist-SFDR ≥ 88 dB, can be calculated to be: $\sigma_{off} \leq 20$ uV. Still, targeting 90% of the samples to pass this specification, $\sigma_{off} \leq 7$ uV is required.

Fig 18 shows the simulation results of this Fs/4 offset spur amplitude for $\sigma_{off} = 7$ uV, over 1500 trials, with a single input CW at 673 MHz:

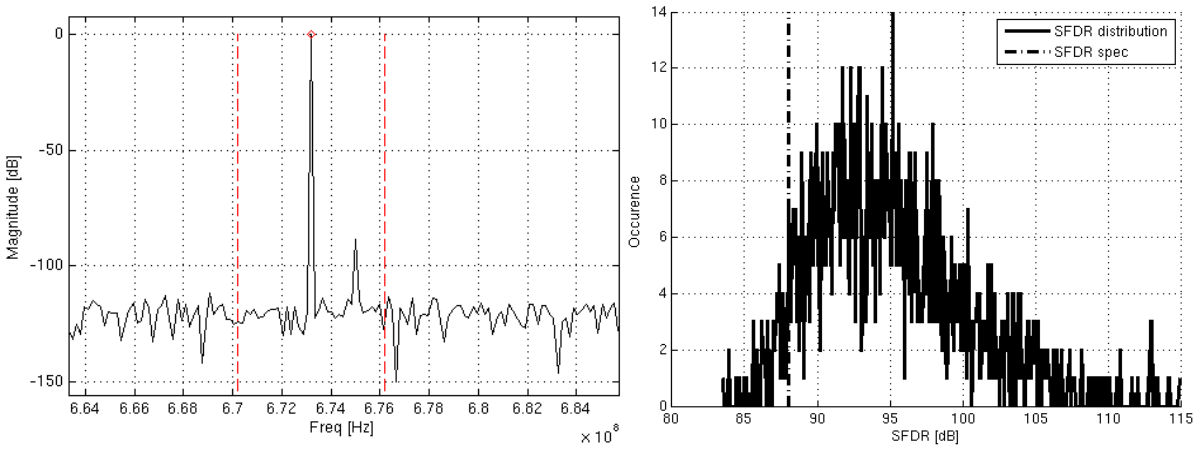


Fig 18. TD simulation of offset mismatch, σ_{off}=7uV. Left: zoom at Fs/4 on ADC output spectrum, right: SFDRFS/4 distribution

3.3.8.2 TH Gain-mismatch specification

Gain mismatch will cause signal images to appear within the cable band (Fin +/- Fs/4). As the cable channels PSD is fairly flat, this impairment will be perceived as white Gaussian noise. Given the 45 dB specification of Table 5 under the TP2 test condition, and using 2.2.7.2, the standard deviation of the gain mismatch can be specified to be:

$$\sigma_{gain} \leq 2.3 \cdot 10^{-3}$$

Targeting 90% of the samples to pass this specification: $\sigma_{gain} \geq 0.9 \cdot 10^{-3}$.

Fig 19 shows the simulation result of the per-channel SNDR with TP2 test condition, for $\sigma_{gain} = 0.9 \cdot 10^{-3}$, over 1500 trials.

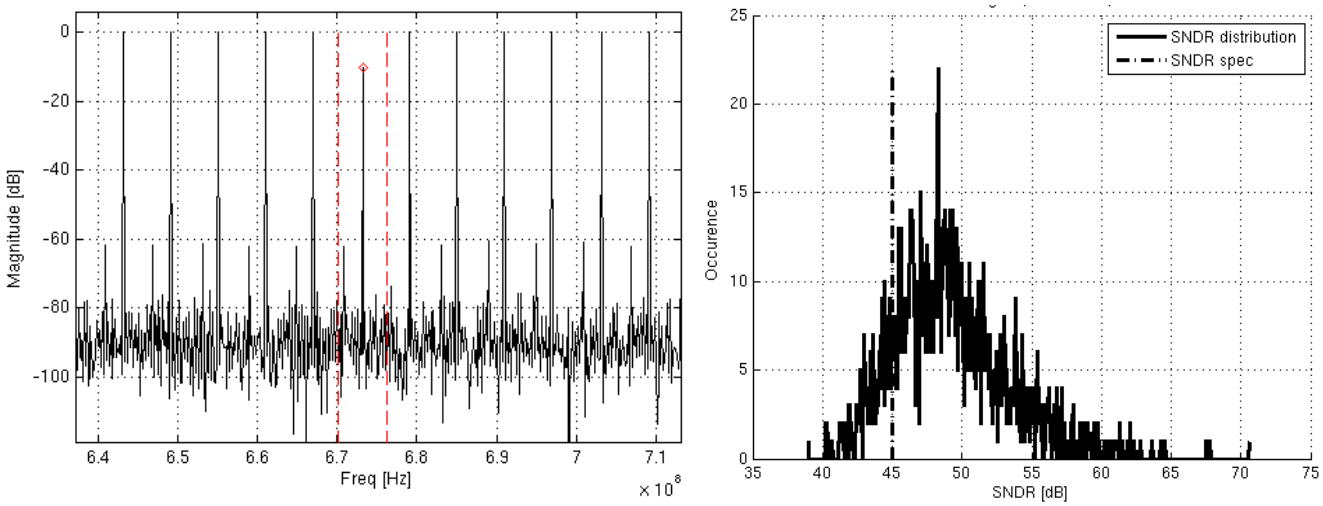


Fig 19. TD simulation with gain mismatch, σ_{gain}=0.9x10^{-3}, Left: zoom on ADC output spectrum, right: per channel-SNDR distribution

The biggest amplitude tones in Fig 19 (left) are the input channels (x158), and the smaller tones are the images caused by gain mismatch.

3.3.8.3 TH time skew-mismatch & BW mismatch specification

Given the 45 dB specification of Table 5, and using 2.2.7.3, the required standard deviation of the time-skew mismatch is:

$$\sigma_{skew} \leq 0.2 \text{ ps}$$

As the error is frequency-dependent, it is mandatory to perform simulations. Fig 20 shows the simulation result of the per-channel SNDR with TP2 test condition time-skew, for $\sigma_{skew} = 0.2$ ps, over 1500 trials, at the worst-case RF frequency:

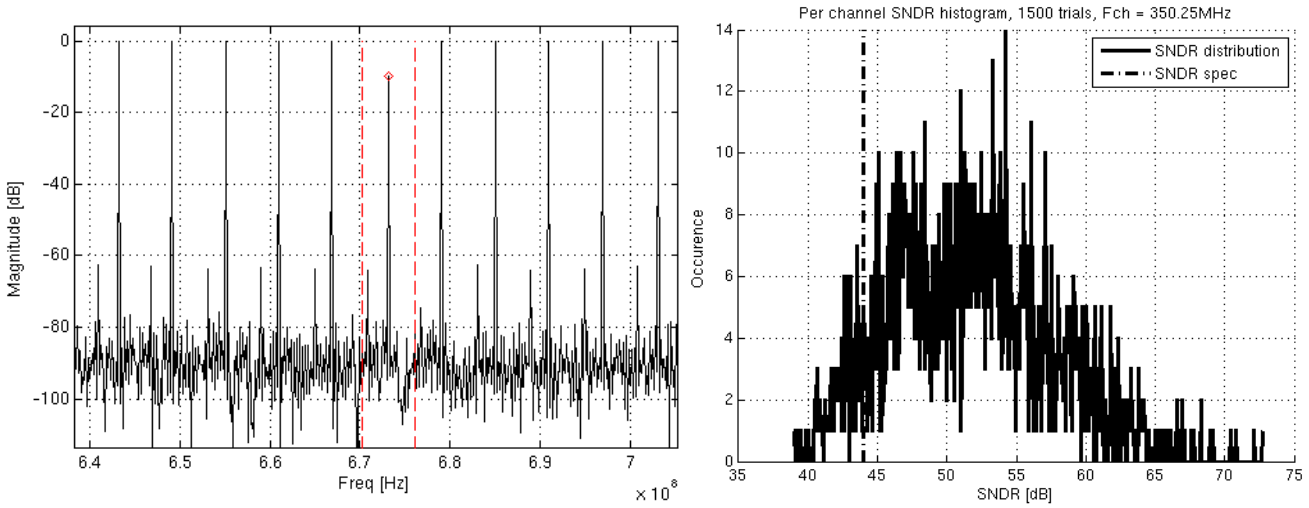


Fig 20. Time-skew mismatch and per-channel SNDR for TP2, σ_{skew}=0.2 ps

With this time skew requirement, 90% of the IC samples meet the 45 dB SNDR requirement per channel. This implicitly means that the remaining 10% of samples are allowed to degrade system performance by slightly more than 0.1 dB, which is considered to be acceptable. As explained in 2.2.7.4, if significant transfer function mismatch is expected, the total phase mismatch budget needs to be shared between time-skew mismatch & transfer function

mismatch.

3.3.9 Sampling clock specification

Sampling clock quality can be specified using the theory developed in 2.2.8. A time-domain ADC model including phase noise has been developed for checking the calculated specifications across all test scenarios.

Specifically, in this section, in-band, close-in and distant phase noise will be specified. This theoretical analysis is compared to the time-domain simulations results.

3.3.9.1 In-band phase noise

The maximum integrated phase noise for receiving 256-QAM with an IL of 0.1 dB is extrapolated to 0.25 °RMS from Fig 51 (chapter 2). Transfer of phase noise from clock to sampled signal is proportional to the ratio of frequency between input signal and clock. Therefore, the worst-case for in-band phase noise is the reception of a 1 GHz channel. This requires a clock with an integrated phase noise $\sigma_{IPN} \leq 0.675$ °RMS. The integration band should be between the cut-off frequency of the QAM demodulator carrier recovery loop (few tens of kHz), and half of the symbol BW (5.36 MHz/2=2.68 MHz). This is equivalent to $\sigma_{tjit} \leq 0.7$ ps time jitter.

3.3.9.2 Close-in phase noise

In these conditions, both adjacent channels (N-1, N+1) are +16 dB above the wanted channel. As these are extreme cases, 0.2 dB of IL is allocated to close-in phase noise in these situations ($SNR_{CLOSEIN} \geq 42.5$ dB). Assuming a flat phase noise density over the integration bandwidth, and using section 2.2.8.2 (D/U=16 dB+3 dB for accounting for both adjacent channels), the required close-in phase noise can be determined to be $Sn_{dBc/Hz}$<=-120 dBc/Hz in the frequency range [+6 MHz-2.68 MHz; +6 MHz+2.68 MHz]. This causes an integrated time jitter=0.2 ps; Fig 21 shows the result of a single-channel simulation with $Sn_{dBc/Hz}$ =-120 dBc/Hz. The SNR is calculated by integrating the noise over the adjacent (N-1) channel BW:

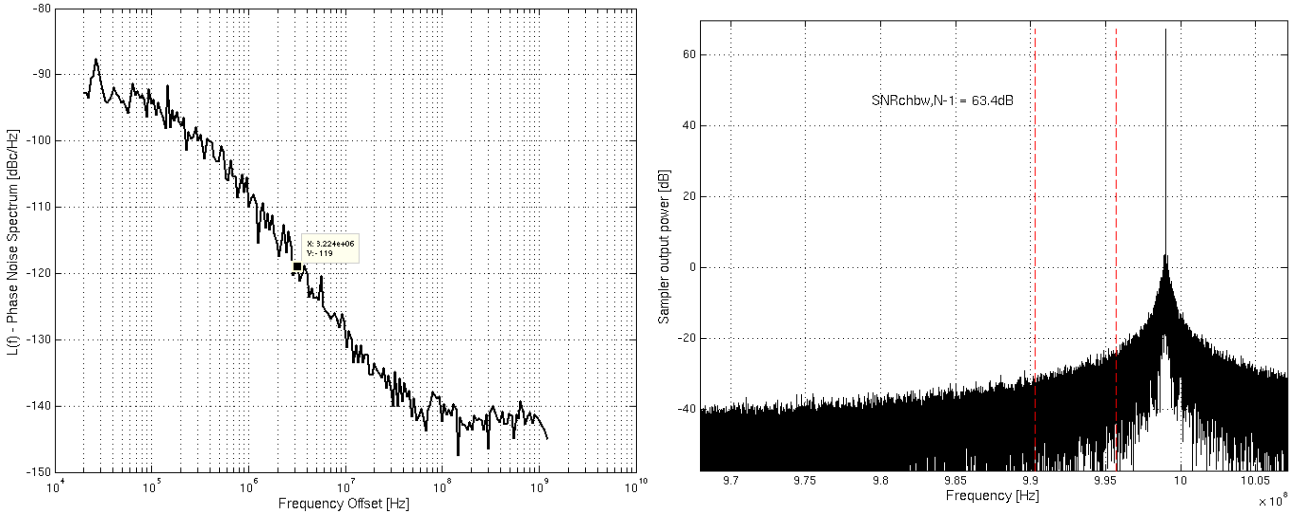


Fig 21. Simulation of close-in phase noise. Left: PLL phase noise density, middle: PLL integrated time jitter, right: sampler output spectrum with a single channel

The simulation reports an SNR of 63 dB, referenced to the adjacent channel level. Since the wanted channel is 16 dB below the adjacent channels in TP4, and since two adjacent channels will be present instead of one, $SNR_{CLOSEIN}$ =64-16-3=44 dB. The small difference (~1.5 dB), compared to theory, is due to the fact that phase noise is not flat across the integration BW.

3.3.9.3 Distant phase noise

Assuming the reception of TP2 with the presence of a maximum-power MoCA channel at 1675 MHz (cf 3.2.2.2, +2 dBm-40 dB attenuation in the triplexer=-38 dBm=+11 dBmV over 50 MHz at receiver input), for specifying distant phase noise, equations in 2.2.8.2 can be numerically evaluated or simulated. Calculations show that $\sigma_{jitt} \leq 0.35$ ps are required to meet the 45 dB per-channel SNR. These calculations are confirmed by the simulation results in Fig 22. The top-left part shows the phase noise density profile which has been used for the simulation (-139 dBc/Hz). The top-right part shows the equivalent integrated time jitter noise ($\sigma_{jitt} = 0.35$ ps). The bottom part shows the sampler output spectrum, including MoCA carriers after non-destructive aliasing:

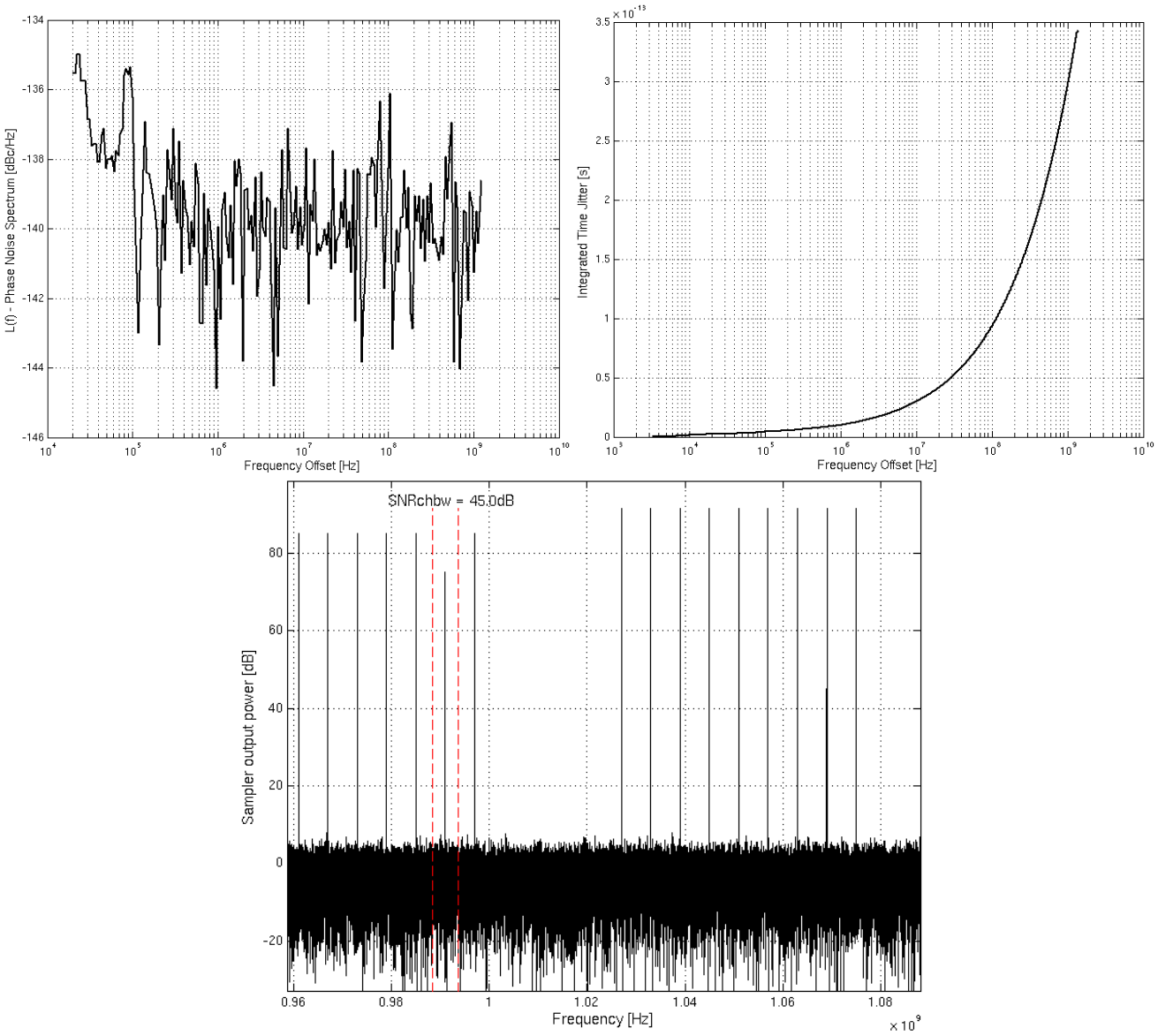


Fig 22. Simulation of distant phase noise. Top left: PLL phase noise density. Top right: PLL integrated time jitter. Bottom: sampler output spectrum with test condition TP2

As the simulation frequency is equal to the ADC sampling rate, it only represents phase noise in the interval [0; 2.7 GHz/2] and does not provision for distant phase noise aliasing. Therefore the distant phase noise specification must include the degradation factor due to broad-band phase noise aliasing (cf 2.2.8.2). Assuming an 8 GHz clock path BW, the phase noise degradation factor is:

$$ClkBWFactor = 3 \cdot \log_2 \left(\frac{8GHz}{\frac{2.7GHz}{2}} \right) = 7.7dB$$

Therefore the required distant phase noise density is -146.7 dBc/Hz.

3.3.9.4 Overall phase noise specification

Finally the phase noise can be fully specified as a function of the frequency offset. In order to let the PLL BW as a degree of freedom during the sub-blocks design, the most generic approach is to specify the integrated time jitter. Fig 23 provides the integrated time jitter specification for a 2.7 GHz clock used in a direct RF sampling cable receiver:

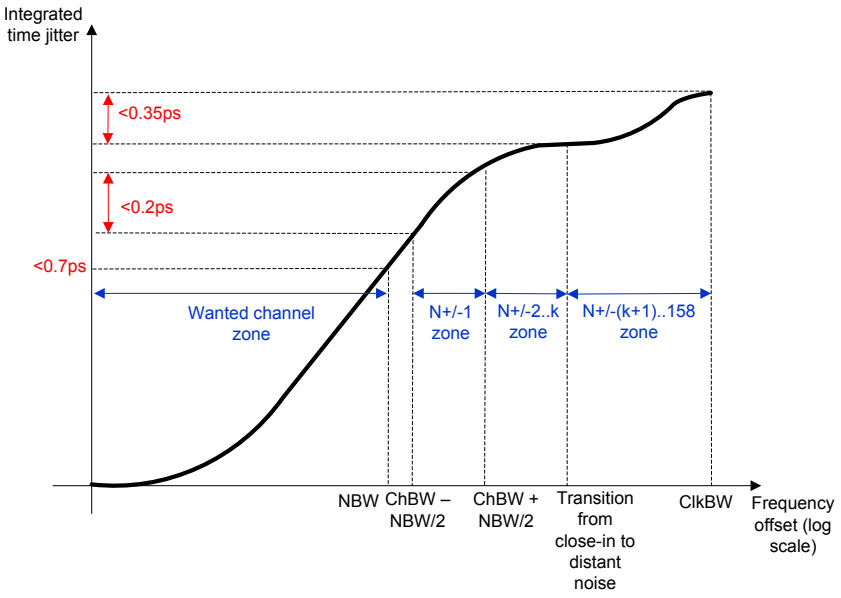


Fig 23. Clock phase noise specification for cable reception

ChBW: channel BW (6 MHz)

NBW: noise BW (= symbol rate = 5.36 MHz)

k+1: index of the 1st channel lying on the distant phase noise region.

This can also be converted to SSB phase noise density using the formula of Fig 47.

3.4 Summary

This chapter has specified the full signal chain. It provided an RF front-end signal conditioning technique that allowed reducing the noise requirements on the ADC.

RFFE gain, ADC noise, ADC time-interleaved impairments, PLL phase noise have been quantitatively specified, complementing the framework provided in CHAPTER 2 with time-domain system simulations.

CHAPTER 4.

Realization & measurements

This chapter takes the step from the system definition to silicon implementation and testing.

The cable multi-channel receiver is implemented with a two-die approach, in order to achieve good signal integrity:

- The RF Front-End (RFFE) processes the sensitive low-level single-ended input signal using the high-performance 0.25um BiCMOS process [98]. It provides gain and amplitude equalization over the 50-1002 MHz input band.
- The Mixed-Signal Front-End (MSFE) samples the differential input signal, quantifies it, and achieves digital channel selection of 24x 6/8 MHz-wide channels using a 65nm CMOS process.

The system solution combines a down-stream multi-channel path, a down-stream single-channel path, and an up-stream path (Fig 1).

This chapter focuses on the down-stream wideband path of Fig 1, and is organized as follows:

- Section 4 & 4.2 present the design & IC-level measurement results of the RFFE/MSFE respectively.
- Section 4.3 and 4.4 provide the concepts of the MSAGC loop and the tilt equalizer algorithm.
- Finally, section 4.5 shows some system-level measurement results.

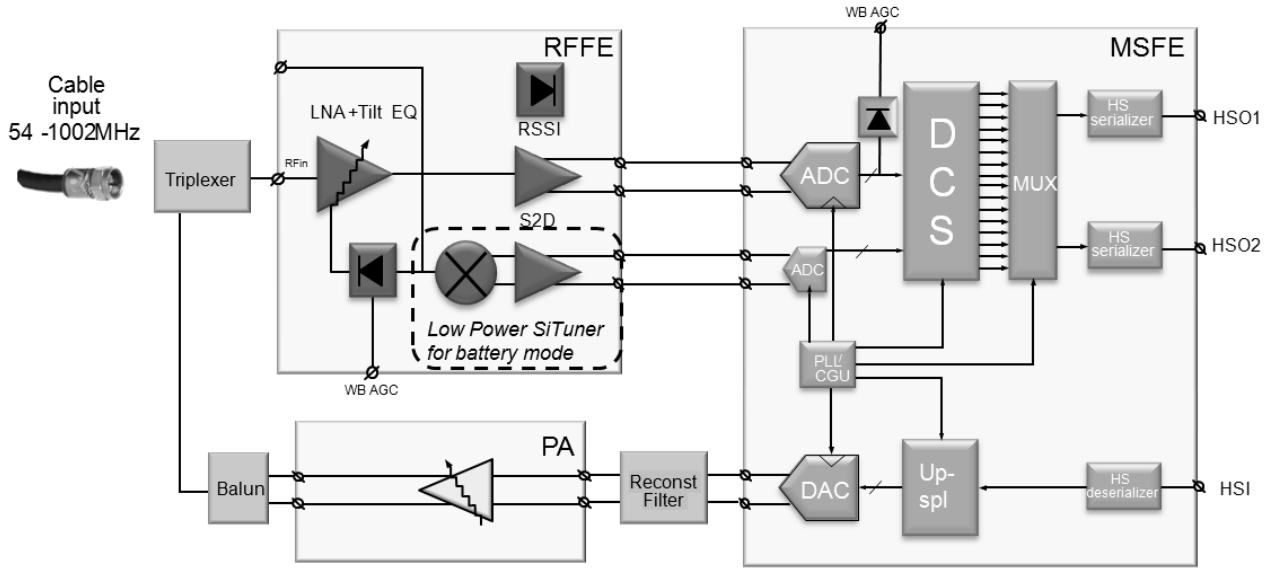


Fig 1. Cable multi-channel receiver system block diagram

4.1 RF front-end

As fully detailed in [97], the RFFE includes a wideband path for multi-channel reception, combined with a single-channel tuner path for power-optimized single-channel reception. The focus on this chapter has been maintained on the wideband path.

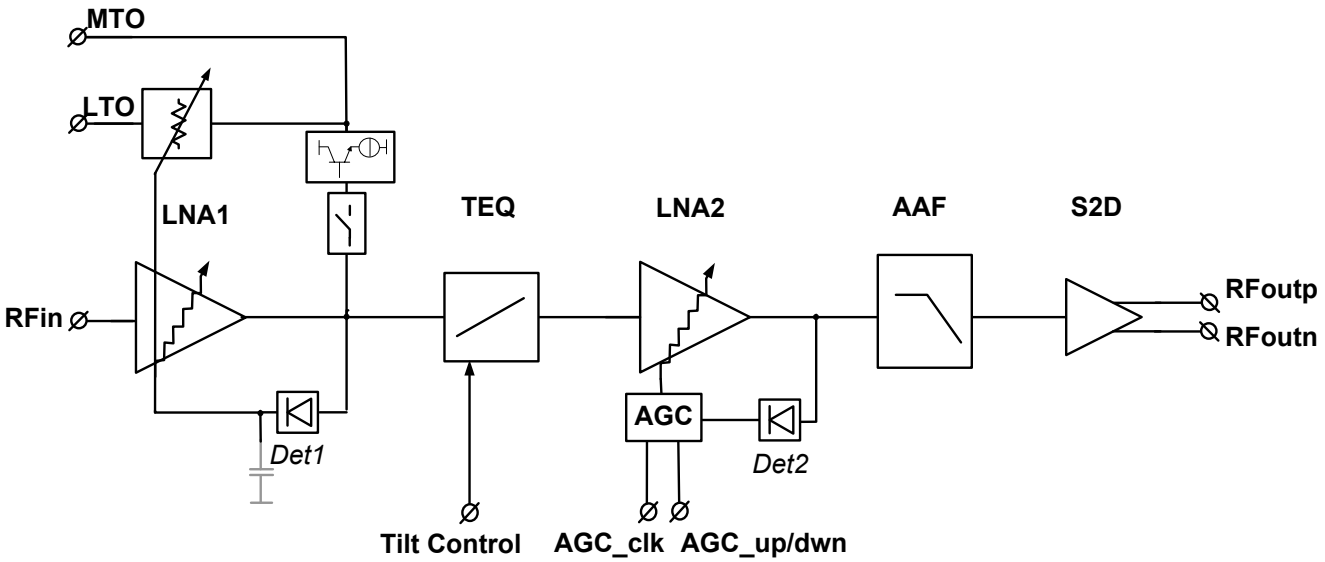


Fig 2. Wideband path of the RFFE IC block diagram

Main choices:

- A single-ended input and RF path have been chosen for avoiding the cost of an external balun, minimizing the cost of internal filters (RF tilt equalizer, AAF), and minimizing power consumption.
- As tilt equalization is not only beneficial for the ADC, but also for RF blocks, TEQ has been placed as closed as possible from the cable input.
- All blocks located between AAF and ADC cause aliasing of noise & non-linear distortion. This motivated the

choice to place the AAF as closed as possible to the ADC input. Still the willing to provide a well-matched RF interface between RFFE and ADC dictated to place it in front of the differential buffer.

The first block of the RF front-end (Fig 2, [97]) is an 18 dB-gain-range LNA (LNA1) for handling part of the input level dynamics from -15 dBmV to +15 dBmV per channel. The LNA has an autonomous AGC loop in order to provide the best NF/linearity trade-off against cable input level changes. LNA1 gain transitions are seamless to preserve the high-level constellation demodulator from amplitude steps. This LNA also serves as an RF splitter for additional tuners or equipments (MTO and LTO outputs).

After signal amplification to a level of +35 dBmV, a passive fully integrated tilt equalizer shapes the input signal to obtain flat amplitude across frequency, observed at the ADC output. Seven correction steps are available from -10 dB to +15 dB amplitude equalization. The 2nd LNA amplifies the signal after tilt correction with a dynamic from -12 dB to +15 dB, with 0.2 dB steps. Its gain is controlled either from an RMS detector located at LNA2 output (Det2 in Fig 2) or from a mixed-signal control loop which detector is connected to the ADC output.

The 3rd order elliptic fully-integrated anti-aliasing filter rejects the potential aliases caused by out-of-band noise and non-linear distortion. The last stage achieves single-to-differential conversion and impedance matching between the RF front-end and the 100 Ω differential ADC input.

The full receiver reports its gain with +/-2 dB absolute accuracy and +/-0.5 dB relative accuracy.

4.1.1 Low-noise amplifier

LNA1 (Fig 3) is a single-ended inverting amplifier with resistive feedback [99], which provides -8 dB input return loss across 50 MHz-1 GHz. It is implemented as a stepped-gain amplifier in order to provide excellent noise figure (NF<3.8 dB) and linearity performance (CSO/CTB > 60 dB). Its ramp-controlled signals applied on triode-mode MOS ensure a smooth gain transitions between 2 consecutive gain settings. A programmable gain derivative (dg/dt) from =0.1 dB/ms to 2 dB/ms is achieved ensuring no picture degradation. This LNA topology combines benefits of both stepped and continuous LNAs.

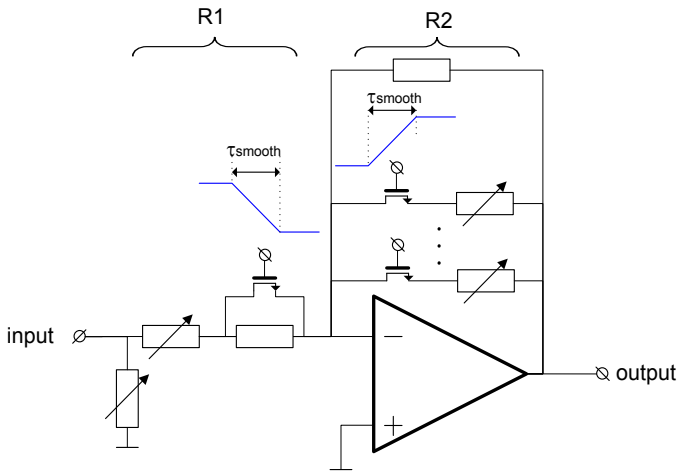


Fig 3. Pseudo-continuous LNA principle diagram

4.1.2 RF Tilt Equalizer Design

The problematic of tilt correction has also been an active research topic on the CATV infrastructure industry. Indeed some tilt equalization solutions have been implemented to cancel the tilt of the infrastructure amplifiers. Discrete solutions of T-bridge LC-based variable tilt equalizer (TEQ) able to correct up to 550 MHz have been proposed in [100] and [101]. Reference [100] corrects for positive tilts only, while [101] corrects for both positive

and negative tilts, but is based on 2 LC resonators (Fig 4).

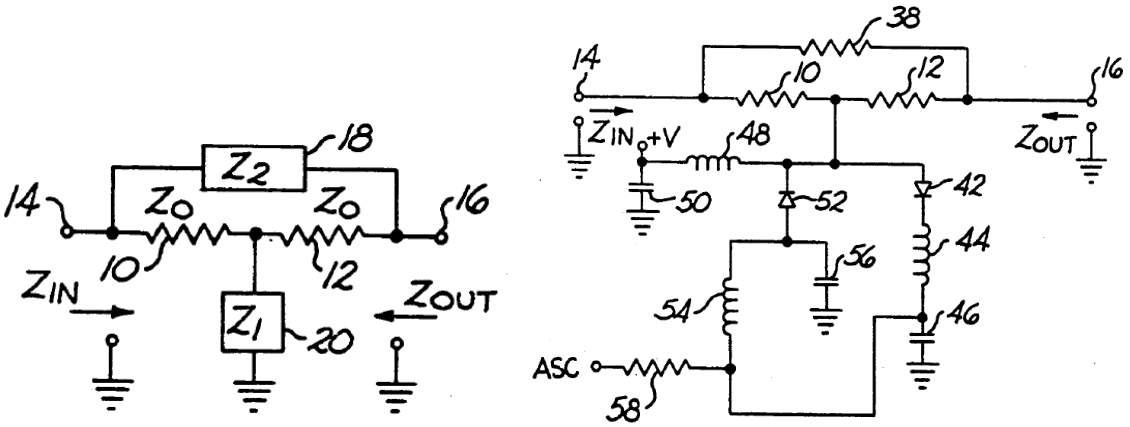


Fig 4. Tilt equalizer state-of-the-art for cable infrastructure

The equalizer concept of Fig 4 is based on the combination of a parallel and series LC resonators for correcting positive and negative slopes, which are coupled to the cable using a T-bridge configuration, in order to control the input and output return losses.

In the selected topology, described in the patent [102], and shown in Fig 5, the fully-integrated variable tilt equalizer uses a single 5 nH inductor configured either in a series or a parallel resonator, and equalizes over a 1 GHz bandwidth.

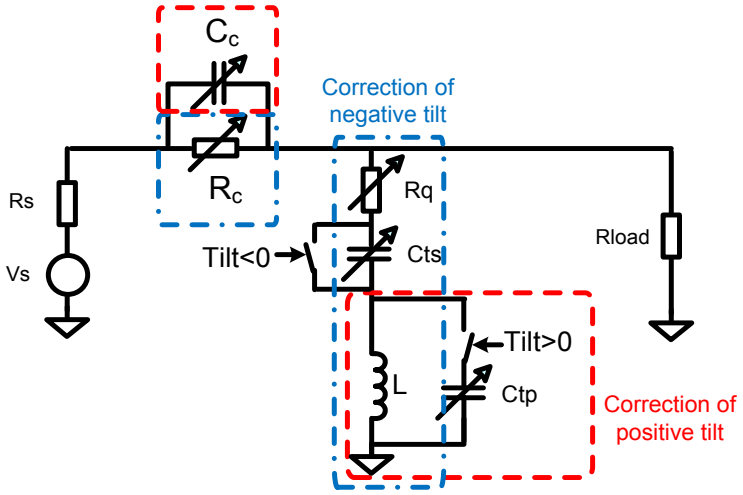


Fig 5. Tilt equalizer topology

In both configurations, the LC circuit resonates at 1.1 GHz. When configured in parallel (L, Ctp in Fig 6), the equalizer attenuates low frequencies (high-pass behaviour). When configured in series (L, Cts in Fig 7), the equalizer attenuates the high frequencies (lowpass behaviour).

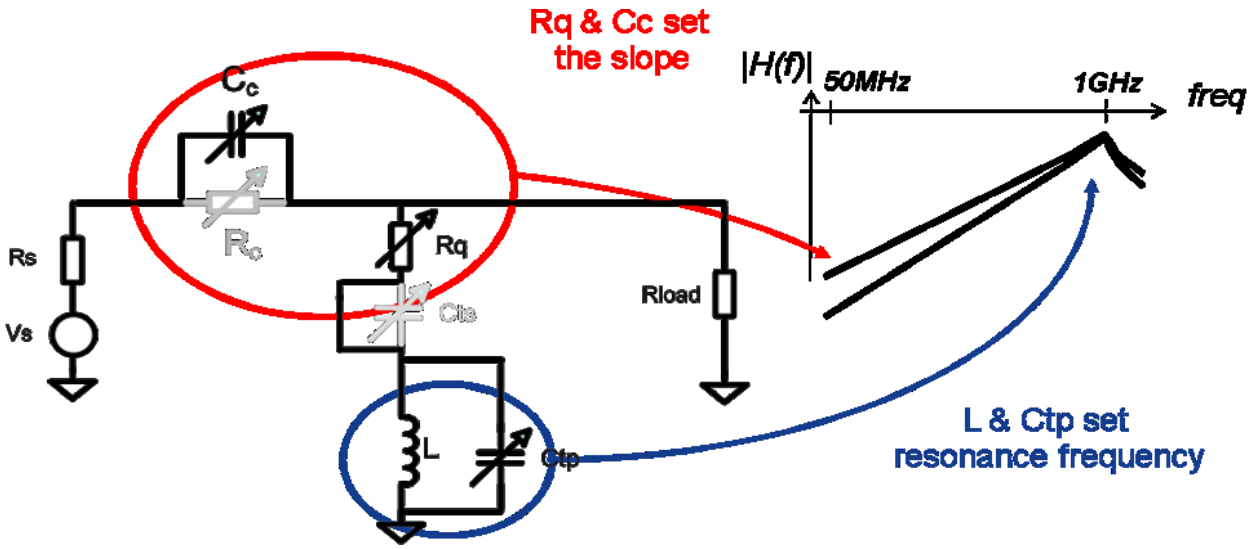


Fig 6. Tilt equalizer configured as a parallel resonator

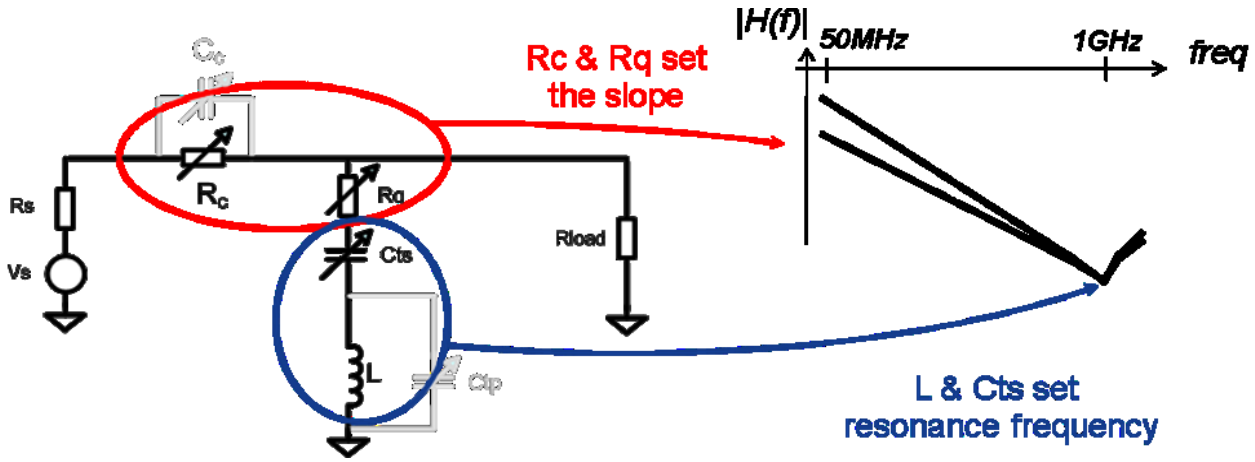


Fig 7. Tilt equalizer configured as a series resonator

The tilt equalizer programmability is achieved using variable components (Rc, Cc, Rq, Cts and Ctp). For this purpose, capacitor and resistor banks are designed (Fig 8).

This also offers the possibility to improve the tilt equalizer flatness over frequency, since the variable passive components are optimized for each tilt equalizer setting. Seven tilt equalizer settings are designed:

- 15 dB/ 10 dB / 5 dB / 3 dB high-pass behaviour (to cancel a lowpass cable behaviour)
- 5 dB / 10 dB lowpass behaviour (to cancel a high-pass cable behaviour)

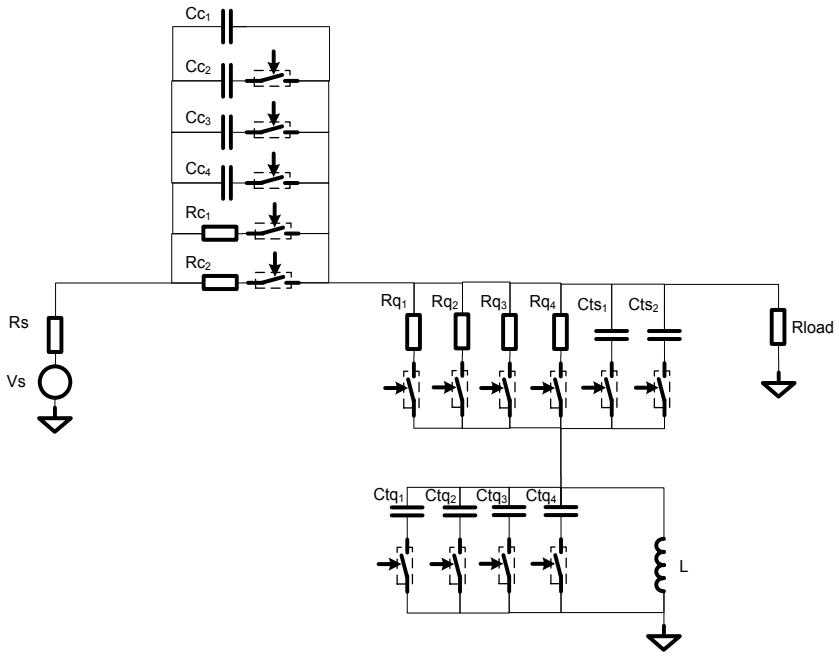


Fig 8. Programmable tilt equalizer principle diagram

The tilt equalizer has also a by-pass option in case the cable is relatively flat.

4.1.2.1 Capacitor and resistor arrays

If the multiple passive components and switches were designed using simple NMOS transistor driven by a ground/VCC gate voltage, the tilt equalizer would exhibit a too high non-linear distortion, because of:

- non-linear Ron of MOS transistor in triode region (Vgs signal modulation, Vt modulated by Vsb)
- parasitic MOS non-linear junction capacitors (Csb, Cdb).

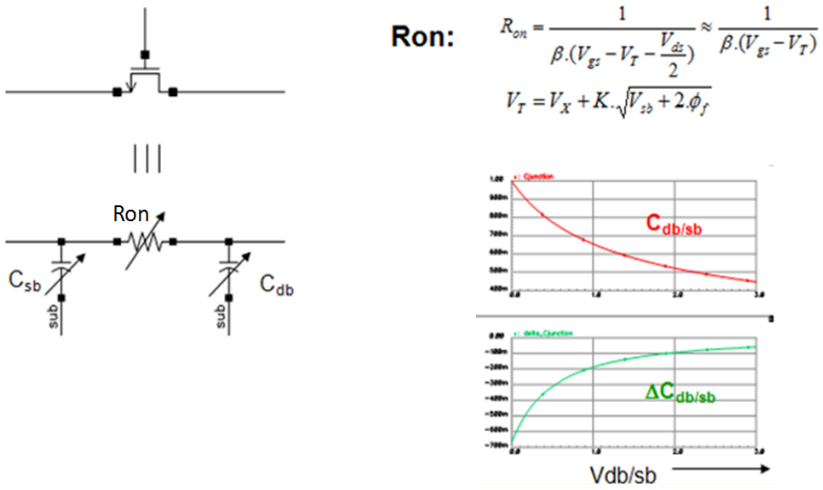


Fig 9. Non-linear Ron and junction capacitances in a MOS transistor in triode mode

To mitigate these effects, special care has been taken on RF switches design to ensure high linearity.

The MOS switches use a triple-well architecture, as shown in Fig 10 (left): this allows connecting the MOS source to the N-well (Buried N layer), so Vsb=0, which cancels the MOS channel resistance (Ron) dependence on the source voltage (Vsb=0).

The use of a boot-strap capacitor (C29 through M26 in Fig 10, right) allows reducing the switch Vgs dependence on the input signal. This leads to a more linear MOS channel resistance (Ron).

In addition, high-voltage drain biasing has been used to reduce the voltage dependency of parasitic capacitors (drain to bulk capacitance) of off-state MOS transistors. This is achieved by M0 in Fig 10 (right).

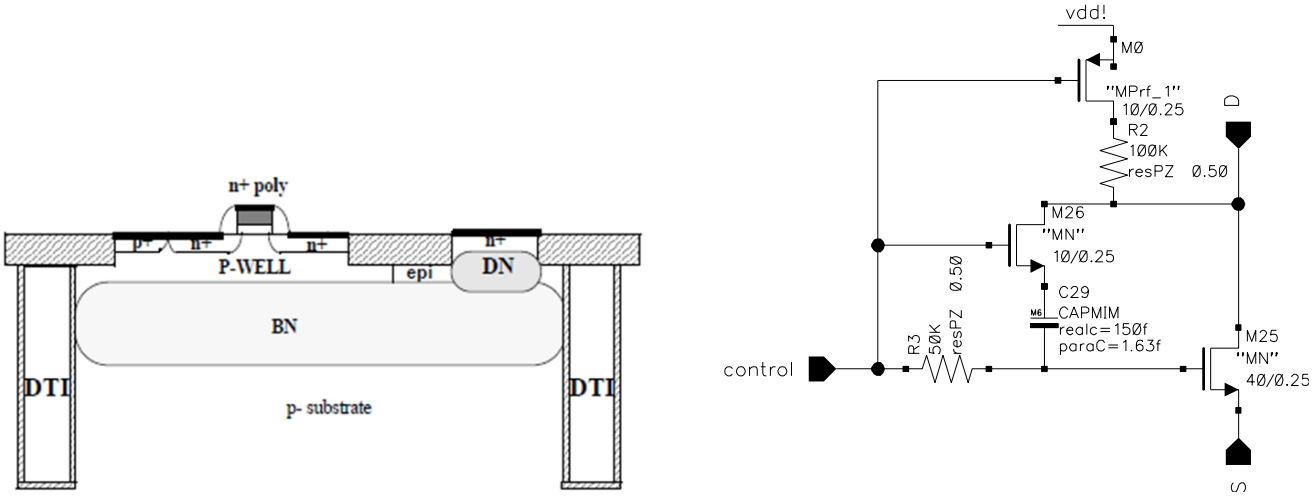


Fig 10. Improved linear RF MOS topology. Left: isolated cross-section, right: bootstrap and drain-biasing switch

4.1.3 Anti-Aliasing Filter

The anti-aliasing filter is based upon a 3rd order elliptic prototype. A passive implementation was selected for its noise, linearity and power consumption advantages. The used BiCMOS process [98] and the single-ended architecture facilitate the integration of a small-area high-Q inductor (L=7 nH, Q>8@1 GHz, area=0.2 mm2).

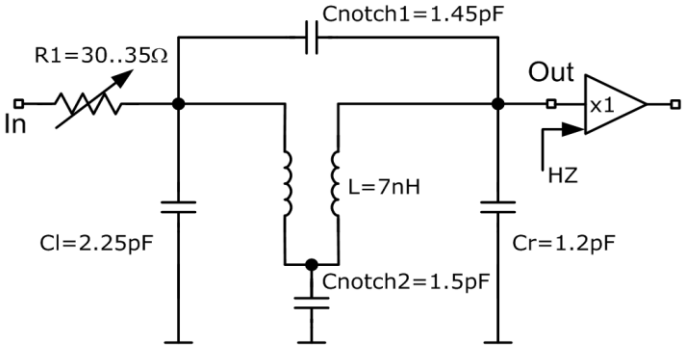


Fig 11. Passive 3rd order elliptic filter with center tap notch

The filter (Fig 11) makes use of a programmable series resistance R1 enabling gain peaking and tuning at 1 GHz. The elliptic classical π implementation is done with Cl, L, Cr and Cnotch1. It has been improved with the placement of Cnotch2 on the center tap of the differential inductor L. That allows maximizing the stop band attenuation without affecting the in-band ripple. This filter is associated with a high-ohmic impedance buffer. The filter provides 25 dB stop band attenuation, with 0.5 dB pass band ripple and with a stop band to pass band ratio of 1.6 GHz/1 G, process and mismatch spread included. It has an output noise lower than 10 dBuVrms integrated in 5 MHz bandwidth, OIP3 (/OIP2) respectively higher than 139 dBuVrms (/165 dBuVrms), mainly limited by the buffer performances.

4.1.4 Single-To-Differential Converter

The Single-To-Differential (S2D) is made with two stages, as depicted in Fig 12. The first stage realizes a signal inversion with a single–ended RF amplifier.

The second stage reduces gain/phase imbalance from 1 dB/30 ° (output of the 1st stage) to 0.5 dB/2 ° respectively (output of the 2nd stage), thanks to its common-mode rejection. It is based on cross-connected differential buffers, and ensures a 100 Ω doubly-terminated impedance matching between the RFFE and the MSFE input.

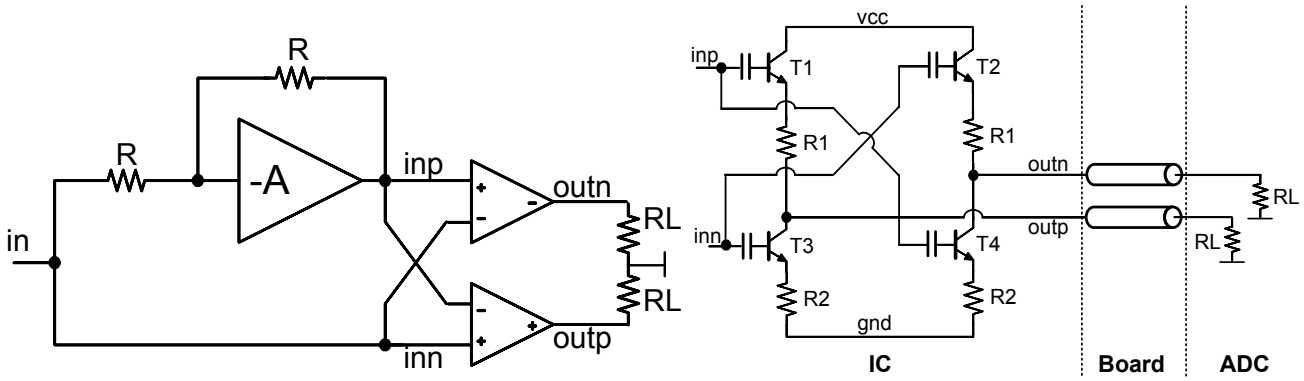


Fig 12. Single-to-differential converter principle diagram (left), Differential-to-differential buffer (right)

4.1.5 RFFE measurements

RFFE gain across frequency is reported on Fig 13, which shows the 7 tilt equalizer transfer functions, and the AAF attenuation (1.75 GHz notch).

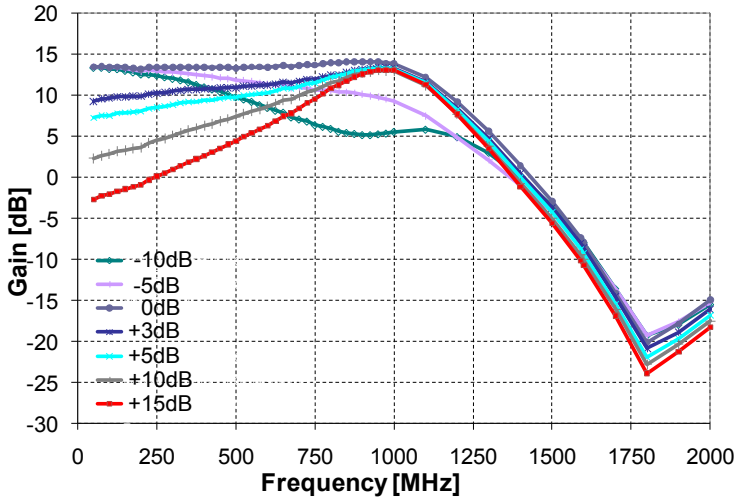


Fig 13. RFFE measured transfer functions for various TEQ settings

Fig 14 (left) reports the RFFE Noise Figure at maximum gain, which is under 4.3 dB across the full cable down-stream band. Fig 14 (right) reports 2nd and 3rd order non-linear distortion products, tested with a flat input signal with 158 CW at +15 dBmV/tone. All non-linear distortion spurs (CSO, CTB) are better than 58 dBc.

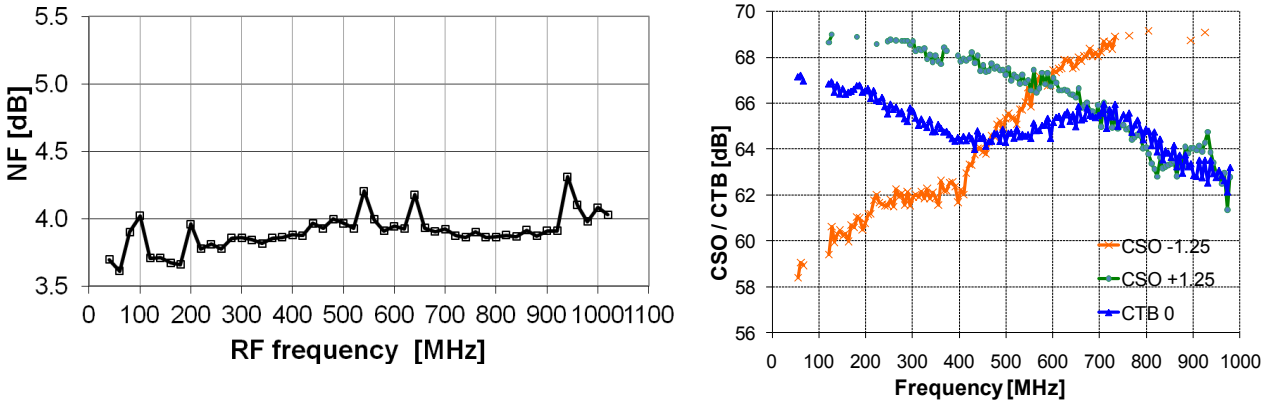


Fig 14. RFFE measured Noise Figure (left), and CSO/CTB (right)

4.2 Mixed-signal front-end

The architecture of the MSFE is shown in Fig 15. It is similar to the technology demonstrator approach we presented in ([103]), but is now a product which includes the simultaneous reception of 24 channels. This dictates the need for a high-speed serializer in order to transfer data to a SoC or FPGA with a low power and pin count.

The differential signal is first sampled by an ADC that is connected to the digital channel selection (DCS) filter that performs down conversion to baseband. The DCS is able to simultaneously select and convert 24 channels (6 or 8 MHz) to a 13.5 MS/s IQ format. After filtering and decimation, the 24 channels are framed and output through two 6 Gbps SATA III serial interface, to a SoC or FPGA fur further processing.

The receiver only requires an external crystal to serve as a reference for the low-noise integrated PLL.

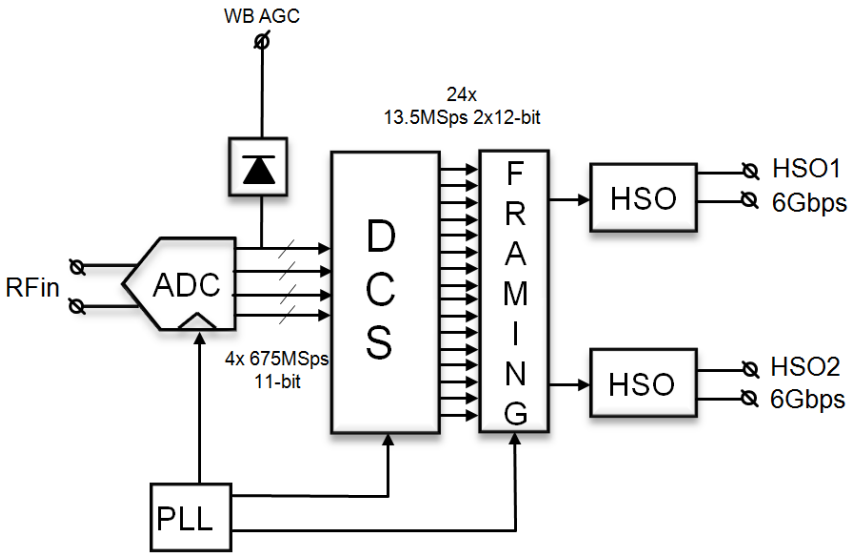


Fig 15. Mixed-signal front-end block diagram (down-stream path)

4.2.1 ADC

A SAR hierarchical interleaved architecture ([86], [87]) is used because of its high potential for parallelism. In order to overcome the limitations detailed in 1.3.5, only four passive THs are being interleaved.

As shown in Fig 16, each TH drives 16 reduced radix SAR ADCs to a combined total of 64 ADC units, arranged in four Quarter ADC arrays (QADC). Each TH drives its QADC array with a feedforward–feedback multiplexed open

loop buffer interface (Fig 17). As the buffer is placed in the SAR loop, its non-linear distortion will be experienced by both the input signal and the feed-back DAC signal. Since the SAR operation is based on zero crossing detection, and both input and DAC signals are equally distorted, the difference signal will still result in the correct decision.

The four sequencers determine the randomization order and chopping sequence that are used to spread the power of any remaining offsets and gain errors in the SAR-ADCs.

Gain flatness and minimum signal reflection are ensured by a broad-band double-terminated impedance matching between RFFE and MSFE. This is achieved by using a 100 Ω differential passive termination, connected in parallel to the TH-bank input, internally to the MSFE. Dynamic impedance variations are minimized by ensuring that two THs (out of four) are always connected to the input node. These measures allow driving the TH-bank directly with the RFFE, without any MSFE input buffer.

Bootstrapping of sampling switch is used in order to limit the impact of bandwidth mismatch at the sampling node, to achieve a sampling linearity of more than 60 dB.

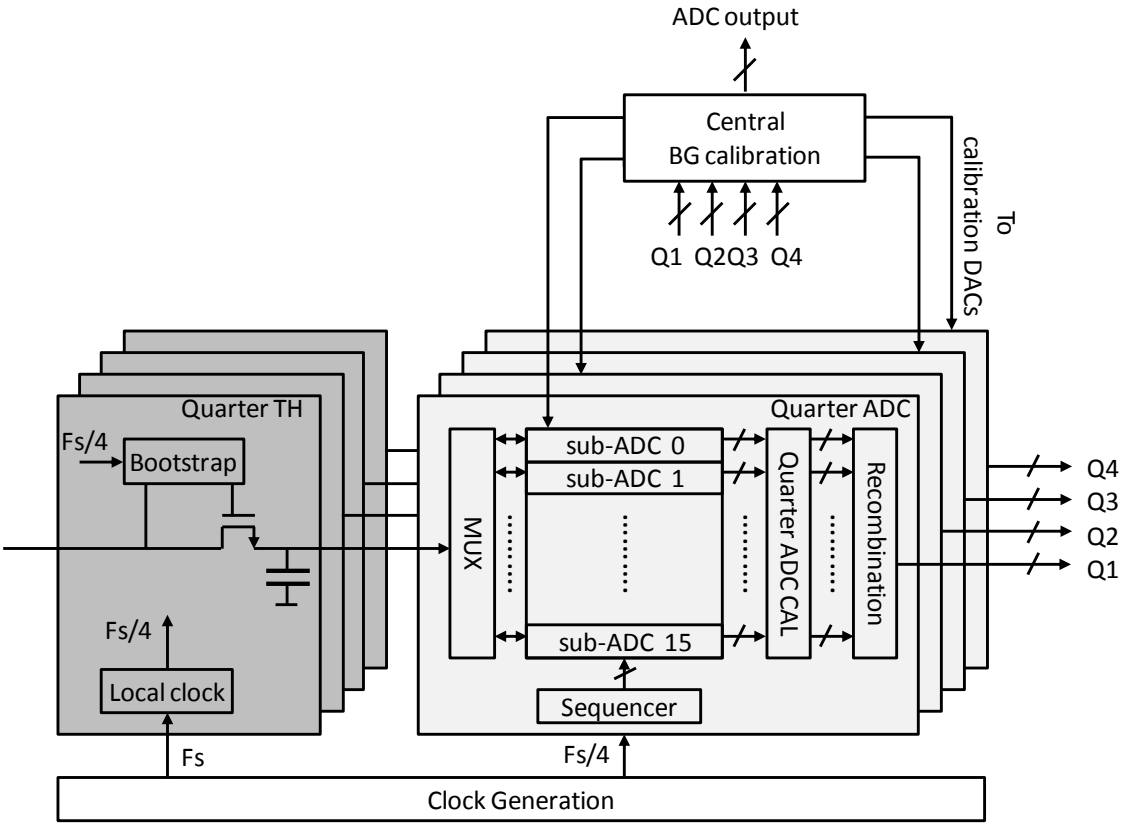


Fig 16. ADC block diagram

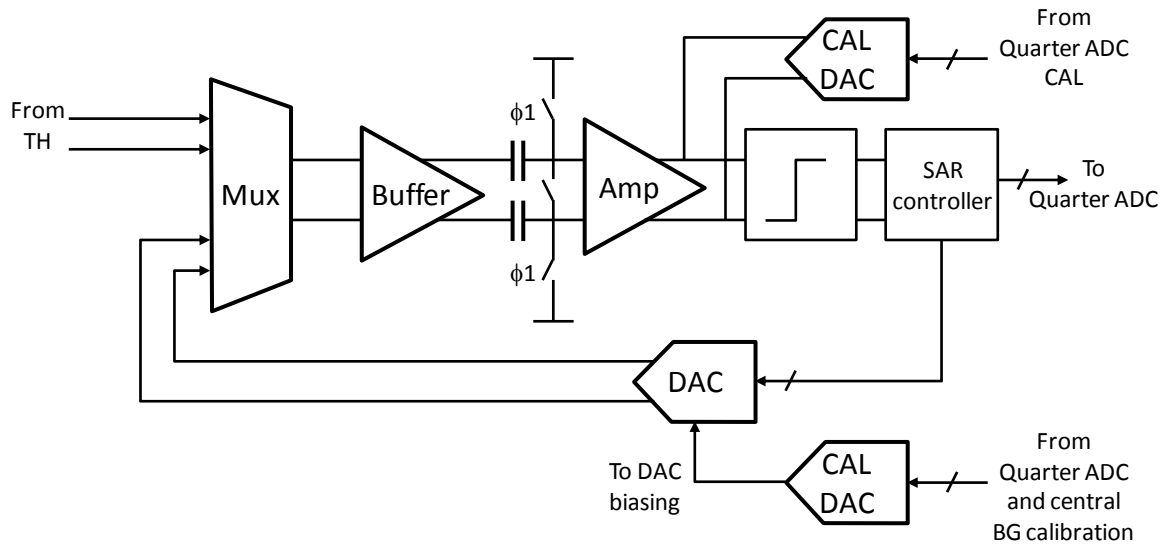


Fig 17. SAR ADC architecture and interface with TH

4.2.2 Digital Channel Selection

A classical multi-channel DCS is shown in Fig 18: each channel selection is composed of a digital down-converter, consisting of a digital mixer, a channel-select filter, and a decimation stage.

Both digital mixer and channel filter are clocked at the ADC sampling rate (2.7 GHz). When 24 channels are required in the receiver, 24 parallel blocks need to be duplicated, which results in a high power consumption, and high level of interference.

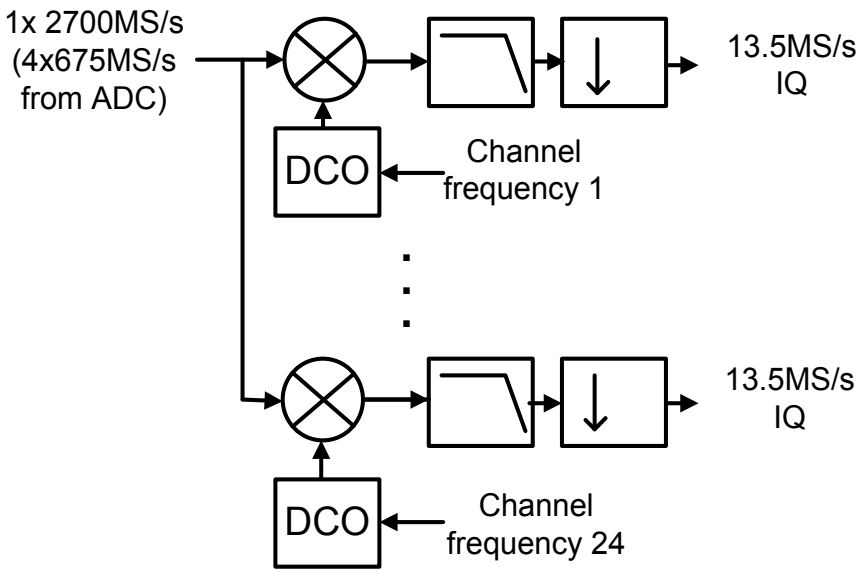


Fig 18. Classical DCS architecture

The implemented approach ([103], [104]) performs channel selection in two steps:

- The input signal spectrum is split into 8 sub-bands (A, B, …, G, H in Fig 19) by a hierarchical band splitter function, based upon a cascade of 3 band-splitting-by-2 stages. As selectivity is performed, the sampling rate can be progressively reduced without consequent aliasing. This function is instantiated once on the IC.

- 24 classical Digital Down-Converters: they are made from a digital mixer and a decimation filter which reduces the sampling rate to 375 MHz to 13.5 MHz.

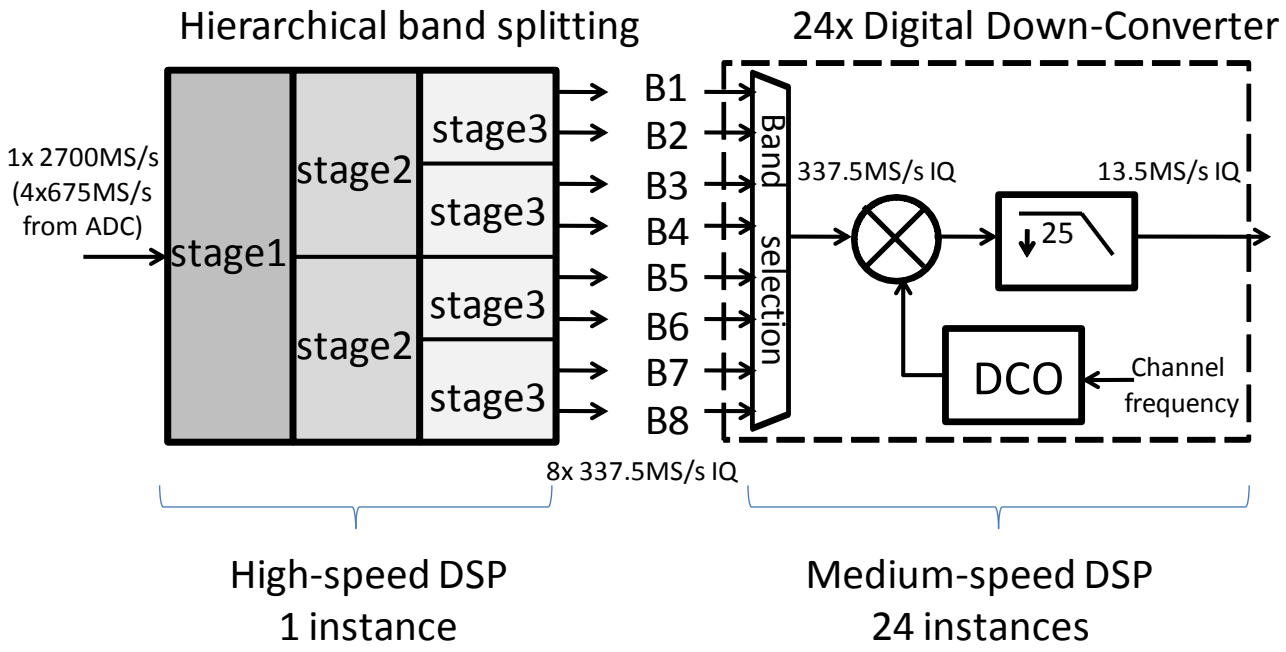


Fig 19. Proposed DCS architecture

4.2.2.1 Hierarchical band splitting

Fig 20 illustrates the process of the 1st band-splitting-by-2 stage, in order to select the lower frequency band of the ADC output signal. The real input signal is first multiplied with a $-\pi/4$ complex sine wave. Secondly, it is low-pass filtered, which reduces its spectrum bandwidth. Finally the signal can be down-sampled by a factor 2, without any consequent aliasing.

Fig 21 illustrates the selection of the ADC output signal upper frequency band. The ADC output signal is multiplied with a $-3\pi/4$ complex sine wave. The remaining process is exactly similar to Fig 20.

The first band-splitting stage has indeed split the input signal into two sub-bands, without any loss of information. A small frequency overlap between the two bands has been implemented in order to receive any 6 or 8 MHz-wide channel.

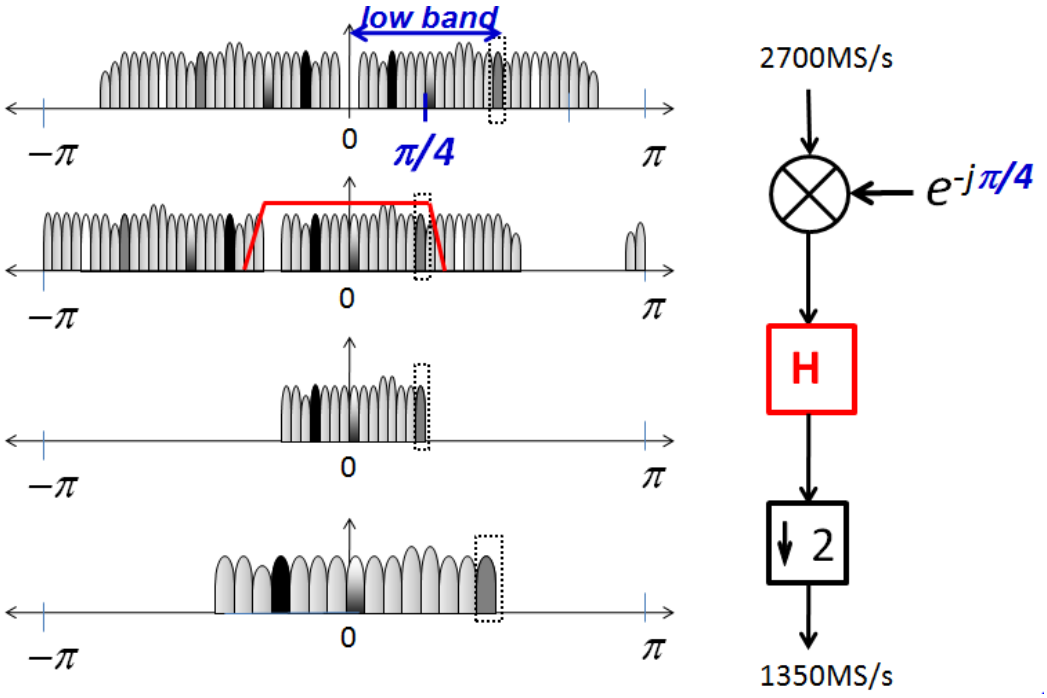


Fig 20. Hierarchical Band Splitting Stage 1: conversion of the input spectrum lower band

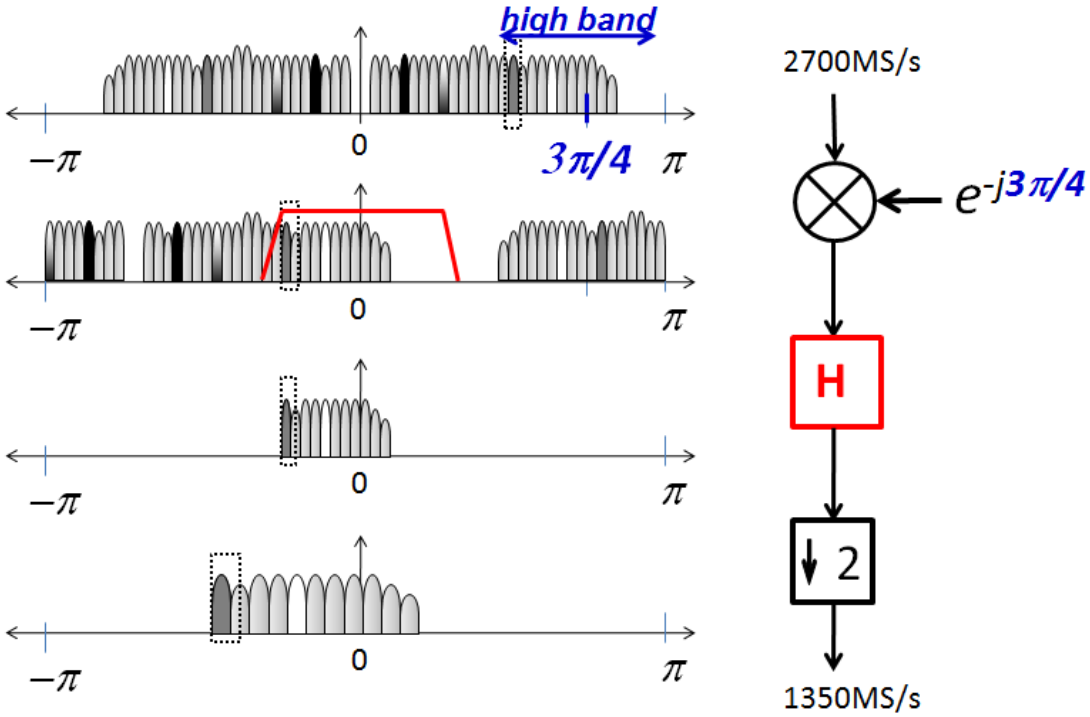


Fig 21. Hierarchical Band Splitting Stage 1: conversion of the input spectrum higher band

The implementation of the band-splitting-by-2 stage ([104]) is shown in Fig 22. Using a polyphase decomposition, the processing starts with a down-sampling-by-2 action. As illustrated in Table 7, $-\pi/4$ and $-3\pi/4$ rotations are achieved by simple multiplications. Indeed, the involved signal processing can be further simplified by careful inspection of Table 7:

- $\sqrt{2}/2$ coefficients, which are required for the processing of the odd samples (2n+1), can be included in the odd taps (2n+1) coefficients of the filter, resulting in simple multiplications by ± 1, $\pm j$, or $\pm(1 \pm j)$ in the mixer.
- By making a proper combination of odd and even samples at the filter output (combiner block of Fig 22), both real and imaginary parts can be calculated from a single (non-complex) signal path. For even samples, imaginary part is the negative of real part. For odd samples, real and imaginary parts are equal.
- Both "low-band" and "high-band" outputs can be provided by the same polyphase mixer-filter stage. Comparison of column 2 ($e^{-j\frac{\pi}{4}2n}$) and column 4 ($e^{-j\frac{3\pi}{4}2n}$) of Table 7 reveals that the real part is equal, the imaginary part is the negative of each other. Comparison of column 3 with column 5 shows that the real part is the negative of each other, the imaginary part is equal. Therefore, by using a combiner block at the polyphase filter output, selection of both "low-band" and "high-band" can be achieved by a common stage.

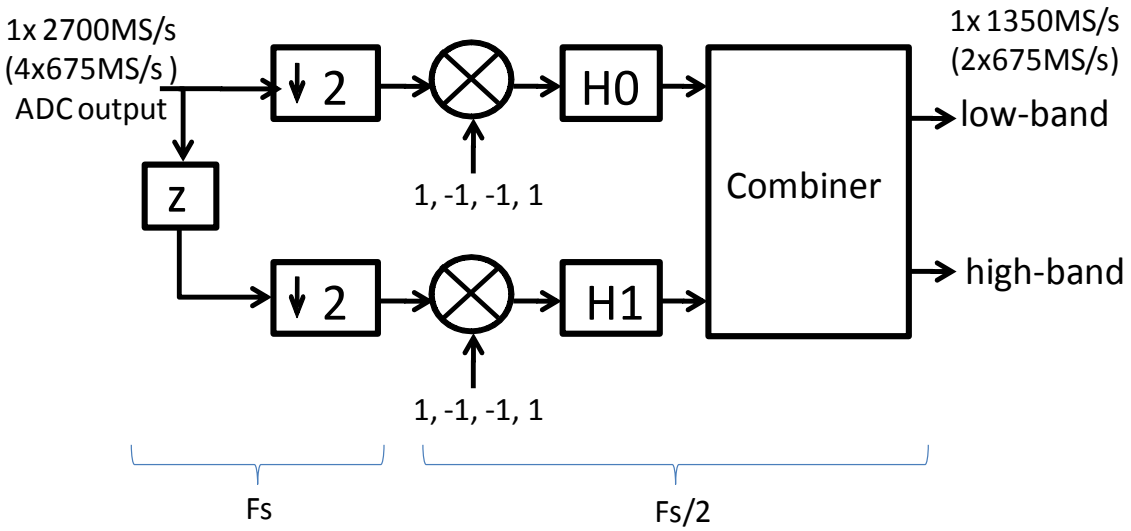


Fig 22. Hierarchical Band Splitting Stage 1

Table 7. Complex mixer coefficients for the hierarchical band splitting

n	$e^{-j\frac{\pi}{4}2n}$	$e^{-j\frac{\pi}{4}(2n+1)}$	$e^{-j\frac{3\pi}{4}2n}$	$e^{-j\frac{3\pi}{4}(2n+1)}$
0	1	$\frac{\sqrt{2}}{2}(1-j)$	1	$\frac{\sqrt{2}}{2}(-1-j)$
1	$-j$	$\frac{\sqrt{2}}{2}(-1-j)$	j	$\frac{\sqrt{2}}{2}(1-j)$
2	-1	$\frac{\sqrt{2}}{2}(-1+j)$	-1	$\frac{\sqrt{2}}{2}(1+j)$
3	j	$\frac{\sqrt{2}}{2}(1+j)$	$-j$	$\frac{\sqrt{2}}{2}(-1+j)$

Fig 23 shows the operation of the 3 band-splitting-by-2 stages in the frequency domain. The 3-stage cascade allows splitting the high-speed input signal into 8 sub-bands, each one sampled at Fs/8.

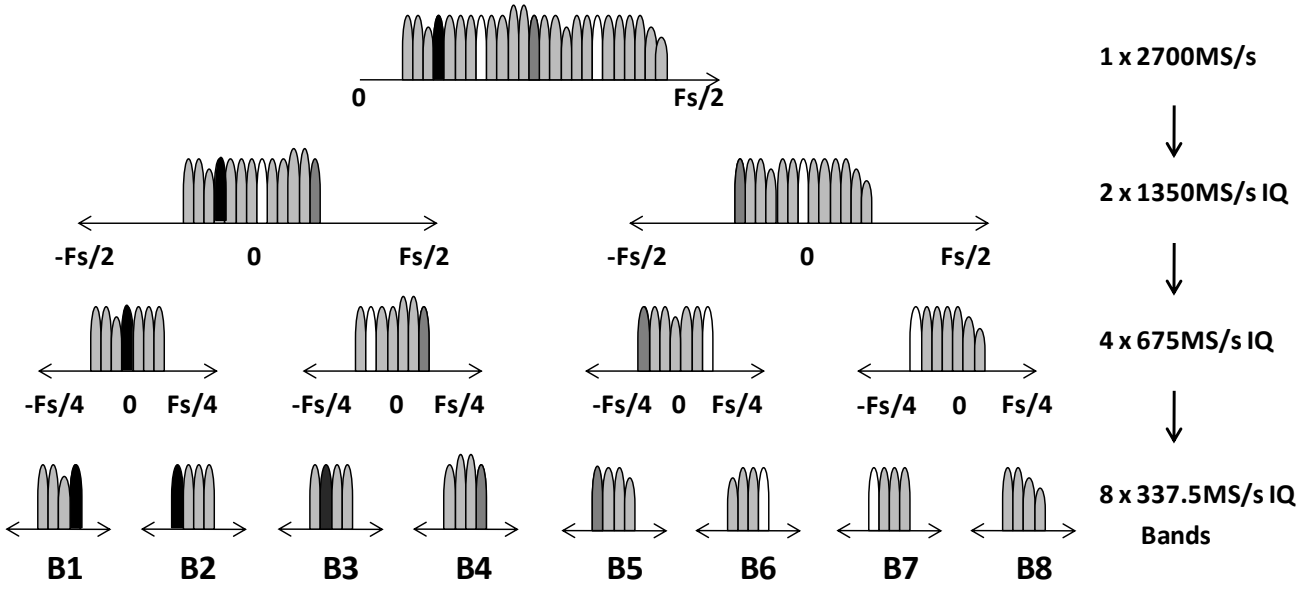


Fig 23. Hierarchical Band Splitting Stage 1, 2 and 3

4.2.2.2 Digital Down-Converter

The DDC section provides down-conversion and selection of up to 24 wanted channels. Each of these 24 blocks performs:

- Frequency translation to DC using the CORDIC algorithm ([96]),
- Down-sampling by factor 20 to 30 based upon a Cascaded-Integrator-Comb architecture.
- Channel selection using a multi-mode FIR filter (Adjacent Channel Interference filter): 6 MHz mode, 8 MHz mode.
- Automatic Gain Control, based upon a RMS detection.

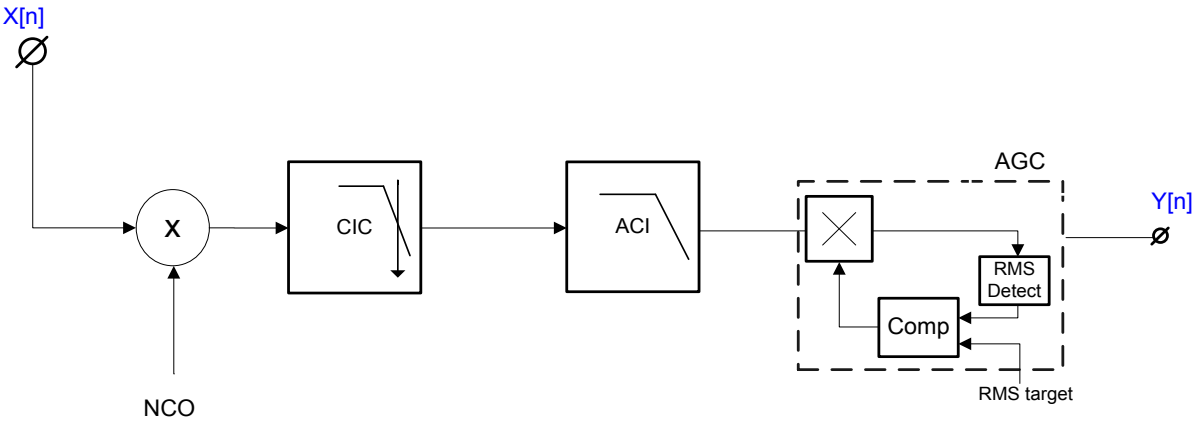


Fig 24. Digital Down-Converter

Fig 25 shows the DDC transfer functions in both 6 MHz and 8 MHz modes:

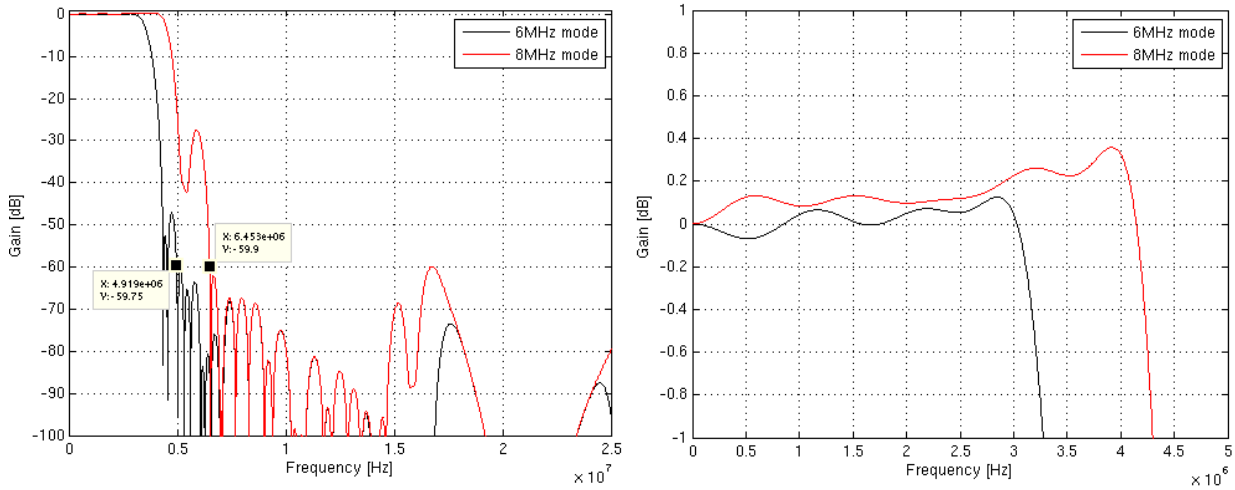


Fig 25. Digital Down-Converter frequency response

The adjacent rejection is better than 60 dB at 4.92 MHz/6.45 MHz frequency offset.

Table 8 shows that the DDC has the ability to reject the power of adjacent N+/-1 channels by more than 14 dB. The remaining adjacent channel power is attenuated in the squared-root-raised-cosine filter integrated in the QAM demodulator (inside the SoC or FPGA).

Table 8. 256-QAM N+/-1 rejection for 6 MHz / 8 MHz mode

BW	N+/-1 rejection
[MHz]	[dB]
6	14.25
8	17.7

4.3 Mixed-signal AGC loop

In mixer-based receiver, RF AGC loops need to guarantee a good trade-off between the RF blocks noise floor and signal compression. Usually, setting the Take Over Point (TOP) of the RF amplifiers within an accuracy of few dBs is sufficient.

In a direct-sampling receiver, the RF signal is sampled by an ADC. Instead of classical 2nd and 3rd order non-linear distortion, the clipping behaviour of ADCs is very abrupt (see 2.2.3.4), and involves very high order harmonic content.

A possible option is to back-off the composite signal from the ADC full-scale by few dBs. In order to preserve the full receiver performance, this would turn into an increase SNDR requirement on the ADC. Given the difficulty of designing an ADC adequate to the cable modems requirements (2.7 GSps, SNDR=54.5 dB), this is not an efficient option. Therefore, a very accurate AGC loop is required (<0.5 dB), in order to fully exploiting the ADC dynamic range.

The AGC is built on the combination of a RMS loop and a peak loop. Its high-level block diagram is shown in Fig 26:

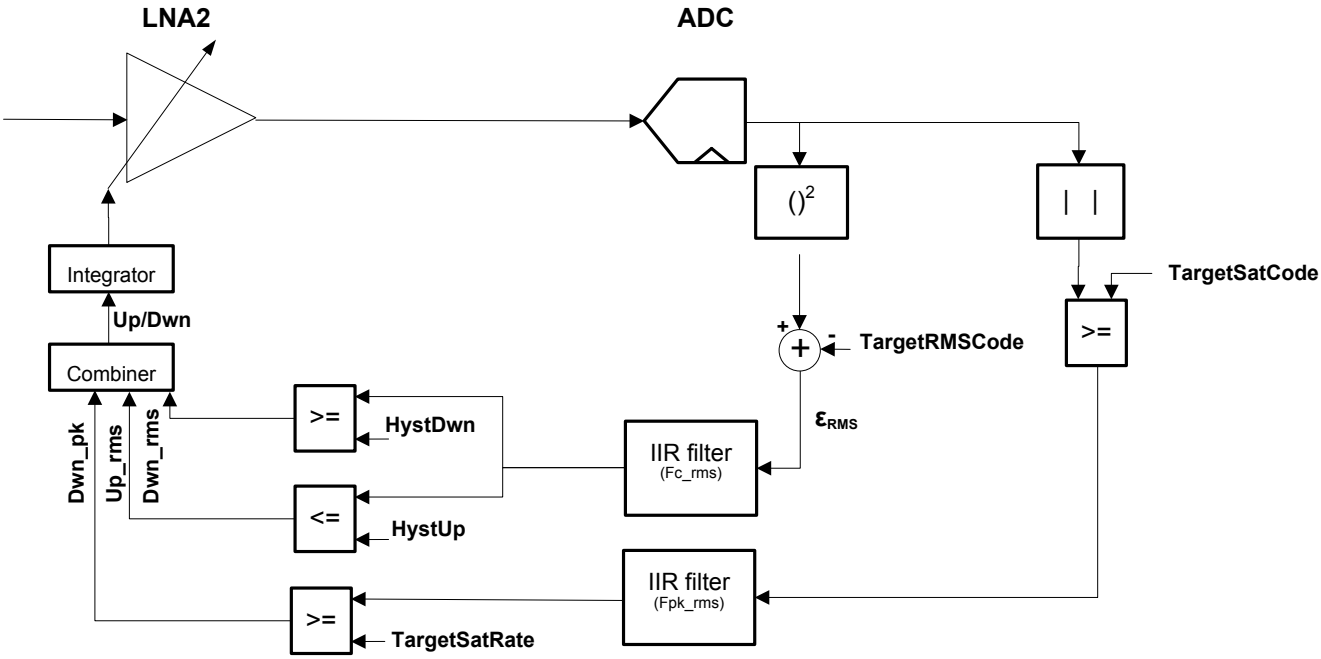


Fig 26. Mixed-signal AGC loop

Fig 27 illustrates the different detections operated by the two loops, with the example of an amplitude-modulated (AM) input signal.

The RMS loop is configured with a large time-constant. It reacts to the "long-term" input signal distribution (blue curve of Fig 27), and detects its RMS amplitude.

The peak loop is able to react on positive alternates of AM signals. To enable this, its cut-off frequency is set higher than the modulation frequency, and the *saturation detection point* (defined by its *target saturation code* and its *target saturation probability*) is set slightly above the expected average Gaussian distribution. This detection point should be set between two and four times the targeted RMS amplitude, in order to accurately discriminate AM positive alternates from non-modulated input signal.

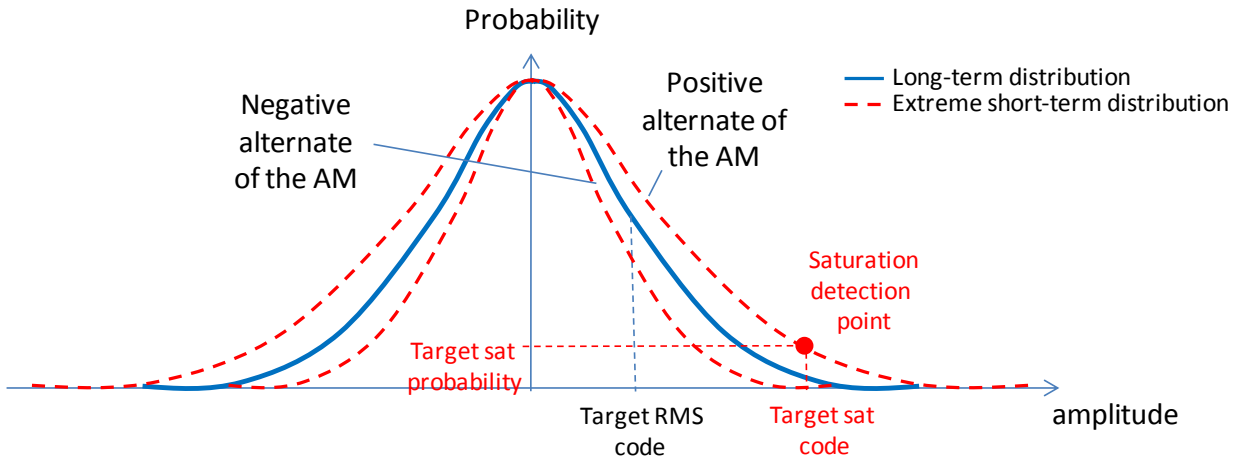


Fig 27. RF signal distribution in presence of amplitude modulation

4.3.1 RMS loop

The ADC output signal is squared, convolved with a programmable impulse response (IIR lowpass filter with programmable cut-off frequency). An error signal is then built on the difference between the ADC output RMS estimate and the targeted RMS code (programmed accordingly with the targeted ADC loading factor). Depending on the error signal polarity, and including a hysteresis, a positive or negative pulse is sent to the gain command integrator, which output directly controls LNA2 gain. The settling time of the RMS loop (1 dB accuracy) is on the order of tenths of seconds. It ensures an accurate convergence point, and avoids reacting to short-term events.

4.3.2 Peak loop

The absolute value of the ADC output signal is compared to a targeted saturation code (Fig 27). The output of the comparator is convolved with a programmable impulse response (IIR lowpass filter with programmable cut-off frequency). The filter output represents the cumulative density function (CDF) of the ADC output signal, evaluated at the targeted saturation code. If the saturation probability exceeds the targeted saturation probability, a negative pulse is sent to the gain command integrator, which output directly controls LNA2 gain. The peak loop can only decrease the gain, in order to ensure a stable combination of RMS and peak loops.

4.4 RF tilt equalizer control loop

The benefit and design of an RF tilt equalizer has been presented in 3.3.4 & 4.1.2. Still a control loop is required to program the tilt equalizer to its optimum setting. For this purpose, a tilt sensor and a tilt decision algorithm are required.

In this direct RF sampling architecture, the full RF signal is digitized and channelized. The DCS include an AGC loop which can provide an RMS estimate for the individual channels amplitude, without any additional hardware.

At start-up, the system is configured to scan the full cable band (158 channels) using simultaneously 24 DCS, each one providing the RMS amplitude of a single cable channel. After 7 runs (158/24), all channel amplitudes are known, and the tilt is estimated using a linear regression method.

The last step is to program the RF equalizer to the settings which best compensates for the cable tilt.

Fig 28 illustrates the algorithm with random-amplitude channels on a 16-dB tilted cable. The linear regression algorithm allows to correctly estimating the tilt, and programming the RF tilt equalizer to its nearest setting (15 dB compensation).

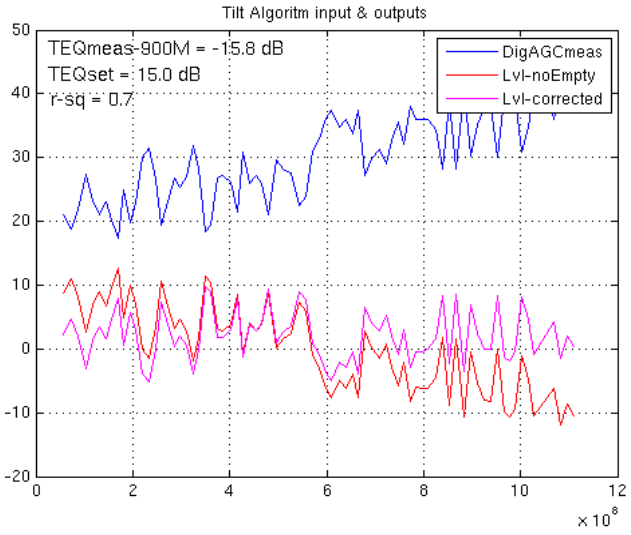


Fig 28. Simulation of the tilt control loop with random channel amplitudes

4.4.1 RFFE measurements

Fig 29 presents the broadband performance of this ADC: it reports the SNDR per 6 MHz –channel, achieved with an input signal consisting of 158 sine waves. 48 dB of SNDR per channel is reached, quite independently of the input frequency, from 50 MHz to 1 GHz. As a broadband input signal is used, this SNDR metric includes ADC noise (quantization and thermal), ADC non-linear distortion, ADC time-interleaving mismatches, DCS re-quantization noise, PLL and clock path phase noise.

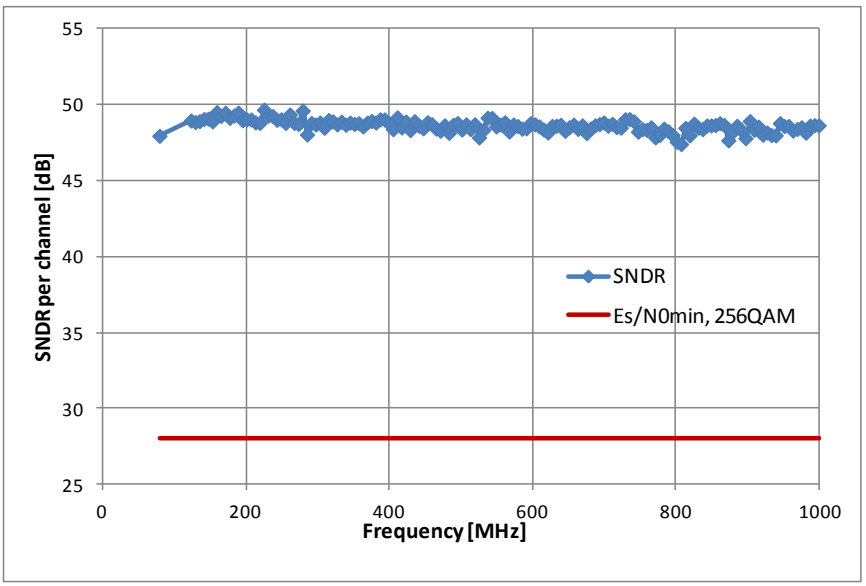


Fig 29. MSFE broadband SNDR performance

4.5 System-level simulations and measurements

The full receiver chipset has been tested together on the system board of Fig 30:

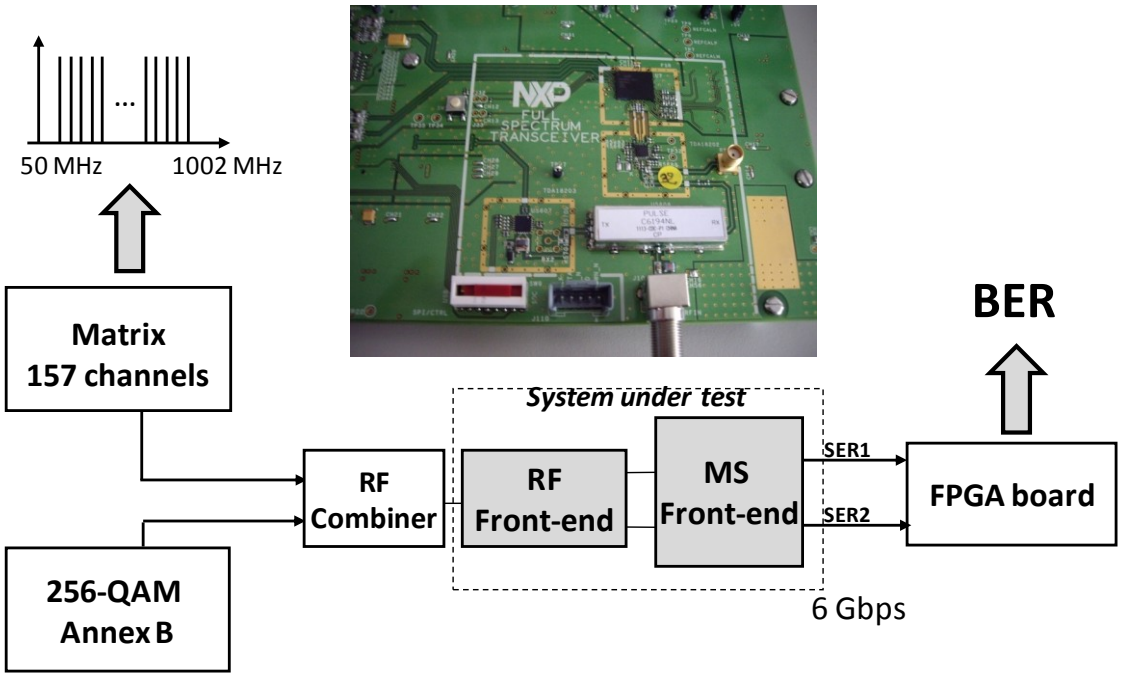


Fig 30. Full receiver board & system test bench

The wanted signal is combined with 151-sine waves, which emulates the unwanted channels. The composite signal is connected to the RFFE. The MSFE output is connected to an FPGA board, which integrates 256-QAM demodulators. This allows testing the full system against various interferers profiles (input noise, tilt, strong N+/-1 adjacent channels, fading) while monitoring the receiver BER.

In Fig 31, the receiver input wanted QAM channel is surrounded by 2 adjacent channels, each one 20 dB above. In addition the cable plant is fully loaded with sine waves at 0 dB. In such a situation, the low-IF output signal spectrum shows that the adjacent channels are rejected by 65 dB at 2 MHz offset from the wanted channel.

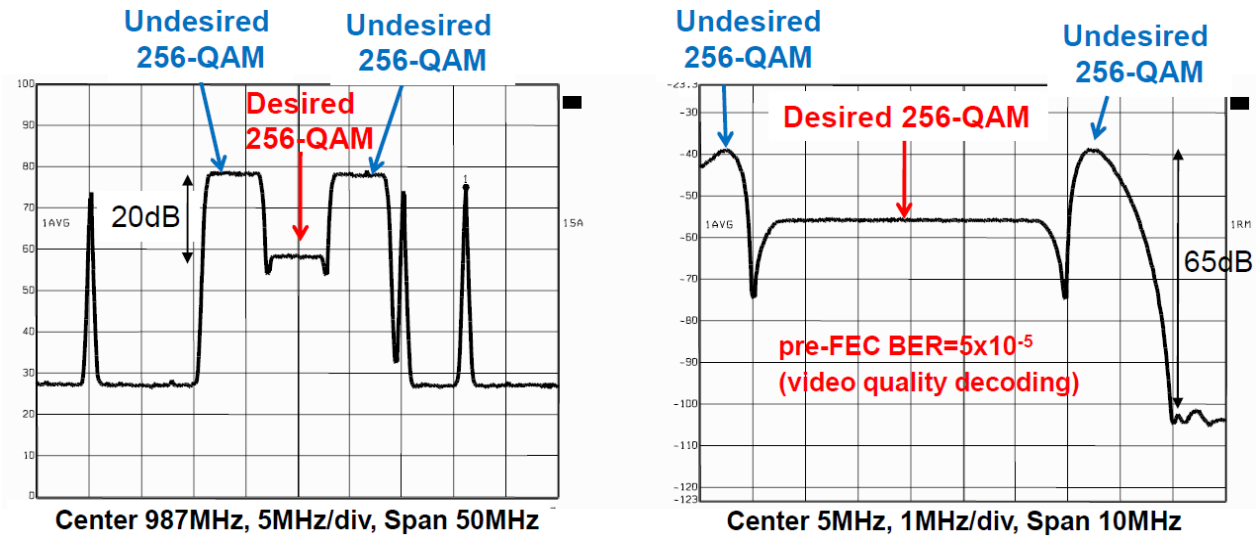


Fig 31. System test with 2 adjacent QAM channels (+20 dBc) and 157 CWs (0 dBc). Left: input signal, Right: output signal

Even in case of strong cable loading (D/U=-10 dB, 158 channels), the receiver output signal quality ensures a high margin compared to error-free reception (Fig 32):

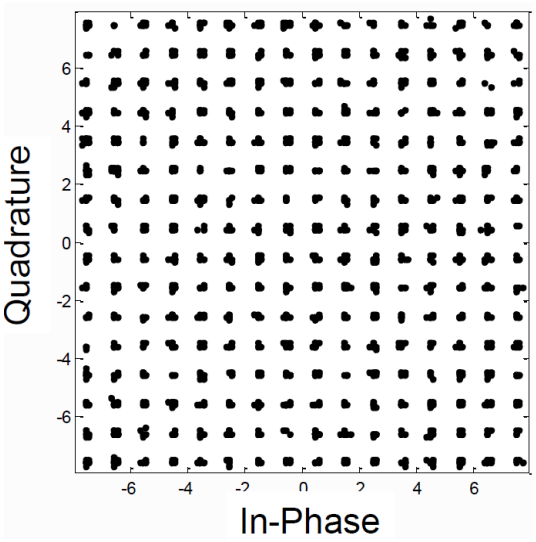


Fig 32. Received 256-QAM constellation captured inside the QAM demodulator, with 157 adjacent channel at +10 dBc

Bit Error Rate (BER) tests have been conducted, demonstrating the reception of 24 independent wanted channels among 157 channels. For each frequency, the wanted channel has been reduced down, as much as possible compared to the interferers (reported as D/U: Desired over Undesired ratio), while the full receiver still maintains a pre-FEC BER $<5x10^{-5}$. Using the input signal condition depicted in Fig 33 (left), the tilt equalizer (+15 dB setting) improves the system performance by 7 dB compared to the nominal configuration (0 dB setting), as reported in Fig

33 (right).

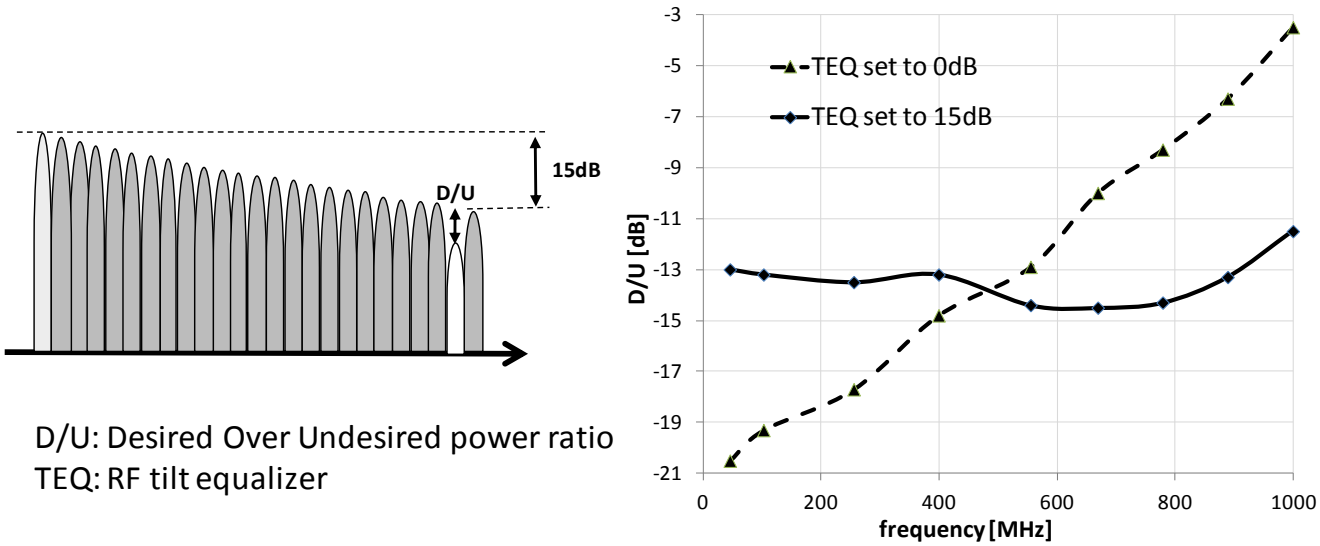


Fig 33. Left:cable input signal containing 15 dB tilt. Right: minimum D/U over frequency, without and with tilt equalizer (BER<5x10^{-5})

System sensitivity for the reception of 256-QAM channels, over the full RF band, is presented in Fig 34. The system performs better than an ideal receiver with a 5.5 dB NF.

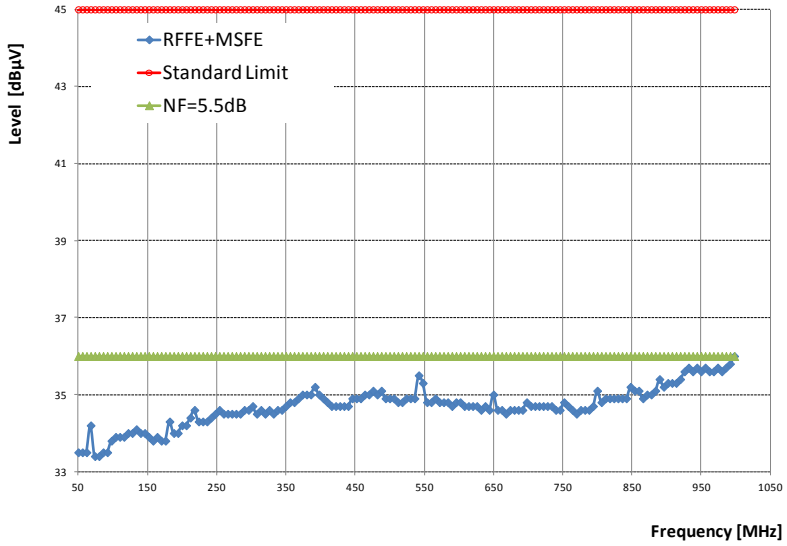


Fig 34. System sensitivity tests with 256-QAM, including RFFE, MSFE and QAM demodulator

Fig 35 compares the power consumed by several receiver front-end (tuner) architectures as a function of the number of received channels. This work exhibits lower power consumption than the state-of-the-art as soon as three channels are received. When receiving 24 channels, this work reduces power reduction by a factor six, compared to a narrowband tuner solution.

In addition, no additional RF splitter is required (compared to a narrowband tuner front-end solution), and the 24 channel frequencies can be completely independent, in opposition to the 64 MHz / 100 MHz channel bonding of wideband-tuners.

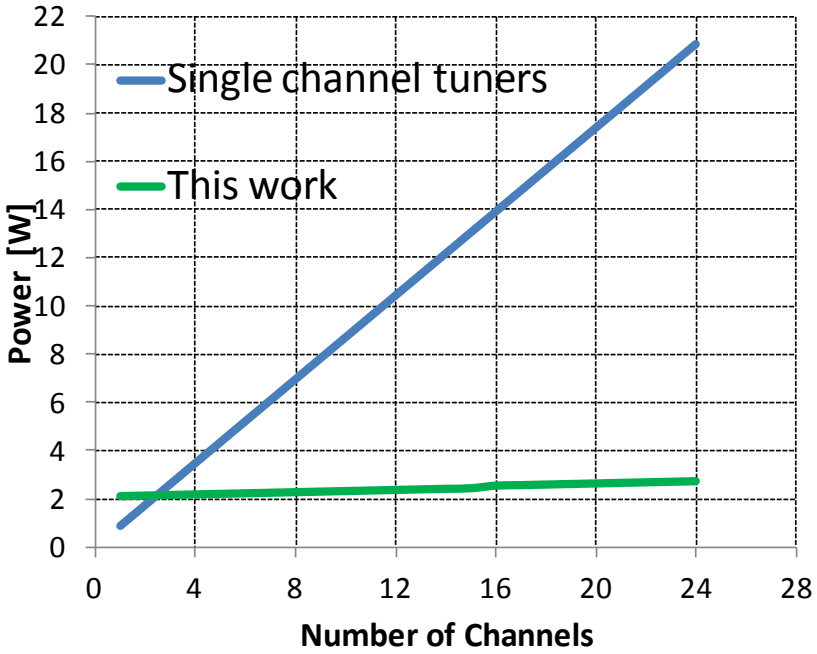


Fig 35. Power consumption against the number of received channels for Single channel tuners and this work

Table 9 provides a collection of radio receivers for cable and terrestrial TV reception. Most of them are single-channel receivers, as these are the most deployed products. The most relevant characteristics are reported.

This work is the first reported RF direct digitization receiver for cable applications, and provides the highest number of received channels, compared to other architectures.

As reported in Table 9, this work is the most power and cost-effective solution, as it provides the lowest power and area per channel.

In addition to the power per channel indicated in Table 9, if 24-channels solutions would have to be built using the ICs referenced in Table 9, additional RF amplifiers would be required to split the RF input signal. As many ICs would be required to build the application, board area would linearly increase with the number of channels, which would severely impact size and cost. Such an application would also require many LC VCOs (at least one per single-channel tuner), which could give rise to VCO pulling and could degrade phase noise performance.

This work features one of the lowest NF, so provides one of the best sensitivities, and shows average linearity performance.

Our solution provides the ability of receiving channels at 24 fully independent frequencies. As it receives two blocks of four channels, the dual low-IF receiver presented in [43] can only receive 8 channels located around two different RF frequencies. In case of channel bonding for high-speed internet, this statistically reduces the spectrum efficiency that cable operators can reach.

Table 9. Cable and terrestrial TV receivers comparison table

		Van Sinderen [32]	Tourret [33]	Stevenson [29]	Gupta [34]	Gatta [43]	Greenberg [35]	This work
Year		2003	2007	2007	2007	2009	2012	2012
Freq range	[MHz]	48-860	48-862	48-864	48-860	48-1000	40-1000	42-1002
Number of channels	[dB]	1	1	1	1	8	1	24
Channels independence		NA	NA	NA	NA	No	NA	Yes
Architecture		Low-IF	Low-IF	Dual-Conversion	Low-IF	Dual Low-IF	Low-IF	Direct RF digitization
NF	[dB]	7	5	8	7	6.5	3.8	5.5
CTB/CSO	[dB]		-57 / -57	-65 / -60	-53 / -115	-64 / -66		-62 / -59
IIP2 min/max	[dBm]				-22.4 / +36.5		+20 / +66	
IIP3 min/max	[dBm]	19 / 27			-13.8 / +17.5		-15 / +35	
LO integrated phase noise			0.5°RMS at 862MHz, 1kHz-4MHz		0.05°RMS to 0.8°RMS	0.2°RMS at 1GHz, 5kHz-10MHz	0.46°RMS at 855MHz	0.17°RMS at 1GHz, 5kHz-4MHz
Power	[mW]	1500	780	1500	750	1950	440	2370
Area	[mm2]	12.37	5.7 (total SIP: 9x9)	7.29	25	10mm2 + ref PLL	5.6	25
Technology		0.5um BiCMOS	0.25um BiCMOS	0.35um SiGe	0.18um CMOS	0.18um SiGe + 65nm CMOS	80nm CMOS	0.25um BiCMOS+ 65nm CMOS
Power / channel	[mW]	1500.0	780.0	1500.0	750.0	243.8	440.0	98.8
Area / channel	[mm2]	12.4	5.7	7.3	25.0	>1.25	5.6	1.0
Integration		LNA loop-through to analog IF	LNA loop-through to analog IF, using SIP	RF to analog IF, with ext. IF filters	RF to analog IF, using a digital IF selectivity	RF to MAC	RF to analog IF, using a digital IF selectivity	LNA loop-through to DCS, integrated RF filters

4.6 Summary

In this chapter, the design of the main critical blocks of a multi-channel direct-digitization RF receiver has been presented.

Targeting a consumer market, a high emphasize has been put on achieving a low-cost receiver, including:

- A fully-integrated BiCMOS RFFE including LNAs, single-inductance multi-slope RF tilt equalizer, AAF, single-to-difference buffer, avoiding any high-quality external RF component.
- An integrated 65nm-CMOS MSFE, including a 2.7 GSps 11-bit ADC, PLL, DCS, high-speed serial interface. In addition, the wideband receiver is part of a more complex IC, including an up-stream path. Time-interleaving and efficient digital down-conversion have been deeply exploited, as well as several algorithms for maximizing the use of the receiver dynamic range (AGC loop, Tilt equalizer control loop).

The receiver exceeds all data/video standards requirements, and equals or outperforms the RF performance of cable-modem mixer-based receivers RF. In addition, it shows the lowest power per channel.

Conclusions & perspectives

The objective of the work that has been carried in this Ph.D thesis was to study direct digitization receivers, and to demonstrate their design integration in a consumer electronics product, at a competitive cost, power, size, and performance.

In chapter 2, a system-level analysis allowed identifying the main technical obstacles to the design of a broad-band direct sampling & digitization receivers. Impairments linked to signal conditioning, sampling, and analog-to-digital conversion, have been analytically modelled in the context of a broadband reception.

This theoretical analysis has been applied to the design of 42 MHz-1002 MHz cable multi-channel receiver product, based on a direct-sampling receiver, in chapter 3. The architecture has been specifically optimized to the application context. An innovative RF front-end has been shown to relax the requirements on the ADC performance.

In chapter 4, the design of the major blocks is presented from RF to DSP and SW algorithm. Finally, measurements results prove that the receiver exceed standard requirements, and has a lower power consumption and area than the state-of-the-art.

The main contributions of this thesis are:

- System-level analysis of direct RF sampling & digitization receivers
- Theoretical analysis of broadband non-linear distortion, for lowpass and bandpass sampling schemes
- Theoretical analysis of time-interleaved ADC in a broadband reception context
- Design of a application-optimized signal conditioner, including:
    - A single-inductance multi-slope programmable RF amplitude equalizer, together with its control algorithm
    - A mixed-signal AGC loop combining RMS and peak detection
- Contribution to the realization of a direct RF digitization product, exceeding state-of-the-art power consumption, cost (silicon area), and equivalent or better performance than legacy silicon tuners

Looking forward, this work opens several perspectives and challenges:

High-performance multi-channels universal tuner: direct RF digitization receivers could replace Silicon Tuners in all multi-channel TV systems, including the most demanding terrestrial TV receivers. This application requests equivalent RF frequency range and an equivalent integration level to the demonstrated cable product, but requires a higher-dynamic range receiver.

Linearization

- *Broad-band transmitter linearization*: PAs are key functions of wireless infrastructure transceivers, and typically consume a large part of the wireless BTS power. High-data-rate services employ non-constant envelope modulation techniques. As a result, designers must achieve high efficiency and linearity over a large amplitude range. Among the existing linearization techniques, Digital Pre-Distortion seems to offer a higher power-efficiency and a greater flexibility. It requires a wideband observation RX (Fig 1) for measuring PA non-linearity and adapting the digital pre-distorter in accordance to the difference between the observed signal and the original digital baseband data. A direct-RF observation path can allow improving the observation path versatility and increase the PA instantaneous bandwidth, which can allow wider signals to be transmitted.

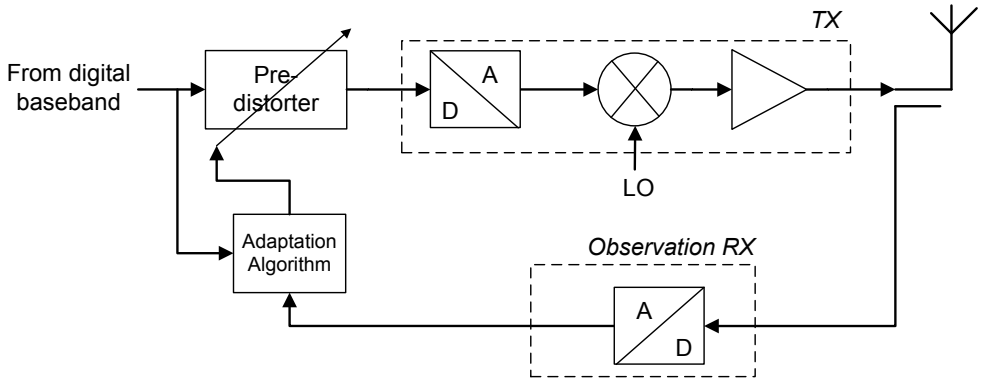


Fig 1. Use of a observation RX in a Digital pre-Distortion loop for PA linearization

- *Broad-band mixer-based receiver linearization* (Fig 2): in mixer-based receivers, using a low-resolution broad-band auxiliary direct RF digitization path to improve robustness against interferers. As the auxiliary path has a wide RF-band visibility, it has knowledge of strong interferers, and could be used to mitigate unwanted broadband effects. As an example, in [106], the main RX suffers from down-conversion of RF blockers with the LO harmonics. The auxiliary path allows these blockers to be selected by the wideband digital signal conditioning, and subtracted from the main RX output using an LMS algorithm. The concept could be extended to the compensation of non-linear distortion. These applications request a highly-integrated and extremely low-power RF direct-digitization path.

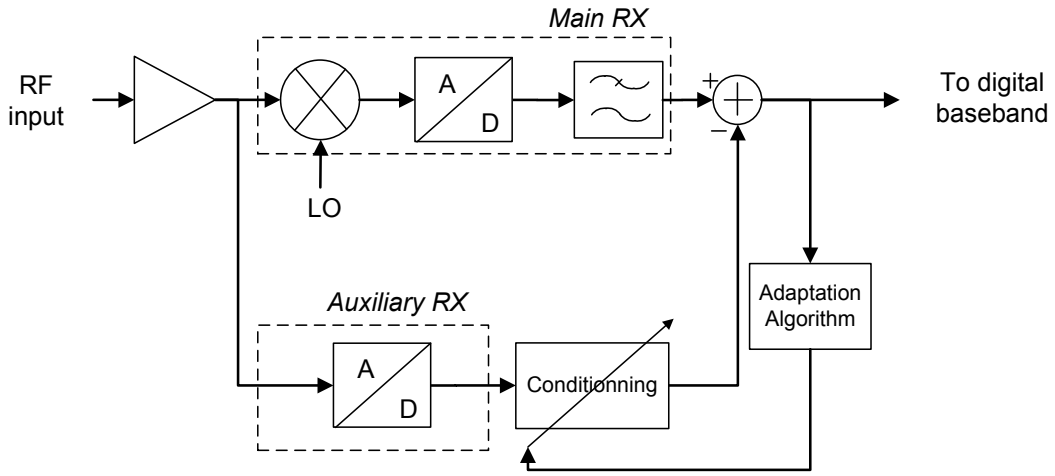


Fig 2. Use of an auxiliary low-resolution broad-band RX to mitigate impairments in a high-resolution narrowband RX

In addition, the low-size, low-power flexible wideband receiver designed on our work could contribute to allow competitive digital beamforming front-ends for scientific, aerospace, military applications, and wideband spectrum sensing front-ends for Cognitive Radios.

Publications and patents

Patent

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Peer reviewed conferences

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Workshops and others

Jamin O., "Broadband RF multi-channel cable receiver based on direct RF sampling" ; presentation to "Journées de la Radio Intelligente, Cognitive et Opportuniste", 2011, Télécom Paris

Jamin O., "RF Direct-Sampling for Cable Multi-Channel Transceiver"; presentation to "Gdr SoC-SiP", 2012, Lip6 Jussieu

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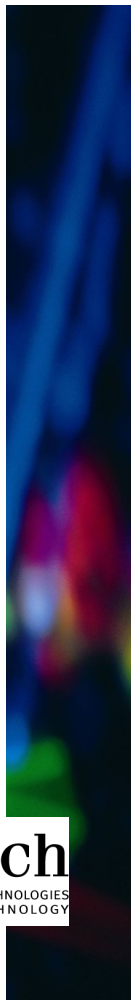
Broad-band Direct RF Digitization Receivers

ABSTRACT : The Holy Grail radio receiver architecture for Software Radio makes uses of RF direct digitization. The early RF signal digitization theoretically provides maximum re-configurability of the radio front-end to multiple bands and standards, as opposed to analog-extensive front-ends. In addition, in applications for which a large portion of the input signal spectrum is required to be received simultaneously, the RF direct digitization architecture could provide the most power-and-cost-effective front-end solution. This is typically the case in centralized architectures, for which a single receiver is used in a multi-user environment (data and video gateways) or in re-multiplexing systems (telecom satellites…). In these situations, this highly-digitized architecture could dramatically simplify the radio front-end, as it has the potential to replace most of the analog processing.

In this PhD thesis, trade-offs, from RF to DSP domains, which are being involved in direct RF digitization architecture, are deeply analyzed. The developed system-level framework is applied to the design of a cable multi-channel direct RF digitization receiver. Special focus is put on the design of an optimum RF signal conditioning, on the specification of time-interleaved analog-to-digital converter impairments, including clock quality, and on some algorithmic aspects (automatic gain control loop, RF front-end amplitude equalization control loop). A two-chip implementation is presented, using BiCMOS and 65nm CMOS processes, together with the block and system-level measurement results. The solution is highly competitive, both in terms of area and RF performance, while it drastically reduces power consumption, which validates the developed approach for a concrete product development.

Keywords : RF receivers, broad-band, ADC, software radio, system-level design, direct RF sampling, direct RF digitization, signal conditioning, Docsis, signal processing, semiconductors, time-interleaving, cable receiver, multi-channel,



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