

Wideband Analog-to-Digital Converter (ADC) design for power amplifiers linearization

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Thèse de doctorat

Wideband Analog-to-Digital Converter Design For Power Amplifiers Linearization

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Résumé

De nos jours, la consommation d'énergie devient un des principaux défis à surmonter dans le développement des réseaux de communications mobiles. L'amplificateur de puissance est le composant le plus gourmand en consommation d'énergie dans les stations de base. L'arrivée de la cinquième génération de téléphonie mobile avec ses bandes de communication plus larges et ses modulations complexes augmente encore plus les contraintes sur l'amplificateur de puissance. Pour palier ce problème, il est courant de faire appel à des techniques de pré-distorsion qui permettent de faire fonctionner l'amplificateur de puissance avec un meilleur rendement énergétique. Une contrainte importante dans la mise en oeuvre de cette technique est la numérisation de la sortie de l'amplificateur qui, dû aux non-linéarités, s'étale sur un spectre significativement plus large que le signal utile, environ 5 fois en pratique voire plus.

Habituellement, pour cette opération de numérisation, un Convertisseur Analogique Numérique (CAN) du type pipeline est utilisé car il permet d'obtenir des résolutions supérieures à 10 bits sur une bande de plusieurs dizaines voire centaines de MHz. Cependant, sa consommation d'énergie élevée pousse à explorer d'autres pistes. L'architecture "Multi Stage Noise Band Cancellation" (MSNBC) à base de modulateurs Delta Sigma a l'avantage de réaliser des dynamiques différentes par sous bande et est ainsi un candidat de choix pour le CAN de la boucle de retour des techniques de pré-distortion.

L'objectif de ce travail est de démontrer la faisabilité de l'architecture MSNBC qui jusqu'à présent a été uniquement étudiée au niveau système. Pour atteindre cet objectif, plusieurs études ont été menées sur des aspects spécifiques de cette architecture tels que l'implémentation de l'annulation du signal primaire à l'entrée des modulateurs secondaires et l'impact du retard de boucle sur sa qualité, le choix de la fréquence centrale des modulateurs primaire et secondaires, et la conception des filtres numériques pour l'annulation du bruit de quantification.

Ces études nous ont permis de proposer une architecture adaptée pour la numérisation d'un signal de bande RF 20 MHz avec des résolutions différentes par sous

bande. Une architecture Zéro-IF temps continu avec un modulateur primaire du second ordre et un modulateur secondaire du quatrième ordre avec des quantificateurs 4 bits a été adoptée. Cette architecture a été implémentée en une technologie CMOS 65 nm. Les simulations électrique du MSNBC 2-4 avec un signal LTE ont permis d'obtenir 84.5 dB de SNDR dans la bande principale et 29.2 dB dans la bande adjacente contenant les produits d'intermodulation.

Abstract

Power consumption is nowadays one of the main challenges to overcome in the development of mobile communications networks. The power amplifier (PA) is the most power hungry component in base transceiver stations. The upcoming fifth generation of mobile telephony with wider communication bands and complex modulations further increases the constraints on the PA. To overcome this problem, it is common to use pre-distortion techniques that enable the power amplifier to operate with greater linearity and efficiency. An important constraint in the implementation of this technique is the digitization of the output of the amplifier which, due to non-linearities, spreads over a significantly wider spectrum than the initial signal, about 5 times in practice or even more.

Pipeline Analog-to-Digital Converters (ADCs) are commonly used for this operation because it allows resolutions of greater than 10 bits to be obtained over a band of several tens or even hundreds of MHz. However, its high energy consumption pushes to find a better solution. The "Multi Stage Noise Band Cancellation" (MSNBC) architecture based on Delta Sigma modulators has the advantage of realizing different dynamics per subband and is thus a prime candidate for the feedback loop ADC of predistortion techniques.

The purpose of this work is to demonstrate the feasibility of the MSNBC architecture that has so far only been studied at the system level. To achieve this objective, several studies have been carried out on specific aspects of this architecture. This includes the implementation of the cancellation of the primary signal at the input of the secondary modulators and the impact of the loop delay on its quality, the choice of the center frequency of the primary and secondary modulators, and the design of the digital filters for quantization noise cancellation.

Our investigations allowed us to propose a suitable architecture to digitize a 20 MHz RF band signal with different resolutions per subband. A continuous time Zero-IF architecture with a second-order primary modulator and a fourth-order secondary modulator with 4-bit quantizers was adopted. This architecture has been implemented in a 65 nm CMOS technology. Transistor level simulations of the

2-4 MSNBC architecture simulations with an LTE test signal resulted in 84.5 dB SNDR in the main band and 29.2 dB in the adjacent band which contains the intermodulation products.

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List of Abbreviations

3GPP	3rd Generation Partnership Project
ACLR	Adjacent Channel Leakage Power Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
BP	Band-Pass
BTS	Base Transceiver Station
BW	BandWidth
CDMA	Code Division Multiple Access
CIFB	Cascade-of-Integrators Feedback Form
CIFF	Cascade-of-Integrators Feedforward Form
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DE	Drain Efficiency
DEM	Dynamic Element Matching
DPD	Digital Predistortion
DR	Dynamic Range
DSP	Digital Signal Processing
DT	Discrete-Time
DWA	Data Weight Averaging
EER	Enveloppe Elimination and Restoration
ELD	Excess Loop Delay
eMBB	enhanced Mobile BroadBand
ENOB	Effective Number Of Bits
ET	Envelope Tracking
EVM	Error Vector Magnitude
FBD	Frequency Band Decomposition
FOM	Figure Of Merit
GBW	Gain BandWidth (product)

IBN	In-Band Noise
ICT	Information and Communication Technology
IM	InterModulation
IoT	Internet-of-Things
ISI	Inter-Symbol Interferences
LIF	Low Intermediate Frequency
LSB	Least Significant Bit
LTE	Long Term Evolution
LUT	Look-Up Table
MASH	Multi-stAge Noise SHaping
MSNBC	Multi-Stage Noise Band Cancellation
NCF	Noise Cancellation Filter
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OBO	Output Back Off
OFDM	Orthogonal Frequency-Division Multiple-Access
OOBG	Out-Of-Band Gain
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PSD	Power Spectral Density
PVT	Process Voltage and Temperature
RF	Radio Frequency
RSTF	Residual Signal Transfer Function
RZ	Return-to-Zero
SAR	Successive-Approximation-Registers
SDR	Signal to Distortion Ratio
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SPI	Serial-to-Parallel Interface
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
UMTS	Universal Mobile Telecommunications System
WCDMA	Wideband Code Division Multiple Access
ZIF	Zero Intermediate Frequency

Introduction

The world of Information and Communication Technology (ICT) is nowadays dominated by telecommunications, mobile Internet and many wireless applications.[1]

In order to understand the rise to prominence of telecommunications and mobile internet, it is useful to briefly review the evolution of the various network technologies. Starting with the late 1980s, the 2G network was first rolled out. Its key attributes included digital encryption of telephone conversations and the enabling of rapid wireless penetration rates. Essentially, the advent of the 2G network acted as a catalyst for the mobile data services such as text messages, i.e. SMS. In the ensuing two decades, the 2G was replaced by the 3G and then 4G telecommunication network. The key advantages of the new networks include fast information transfer rate and mobile broadband access to mobile phones to name but a few. The implications for the business world were far-reaching. For instance, telephone companies started offering services such as MMS, video calls and mobile TV technologies. Other businesses seize these advantages to introduce disruptive innovation. For instance, the ride-hailing mobile application Uber has taken advantage of the opportunities available thanks to the 4G network to really disrupt the taxi industry. In a similar vein, Netflix leveraged the improved speed of data transfer to introduce their offering, which changed the paradigm in the media industry.

As I embark on this thesis, there are growing talks of the 4G being replaced by the 5G network. The Fifth Generation (5G) mobile networks will see the initial deployment around 2020, promising wireless download speed of 10 Gbps for eMBB (enhanced Mobile Broadband) [2], and subsequently enabling billions of wireless connected devices for IoT (Internet-of-Things), autonomous driving, remote surgery. According to the World Economic Forum, the 5G holds the promise of sparking a profound digital transformation. Figure 1 [3] gives an overview of the different areas where the 5G technology can make a noticeable impact. For instance, its low latency potential will be very important for the industry on high-frequency/algorithmic

[1] About $2-3\,\%$ of the world-wide energy consumption is for ICT, which causes about $3\,\%$ of the total CO2 emissions [1].

trading. Its reliability could transform the health care industry by enabling surgeons to remotely carry out complicated procedures on patients.



Figure 1: 5G mobile network applications

The usage cost of mobile services is likely to increase, and, in particular, the energy consumption might grow with the number of Base Transceivers Stations (BTS) and data centers in the network. Hence, as the demand for ICT services rises, higher and higher energy consumption is expected for mobile radio networks.

In order to preserve the environment, cellular network operators try to deploy various strategies to reduce energy consumption. BTS consume about 85 % of the total energy of the network [4]. Their power consumption depending on the size, the coverage area and the technology used. The main axes of finding out efficient ways to reduce the energy consumed are: the optimization of hardware, the usage of renewable energy sources and the smart usage of resources through power saving models and efficient algorithms.

For hardware optimization, the power is consumed by the following components:

- The rectifier transforms the signal from AC to DC. The efficiency of the rectifier is about 92 % for a conventional rectifier and about 97 % for the case of latest products, for amperage loads between $40 - 90\,\%$ [5].

- The Baseband Digital Signal Processing Circuit is considered as having a constant power consumption. This power is dissipated as heat and has to be removed, e.g., by the cooling system.

- The PA is a device that magnifies the amplitude of a signal. Radio-frequency (RF) PAs, such as the one used in cellular BTSs and broadcast transmitters, has an efficiency about 15 %. The excess energy is transformed into heat.

- The feeder is the cabling system connecting the BTS to the antenna. In conventional BTSs, antennas and equipments are a few meters apart, and connected through a coaxial cable or Remote Radio Heads (RRH). Its efficiency approaches 1 when using RRH, and 0.5 when using coaxial cabling [4].

- The cooling system to keep the temperature of most components of the BTS within specified design limits. Air conditioners, free ventilation, forced-air cooling and heat exchangers are often the choice for radio sites. Such cooling requires as much power as one third of the heat power generated inside the BTS [6].

Given the efficiency of each of those components, a useful manner to optimize the hardware power consumption of a base station is to focus on the component with the lowest power efficiency, the PA.

In order to save energy and achieve high efficiency, PAs need to operate in the saturation region [7]. However, PAs exhibit high nonlinear distortion in that region, and this creates problems related to preserving high signal quality. The main trends in the design of wireless transmitters remains to provide enhanced transmitter functionalities with Digital Signal Processing (DSP) by using linearization techniques. There are a number of linearization techniques to improve the linearity of the power amplifiers and which enable, at the same time, to improve the efficiency. One of them, the digital predistortion (DPD), is of particular interest because it benefits from the technical advances of the digital part and communications systems increasingly use digital modulation.

Its implementation, in current and future emission chains, is a relatively low extra cost in the digital part, however it requires a measurement of the distortion generated by the amplifier and thus, a possibly dedicated, feedback path to convert the distorted analog RF signal to digital domain. In this system the analog-to-digital converter which is in charge of the measurement of the distorted signal must meet the requirements on the signal resolution and bandwidth. These needs are quite challenging in the context of digital predistortion and, in addition, here too, its energy consumption must be as minimum as possible.

Latest communication systems use relatively wide bandwidths. The distorted signal contains unwanted signals called intermodulation products, and is characterized by a spectrum P times wider than the original, where P is the considered

intermodulation order. In practice, we aim at digitizing at least intermodulation products of order 5. In addition, these signals are centered at a high transmission frequency. We realize that in this type of application, which is the digital predistortion, validating the sampling theorem establishes the frequency converter to very high values if we do not reduce the center frequency of the signal to a low value. Second, the resolution conversion of these distorted signals must be very high: because, on the one hand, multi-carrier signals have very high dynamics and on the other hand, the distortions may be small changes in the original signal. Various techniques are used to increase the performance of Analog-to-Digital Converters (ADC) as time-interleaving often used with pipelined ADCs or the parallelization of processing such as processing with decomposition into smaller frequency bands. Among the various converters, $\Sigma\Delta$ modulators architectures are of particular interest: a high accuracy can be achieved for band-pass signals centered around high frequency with few components. Despite a strong limitation of the converter bandwidths due to their operating principle based on over-sampling, recent literature reports some circuits whose bandwidths allow to consider a possible use for broadband telecommunication applications. The purpose of this thesis is to develop and prove at silicon level an ADC for the measurement of the signal in the feedback path of DPD in base stations transceivers.

The remainder of the thesis proceeds as follows:

- Chapter 1 presents the architectures of PAs used in base station transceivers and their design constraints. It discusses several linearization techniques including digital predistortion. The proposed ADC specifications are then defined.

- Chapter 2 discusses the choice of the ADC type. It contains a discussion of the state-of-the-art $\Sigma\Delta$ ADCs and key ADC design parameters are explained.

- Chapter 3 shows the high level design choices and degrees of freedom of our proposed ADC. The chapter elaborates on the choice of architecture and analyzes the impact of non-idealities of the selected architecture. This chapter concludes with high level simulations results .

- Chapter 4 explains the choices made for the transistor level design of the proposed ADC. It contains a discussion of the floor plan, transistor level simulations as well as measurements results of the ADC.

Chapter I

From DPD to ADC Specifications

In typical mobile communications BTS, the Power Amplifier consumes 50-80 % of the total power consumption [8]. With the increasing demand for higher data transfer rates in new communication standards, the situation gets worse. Therefore, the PA needs to be more power efficient.

I.1 Power Amplifier

From that total DC power consumed, typically only approximately 30 % is converted into useful transmitted RF signals [9]. The main challenge in producing a high efficiency power amplifier in such applications is the high peak to average power ratio (PAPR) of the RF signal, which in some cases is in excess of 10 dB [8].

This is because the PA needs to be efficient not only at peak power but also at average power levels several dB's below where the PA would spend most of its time operating. As the demand for higher bandwidth increases, more complicated and dynamic modulation schemes are used, driving the signal PAPR increasingly higher. From a PA design standpoint, this puts a lot of pressure on the PA design community to provide solutions that continually improve PA efficiency and to react to the advancements in spectrally-efficient schemes, while respecting the stringent linearity requirements implicit in new wireless standards.

The 3G/4G wireless services not only have complicated modulations which reduce the Error Vector Magnitude (EVM) tolerance for systems, but also bring in non-constant-amplitude waveforms. The PAPR for the amplitude of EDGE, WCDMA and CDMA2000 is 3.2-5 dB. [10] Furthermore, new spectrally efficient protocols employed in 4G communication systems utilize orthogonal frequency-division multiplexing (OFDM). These OFDM signals have even high PAPRs on their amplitude waveforms. The uplink PAPR of LTE is in the order of 7.5 dB [10] and >10 dB,

respectively.

	GSM	EDGE	UMTS	CDMA2000	LTE
Max Power (dBm)	35	29	26	25	25
Min Power (dBm)	7	7	-48	-48	-40
PAPR (dB)	0	3.4	3.4	3.5-5	6-8
EVM limit	-	9%	17.5%	-	12.5%
ACLR1 (dBc)	20	20	33	28	44.2
ACLR2 (dBc)	60	60	43	43	44.2

Table I.1: Uplink Transmitters Requirements for PAs

Table I.1 contains some of the most relevant uplink transmitter performance parameters for 2G GSM, 3G WCDMA/CDMA 2000, and 4G LTE/WiMAX. A saturated or switching PA can deliver a maximum output power of 35 dBm and an efficiency of >60 % at this power level for GSM (an industry benchmark). The main impact of EDGE is to introduce an amplitude component to the modulation scheme (8PSK). Maximum output power is reduced to 29 dBm, partly in recognition of the crest factor of 3.2 dB and partly due to the need to use a linear amplifier with reduced efficiency. Power control range is still a modest 22 dB. The industry-driven target figure for PAs used for EDGE signals is 45 %. As far as WCDMA and CDMA2000 are concerned, the challenge for efficiency recovery is similar to EDGE despite the apparent threat from an increased power-control in the range of 75 dB. Fortunately, power budgets in the transmitter are such that worthwhile efficiency enhancement only applies to the top 20 dB dynamic range.

Unlike constant-amplitude modulations such as GSM, the non-constant-amplitude modulated signals with the inherent high PAPR and wide bandwidth require highly linear PAs having very low signal distortion. One way for the PA to satisfy the stringent linearity requirements is to back off from its compression region. This is a major bottleneck for realizing highly efficient mobile transmitters.

I.1.1 State-of-the-Art of PAs Used in BTS

The efficiency of a PA, or drain efficiency (DE), is defined as the ratio of the fundamental output power to the DC supplied power. Another metric that is often used is power added efficiency (PAE) which takes into account the gain of the PA, and is defined as the ratio of the difference between output and input fundamental power over the DC supplied power. For a PA with high gain, DE and PAE will be similar, but if the PA gain goes below for example 10 dB, the DE and PAE difference would

be more than 10 % [11].

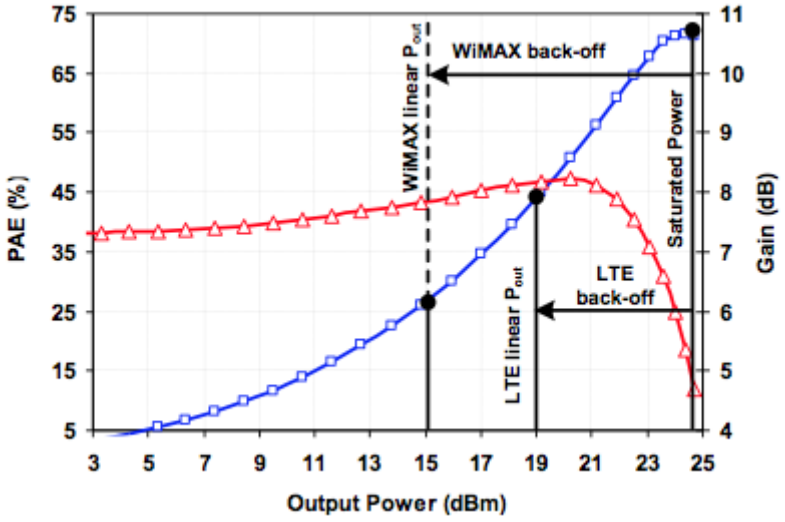


Figure I.1: Power Added Efficiency of a PA

Figure I.1 shows the efficiency of a typical 1-stage common-emitter SiGe PA. The PAE reaches the peak value at saturation power, but drops dramatically at back-off that depends on different PAPR values and different linearity specifications. This is opposed to saturated PAs that work with constant-amplitude signals but exhibit high efficiency.

Several techniques have been developed in improving PA efficiency. The basis of these techniques is the reduction of the overlapping region between the current and the voltage at the device current generator plane by reducing the conduction angle, as well as increasing the drive level to an optimum point [12].

While high-efficiency PA modes yield promising efficiency gains, they are only efficient near peak power when the device starts to go into compression. However, when the PA operates below peak power under output back-off (OBO) conditions, the efficiency drops significantly. Signals with high PAPR such as LTE and WCDMA present a challenge to a PA in maintaining efficient operation over dynamic range, as the PA spends most of its time in output back-off.

Therefore, in this backed-off region of operation, a different solution is needed to maintain the same efficiency performance achieved at peak power. The 5G waveforms with high PAPR will degrade PA's efficiency at power back-off, making both Doherty PA and supply-modulated PA (envelope tracking (ET), envelope elimination and restoration (EER)) very attractive for efficiency enhancement of 5G PA design.

Envelope Tracking PA

The envelope tracking technique modulates a device's DC supply according to the input envelope magnitude to improve the efficiency during output back-off. The approach evolved from the EER amplifier technique of Kahn [13]. In ET, an envelope amplifier is used to bias the drain of the RF PA based on the input envelope signal as shown in Figure I.2. The envelope information is obtained either through an envelope detector on the input path or digitally from baseband processing. Its relationship with the drain bias voltage is defined by an envelope shaping function to generate the desired ET system-level efficiency shown in Figure I.2. The overall efficiency of an ET PA is calculated as the product of the efficiency of the RF PA and the envelope amplifier. Therefore to improve the ET PA efficiency, careful design considerations must be given to both amplifiers.

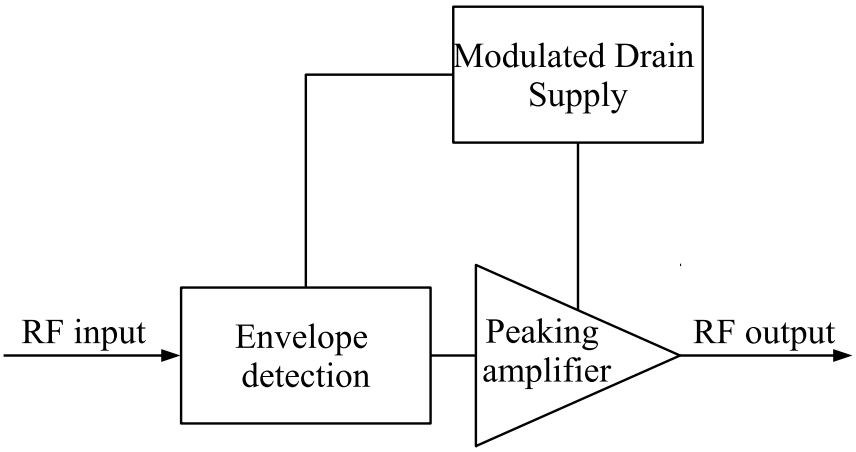


Figure I.2: Enveloppe Tracking PA

One constraint to implement ET in macro base stations is the lack of efficient, linear and sufficiently wide-band high-power supply modulators [14]. This limitation is mainly due to the trade-off between the transistor breakdown voltage and its switching speed, hence ET implementations tend to be limited to low power applications such as mobile phones [15]. A simplified version of ET called the average power tracking (APT) is widely used for mobile phones PA's where the supply voltage is changed slowly. However with the advancement of low-power modulators, a complete ET system is emerging as the future trend, especially with ET's ability to work over extended bandwidths and accommodate multi-band operation [16]. The other issue with the ET supply modulator is that it can potentially be a source of distortion for the RF PA. It therefore makes sense that much of the ET research focus is around the ET supply modulator, for example in [17],[18].

Recent works in this field have further improved efficiency numbers or higher frequency of operation. A GaN HEMT operating in class-E is used in [19] in an ET system at 2.6 GHz. With the RF PA having a drain efficiency of 74 % and the ET modulator at 92 % efficiency, the overall ET efficiency was 60 % when a 6.5 dB PAPR 10 MHz LTE signal was applied producing a 40 W average output power. In [20] an ET PA utilizing a GaN device operating in inverse class-F at 880 MHz was able to produce a PAE of 53 % at 7.4 W output power for a 6.6 dB PAPR 20 MHz LTE signal. A higher bandwidth was achieved in [21] where an X-band GaN MMIC PA was used in ET for a 60 MHz LTE signal with 6.6 dB PAPR. With the RF PA operating in class-E at 9.23 GHz, the overall PAE achieved was 35 % at 1.1 W average output power.

Doherty PA

The Doherty architecture was first introduced by William H. Doherty in 1936 to improve the PA efficiency in amplitude modulation (AM) broadcasting applications [22]. The basic form of a Doherty PA consists of a carrier amplifier, typically biased in class-AB, and a peaking amplifier biased in class-C as shown in Figure I.3. This classical structure can maintain high-efficiency operation over 6 dB OBO using the concept of load modulation [23].

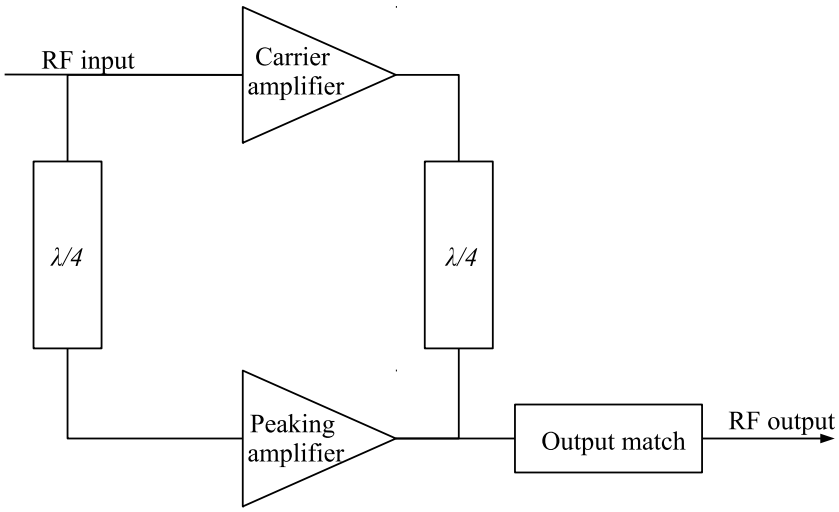


Figure I.3: Doherty PA

The high-efficiency output range can theoretically be extended further up to 12 dB OBO using a 3-way [24] or even 18 dB for a 4-way Doherty [23]. An asymmetric Doherty amplifier, where the peaking device is larger than the carrier device is also used to extend the high-efficiency region as for example up to 12 dB OBO as

demonstrated in [25], with only a 7 %-point drop over the dynamic range. The application of an "envelope tracking" technique on the gate bias of the peaking device was presented in [26] to address load modulation issues that are causing the dip in the high efficiency region. The work in [27] tackles this by applying ET on the drain bias of the peaking device, and a relatively flat high efficiency performance was achieved over 18 dB of dynamic range in a simulation environment. However the analysis did not include a fabricated hardware and the efficiency of the drain supply modulator was not considered.

The main limitation of Doherty PA is the narrow bandwidth introduced by the use of the quarter wavelength combining transformer. This presents a challenge in 4G LTE where not only the bandwidth is wider, but with carrier aggregation, PA's ideally need to accommodate multiple-bands. Research focusing on extending the bandwidth of a Doherty PA is ongoing and recent examples include [28] which is capable of handling a 100 MHz instantaneous bandwidth, and [29] where a 1.5 - 2.14 GHz design was developed corresponding to a 35 % fractional bandwidth.

In [30], a multiband Doherty was designed and fabricated for 1.9, 2.14, and 2.16 GHz obtaining a 60 % PAE at 6 dB OBO. In a more recent study, a quad-band Doherty PA was developed at 0.96, 1.5, 2.14, and 2.16 GHz, although with a relatively lower PAE at 6 dB OBO, ranging from 20 to 43 % [31]. There are also patented wideband and multiband Doherty PA's as shown in [32].

Doherty is currently the architecture of choice for base station power amplifiers [23], mainly because of its relative simplicity in comparison with other highly efficient solutions such as ET.

I.1.2 Linearization Techniques

The design of the power amplification stage is driven by a linearity and power efficiency tradeoff. Doherty and ET power amplifiers have a high efficiency and operate in compression or even saturation. Consequently, it produces signal distortions. Thus, the need for some form of linearization is essential.

"Linearization" is a process which enables linear amplification of a signal in the presence of nonlinear components, by canceling the distortion introduced by those components. There are 3 main techniques to improve linearity of power amplifiers: feedback, feed forward and predistortion.

Table I.2 compares those techniques in terms of size, bandwidth, efficiency and harmonic distortion cancellation. Depending on the application and the requirement of a system, one technique is preferred to another.

The feedback technique has moderate linearity results and is simple to imple-

Technique	Cancellation	Bandwidth	Efficiency	Size
Feedback	Low	Low	Medium	Medium
Feedforward	High	High	Low	Large
Predistortion	Medium	High/Medium	High	Small

Table I.2: Comparison of PAs linearization techniques

ment. Moreover, this technique decreases the gain of the system, and there are some stability issues to deal with. Its narrow band of operation, makes it not suitable for 4G/5G mobile standard.

The concept of feedforward systems is simple, but its hardware implementation is quite costly.

Feedforward methods exhibit a good linearization performance with a high stability and wideband signal capability. The feedforward technique is historically less popular and is mostly applied in base stations. However, it has low efficiency and high complexity resulting in the big size of the circuit and high cost.

For example, feedforward is mainly used in base station transceivers instead of PA handsets because of its high cost. However, with all the progress made in the digital field and the need to integrate and miniaturize systems, DPD is used in many applications nowadays.

State-of-the-art power amplification systems often use a Doherty PA for high efficiency at output power backoff, and a digital predistorter to restore the required linearity performance. Digital predistortion is currently the preferred linearization technique and is widely used for applications with, typically, up to 20 MHz bandwidth. [33]

I.2 Digital Predistortion Technique

Predistortion is the most popular linearization technique of power amplifiers today. This technique consists in applying the inverse characteristics of a PA to the input signal before feeding it to the PA, so that the cascade behaves as a linear amplification system, as presented in Figure I.4. Thus, this inverse function called Predistorter compensates for AMAM and AMPM distortions.

I.2.1 DPD Implementation

The predistortion function can be implemented with analog components, or DSP operations and digital components. Then we talk about Analog and Digital pre-

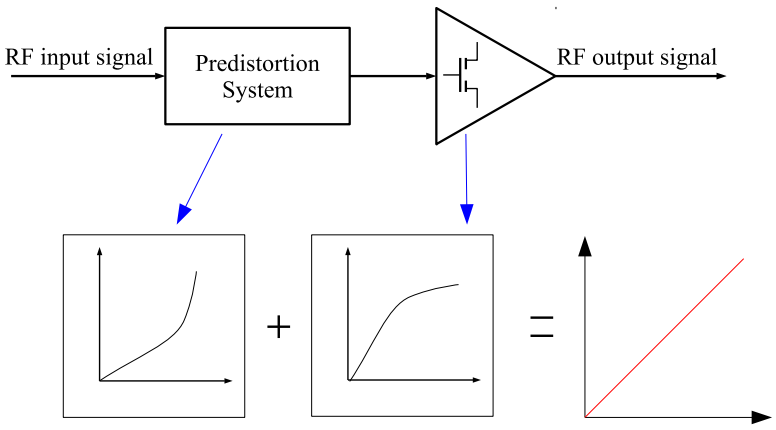


Figure I.4: Predistortion principle

distortion. Analog predistortion uses components like diodes and FET for implementing the predistorter. The cubic analog predistortion technique mainly uses non linear components, and RC circuit for phase shift which aims to eliminate 3^{rd} and 5^{th} order distortion. The diode/FET analog predistortion uses a parallel diode or a FET transistor for implementing the inverted magnitude and phase of the PA transfer function.

Analog predistortion is not adapted to cancel high order effects due to signal expansion and compression which are more difficult to handle in analog domain compared to digital. Moreover, analog predistortion is not well suited to system with high memory effects because this requires the implementation of a high number of analog delays. The main advantages of the analog predistortion are simplicity of realization, low cost, simple integration procedure, and possibility to linearize wideband power amplifiers. However this technique has small-to-moderate linearizing performance, power loss in the additional RF components which decreases the overall efficiency, and difficulty in providing adaptation, which significantly increases complexity of the circuit.

With the progress of DSP and FPGA, processors can nowadays do more complex operations with very good accuracy at a very low price. Digital predistortion has thereby become a great linearization technique research area for the last years as DSP are used to estimate the PA model and calculate the predistortion function. DSP increases the possible number of algorithms that can be used to estimate PA characteristics. Combined with feedforward or feedback, DPD benefits from high flexibility, controllability and possibilities to provide algorithm.

Depending on where the predistortion is applied, predistortion can be implemented in RF, IF or baseband. When the predistorter is applied before the up-

conversion, we talk about baseband predistortion. When the signal is up-converted before being predistorted, it is an RF predistorter and when it is between two up-conversion, it is called intermediate frequency (IF) predistortion.

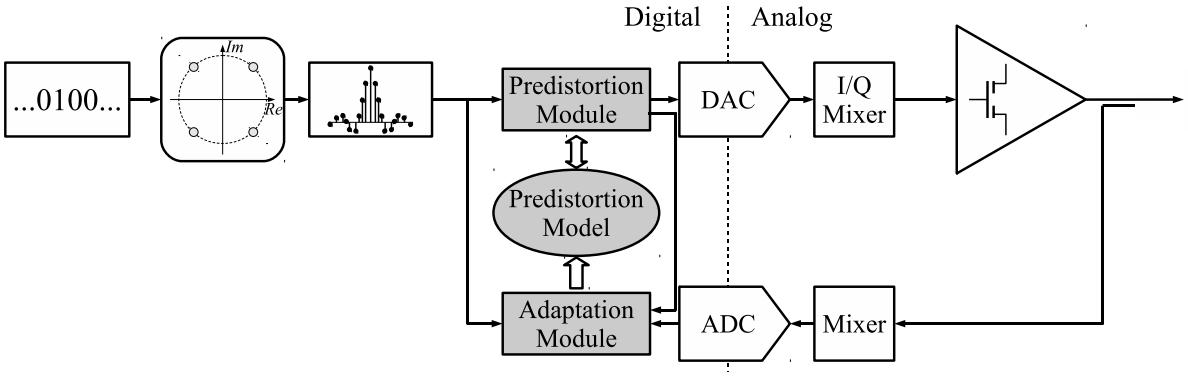


Figure I.5: Main components of a DPD system

A simplified DPD architecture in Figure I.5 allows us to identify conceptually the main subsystem components of a DPD system:

- Components in the transmission and acquisition paths: mixers and the PA.
- Data Converters: the ADC and DAC.
- DSP and control system: digital hardware for the predistorter.

Each of the subsystems contributes to the design targets which are evaluated in terms of linearity, dynamic range, bandwidth, power consumption and hardware cost. However, new communications bandwidths lead to high design constraints on the ADC.

I.2.2 ADC Implementation Trade-offs

Although it already seems to be a well-established technique at the current stage, DPD is still facing new challenges. New issues are coming with recent modulation schemes and multi-band scenarios presenting higher PAPR leading to higher order of non-linearity for the PA. This trend has a large impact on DPD design in many aspects, not the least of which is the wide band signal to be processed [34]. DSPs and Data converters are highly impacted by this evolution because the number of coefficients required to model the PA inverse transfer characteristic increases and at least 5 or 7 times the original signal bandwidth have to be processed which is a huge band. Generally, the DPD system contains ADCs to sample the PA output and feed it back to the DPD, in which the transmission path and acquisition path are both based on direct conversion structure.

One issue relating to ADC in the acquisition path is the resolution. Before training the DPD model, the output signal of the PA is digitized. The number of quantization bits depends on the actual system requirement. In order to have a noise floor at $-80\,\mathrm{dBc}$, a 14-bit ADC is needed. Designing a 14-bit ADC is challenging and costly [35] for the considered bandwidth (hundreds of MHz). It is therefore desirable to reduce the resolution; however, this is not a straightforward task, since reducing the resolution of ADC is equivalent to increasing the noise floor of the feedback signal, which is critical to the accuracy of DPD modeling. Liu et al. [36] proposed a method to reduce the ADC dynamic range, but a minimum 8-bit ADC is required to achieve linearization performance comparable to the conventional DPD.

Besides the resolution, the main issue relating to ADC in DPD implementation is the bandwidth requirement of the feedback path that is used to capture the output signal from the PA for the purpose of model extraction. In DPD, the bandwidth of the feedback path usually requires five times the signal bandwidth. For an acquisition path that is based on direct conversion structure, for instance, the sampling rate of the ADCs should be at least 500 MHz if an LTE-Advanced signal is applied. The existing and forthcoming data converter technologies could hardly meet this requirement.

Some solutions have been proposed to reduce the signal bandwidth requirement. The band-limited method was proposed in [37], but requires an extra bandpass filter in the RF transmit chain that is difficult and costly to design. The analog aliased sampling method in [38] can reduce the sampling rate, but it needs additional analog aliasing operation. The spectral-extrapolation-based algorithm was reported in [34], and a forward model was first carried out and then DPD coefficients can be estimated. In [39], a two-stage DPD, i.e., a static nonlinear box cascaded with a dynamic weak nonlinear box, was proposed to decrease the feedback bandwidth. All the methods mentioned above require the acquisition bandwidth not narrower than the signal bandwidth.

There have been substantial research efforts over the past 20 years with respect to developing efficient and elaborate DPD techniques for various single-band transmission schemes where linearization for the whole transmit band is essentially pursued. These conventional DPD approaches take as their inputs the full composite transmit band, and we thus refer to these DPD approaches as full-band DPD.

I.3 ADC Specifications for DPD

The feedback path of a DPD system can be considered as a direct conversion receiver (DCR). DCRs suffer from RF and baseband impairments such as I/Q imbalance and nonlinear distortions [40]. In order to set the design parameters for the ADC in the full-band DPD feedback path, we will successively consider different nonlinear effects and evaluate their impact on DPD correction.

For this study, the correction performance are simulated using a 20 MHz mono-carrier LTE signal. This signal is distorted using the memory polynomial PA model proposed in [41]. The linearization of this system is achieved with a memory polynomial model identified by a least-square method [41]. The nonlinear order of the inverse model is set to 9 and its memory depth is 3 in order to provide 55 dB adjacent channel power ratio and 0.2 % error vector magnitude when all blocks in the feedback path are ideally linear and there is no quantization error. This configuration exhibits some margins compared to the standard specifications.

I.3.1 Mixer I/Q Imbalance

As a first step, we focus on the effect of the I/Q imbalance. I/Q imbalance is assumed to be caused by the mixer and the baseband I/Q paths. We assume in this subsection that the mixer I/Q imbalance predominates over the baseband I/Q imbalance and there is no quantization error. As explained in [40], the I/Q imbalance can be modeled on the complex baseband signal with the following equation:

$$\tilde{y}(t) = \frac{1+g_m\,\mathrm{e}^{-j\Phi_m}}{2}\,y_{att}(t) + \frac{1-g_m\,\mathrm{e}^{j\Phi_m}}{2}\,y^*_{att}(t), \tag{I.1}$$

where $\tilde{y}(t)$ and $y_{att}(t)$ are respectively the I/Q imbalanced and the ideal baseband complex envelope, g_m is the relative amplitude mismatch between I and Q branches, Φ_m is the phase mismatch and $(\cdot)^*$ denotes the complex conjugate.

The upper and lower parts of Figure I.6 show respectively the ACPR and the EVM versus the relative amplitude mismatch g_m. In both graph, each line corresponds to a given phase error Φ_m ($\pm 20°$, $\pm 13°$, $\cdots$, $0°$). As expected, the worst results are achieved for large values of phase error and large relative amplitude mismatch. It can be seen on Figure I.6 (a) that the relative amplitude mismatch must be such that $0.9 \leq g_m \leq 1.1$ and the phase error should be less than about $10°$ to meet the 3GPP LTE standard requirements [42]. Regarding the EVM (Figure I.6 (b)), the standard requirements are met for the same range of g_m and Φ_m as ACPR.

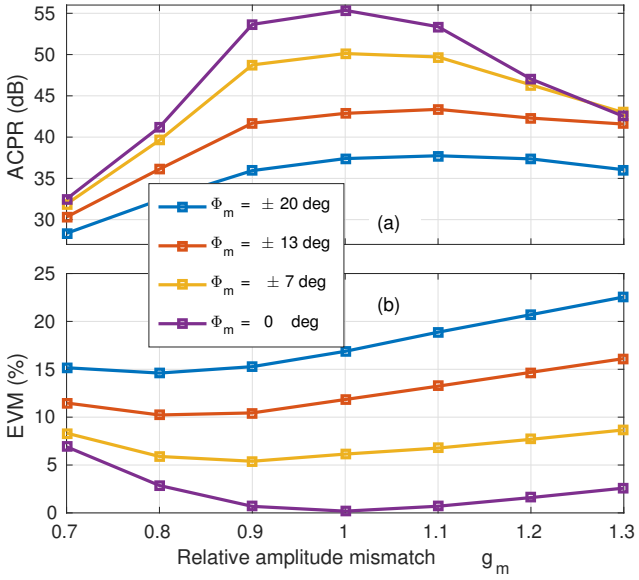


Figure I.6: DPD performance in terms of ACPR (a) and EVM (b) vs I/Q mismatch: simulation results

I.3.2 Fullband Nonlinear Feedback Path

The effect of a nonlinear distortion generated in the feedback path is now considered. This distortion may be caused by compression in the active blocks of the feedback path. We assume that distortions are modeled by a 3rd order nonlinearity and that higher orders nonlinearities have minor effects. As mentioned in [40], this nonlinearity can be modeled on the complex baseband signal by:

$$\tilde{y}_{BB}(t) = y_{att}(t) + \alpha \left([y^*_{att}(t)]^2 + 3\, y^2_{att}(t) \right) y^*_{att}(t), \tag{I.2}$$

where α is the nonlinearity coefficient. We define the fullband signal to distortion ratio (SDR) as:

$$SDR = \frac{P_{mean}\left\{ y_{att}(t) \right\}}{P_{mean}\left\{ \alpha \left([y^*_{att}(t)]^2 + 3\, y^2_{att}(t) \right) y^*_{att}(t) \right\}}, \tag{I.3}$$

Figure I.7 shows the ACPR and EVM of the linearized PA output obtained by simulation. As long as the distortions generated by the feedback path are low enough ($SDR \geq 55\,\text{dB}$), correction performance are maximum. For $SDR \leq 55\,\text{dB}$, the ACPR drops. The EVM is less sensitive to this 3rd order nonlinearity as it remains constant for a wider range of distortion level: its effect is significant for $SDR \leq 40\,\text{dB}$. In order to cope with circuit non idealities, the target linearity of the ADC is set to 60 dB.

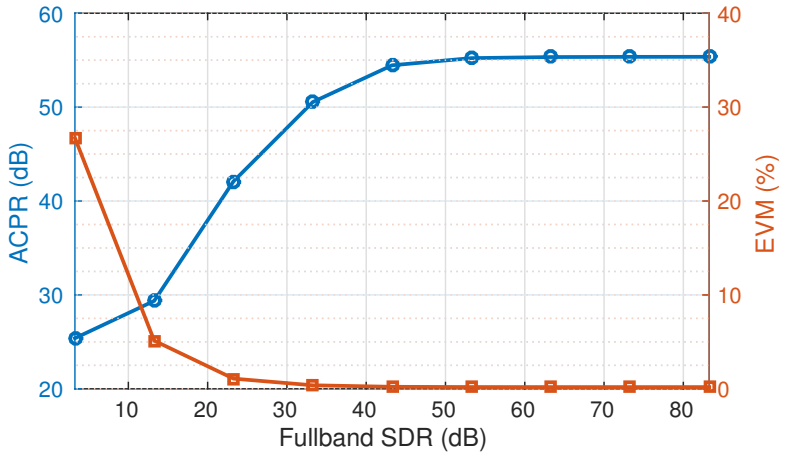


Figure I.7: DPD performance in terms of ACPR and EVM vs nonlinearity of the feedback path

I.3.3 Subband ADC Requirements

The non-linearity study presented above assumed that a full-band single ADC is used to digitize the signal in the feedback path of the DPD. This ADC needs to have a high dynamic range in $M \times BW$ bandwidth in order to capture both high power signals and low power distortion signals (IMD products).

Subband DPD [43] is particularly attractive as it relaxes the design of the ADC. With the subband approach, as presented in Figure I.8, the main signal band and adjacent bands will have different DR requirements.

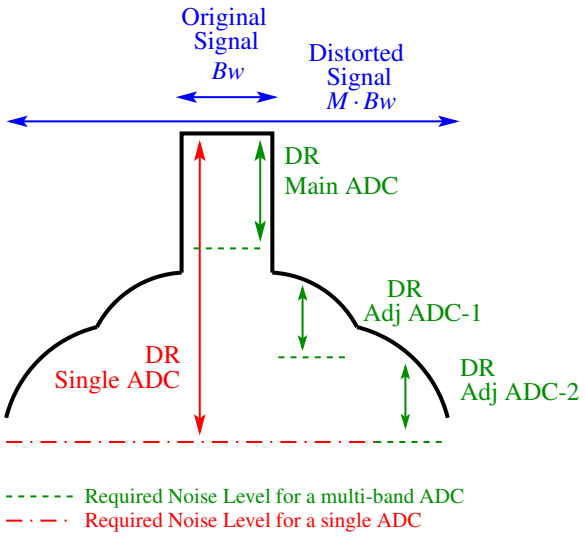


Figure I.8: Single ADC vs. multi-band ADC

The digitization is performed with several ADCs, one for the main signal and

one for each subband. This architecture provides new degrees of freedom such as the possibility of having different quantization noise level for each subband. The ADC dimensioning is now studied assuming a multi-band ADC.

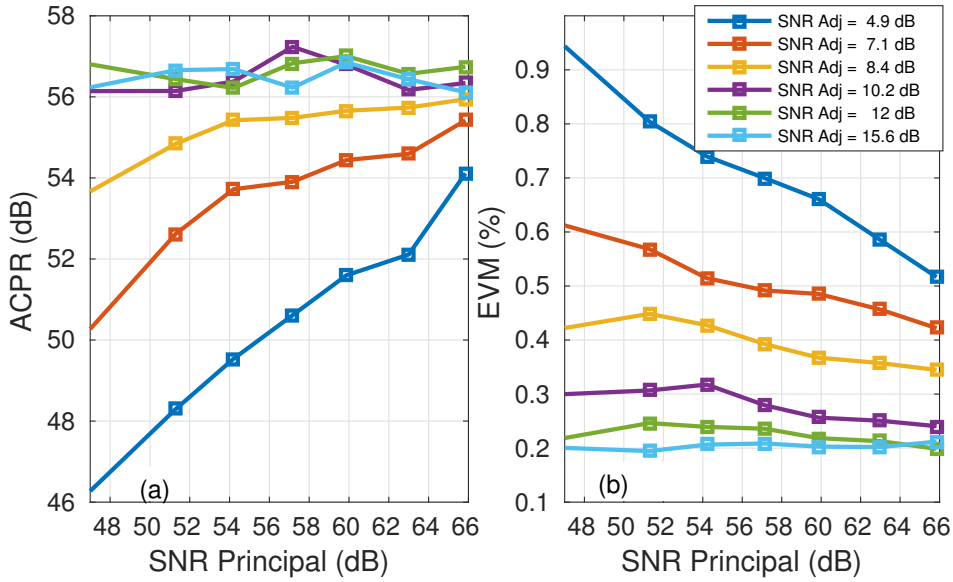


Figure I.9: DPD performance in terms of ACPR and EVM vs. subband quantization SNR; ACPR without DPD: 30 dB ; EVM without DPD: 4.3 %

The difference in DR requirements can be achieved by setting different quantization step sizes for the modulator quantizer in each subband. The effect of this subband quantization on the linearization results is simulated and ACPR and EVM are shown in Figure I.9. The x-axis is the SNR in the principal subband, which corresponds to the ideal 20 MHz transmit band and each colored line represents a specific SNR in the 20 MHz adjacent subband.

As expected, the higher the SNR, the better the ACPR and EVM. The ACPR is independent of principal subband SNRs between 48 and 66 dB for adjacent subband SNR greater than 10.2 dB. The EVM has a similar characteristic for adjacent subband SNRs greater than 12 dB.

By considering the input signal peak-to-average power ratio in these simulation results, the minimum performance of a multi-band ADC is set to 60 dB SNR in the principal subband and 22 dB SNR in the adjacent subband. [1]

[1]The SNR in the adjacent subband may seem low. However the power of the signal in this subband is very low. For sake of clarity, the detailed spectrum decomposition is not discussed here.

I.4 Conclusion

In this chapter, we saw several techniques to solve the linearity and efficiency trade-off of RF power amplifiers in base station transceivers. DPD is an attractive linearization technique which is nowadays extensively used. Non-linearities in the feedback path of DPD alter the signal used for the PA inverse model computation. Simulations show that for some distorsion levels, DPD is not significantly affected and for high distorsion levels, DPD performance are reduced because the extracted PD model is erroneous. In case of a full-band DPD for LTE applications, the feedback ADC should at least have 60 dB SNR in $M \times BW$ with M is the highest significant nonlinear order at the output of the PA and BW the input signal bandwidth. For a sub-band DPD approach the main sub-band ADC should at least have 60 dB SNR and adjacent sub-bands should have 22 dB SNR.

With these requirements, several ADC architectures can be used to digitize the attenuated output of the PA in a DPD system.

Chapter II

Analog-to-Digital Converters State-Of-The-Art

An Analog-to-Digital Converter transforms real world signals like temperature, voltage, light intensity into a digital signal. This digital signal can thus be easily computed, processed or stored. In DPD for example, digital signals are required to estimate the Power Amplifier model and apply predistortion algorithms. Thus, the accuracy of the analog-to-digital converter is crucial as it affects the PA model calculation.

II.1 A/D Conversion

Analog signals are converted in the digital domain with two functions: sampling and quantization.

II.1.1 Sampling and Quantization

Analog signals are continuous both in time and amplitude and their spectrum contains non-zero tones in a finite frequency band as an effect of their continuity in amplitude. The analog-to-digital conversion requires the analog input signal to firstly be sampled by a sample-and-hold which transforms it into an analog, discrete-time signal, only changing its amplitude at periodic intervals. Because sampling introduces instantaneous amplitude changes in the analog signal, the spectrum of the sampled signal has infinite bandwidth, by replicating the input signal spectrum around the multiples of the sampling frequency. A bandwidth constraint on the analog input should then be taken into account.

According to the Nyquist Theorem, to prevent information loss, a signal must

be sampled at a minimum rate of $f_N = 2\ BW$, often referred to as the Nyquist frequency. Sampling with frequencies lower than f_N introduces aliasing which changes the image of input signal spectrum in the sampled signal. Aliasing defines the overlapping of the input signal spectrum with the first replica of itself introduced by sampling at $2 \cdot f_N$. On the basis of this criterion, ADCs in which analog input signal is sampled at the minimum rate ($f_s = f_N$) are called Nyquist rate ADCs. Conversely, ADCs in which $f_s > f_N$ are called oversampling ADCs. How much faster than required the input signal is sampled is expressed in terms of the oversampling ratio (OSR), defined as

$$OSR = \frac{f_s}{2 \cdot BW} \tag{II.1}$$

The oversampling process influences the anti-aliasing filter (AAF) requirements of the ADC as showed in Figure II.1. In Nyquist-rate ADCs, the input signal bandwidth BW coincides with $f_s/2$, aliasing will occur if the input signal contains frequency components above $f_s/2$. High-order analog AAFs are thus required to implement sharp transition bands capable of removing out-of-band components with no attenuation of the signal band.

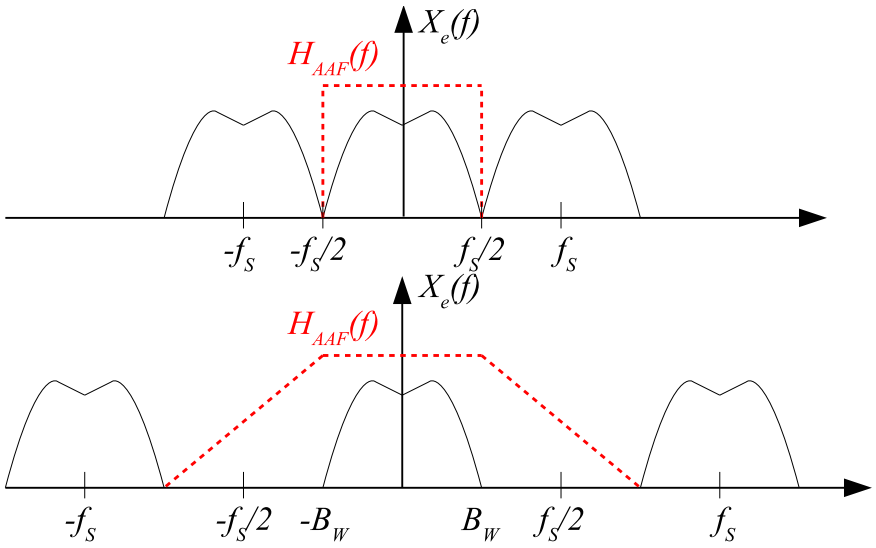


Figure II.1: AAF requirements

Given that $f_s/2 > BW$ in oversampling ADCs, the replicas of the input signal spectrum that are created by the sampling process are farther apart than in Nyquist-rate ADCs. Thus, frequency components of the input signal in the range $[BW, f_s - BW]$ do not alias within the signal band, so that the filter transition band can be smoother. This greatly reduces the order required for the AAF and simplifies its design.

The quantization operation consists in sampling the signal in the amplitude domain as presented in Figure II.2. Input amplitudes within the full-scale (FS) input range $[-X_{FS}/2, +X_{FS}/2]$ are rounded to 1 out of the 2N (where N is the resolution of the quantizer) different output levels, which are usually encoded into a binary digital representation.

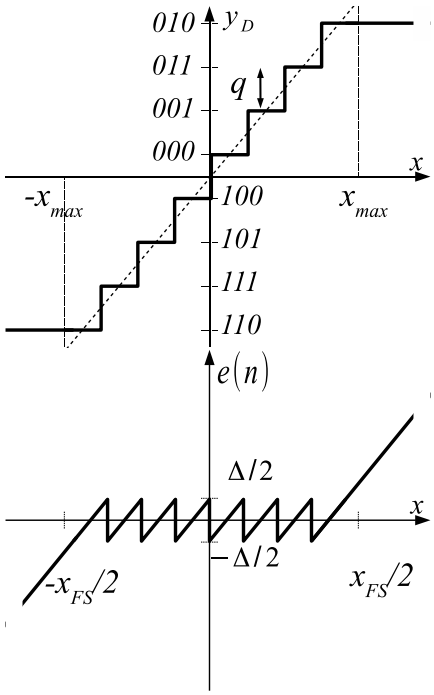


Figure II.2: N-bit quantization operation

If these levels are equally spaced, the quantizer is said to be uniform and the separation between adjacent output levels is defined as the quantization step

$$\Delta = \frac{Y_{FS}}{2N-1} \tag{II.2}$$

where Y_{FS} stands for the full-scale output range. The quantizer operation thus inherently generates a rounding error that is a nonlinear function of the input. If $q(n)$ is kept within the range $[-X_{FS}/2, +X_{FS}/2]$, the quantization error $e(n)$ is bounded within $[-\Delta/2, +\Delta/2]$. Assuming $q(n)$ changes randomly from sample to sample within the range $[-\Delta/2, +\Delta/2]$, $e(n)$ will also be uncorrelated from sample to sample. Under these requirements, the quantization error can be viewed as a random process with a uniform probability distribution in the range $[-\Delta/2, +\Delta/2]$. The power emerging from the quantization error can thus be computed as

$$\bar{e^2} = \sigma_e^2 = \int_{+\infty}^{-\infty} e^2 PDF(e) de = \frac{1}{\Delta}\int_{+fs/2}^{-fs/2} e^2 de = \frac{\Delta^2}{12} \tag{II.3}$$

The former assumption implies that, the power of the quantization error will also be uniformly distributed in the range $[-fs/2, +fs/2]$, yielding to:

$$\bar{e^2} = \int_{+\infty}^{-\infty} S_E(f)df = S_E \int_{+fs/2}^{-fs/2} df = \frac{\Delta^2}{12} \tag{II.4}$$

Therefore, the power spectral density (PSD) of the quantization error in the range $[-fs/2; +fs/2]$

$$S_E = \frac{\Delta^2}{12fs} \tag{II.5}$$

On the basis of this approximation of the quantization error to a white noise, the performance of ideal ADCs can be easily evaluated.

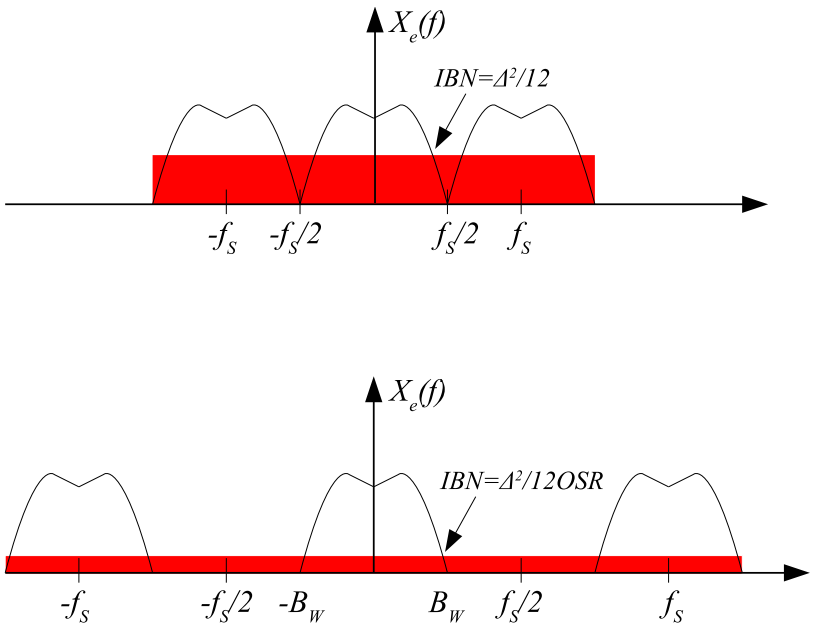


Figure II.3: Quantization noise in Nyquist and oversampled ADCs

For a Nyquist ADC, all the quantization noise power falls inside the signal band and passes to the ADC output as part of the input signal itself as illustrated in Figure II.3. Conversely, if an oversampled signal is quantized, because $f_s > 2BW$, only a fraction of the total quantization noise power lies within the signal band. The in-band noise power (IBN) caused by the quantization process in an ideal oversampling ADC is thus,

$$IBN = \int_{+BW}^{-BW} SE(f)df = \int_{+fs/2}^{-fs/2} \frac{\Delta^2}{12fs} df = \frac{\Delta^2}{12OSR} \tag{II.6}$$

so that the larger the OSR, the smaller the IBN.

Data converters are all evaluated by some performance metrics which allows to compare them and helps to select the appropriate converter for a given specification.

II.1.2 Performance Metrics

Most Analog-to-Digital Converters performance metrics are obtained by translating the output signal of the ADC in the frequency domain. The most commonly used dynamic performance are expressed with Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), Signal-to-Noise plus Distortion Ratio (SNDR), Dynamic Range (DR), Spurious Free Dynamic Range (SFDR).

Those metrics are illustrated in a signal spectrum in Figure II.4, where exemplarily a flat noise floor with a one tone signal and its harmonics are illustrated.

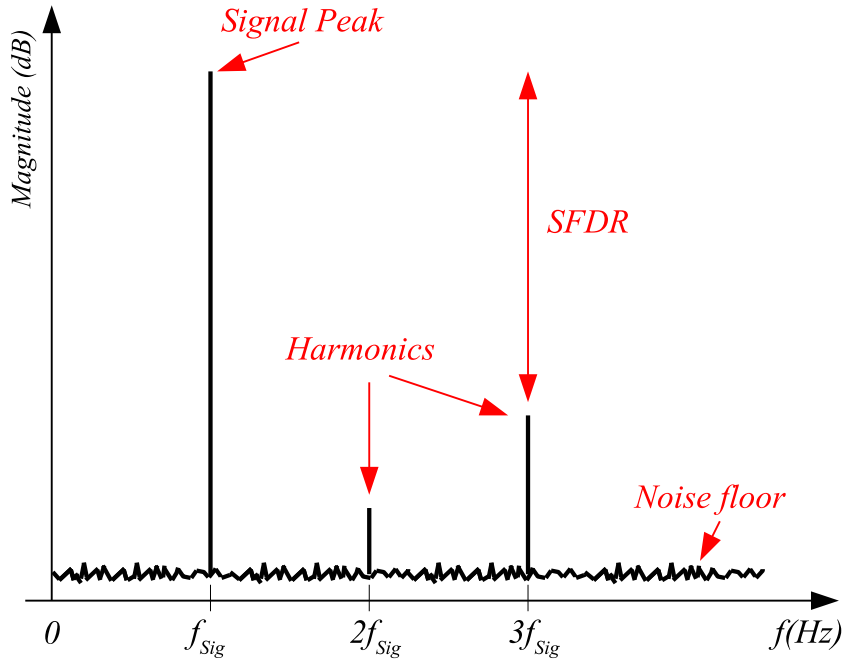


Figure II.4: SNR

- The signal-to-noise ratio of a converter is the ratio of the signal power to the noise power at the output of the converter, specified for a certain input amplitude and bandwidth.

- The signal-to-noise and distortion ratio is the ratio of the signal power to the noise and all distortion power components. Thus, the corresponding spectra are obtained by applying a signal at $f_{sig} \leq f_B/3$ to include at least the second and third harmonic inside the band of interest.

- The dynamic range is the ratio between the maximum signal power and minimum detectable signal power within a specified bandwidth. It is the root mean squared value of the maximum amplitude input sinusoidal signal.

- The spurious free dynamic range is defined as the ratio of the signal power to the power of the strongest spectral tone. Its importance strongly depends on the application, since it dominates the resulting ADC linearity.

- Total harmonic distortion is the ratio of the sum of the signal power of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency. The x^{th} harmonic itself is the ratio between the signal power and the power of the distortion component at the x^{th} harmonic of the signal frequency.

It should be noted that these performance parameters are all relative numbers. Information about the (maximum) input power is needed for a complete qualification.

Because one parameter is sometimes not enough to compare ADCs, Figure Of Merits (FOM) combine several ADC parameters such as speed, bandwidth, conversion resolution, power consumption to compare ADCs. Two FOMs are widely used in ADC literature.

The Walden FOM [44] illustrates the power efficiency of an ADC with the following expression:

$$FOM_W = \frac{P}{2BW \times 2^{ENOB}}, \tag{II.7}$$

where P is the power consumption of the ADC, BW denotes the ADC's bandwidth and $ENOB$ its Effective Number Of Bits. The Walden FOM is expressed in picojoules per conversion-step (pJ/conv). In addition to the Walden Figure of Merit, ADCs can also be compared using the Shreier FOM [45].

$$FOM_S = SNDR(dB) + 10\log_{10}(\frac{BW}{P}) \tag{II.8}$$

If FOM_S is rewritten in linear form and inverted, it is then proportional to

$$\frac{P}{BW \times 2^{2\times ENOB}} \tag{II.9}$$

Equations (II.8) and (II.9) account for the fact that due to thermal noise limitations, achieving twice the conversion accuracy requires 4 times increase of the

power consumption. Shreier FOM is still standard in literature and is better to use to compare ADCs with same resolution.

II.1.3 ADC Architectures

Analog-to-Digital Converters cover many applications depending on the requirements of the system regarding speed or power consumption. Depending on the targeted application, different ADC architectures such as Flash ADC, Sigma Delta ADC, Pipeline ADC, SAR ADC for example can be used.

The flash topology is the typical choice for high-speed, low-resolution converters. Flash ADCs achieve the highest sampling rates by comparing, in parallel, the analog input to every transition voltage, producing the output in one period with no feedback required between conversions; however, exploiting parallelism to increase speed in this manner requires the number of comparators to double the resolution of the converter in bits. Some techniques like interpolating [46] and folding [47] flash ADCs can reduce the number of preamplifiers and latches, respectively, but the general exponential growth of comparators remains a fundamental problem with this topology [48]. The widest range of applications of this type of converter is video signal processing. They are used in video tape compression, digital video transmission, radar signal analysis in particular. These applications require conversion speeds in the range of 50 MHz to 1 GHz or beyond.

The SAR ADC is generally used for medium-high resolution, medium-low frequency operation. By determining the digital output one bit at a time, SAR ADCs only make b comparisons for a b-bit converter but require at least $b+1$ clock periods to produce the output, much slower than the flash topology. Although SAR ADCs have also been applied to high-resolution commercial products, the requirements of trimming/calibration procedures and the use of high supply voltage to maximize the SNR increase the production cost and power consumption [49]. The resolution of a SAR ADC is typically limited by several factors: the non-linearity due to digital-to-analog converter mismatch, the comparator noise and the size of the capacitor to decrease kT/C noise. By time-interleaving SAR ADCs [50], high speed can be achieved without sacrificing the SAR's inherent low power.

In a pipeline ADC, different stages are cascaded and the number of stages to be cascaded depends on the resolution needed at the output. The pipeline ADC needs L clock periods to perform the conversion, where L is the resolution of the ADC. However, as L voltage values are simultaneously being converted, a new digital code is presented at each clock period. This digital code will be delayed in time from the sampling instant of a value proportional to the ADC resolution [51]. Most

commonly used applications of Pipeline ADCs include high quality video systems, healthcare, radio base stations, radar systems, Ethernet, cable modems, high performance digital communication system. The accuracy requirement for a pipeline ADC decreases from first stage to the last stage. The first stage must be more accurate than the later stages. The main limitations of this type of converter is the fairly complex logic, a sample-and hold circuit on every stage and the nonlinearity of the amplifiers, which must have a good match to get a linear conversion.

Flash, SAR and pipeline ADC architectures are considered as Nyquist data converters. The maximum frequency of the signal in this kind of converters is approximately half the sampling frequency. Sigma Delta ADCs are oversampled ADCs. For oversampled conversion, the maximum signal bandwidth is low compared to the sampling frequency. Thus, those converters are used for small signal bandwidth, but can achieve high resolution.

$\Sigma\Delta$ converters are based on the principle of oversampling and noise-shaping of a given input signal. Noise shaping is combined with oversampling to further improve the conversion resolution N at the same sampling speed f_s and with the same number of ADC bits n. This is accomplished by high-pass filtering the quantization noise to displace most of its power from low frequencies where the input signal spectrum is placed to higher frequencies close to $f_s/2$. The amount of quantization noise power still left inside the signal bandwidth depends on the exact filtering applied in terms of filter order and cut-off frequency. In $\Sigma\Delta$ modulators, the inherent loop filter has the particularity to reject the quantization noise away from the desired band, and therefore contributes to increase the overall modulator resolution. $\Sigma\Delta$ converters thus offer high resolution, high integration, low power conversion and low cost.

Table II.1 compares ADC architectures presented in terms of speed, resolution, size and power consumption. For a given technology, the flash ADC achieves the fastest sampling rate among various single-channel ADC architectures. However, its size and high power consumption of this architecture make it unsuitable for high bandwidth and low power consumption applications.

	Flash ADC	SAR ADC	Pipeline ADC	Sigma Delta ADC
Speed	High	Low-Medium	Medium-High	Low
Resolution	Low	Medium-High	Medium-High	High
Size	High	Low	Medium	Medium
Power cons.	High	Medium	High	Low

Table II.1: ADC architectures comparison

SAR ADCs have a relatively low power consumption compared to other architectures. This is because no amplifiers is needed in this ADC architecture. Pipeline ADCs are well suited for wide bandwidth and medium resolution applications, but consume a lot of power. They are in fact widely used in the feedback path of BTS digital predistortion. The ΣΔ architecture is an excellent candidate for DPD because of its trade-off between power consumption and high resolution. However, as ΣΔ converters are typically used for small bandwidth applications like audio which requires 20 kHz bandwidth, techniques to enable wider bandwidth operation like parallelism can be used to cope with large telecommunications signal requirements.

Several approaches to achieve high speed and high resolution ADCs have been proposed in the literature. One approach is to extend the resolution of a Nyquist rate ADC such as a pipelined converter by calibrating the converter [52]. The bandwidth can then be further extended by time-interleaving pipeline converters [53]. The previous two solutions will considerably increase the power consumption of the DPD system. Another approach is to use a very high resolution converter such as a ΣΔ ADC for relatively low bandwidth signals and extend the bandwidth by reducing the oversampling ratio [54].

For our application, we can take advantage of the information on the form of the signal in order to choose the ADC architecture. In the following sections, we focus on ΣΔ converters architectures for our feedback DPD ADC.

II.2 Basics of ΣΔ ADCs

Sigma-Delta Analog-to-Digital Converters exploit oversampling, noise shaping, and digital signal filtering to generate a high-resolution digitized output. As presented in Section II.1.1 oversampling allows to spread the quantization noise in a wider bandwidth. Figure II.5 illustrates the three aforementionned techniques. In a typical Nyquist-rate N-bit ADC, the quantization error is considered as a noise and to be uniformly distributed within the Nyquist band of DC to $f_s/2$, where f_s is the sampling rate Figure II.5-A.

Applying the technique of oversampling to the same N-bit ADC, which is sampling at a higher rate by a factor of OSR, the same amount of rms quantization noise is found in the system, but the noise is now distributed over the wider bandwidth of DC to OSR f_s Figure II.5-B. By applying a digital low-pass filter (LPF) to the output, much of the quantization noise can be removed without affecting the desired signal. Therefore, a high-resolution AD conversion can be achieved by using an otherwise low-resolution ADC.

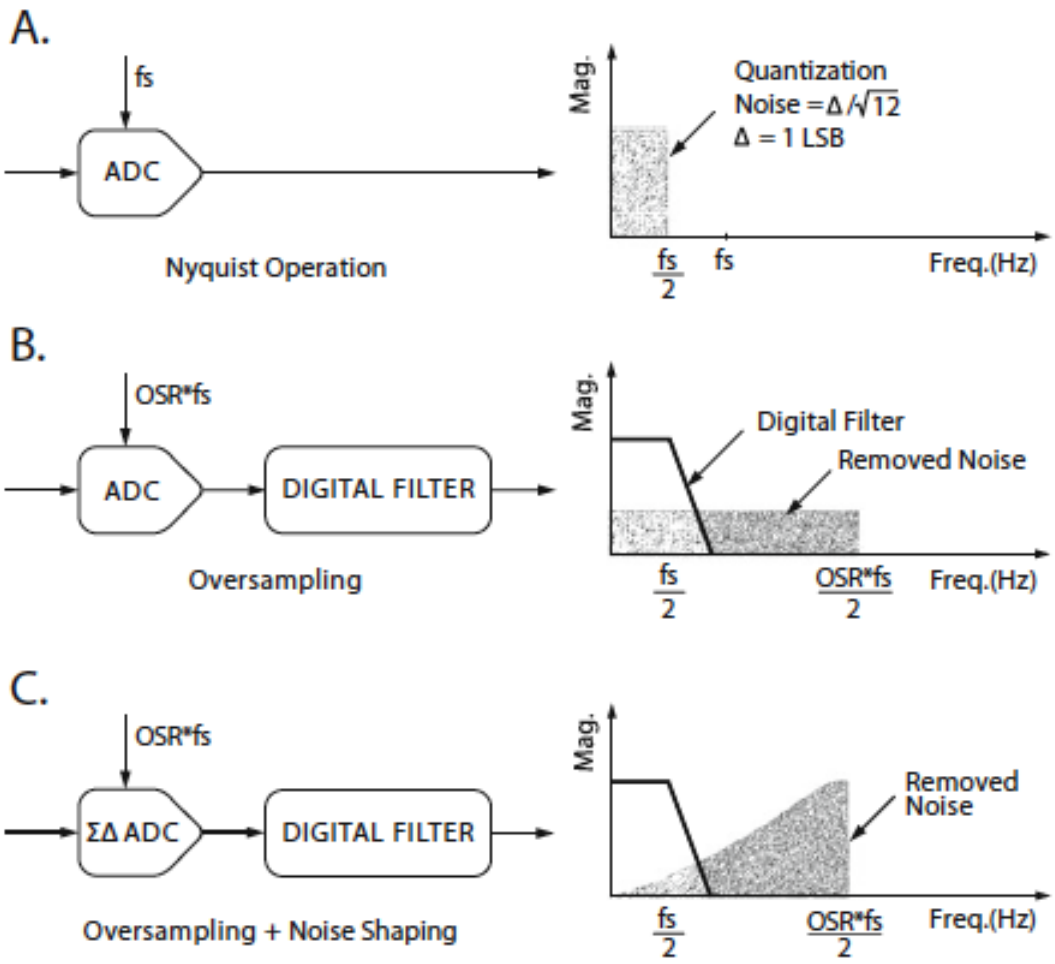


Figure II.5: Output spectra of Nyquist, oversampled and ΣΔ ADCs

The main drawback of oversampling is that in order to lower the in-band quantization noise such that an N-bit increase in resolution is achieved, the system must be oversampled by a factor of $2^2 \cdot N$. In other words, oversampling achieves a 0.5-bit increase per doubling of OSR. This is impractical to achieve high resolutions as high-speed systems are difficult to design and lead to high power consumption. To keep the oversampling factor at a reasonable value while achieving very high resolution, the technique of noise shaping, which is shaping the quantization noise such that most of it resides outside the signal passband of interest, comes in handy. The technique is illustrated in Figure II.5-C, and is the main concept behind all ΣΔ converters since it is the ΣΔ modulator in such converters that allow achieving the noise-shaping characteristic.

A ΣΔ ADC has three major components:

- an anti-aliasing filter which band limits the analog input signal to avoid aliasing during its subsequent sampling. As illustrated previously, oversampling

considerably relaxes the attenuation requirements of the AAF, so that smooth transition bands are usually sufficient compared to Nyquist rate ADCs.

- a ΣΔ modulator in which the oversampling and quantization of the band-limited analog signal take place. The quantization noise of the embedded B-bit quantizer is shaped in the frequency domain by placing an appropriate loop filter before it and closing a negative feedback loop around them. Low-resolution quantizers, with B typically in the range 1 to 5 bits, are sufficient for obtaining small IBN and high accuracy in the A/D conversion.

- a decimation filter in which a high-selectivity digital filter sharply removes the out-of-band spectral content of the output and thus most of the shaped quantization noise. The decimator also reduces the data rate from F_s down to the Nyquist frequency, while increasing the word length from B to N bits to preserve resolution.

We will now focus on the basics of a ΣΔ modulator as it is the block that influences the most the ADC performance. As illustrated in Figure II.6, a ΣΔ modulator is made of a loop transfer function, a clocked quantizer and feedback digital-to-analog converters.

Assuming that the quantizer can be modeled with a linear additive white noise model, the modulator is modeled as the two-input (x and e) one-output (y) linear system illustrated in Figure II.6. The loop filter has two sections, a forward filter $G(z)$ and a feedback filter $H(z)$. The input signal $X(z)$ is applied and compared with the signal fed back by $H(z)$, filtered through $G(z)$ and quantized to give the digital output. The quantization introduces an error $E(z)$ which is modeled as input-signal-independent and directly added to the output, in the quantizer (represented as a summation point).

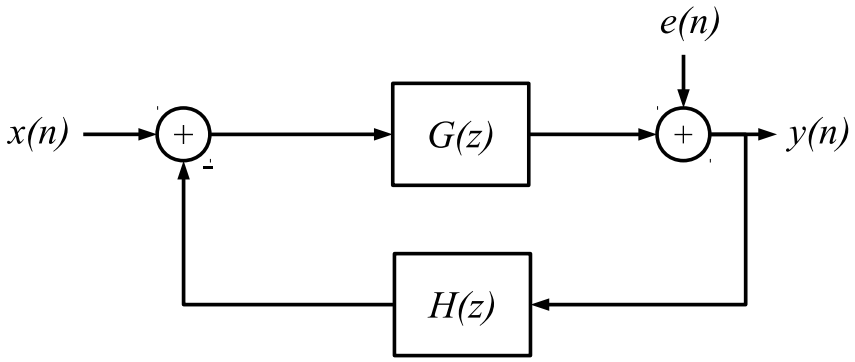


Figure II.6: Linear model of a ΣΔ modulator

The input e is assumed to be independent of the circuit input x. The output of the modulator is then described in the Z-domain as

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{II.10}$$

where $STF(z)$ and $NTF(z)$ are the Signal Transfer Function and the Noise Transfer Function respectively. $X(z), Y(z)$ and $E(z)$ are the DT Z-domain transform of the input, output and quantization noise, respectively.

The quantization noise is shaped by the transfer function of the close loop system since the input signal is injected in a different node. Based on the feedback theory, the NTF which is in fact the transfer function for the quantization noise, is approximated as

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + G(z)H(z)} \tag{II.11}$$

where $H(z)$ is the the loop filter function. If the loop is linearized and assuming that the gain of the quantizer and DAC is unity, by using $H(z)$ with high passband gain, the quantization noise will be further reduced.

The transfer function for the input signal (STF) for the specific case in Figure II.6 is obtained by

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{G(z)}{1 + G(z)H(z)} \tag{II.12}$$

The STF depends on the NTF and the topology of modulator.

Considering again the linear system of Figure II.6 and $H(z) = 1$. With a simple integrator

$$G(z) = \frac{1}{z - 1} \tag{II.13}$$

as the loop filter and a one-bit quantizer which produces output bits with values ± 1. From Equation (II.10), we obtain:

$$STF(z) = z^{-1}, NTF(z) = 1 - z^{-1} \tag{II.14}$$

At DC (i.e., at f = 0), $G(z)$ is infinite, which means input signals near DC should be reproduced faithfully in the output bit stream. In fact, $|STF(z)| = 1$ everywhere, so we at least expect the magnitude (if not the phase) of an input at any frequency to be reproduced at the output. As well, $NTF(z)$ is close to 0 at DC, and it increases away from DC; hence, we say the quantization noise is "shaped away from DC". The simplest first-order $\Sigma\Delta$ modulator provides a 1.5-bit increase per doubling of OSR, resulting in it being much more efficient than using only oversampling.

By designing a higher order loop filter, the portion of in-band noise can be further reduced. In the case of a low pass filter, the generalized simplest expression of the NTF is given by:

$$NTF(z) = (1 - z^{-1})^L \tag{II.15}$$

where L is the order of the loop filter. Figure II.7 illustrates the cases where L is set to 1, 2 and 3. By increasing the order of the modulator, the noise is more

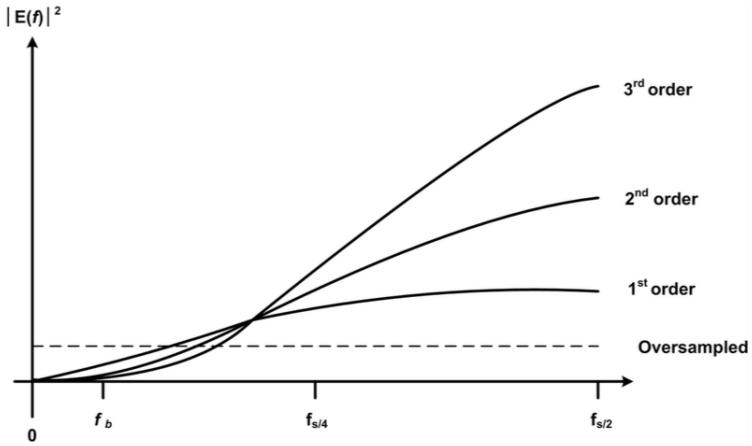


Figure II.7: NTFs obtained with 1st, 2nd and 3rd order loop filters

rejected away from the low frequencies. The relation between the SNR of a Sigma Delta ADC, the loop gain, the total quantization noise power and the sampling frequency is expressed as:

$$SNR_{max} = 10\log_{10}\frac{1.5(N+1)OSR^{N+1}}{\pi^N} + 6.02(B-1) \tag{II.16}$$

where N is the order of the loop filter, OSR is the oversampling ratio and B is the resolution of the quantizer and feedback DACs. To achieve for example 60 dB SNR, several set of parameters can be selected. Increasing these parameters improves the resolution of the ΣΔ ADC assuming the overall system is stable.

Out-Of-Band Gain (OOBG) and Stability

The out-of-band gain (OOBG) of a modulator is defined as the gain at the frequency $F_s/2$. The higher order NTF magnitudes are increasing 6 dB/order at $F_s/2$ and need to be limited to ensure stability. High OOBG may cause overloading of the quantizer and consequently make an unusable modulator. In order to increase stability, the reduction of the loop gain is done by properly adjusting internal scaling

stage. Stability is guaranteed if the internal modulator states or equivalently the integrator outputs are bounded over time. To ensure stable operation, the input level needs to be less or equal to the full scale of the first feedback DAC. In higher-order single-bit ΣΔ modulators, this input range is few dBs below the DAC full scale. This stable range is mainly determined by the NTF and the number of quantizer bits. A stability condition for single-bit modulators widely in use is the Lee's Criterion [55]:

$$|NTF_{MAX}| \leq 1.5 \tag{II.17}$$

where NTF_{MAX} is the maximum magnitude over all frequencies. A NTF with the OOBG set at 1.5 suffers significantly in terms of in-band noise suppression compared to the ideal NTF. Also as the order of the modulator increases, the performance starts to saturate and the desired performance boost due to higher order filters, loses its leverage. However, the introduction of multi-bit quantization enables higher order systems to be stable even with a large OOBG.

II.2.1 Design Parameters

When designing a ΣΔ modulator several high level parameters need to be fixed. Table II.2 gathers some of those parameters.

Criteria	Classification
The order of the loop filter	1 to 5
The NTF characteristic	Low pass Bandpass
The loop filter circuitry	Discrete time Continuous time
The number of bits in a quantizer	Single-bit Multi-bit
The number of quantizers employed	Single loop Cascaded

Table II.2: ΣΔ modulators classification

Each of those criteria is discussed in the following sections.

Oversampling ratio, modulator order and quantizer resolution

Generally, the order of $H(z)$ (which must be strictly proper to ensure causality) is the maximum power of z in the denominator. It is possible to use a second-, third-, or even higher-order $H(z)$ as a loop filter; generally, a converter of order

L is built as a cascade of L integrators usually surrounded with feedforward and feedback coefficients.

Oversampling is beneficial for improving the measured signal-to-noise ratio. This is true if the quantization noise inside the signal band is white, as it is in a traditional ADC: doubling the OSR (i.e., increasing it by an octave) halves the bandwidth, and hence the noise power, so that SNR improves by 3 dB. The SNR in an order-L ΣΔ modulator improves by $6L + 3$ dB per octave of oversampling [56] because the noise is shaped by the loop filter. Thus, a high-order modulator is desirable because of the huge increase in converter DR obtained from a doubling of the OSR.

Not surprisingly, using a high-order modulator has drawbacks. First, the stability of the overall system with $H(z)$ above order two becomes conditional: input signals whose amplitudes are below but close to full scale (to be defined later) can cause overload at the output of the integrators closer to the quantizer, which degrades DR [57]. As well, the placement of the poles and zeros of $H(z)$ becomes a complicated problem, though many solutions have been proposed in the literature [58], [56]. Furthermore, the technology in which the circuit is implemented and the circuit architecture itself will limit the maximum-achievable sampling rate and hence, limit the OSR. Finally, the design of the decimator increases in complexity and area for larger oversampling ratios.

It is possible to replace the single-bit quantizer with a multibit quantizer, e.g., a flash converter [59]. This has three major benefits: it improves the overall ΣΔ modulator resolution, it decreases constraints on the decimation filter and it tends to make higher-order modulators more stable. Furthermore, nonidealities in the quantizer (e.g., slightly misplaced levels or hysteresis) don't degrade performance much because the quantizer is preceded by several high-gain integrators, hence the input-referred error is small [60]. Its two major drawbacks are the increase in complexity of a multibit vs. a one-bit quantizer, and that the feedback DAC nonidealities are directly input-referred so that a slight error in one DAC level reduces converter performance substantially. There exist methods known as dynamic element matching techniques to compensate for multibit DAC level errors [61]. These aren't needed in a single-bit design because one-bit quantizers are inherently linear [57].

II.2.2 NTF Implementation: Continuous Time vs. Discrete Time

In ΣΔ modulators, the sampling operation can be done at two different places as depicted in Figure II.8:

- before the adder block, it is called Discrete Time ΣΔ modulator
- between the loop filter and the quantizer, we then call them Continuous time ΣΔ modulator.

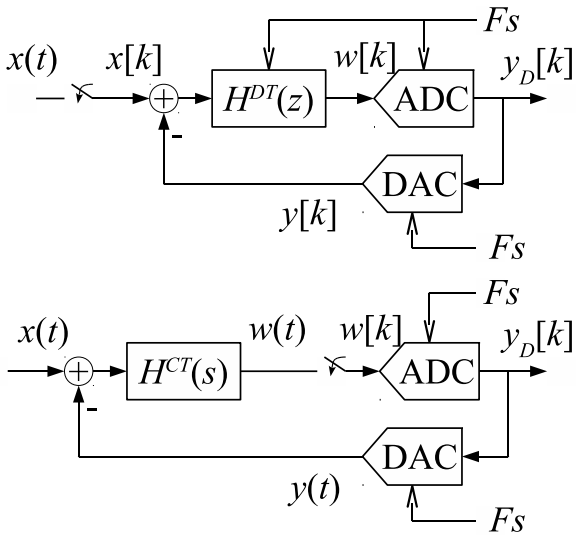


Figure II.8: Continuous time and Discrete time ΣΔ architectures

DT ΣΔ modulator can be implemented with switched-capacitor (SC) [62] or switched current (SI) [63] circuits. Those circuits have a maximum clock rate limited by op amp bandwidths and by the fact that circuit waveforms need several time constants (i.e., clock periods) to settle. For a ΣΔ modulator built in a process with maximum transistor speed f_T, the maximum clock rate of an SC modulator is on the order of f_T. Furthermore, large glitches appear on op amp virtual ground nodes of DT modulators due to switching transients. Another issue of DT domain is aliasing: signals separated by a multiple of the sampling frequency are indistinguishable.

DT ΣΔ modulators thus require a separate filter at their inputs to sufficiently attenuate aliases. It is possible to build the loop filter as a continuous-time (CT) circuit (s), for example with transconductors and integrators [64]. The circuit techniques to build CT integrators rely on integrating a current proportional with the input signal on a capacitor and read the output voltage. A simple, passive RC filter cannot be used to implement the desired transfer function since its pole is not at DC. With passive filters, a design method which takes into account this pole shift has to be employed to map the desired NTF to the target loop topology.

Assuming the input signal is largely oversampled, the CT ADC in Figure II.8 can be designed to be equivalent with the DT-based version if, for an identical input x(t) during a clock cycle, w(t) presented to the quantizer at the end of the current

clock cycle is identical with the one in the DT version, denoted as $w(k)$ for $t = kT_s$ [65],

$$w^{DT}[k] = w^{CT}(k)_{|t=kT_s} \tag{II.18}$$

To satisfy this condition, the impulse response of the filters connecting the input to the quantizer and the DAC output to the quantizer should have the same impulse response in the DT and the CT variants,

$$\mathcal{Z}^{-1}\left[H^{DT}(z)\right] = \mathcal{L}^{-1}\left[\mathcal{R}_{DAC}(s) \cdot H^{CT}(s)\right](t)_{|t=kT_s} \tag{II.19}$$

where $H^{DT}(z)$ is the equivalent loop filter transfer function in Z-domain, $\mathcal{R}_{DAC}(s)$ and $H^{CT}(s)$, respectively, the Laplace transfer functions of the DAC response and of the loop filter. $\mathcal{Z}^{-1}$ and $\mathcal{L}^{-1}$ are the inverse transform of each domain, the first one resulting in an inherently sampled signal and the second one in a continuous signal that is sampled at the instants $t = nT_s$.

With the equations above satisfied, the time-domain signal sampled by the quantizer is identical in the DT and the CT designs, and, ideally, time-domain simulation results obtained for the DT loop also apply to the CT loop. This is a major advantage since behavioral time-domain simulations for CT loops typically take more times for processing compared to DT loops.

There are different architectures for ΣΔ ADCs and classification is usually based on the number of modulators and the circuit realization of the loop filter. In general, ΣΔ ADCs are grouped as single-stage or multi-stage architectures.

II.2.3 Single Loop and Cascade Architectures

Single-stage ΣΔ ADCs are characterized by the presence of single quantizer in their architectures. Based on the loop filter configuration, there are two generalized single-stage topologies: the cascade of integrators or resonators with feed forward (CRFF) and with feedback (CRFB) [45]. Assuming a 4^{th} order DT ΣΔ ADC for example, Figure II.9 shows two different architectures.

In CRFF architecture all the output of the integrators feed forward to the input of the quantizer and there is an additional path directly from input to the quantizer. In CRFB, Figure II.10 instead of feed-forward paths, there are feedback paths between integrators and DACs. Coefficients a_i in the feedback path of the digital-to-analog converter determine the noise transfer function and are required to obtain a stable operation of the converter. Coefficients g_i are introduced to obtain zeros at

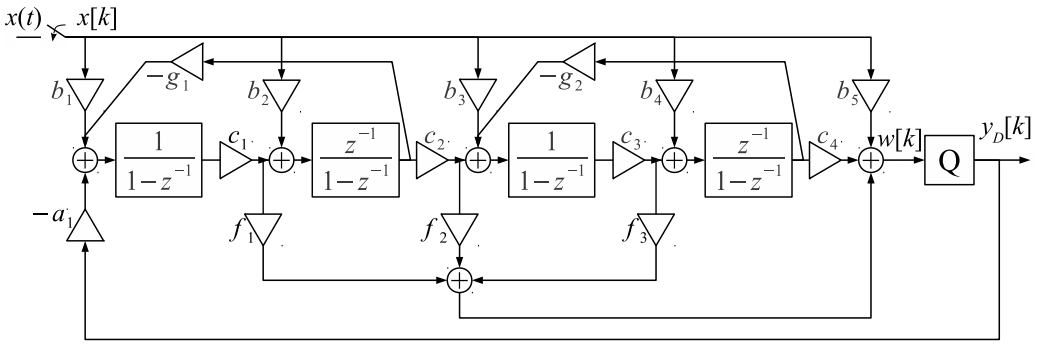


Figure II.9: CRFF architecture

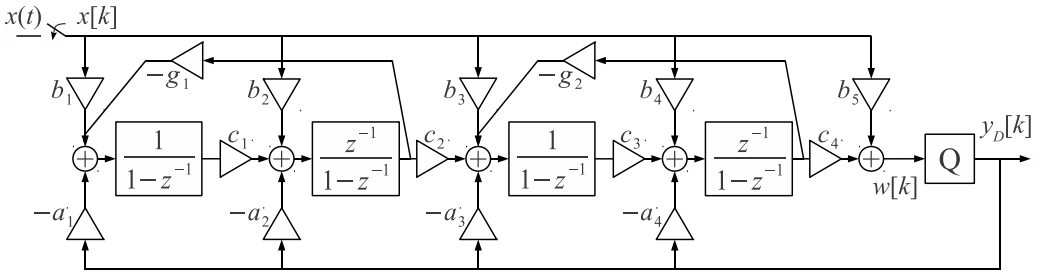


Figure II.10: CRFB architecture

a signal frequency in the passband of the converter. In this manner an increase in dynamic range over the passband is obtained. c_i coefficients determine the gain of the integrator stages. Both architectures have enough degree of freedom to control the desired STF and NTF, and both have their own advantages and drawbacks.

In CRFF, synchronization issues are minimum since there is only one feedback DAC. The input signal is directly passed to the input of the quantizer through b_5 path in CRFF making the swing of the internal nodes between integrators smaller and relaxing the linearity requirement of the filters. However, the design of the adder in front of the quantizer in CRFF is a challenge especially in the application with high sampling frequency. The adder is connected to several resistive and capacitive loads but the bandwidth requirement is extremely large to prevent excessive loop delay. In addition, with non-ideal integrators in the ADCs, the out-band blocker rejection is minimized in CRFF due to the b_1 feedforward path.

Compared to the $\Sigma\Delta$ modulator using CRFB topology, the modulator using CRFF architecture requires only one feedback DAC, which can reduce the power consumption and area. On the other hand, the STF(z) of $\Sigma\Delta$ modulator using CIFF topology shows out-of band peaking and in some cases results in loop instability if there exists large out-of band interferences.

Cascade Architectures

In order to perform high order modulator with high stability, low order modulators are cascaded. Most of them are composed of modulators of order 1 to 3. Each modulator processes a portion of the quantization noise of the previous modulator and digital reprocessing is performed on the outputs. This gives a better accuracy in the useful band. There are several cascade architectures. Among those architectures, the most common is the Multi stAge noise SHaping (MASH) [66]structure Figure II.11 .

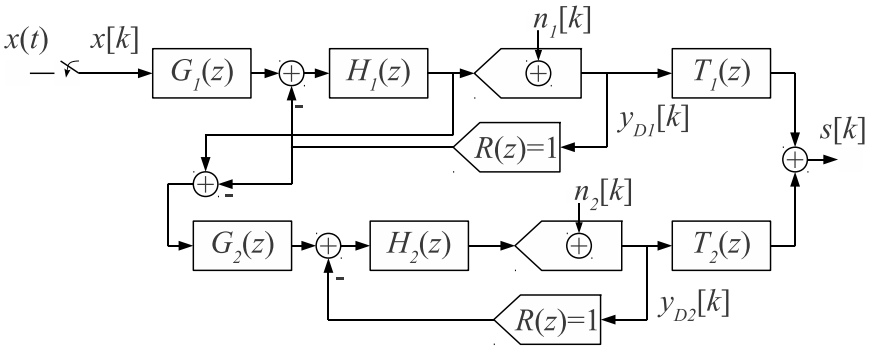


Figure II.11: Dicrete Time MASH architecture

The MASH architecture is to digitize the difference between the input of the quantizer and the output of the DAC at each clock pulse. Thus each modulator processes the quantization error made by the previous stage.
For DT implementations, the required cancellation noise filters $T_1(z)$ and $T_2(z)$ are easily derived so that the noise contribution of each stage is null except for the last modulator of the chain:

$$S(z) = \frac{T_1(z)G_1(z)H_1(z)}{1+H_1(z)}X(z) + \left(\frac{T_1(z)}{1+H_1(z)} - \frac{T_2(z)G_2(z)H_2(z)}{1+H_2(z)}\right)N_1(z) + \frac{T_2(z)}{1+H_2(z)}N_2(z) \tag{II.20}$$

$$\frac{T_1(z)}{1+H_1(z)} - \frac{T_2(z)G_2(z)H_2(z)}{1+H_2(z)} = 0 \quad \Leftrightarrow \quad \frac{T_1(z)}{T_2(z)} = \frac{G_2(z)H_2(z)\,(1+H_1(z))}{1+H_2(z)} \tag{II.21}$$

In the case of CT implementations, this filter identification requires to take into account additional information. Therefore the hardware complexity is increased and the circuit is more prone to mismatches. The derivation of the noise cancellation

filters consists in writing the exact transfer functions achieved all along the cascaded modulator.

II.3 ΣΔ ADC State-Of-The-Art

We saw in Chapter 1 that in order to perform DPD, the feedback ADC should have at least 60 dB SNR in the bandwidth of interest. In the case of a 20 MHz LTE signal, assuming we capture up to the third non-linearity order, this leads to an SNR of at least 60 dB in 100 MHz bandwidth. Table II.3 compares performance of few ΣΔ modulators. Some of those modulators have their performance close to our ADC specifications for DPD. The architectures of [67], [68], [69] and [43] have a band close to or equal to 20 MHz and consume between 8.5 and 20 mW with a single loop. Assuming that each channel has a similar consumption, this would correspond to a total consumption between 42.5 and 100 mW. [70] and [71] have ΣΔ modulators with respectively 125 and 150 MHz band and consume 256 and 550 mW. Their high performance can be achieved thanks to high oversampling ratios.

Year	FoM [J/step]	Techno [nm]	Area [mm^2]	BW [MHz]	SNDR [dB]	Quant	Order	P [mW]	Fs [MHz]
2006 [72]	122f	130	1.2	20	74	4b	3	20	640
2011 [73]	704.7f	45	0.9	125	65	4b	3	256	4000
2012 [67]	190.4f	45	0.49	60	60.5	1b	3	750	6000
2012 [70]	0.19p	40	0.4	20	70	1b	6	20	3200
2012 [74]	0.8p	65	5.5	150	-	17 l[1]	6	550	4000
2013 [68]	207f	90	0.266	61.7	50	4b	3	20.6	1000
2014 [71]	0.38p	65	0.2	24	58	9 l	4	12	800
2014 [75]	697.3f	28	0.9	53	71.8	17 l	0-3	235	3200
2014 [69]	88f	90	0.19	25	67.5	4b	3	8.5	500
2015 [76]	177f	28	0.34	50	74.9	15/7 l	3-1	80.4	1800
2015 [43]	74.2f	20	0.1	80	67.5	3b	4	23	2184

Table II.3: State-of-the-art CT ΣΔ ADCs

Cascaded architectures are used to achieve better performance by maintaining the stability of modulators. [75] and [76] are cascaded architectures having approximately 50 MHz bandwidth and consuming respectively 235 and 80.4 mW. However, cascaded ADCs such as MASH or Sturdy MASH (SMASH) [77] are sensitive to process, voltage and temperature variations.

In order to increase the signal bandwidth that the modulator can deal with, a variety of methods can be used such as using higher sampling frequency, increasing

the order of the modulator and the number of quantizer bits. However, each of them has a price and is restricted by technology deployed. Using above mentioned methods to increase OSR make the design of the modulator more complicated and may cause stability problem which require to be dealt with carefully. Furthermore, low power consumption is required to decrease the overall DPD power consumption.

Another efficient and attractive way to increase the OSR, is to consider the time-interleaving technique where parallelism can be incorporated in ADCs in order to increase the effective sampling rate [78], [79], [80], [81]. This approach is a practical solution that does not necessitate state of art technologies. A time-interleaved ΣΔ modulator can be a good solution for this problem, since the signal bandwidth of the modulator can be simply extended by adding more channels instead of increasing the sampling clock frequency. The most simplistic parallel TI ΣΔ ADC can be constructed by placing ΣΔ ADCs in parallel and applying the input signal to all of the channels simultaneously.

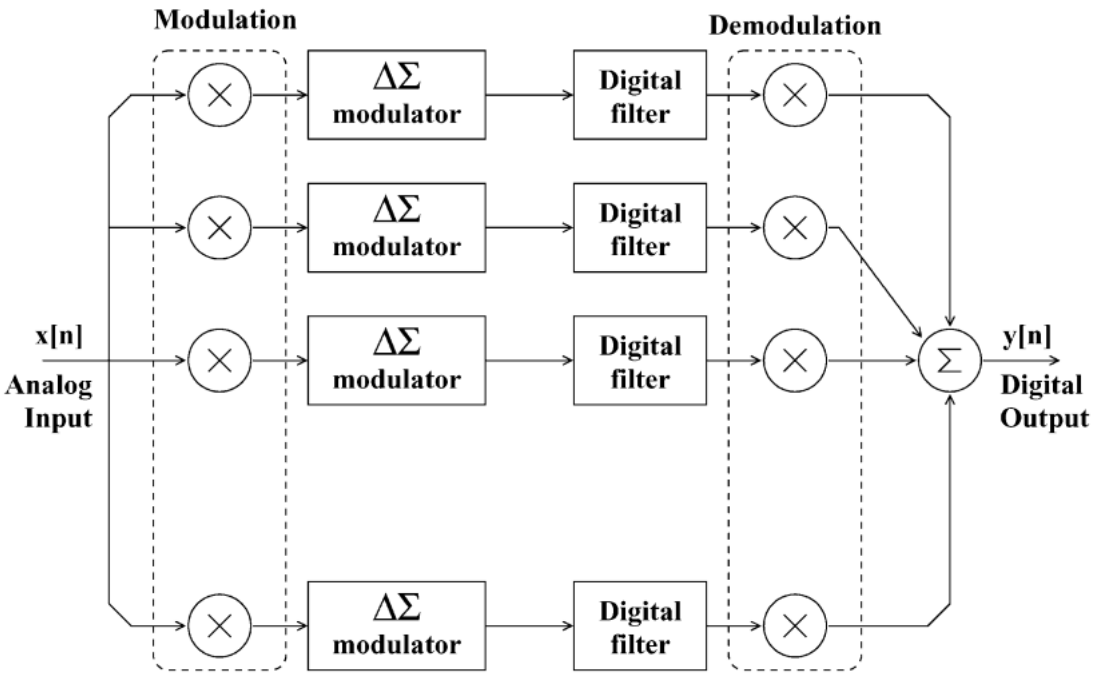


Figure II.12: Block diagram of a parallel ADC [54]

As shown in Figure II.12, the outputs from all of the channels are then digitally recombined to create the overall output.

Even though the two-channel TI modulator is the simplest form, the circuit-level implementation using the above approaches still has drawbacks due to several practical limitations that are discussed in the following sections. Furthermore, time-interleaving requires calibration technique to cope with mismatch between channels.

The above show that TI ΣΔ modulators is not a simple circuit implementation, low power consumption, and high area efficiency solution for a DPD system.

Another approach to combine ΣΔ in parallel is to use the frequency band decomposition architecture [82] [83] [84]. In this architecture, each channel consists of a bandpass ΣΔ modulator with a quantization null at a different frequency. Thus, each channel passes one M^{th} of the signal frequency band when there are M channels

The frequency-band-decomposition (FBD) ADC is derived from the concept of filter banks [54].

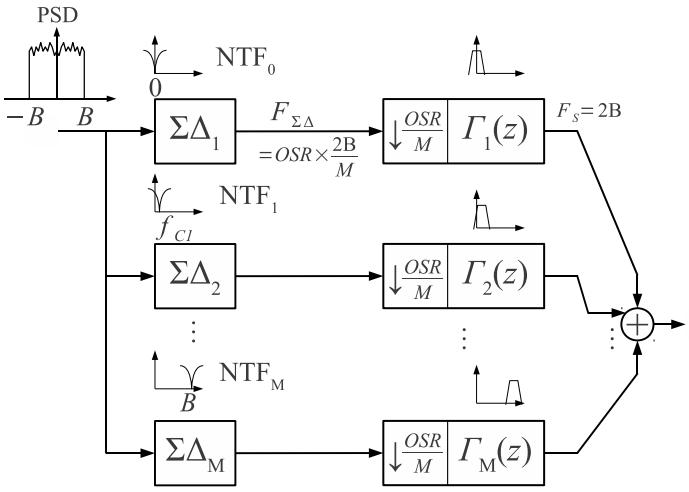


Figure II.13: FBD ADC

Each channel converts a band of frequencies and, when the outputs are recombined, the overall system is all-pass. An example of the FBD architecture is illustrated in Figure II.13. The ΣΔ modulator on each channel has been broken up into the signal path and the quantization noise path. As shown in the figure, the quantization noise filter is determined by the bandpass ΣΔ modulator on each channel and thus is different on each channel. Following each ΣΔ modulator is a digital filter that passes a band of frequencies corresponding to the null in the quantization noise filter. The signal path consists of a simple delay which corresponds to the group delay of the ΣΔ modulator. Since the quantization noise among different channels is uncorrelated, the total power of the quantization noise is the sum of the quantization noise power of each channel. The high sensitivity to central frequencies of modulators is the main drawback of the FBD technique. An extended FBD proposed in [83] decreases the impact of manufacturing variations. However, it requires a digital calibration.

The architecture of the Multi Stage Noise Band Cancellation (MSNBC) ADC is presented in Figure II.14.

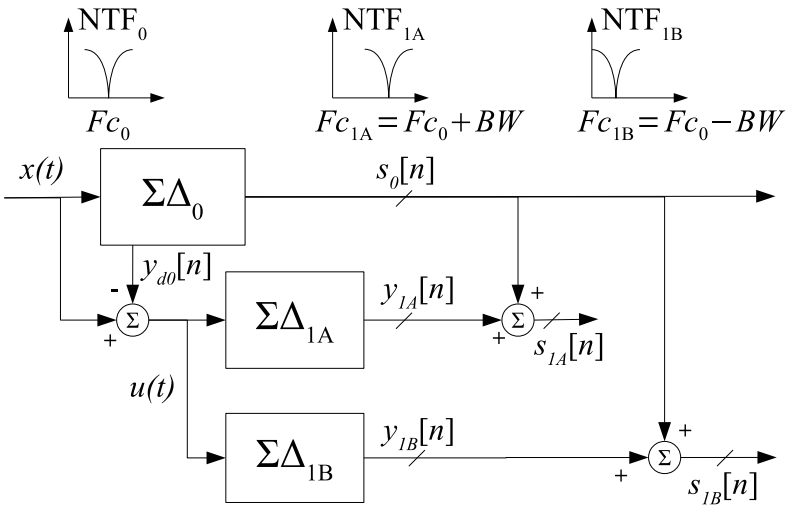


Figure II.14: MSNBC ADC architecture [85]

The signal to digitize is assumed to be made up of a band of high power and low power adjacent bands as shown in Figure I.8 centered at Fc_0. $\Sigma\Delta_0$ modulator digitizes the high power main band. Then, the output of the modulator consists of that part of the signal and the shaped quantization noise. The signal u, which is the attenuated main signal and shaped quantization noise, is digitized in adjacent channels with Fc_{1A} and Fc_{1B}. Combining the outputs of $\Sigma\Delta_0$ and $\Sigma\Delta_{1A}$ and $\Sigma\Delta_{1B}$ subtract quantization noise of $\Sigma\Delta_0$ in adjacent channels.

II.4 Conclusion

ADC requirements for DPD obtained in Chapter 1 added to a study of state-of-the-art, allowed us to select architecture in this chapter. We saw that pipeline ADCs are commonly used in the feedback path of BTS DPD systems. They can digitize wide bandwidth signals but consume a lot of power. $\Sigma\Delta$ ADCs combine oversampling and noise shaping techniques to push quantization noise out of the band of interest and improve the SNR. They are extensively used in audio applications, where the signal bandwidth signals is low. Therefore in order to take advantage of the energy efficiency of $\Sigma\Delta$ ADCs and use them for wide bandwidth applications, they should be combined with techniques such as time-interleaving and parallelization. The MSNBC architecture is particularly attractive for subband DPD given that the shape of the signal at the output of the PA is known and the use of bandpass $\Sigma\Delta$ converters avoid using complex analog filters.

Chapter III

MSNBC System Level Specifications

ADC specifications for Digital Predistortion in terms of mixer I/Q imbalance and non linearity are presented in Chapter 1. We defined ADC specifications in case of fullband and subband ADCs. The subband approach relaxes dynamic range requirements in adjacent bands. In Chapter 2, we showed that $\Sigma\Delta$ ADCs are well-suited to design an ADC for subband DPD. Several $\Sigma\Delta$ modulator based architectures are discussed with their features. We saw that cascaded architectures enable the design of high resolution converters and the parallel frequency decomposition architectures have been proposed to convert wide-band signals. An alternative approach digitizes the signal in subband which relaxes the ADC design and enables the digital processing to operate at lower frequencies. The Multi Stage Noise Band Cancellation (MSNBC) ADC presented in [85] has been proposed to optimize the ADC structure to the DR requirements and is then an excellent candidate for subband DPD. This new approach provides more degrees of freedom for the design of the ADC to optimize the DPD problem in order to keep as low as possible the cost of the DPD implementation.

III.1 The MSNBC Architecture

The MSNBC modulator has the feature to implement several DR specifications depending on the number of channels to digitize.

III.1.1 Mode of Operation

Figure III.1 depicts the mode of operation of the multi-stage noise band cancellation architecture. The modulator consists of several $\Sigma\Delta$ modulators and the input is a distorted baseband signal output from a PA as illustrated by (a) in Figure III.1.

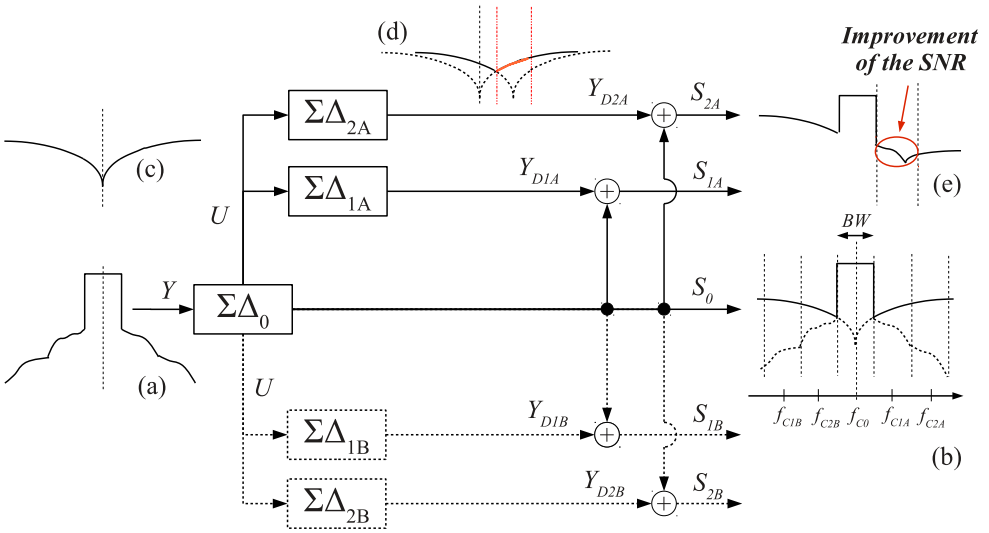


Figure III.1: MSNBC modulator operating mode

The primary modulator $\Sigma\Delta_0$ is centered at F_{c0} and digitizes the high power central subband of bandwidth BW. Modulators $\Sigma\Delta_{1A}$ and $\Sigma\Delta_{1B}$, respectively centered at $F_{c0}+BW$ and $F_{c0}-BW$ digitize the first adjacent subbands of bandwidth BW. Second adjacent subbands are digitized by $\Sigma\Delta_{2A}$ and $\Sigma\Delta_{2B}$ modulators centered at $F_{c0}\pm 2BW$.

The discrete-time linear model of the output signal of $\Sigma\Delta_0$, is:

$$S_0(z) = STF_0(z)Y(z) + NTF_0(z)N_0(z) \tag{III.1}$$

with STF_0 and NTF_0 respectively the signal and noise transfer functions of $\Sigma\Delta_0$, and N_0 its quantization noise. This signal is shown in Figure III.1 (b). Due to quantization noise, S_0 is not adapted to accurately predistort the input signal of the PA and adjacent channels should be digitized for an accurate DPD. Assuming for the sake of simplicity a unitary STF in the band of operation, the signal U defined by $U(z) = Y(z) - S_0(z)$ can be seen as a negative version of $\Sigma\Delta_0$ shaped quantization noise. The residual signal transfer function (RSTF) defined as

$$RSTF(z) = 1 - STF(z) \tag{III.2}$$

is introduced for this architecture. This function represents the cancellation of Y in U.

S_0 is subtracted to the continuous time input signal and fed to $\Sigma\Delta_{1A}$ and $\Sigma\Delta_{1B}$. Assuming that there is no gain between the two stages, the output of secondary

modulators can be modeled as:

$$\begin{aligned} Y_{D1A}(z) = STF_{1A}(z)\,(Y(z)\,RSTF(z) - N_0(z)\,NTF_0(z)) \\ + N_{1A}(z)\,NTF_{1A}(z) \end{aligned} \tag{III.3}$$

Figure III.1 (d) illustrates Y_{D1A}, the output of $\Sigma\Delta_{1A}$ made of U and $\Sigma\Delta_{1A}$ shaped quantization noise. Figure III.1 (e) the results of the addition of S_0 and Y_{D1A}. This is expressed as following:

$$\begin{aligned} S_{1A}(z) = Y(z)\,(STF_0(z) + STF_{1A}(z)\,RSTF(z)) \\ + N_0(z)\,NTF_0(z)\,(1 - STF_{1A}(z)) \\ + N_{1A}(z)NTF_{1A}(z) \end{aligned} \tag{III.4}$$

We furthermore assume that the STF of $\Sigma\Delta_{1A}$ is equal to 1. Thus, the RSTF vanishes and Equation (III.4) is expressed as:

$$S_{1A|STF_i=1}(z) = Y(z) + N_{1A}(z)\,NTF_{1A}(z) \tag{III.5}$$

Adding the output of $\Sigma\Delta_0$ to the $\Sigma\Delta_{1A}$ cancels out the noise of the primary modulator in the adjacent bandwidth as shown in Equation (III.4).

This leads to an improvement of the signal-to-noise ratio in this subband. The same principle applies to other adjacent modulators and enables to improve the SNR. Then, the signal in the adjacent band can be selected using a digital signal processing as if one had used a dedicated $\Sigma\Delta$ M but without the use of an analog filter.

General case: $STF(z) \neq 1$

In the previous paragraph, the mode of operation of the MSNBC architecture and linear model were depicted by presuming that the STF is equal to 1. This is can be easily achieved in discrete time modulator, but is not always the case especially for continuous time modulators.

When the assumption on the unitary STF is not valid, Noise Cancellation Filters (NCF) should be applied to the output of the primary and secondary modulators before performing the sum of those signals. The NCFs allow to achieve the right noise suppression we will have to process the output of each modulator.

Figure III.2 portrays the structure of the General MSNBC architecture which includes noise cancellation filters.

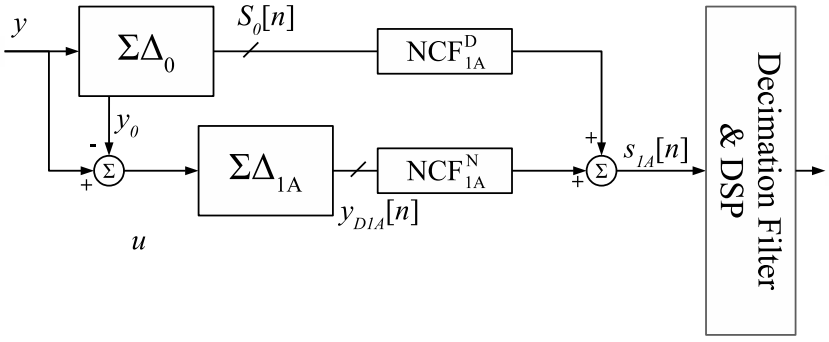


Figure III.2: The general MSNBC Architecture

The Z-transform of the output signal of $\Sigma\Delta_{1A}$ can be expressed as:

$$Y_{D1A}(z) = STF_{1A}(z)\left(X(z)\,RSTF(z) - N_0(z)\,NTF_0(z)\right) + N_{1A}(z)\,NTF_{1A}(z) \tag{III.6}$$

Summing $S_0(z)$ and $Y_{D1A}(z)$ leads to:

$$S_{1A} = NCF^D_{1A}(z)\cdot S_0(z) + NCF^N_{1A}(z)\cdot Y_{1A}(z) \tag{III.7}$$

Expanding the expression of $Y_{D1A}(z)$:

$$\begin{aligned} S_{1A} = X(z)\left(NCF^D_{1A}(z)\cdot STF_0(z) + NCF^N_{1A}(z)\cdot RSTF(z)\cdot STF_{1A}(z)\right) \\ + NTF_0(z)\cdot N_0(z)\left(NCF^D_{1A}(z) - NCF^N_{1A}(z)STF_{1A}(z)\right) \\ + NCF^N_{1A}(z)\cdot NTF_{1A}(z)\cdot N_{1A}(z) \end{aligned} \tag{III.8}$$

We then deduce from Equation (III.8) that $N_0(z)$ is be suppressed if:

$$\frac{NCF^N_{1A}(z)}{NCF^D_{1A}(z)} = \frac{1}{STF_{1A}(z)} \tag{III.9}$$

We define:

$$NCF_{1A}^{N}(z) = \text{Numerator}\left(\frac{1}{STF_{1A}(z)}\right) \tag{III.10}$$

$$NCF_{1A}^{D}(z) = \text{Denominator}\left(\frac{1}{STF_{1A}(z)}\right) \tag{III.11}$$

Thus, NCF expressions depend only on the STF of the secondary modulator.

III.1.2 Degrees of Freedom / Key Design Parameters

Given the mode of operation presented above, several degrees of freedom can impact the design of the MSNBC modulator. The first and key design parameter is the center frequency F_{c0} of the primary modulator, as first adjacent modulators will be centered at $F_{c0} \pm BW$. In fact depending on the frequency at which the signal is down-converted by the mixer, one might need that the center frequency is at a Low Intermediate Frequency (LIF) or at an Intermediate frequency (IF).

The quantizer of secondary modulators is important as well. As presented in the mode of operation, the signal sent to the second modulator U is the shaped quantization noise of the first modulator. This means that the rms voltage of this signal is low compared to the rms voltage of the input signal of the first modulator. Thus, two options are offered for adjacent modulators: on the one hand, the input signal can be scaled so that an identical quantizer as the one in the first modulator can be used. This means that a gain should be applied to the shaped quantization noise before being digitized by the adjacent modulator. On the other hand, the signal is not scaled, thus, the reference voltage of the quantizer of secondary modulators is decreased.

The following section explains in more details design choices for the MSNBC.

III.2 Impact of Non-Idealities

For wide-band and medium-resolution applications, continuous-time modulators are preferred over discrete time modulators because of their better energy efficiency and inherent anti-aliasing filter. However, design constraints that were not considered in discrete time must be taken into account.

A CT $\Sigma\Delta$ modulator consists of three major building blocks: a continuous-time loop filter $H(s)$, a clocked internal quantizer (ADC) and a continuous-time feedback DAC. Due to variations during the IC manufacturing process and through circuit imperfections, each of these components deviates from its ideal behavior. Thus,

the first classification of errors is their originating building block. Furthermore, the deteriorating influence of the different errors on the ideal modulator behavior can be used to specify two categories of non-idealities: those, which alter the ideal STF and NTF function by altering their poles and zeros, and aside the non-idealities which introduce noise or distortion into the system.

In order to present a clearly arranged summary of the influence of non-idealities on continuous-time ΣΔ modulators, it is important to identify the errors by their originating building block. Table III.1 gather some of those non-idealities.

Block		Non-ideality	Impact
Integrator	Op-amp	Finite Gain	Noise floor, stability
		Finite Gain bandwidth	Noise floor, distortions
		Finite Slewrate	Quantization noise, distortions
		Thermal and Flicker noise	Noise floor
	Gain	Time constant mismatch	Noise shaping, stability
Quantizer		Metastability	Stability, Noise, distortions
		Hysteresis	Noise floor
DAC		Delay	Stability, Noise floor
		Unequal rising and falling times	Noise floor, distortions
		Non-linearity	Noise and distortions
Clock		Random clock jitter	Noise
		Accumulated jitter	Skirt around signal

Table III.1: Non-idealities in CT ΣΔ modulators

The impact of those non-idealities is studied for the case of the MSNBC architecture.

III.2.1 Loop Filter

The loop filter transfer function is the main performance determining part in a ΣΔ modulator, because it defines the noise-transfer function and therewith the quantization noise-shaping behavior. Principally, the complete loop filter usually consists of several first-order filters, which are commonly arranged in a feedback or forward architecture. Taking CT ΣΔ modulators into consideration, the single filters are realized using either RC-integrator or g_mC-integrator or even LC-resonators for bandpass noise shaping. Without loss of generality, in the following active RC-integrators are considered because they have higher linearity performance and better robustness over Process Voltage and Temperature (PVT) variations compared to g_m-C integrators.

As shown in Table III.1, the loop filter has imperfections mainly derived from the variation of the time constant, gain, product gain band and slewrate finite operational amplifiers, mismatch coefficients and noise.

Finite Gain and Gain-bandwidth

One of the most well-studied non ideal effects in ΣΔ modulators is that of finite DC gain of the operational amplifiers. An ideal integrator can be modeled by the following function:

$$H_{ideal}(s) = \frac{1}{s.Ts} \tag{III.12}$$

From Equation (III.12), for a frequency-independent, but finite amplifier gain A_{DC}, the transfer function of an RC-integrator can be derived to:

$$H_{RC}^{A_{DC}}(s) = \frac{1}{\frac{1}{A_{DC}} + s * RC} \tag{III.13}$$

In the case of single-loop ΣΔ modulation, the DC gain of the incorporated amplifiers should be in the range of the oversampling ratio $A_{dc} \approx OSR$ of the modulator [86]. This requirement keeps every part of the in-band noise proportional to the ideal noise shaping suppression. In contrast to single-loop architectures, multi loop ΣΔ modulators suffer tremendously from integrator leakage. This is due to the principle of noise cancellation of the lower stages by the higher loops in the cascade. These are designed to eliminate the ideal quantization noise from the previous stages, but they are not able to also reject the non ideal noise components. Thus, these non ideal parts of the quantization noise leak into the overall output.

The impact of finite DC gain is studied for an 2-4 MSNBC. Simulations are performed with VerilogA model of integrator and by using the relation in Equation (III.12) for ideal integrators and Equation (III.13) for the cases called real integrators. We assume for those simulations that all integrators have the same DC gain. Results are presented in Figure III.3. Figure at the top present the impact of DC gain variations on SNR_{1_prim}, which corresponds to the SNR in the primary band of the reconstructed signal $S_1(z)$. The figure at the bottom is the impact of DC gain variations on SNR_{1_adj}, which is the SNR in the adjacent band of the reconstructed signal $S_1(z)$. The impact is studied for two cases: one assuming a unitary STF in $\Sigma\Delta_0$ (STF_0) and the other with a filtering STF_0. As expected DC gain do not impact performance of an architecture with ideal integrators. We observe however a degradation of the SNR in the primary and adjacent channels

when the gain of integrators are lower than 40 dB. For DC gain greater than 40 dB performance of ideal and real integrator are the same for SNR_{1_prim} and SNR_{1_adj}. Furthermore, the type of STF is not critical for DC gain variations.

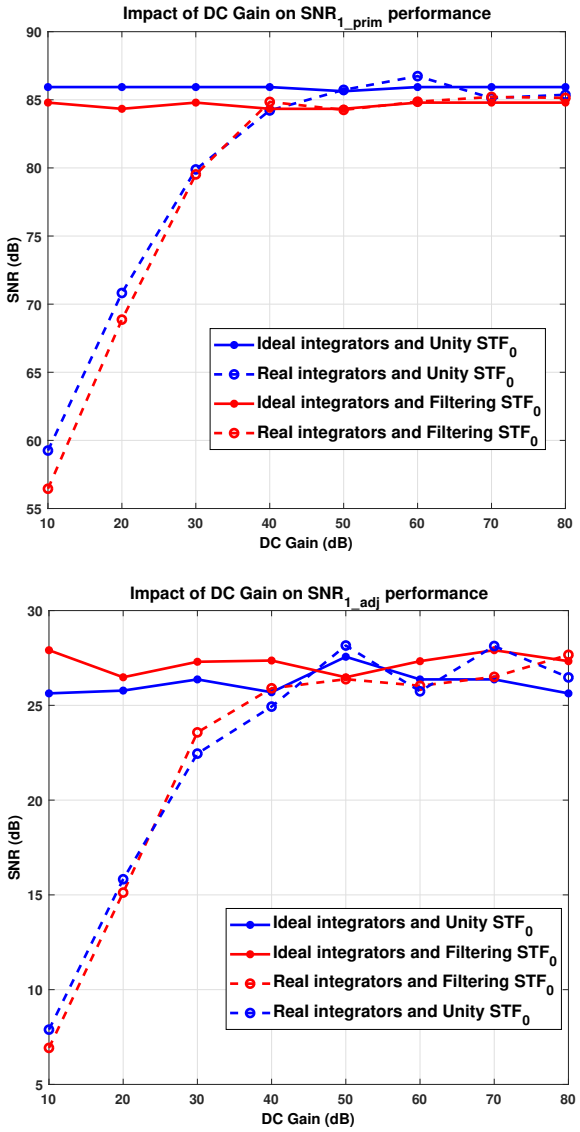


Figure III.3: Effects of finite DC gain on SNR

Another important cause of non-ideal behavior are errors due to the integrator dynamics; here, the first influence to consider is a finite gain-bandwidth product (GBW) of the operational amplifiers in the integrators, which introduces non-dominant poles into the integrator transfer function.

Finite GBW is known from DT modulator implementations to cause distortion and increased in-band noise. The requirements can actually be very high: Boser found that in many sampled-data analog filters, the unity-gain bandwidth of the

OpAmps has to be at least an order of magnitude higher than the sampling rate; in DT ΣΔ modulators, this is somewhat relaxed.

In contrast, CT implementations are claimed throughout the published literature to work with much lower GBW of the OpAmps. This has been largely attributed to the lack of the high-current peaks of switched capacitor implemented DT circuits.

The impact of finite Gain Bandwidth product is studied for an 2-4 MSNBC modulator. The transfer function of an RC-integrator with finite gain-bandwidth GBW can be derived to:

$$H_{RC}^{GBW}(s) = \frac{1}{s * RC} * \frac{\frac{GBW}{GBW+\frac{1}{RC}}}{\frac{s}{GBW+\frac{1}{RC}} + 1} \tag{III.14}$$

Results are presented in Figure III.4. In this simulation, all integrators have the same GBW. Simulations are performed with VerilogA model of integrator and by using the relation in Equation (III.12) for ideal integrators and Equation (III.14) for the cases called real integrators. We assume for those simulations that all integrators have the same GBW. As expected again, the higher the gain bandwidth product, the better the performance of the modulator. Ideal and real integrator show the same performance for when GBW in Hz or rad/s, is greater than $2\pi F_s$.

A straightforward solution to compensate for finite DC gain and GBW is to tune the passive components. However this requires a large and accurate capacitor array for every integrator, thus increasing the core area of the circuit enormously.

Time constant variations

Variations of the integrator gain, determined by the scaling coefficients are a well known non-ideal characteristic of single-loop and even more of cascaded ΣΔ modulators. In DT modulators implemented in SC technique, the integrator gains are mapped into capacitor ratios, which are intrinsically precise and variations lower than 0.1 % are typical. In contrast, in CT ΣΔ modulators, integrator gains are mapped into resistor-capacitor products, which are known to largely vary over process, temperature, etc.; process variations of the absolute component values of $10-20$ % are not unusual, which increases the possible variation of the RC-product to more than 30 %. Therefore this error is a major one to investigate.

The impact of Time constant variations is studied for an 2-4 MSNBC. The transfer function of an RC-integrator with time-constant variation can be derived to:

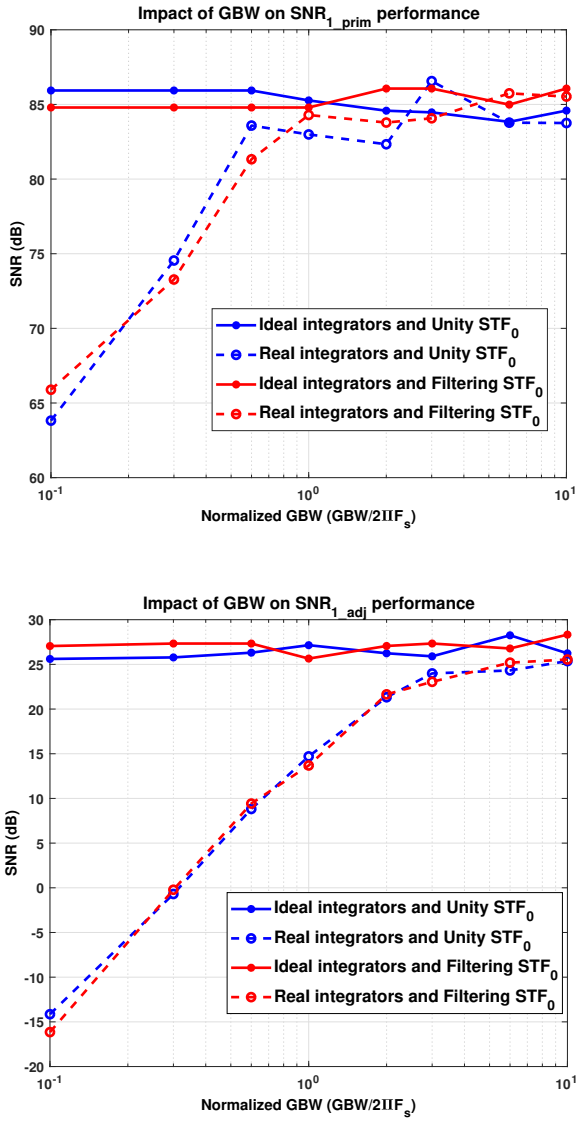


Figure III.4: Effects of finite Gain - Bandwidth on SNR

$$H_{RC}^{\Delta RC}(s) = \frac{1}{s * RC(1 + \Delta RC)} \tag{III.15}$$

Simulations are performed with VerilogA model of integrator and by using the relation in Equation (III.12) for ideal integrators and Equation (III.15) for the cases called real integrators. We assume for those simulations that all integrators have the same RC variation. Results are presented in Figure III.5.

RC time constant variation has an impact on the SNR. As shown in Figure III.5 a 10 % variation of the SQNR reduces the SQNR by 5 dB.

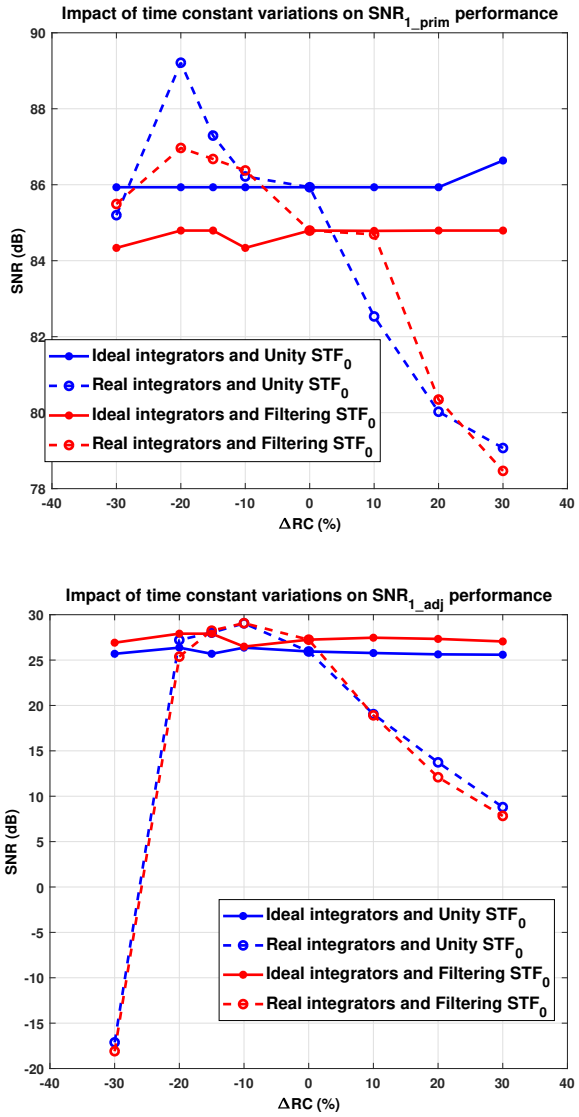


Figure III.5: Effects of RC variations on SNR

III.2.2 Digital-to-Analog Converters

Delay

For an ideal modulator, the steps of quantizing and converting digital to analog signals are instantaneous. However, in the real case, there is a processing time due to the transition time of the transistors. This delay, called excess loop delay, greatly affects the performance of modulators and can make them unstable. As a result, several delay compensation techniques have emerged. The method proposed by [87] makes it possible to design a loop filter identical to the filter without delay by compensating for a delay up to a clock period. This compensation is to the detriment

of an additional amplifier and DAC that results in increased power consumption. [72] enhances the previous technique using a digital differentiator and gets rid of the use of the additional amplifier. [88] suggests a compensation by modifying the integrators, [89] a residual delay compensation by modifying the last integrator and [90] a purely digital compensation.

Among those techniques, [72] is simple to implement and does not have a big impact on the STF. Moreover, since this method restricts us to compensate for delays τ_d such that $\tau_{eld} + \tau_d \leq T_s$, we choose to compensate for delays of up to half a delay clock period.

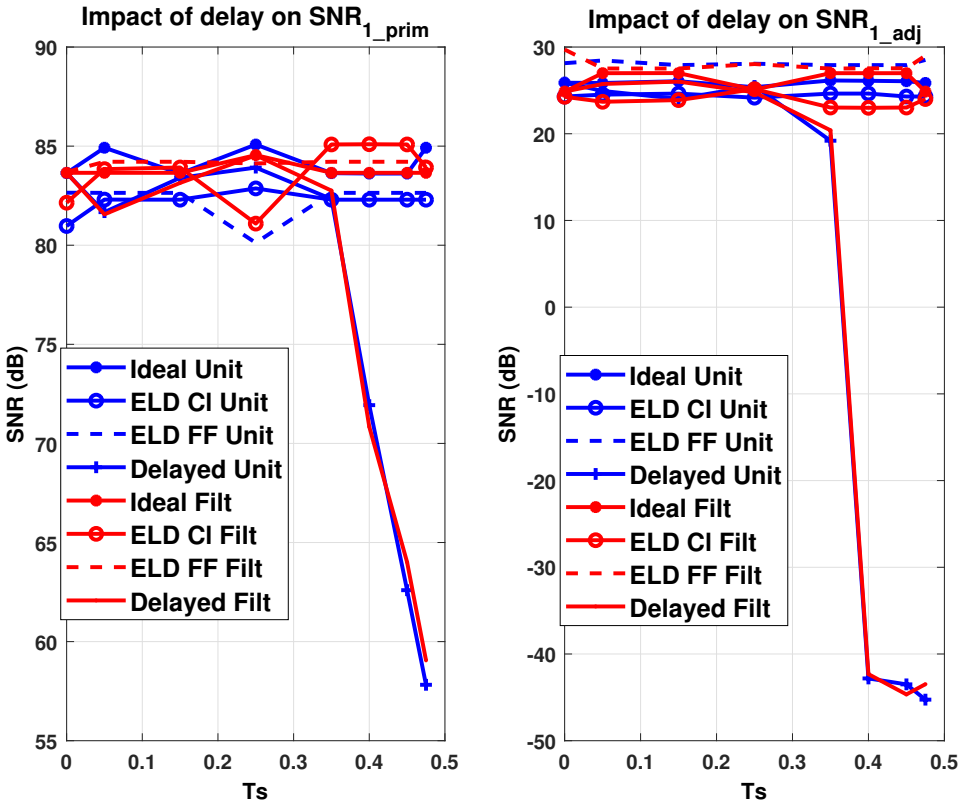


Figure III.6: Effect of loop delay on the SQNR

Figure III.6 shows the influence of the loop delay on the converter and the effect of the compensation of the same delay on SNR_{Y0_pri} and SNR_{S1_adj}. For thsose simulations 2 STF cases are studied: in one case the STFs are unitary in all modulators, and in the other cases the STFs are filtering. For each STF case, the impact of delay is studied for the ideal integrator without delay as in Equation (III.12), with delay, with classical and feedforward delay compensation techniques.

It follows that the modulator becomes unstable for a delay greater than $0.35T_s$

and that the classical and feedforward ELD compensation technique used perfectly corrects this delay up to $T_s/2$.

Unequal rising and falling times and mismatch

At the opposite of DT modulators, CT modulators are affected by inter-symbol interference (ISI). ISI is an error which shows up during transition of DAC elements and can be caused by asymmetric on and off switching. ISI error is problematic for high speed CT modulators as it increases with sampling frequency.

An analog approach to reduce ISI error is to use return-to-zero (RZ) coding in DACs. However, it increases sensitivity to clock jitter compared to non-return-to-zero (NRZ) coding. RZ coding also reduces the output signal amplitude for the same total DAC power, and introduces large discontinuities in the output waveform. This in turn increases the linearity and slew rate requirements of the output filter [91].

In addition to ISI, DACs and more generally analog components suffer from mismatch. Two transistors or capacitors, for example, that are ideally supposed to be identical suffer from mismatch due to process variations. Dynamic Element Matching (DEM) algorithms can be used to handle mismatch errors of DACs. Among those techniques Data Weight Averaging (DWA) is fairly easy to implement. The purpose of the DWA is to use the maximum number of unit current cell in order to average the static mismatch error over time. However, DWA increases the switching activity of the DAC. Thus, for a DAC suffering from inter-symbol interference, DWA degrades performance.

The ISI error model presented in [91] was implemented in Matlab with the MSNBC architecture. For those simulations, all DACs are assumed to have different rising and falling times. For a current quantizer value $Y[n] = 4$ and a previous value $Y[n-1] = 3$, thermometric and DWA encoders as presented in Figure III.7 are used to estimate the states of the quantizer output.

Figure III.8 explains the methodology used to estimate analog errors in the Matlab code.

Thus, the number of changed and unchanged states are calculated and total error is added to the ideal signal. This methodology is applied to a 2-4 MSNBC modulator. The primary modulator is a second order lowpass modulator and the secondary modulator is a fourth order bandpass modulator centered at $F_c = 20\,\text{MHz}$. The input signal is at $F_{in} = 2.5\,\text{MHz}$ and the sampling frequency is $F_s = 640\,\text{MHz}$. Several cases are studied in Figure III.9 and Figure III.10:

- Case 1: no mismatch, DWA OFF

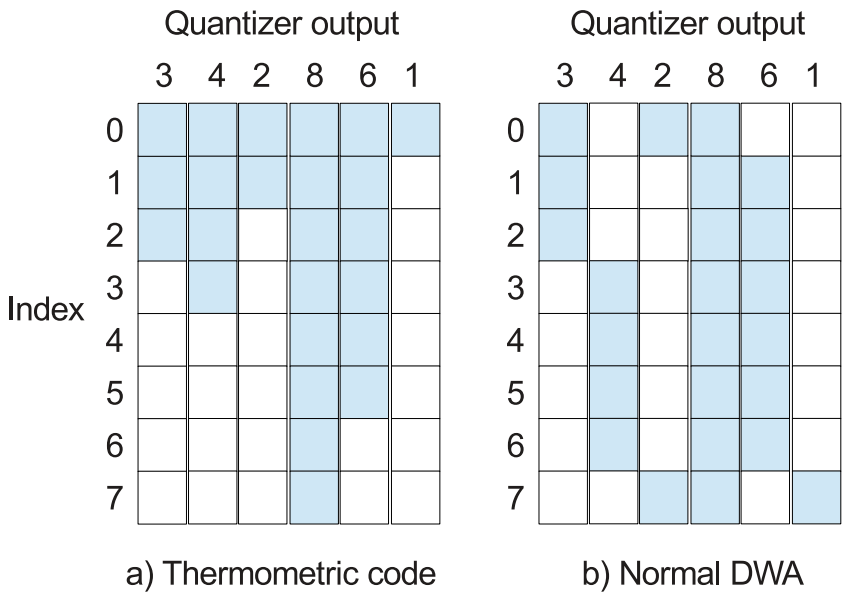


Figure III.7: Quantizer output with the thermometric code and normal DWA

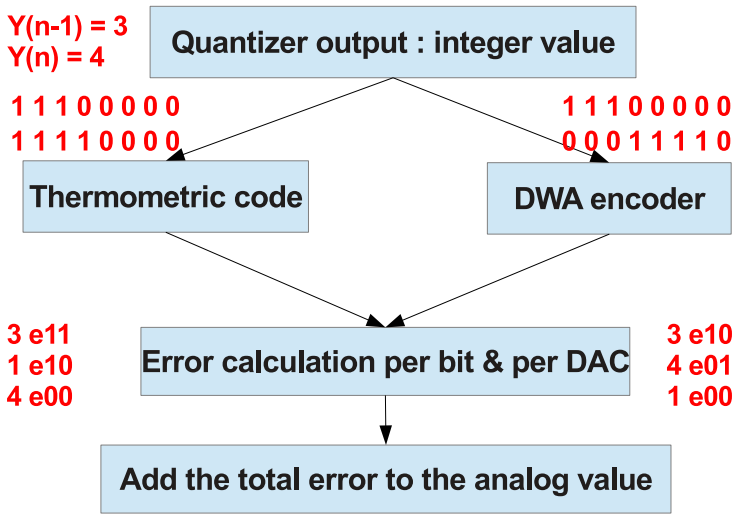


Figure III.8: Method used to calculate errors

- Case 2: 1% mismatch, DWA OFF
- Case 3: 1% mismatch, DWA ON

Figure III.9 illustrates Case 1. When $tr = tf$, the SNR in the primary band of S_0 $SNR_{pri_S_0}$ and the SNR in the adjacent band of S_1, $SNR_{adj_S_1}$ are constant over 10% variation. When $tr \neq tf$, performance are degraded as the difference is high.

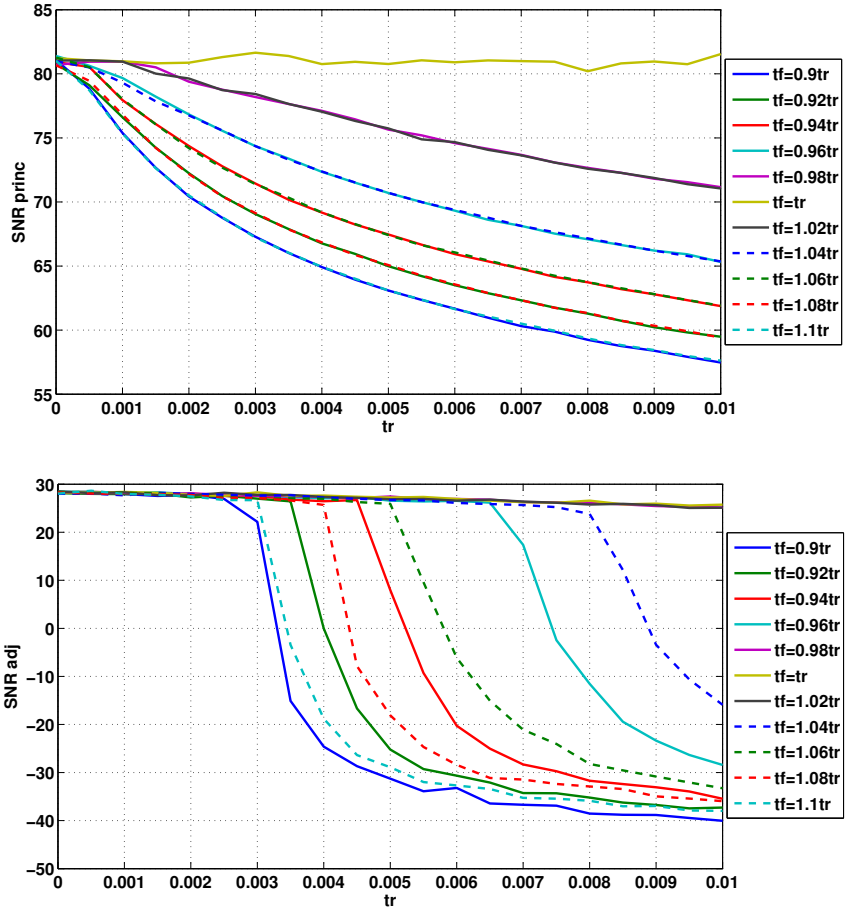


Figure III.9: Impact of rising and falling times on the MSNBC performance

Case 2 and 3[1] are presented in Figure III.10. Those results proves the impact of DWA on a system with 1% DAC mismatch. The left plots are $SNR_{pri_S_0}$ and $SNR_{adj_S_1}$ values without DWA. $SNR_{pri_S_0}$ is 30 dB less compare to Case 1, where there is no mismatch.

The right plots represent Case 3. We can see that DWA improves $SNR_{pri_S_0}$ values, but performance is rapidly degraded compared to those obtained in Case 1. We decide not to use DWA and to take care of mismatch in the design by using big size components.

III.2.3 The Clock Signal

Clock jitter, i.e., statistical variations of the sampling frequency, depends on the purity of the clock source. Typically, $\Sigma\Delta$ modulators were found to be rather tolerant to timing jitter. However, continuous-time modulators are affected more

[1]The same legend is used for all cases

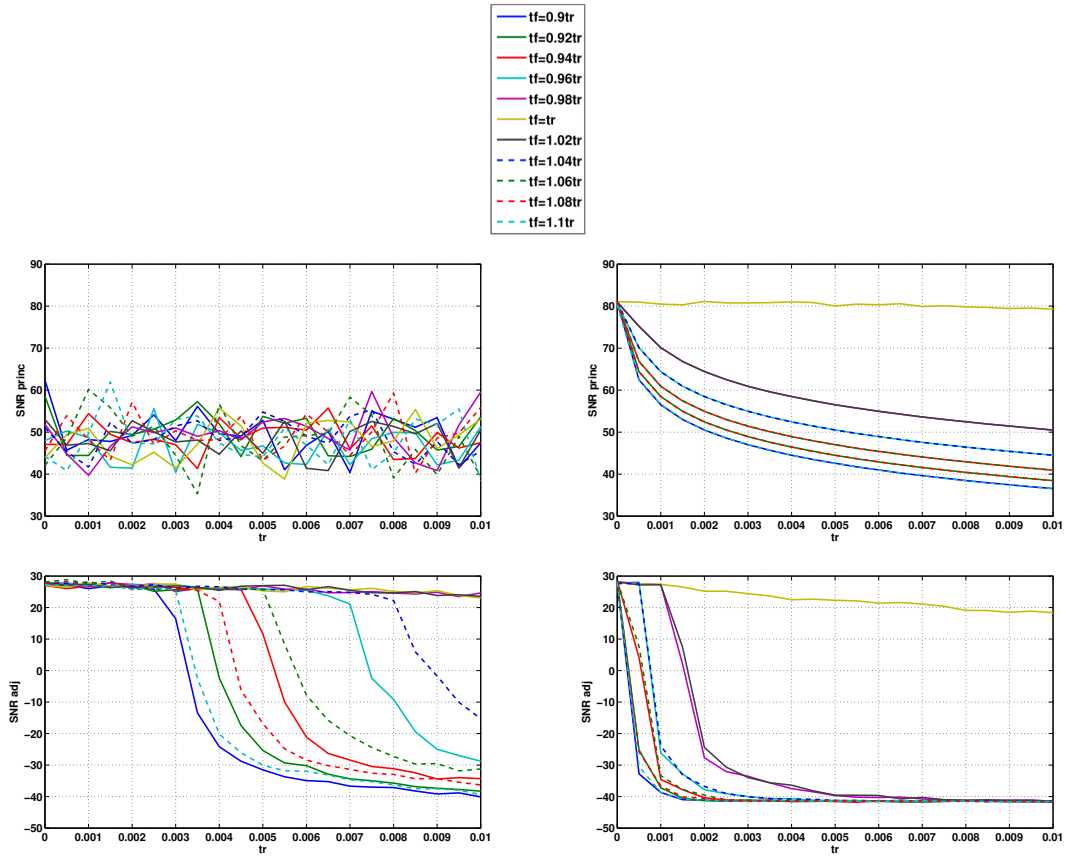


Figure III.10: Impact of DWA on performance of a MSNBC with 1% DAC mismatch. Left figures are results with mismatch and DWA OFF, and right figures are results with mismatch and DWA ON

severely by clock jitter than their discrete-time counterparts, as shown manifold in the published literature.

The difference of clock jitter influence on DT and CT $\Sigma\Delta$ modulators appears since both feature different sources of clock jitter errors in the modulator loop. Suppose nonuniform sampling takes place, the decision of the quantizer in DT modulators remains correct in first-order approximation, because the integrators are designed to settle to a given accuracy within half the sampling period. Therefore, the performance degradation due to clock jitter is primarily caused by errors in the front-end S/H circuit, where jitter caused sampling misalignment produces an equivalent amplitude error that degrades the SNR.

A CT implementation faces two error sources due to clock jitter: first, similar to the sampling errors in the DT modulator, the sampled internal quantizer is prone to jitter affected sampling errors. But these errors enter the system at the point of maximum error suppression, i.e., at the quantizer, and hence may be neglected

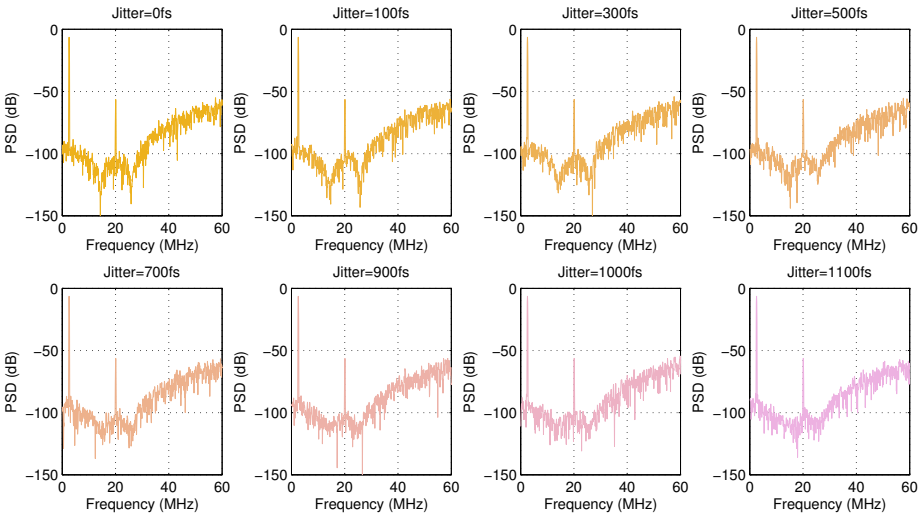


Figure III.11: Effects of clock jitter on S_1

in practice. The dominant influence of clock jitter in CT implementations appears through errors resulting from the feedback DAC: this is because a CT $\Sigma\Delta$ modulator integrates the feedback waveform over time. Thus, a stochastic variation of the feedback waveform results in a stochastic integration error and consequently in increased noise.

Using multi-bit quantizers helps to reduce CT $\Sigma\Delta$ modulators sensitivity to clock jitter. When using multi-bit feedback and Non Return to Zero pulses, the difference of two adjacent feedback pulses will differ mostly by only one LSB (least Significant Bit), thus reducing the jitter influence by orders of magnitude. The clock jitter improvement is approximately 6 dB for each additional bit.

The impact of clock jitter was studied on a 2-4 MSNBC modulator. The primary modulator is a second order lowpass modulator and the secondary modulator is a fourth order bandpass modulator centered at $F_c = 20\,\text{MHz}$. The input signal is at $F_{in} = 2.5\,\text{MHz}$ and the sampling frequency is $F_s = 640\,\text{MHz}$. A 100 to 1100 fs jitter is added to the clock generating the sampling frequency for both modulators. Figure III.11 illustrates the spectra of the output signal after reconstruction with noise cancellation filters.

The jitter increases the noise floor and clearly degrades the performance of the modulator. As presented in Table III.2, a jitter of 1.1 ps degrades the SNR in the adjacent channel of the reconstructed signal by 2 dB. However, the main signal is more affected with this non ideality. The impact of Jitter can therefore be neglected if using a clock with less than 300 fs jitter.

Jitter	S_0	S_1
0	92.39	27.29
100 fs	88.42	26.30
300 fs	80.43	27.20
500 fs	77.34	26.02
700 fs	73.95	24.53
900 fs	72.22	24.26
1000 fs	71.16	25.15
1100 fs	70.35	25.12

Table III.2: SNR vs. clock jitter

III.3 MSNBC Architectural Design Choice

Before jumping into the design of the CT MSNBC ADC, several design choices should be made.

III.3.1 Zero IF vs. Low IF

The MSNBC modulator consists of several $\Sigma\Delta$ modulators with different center frequencies: F_{c0}, $F_{c0} \pm BW$ and $F_{c0} \pm 2BW$. Thus, two implementations of this modulator are possible: at an *intermediate frequency* (*IF*) with $F_{c0} = F_S/4$ for example, where F_S is the sampling frequency of the modulator, or at *zero IF* with $F_{c0} = 0\,\text{Hz}$.

Figure III.12 illustrates the Low IF and Zero IF MSNBC archtectures. The choice of one design compared to the other depends on specifications.

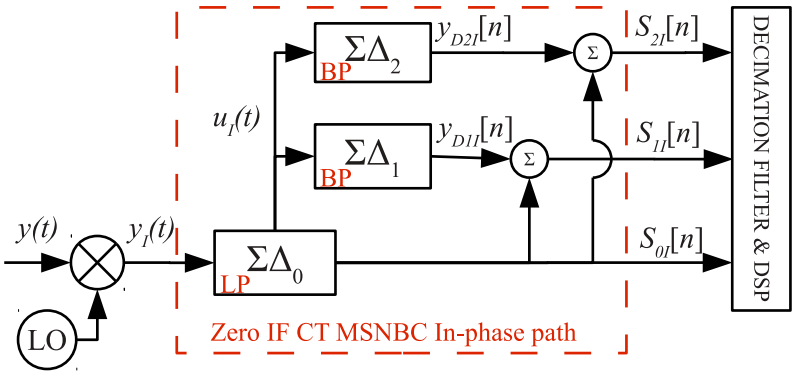


Figure III.12: In-phase path of the CT zero IF MSNBC architecture

Modulator characteristics

First, in a zero IF architecture, the NTF complex conjugate zeros are closer to each other, which improves significantly the SNR. The direct impact can be seen on the order as well as the resolution of the quantizer of the first modulator. We have to fix the order, out-of-band gain, and quantizer resolution for all modulators. The zero IF architecture requires to design less different modulators compared to the IF architecture which needs as many different modulators as subbands to digitize.

As presented in Figure III.12, each identical (I/Q) path of a zero IF MSNBC modulator is made of a lowpass modulator and two bandpass modulators.

For this case, Matlab simulations were run to find optimal values for those three $\Sigma\Delta$ modulators parameters. The sampling frequency used is set to $F_S = 640\,\text{MHz}$ and adjacent modulators are centered at $\pm 20\,\text{MHz}$. The proximity of NTF zeros improves the signal to noise ratio as well as distortions.

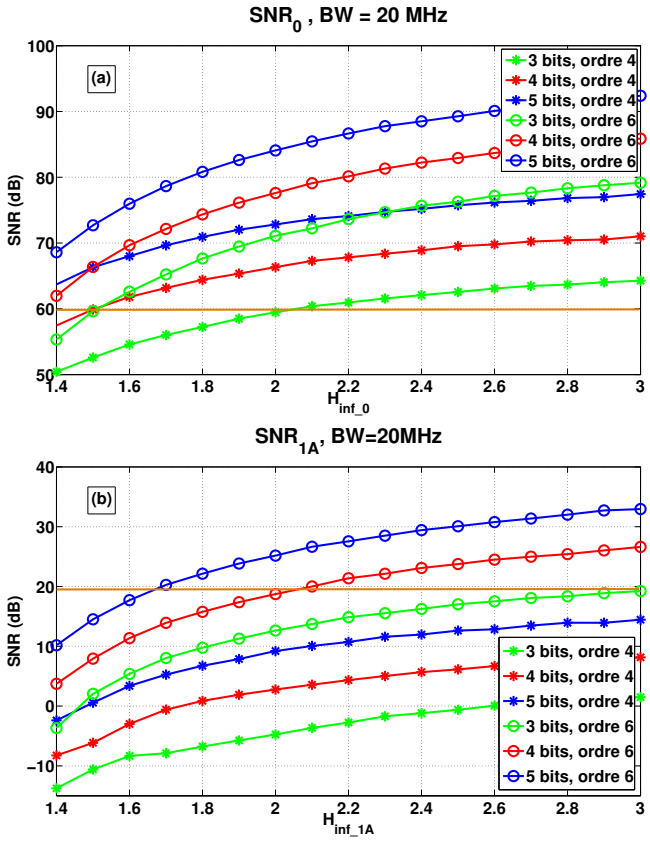


Figure III.13: Impact of loop filter order and quantizer resolution on SNR_0 and SNR_{1A} performance for a bandpass primary modulator with $F_{c0} = F_S/4$

For the the LIF case where the central frequency is at $F_{c0} = F_S/4$, Matlab simulations were also carried out to extract key modulators parameters to meet per-

formance specifications. Figure III.13 presents the impact of the modulator order, OOBG and quantizer resolution on the SNR. The sampling frequency used is set to $F_S = 640\,\text{MHz}$ and the input signal is centered at $F_{c0} = 140\,\text{MHz}$. Adjacent modulators are centered at 120 and 160 MHz. As presented in Figure III.14, several simulations with different cases of quantizer orders in the secondary modulator were performed. Top figures represent the SNR in the main bandwidth, bottom figures represent SNR in adjacent bandwidth. We can see that the primary modulator should at least be a fourth order modulator with 4-bit quantizer to meet our specifications. Adjacent modulators should be sixth order modulator with 4-bit quantizer for this LIF case.

Figure III.15 presents simulation results of a 2-4 ZIF MSNBC configuration. Different cases of quantizer orders are performed. Thanks to those results, the primary modulator of the ZIF architecture should at least be a second order modulator with 4-bit quantizer to meet specifications. Adjacent modulators with 20 MHz bandwidth can at least be fourth order modulator with 4-bit quantizers.

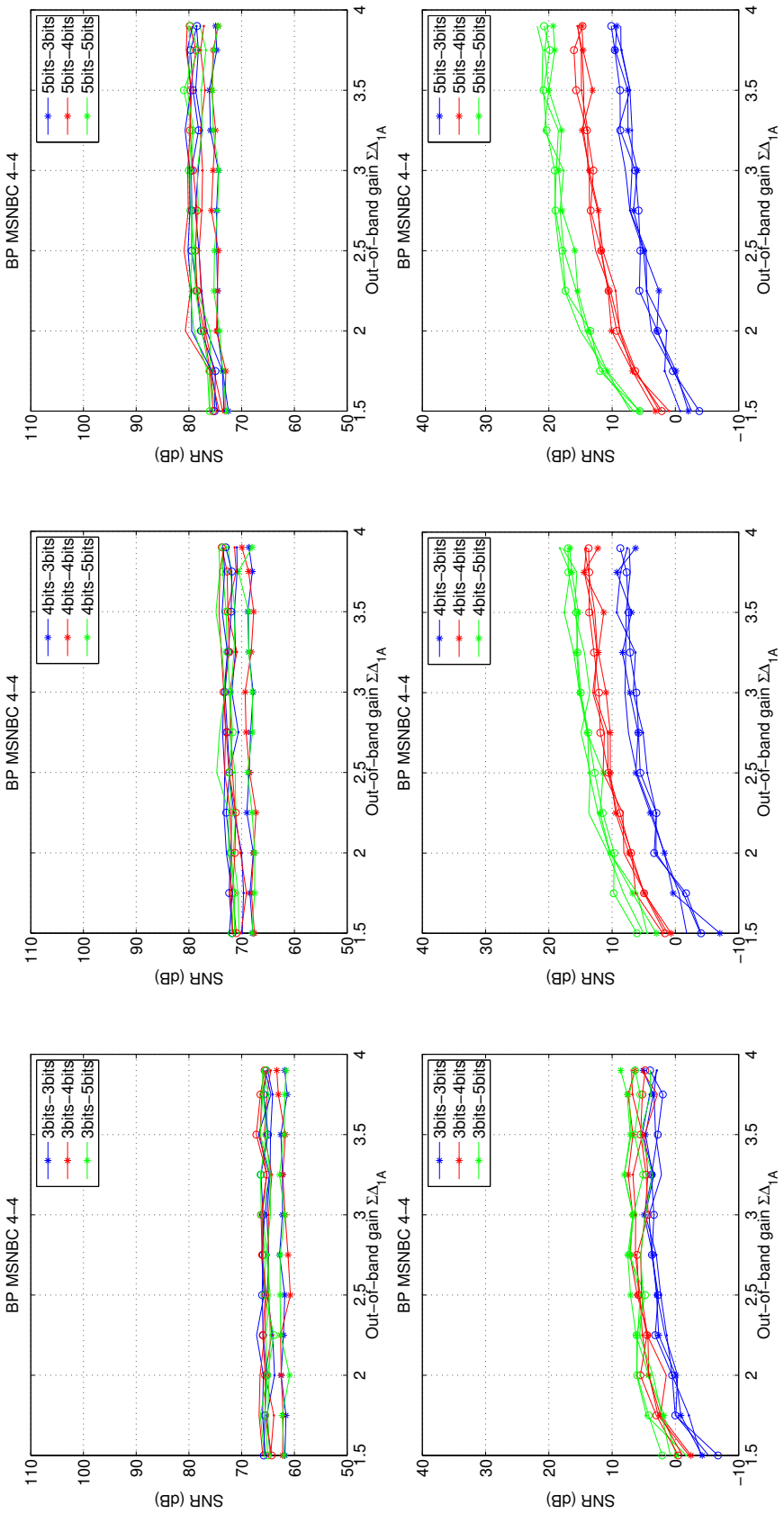


Figure III.14: Impact of quantizer resolutions on SNR_{1A} performance for LIF MSNBC

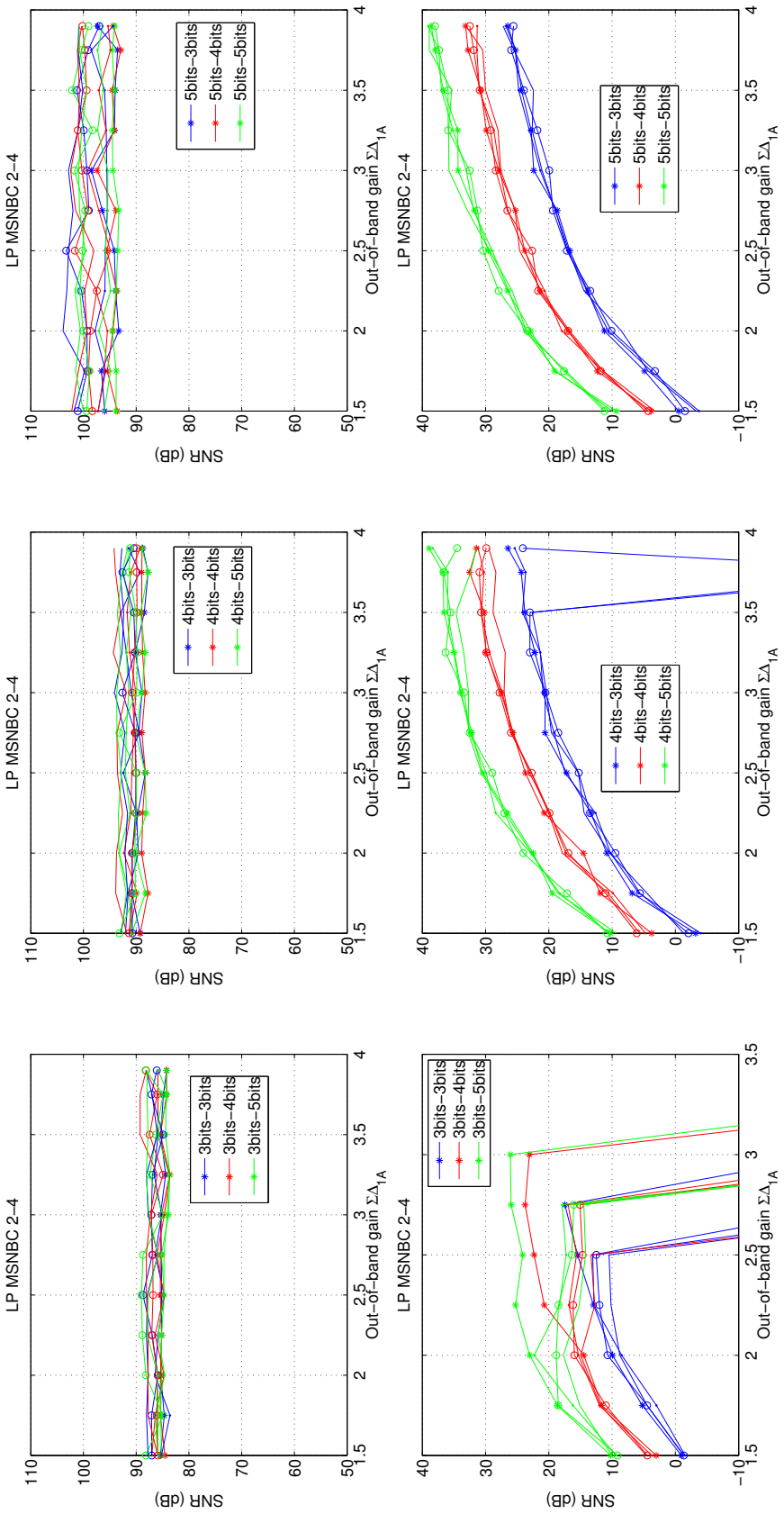


Figure III.15: Impact of quantizer resolutions on SNR_{1A} performance for ZIF MSNBC

Impact of delay

Another important aspect in MSNBC modulators is the delay. The delay of the loop filter alters the RSTF and thus limits the cancelation of the input signal at node U. Moreover, since a CT modulator implementation has been chosen for the modulators, the architecture is sensitive to *Excess loop delay* (ELD). This delay has been widely studied over the past and several methods have been proposed to deal with this non ideality. In [92] some compensation methods are compared. While those techniques will maintain the STF and SNR performance of a modulator, they may degrade the RSTF. Figure III.16 compares the RSTF of a 4^{th} order lowpass modulator to the RSTF of a 4^{th} order bandpass modulator centered at $Fs/4$. For each implementation, two cases are presented: the ideal modulator without ELD and the modulator with ELD and the classical compensation [92]. It can be seen that ELD compensation considerably impacts the RSTF of the bandpass modulator. The signal attenuation around DC is close to 44 dB for the ideal and the ELD compensated lowpass modulator. However, for the bandpass modulator, the RSTF notch located at $Fs/4$ is shifted because of the delay. The attenuation around $Fs/4$ drops from 36 to 5 dB. Thus, a better RSTF is achieved with the zero IF CT MSNBC compared to the IF CT MSNBC.

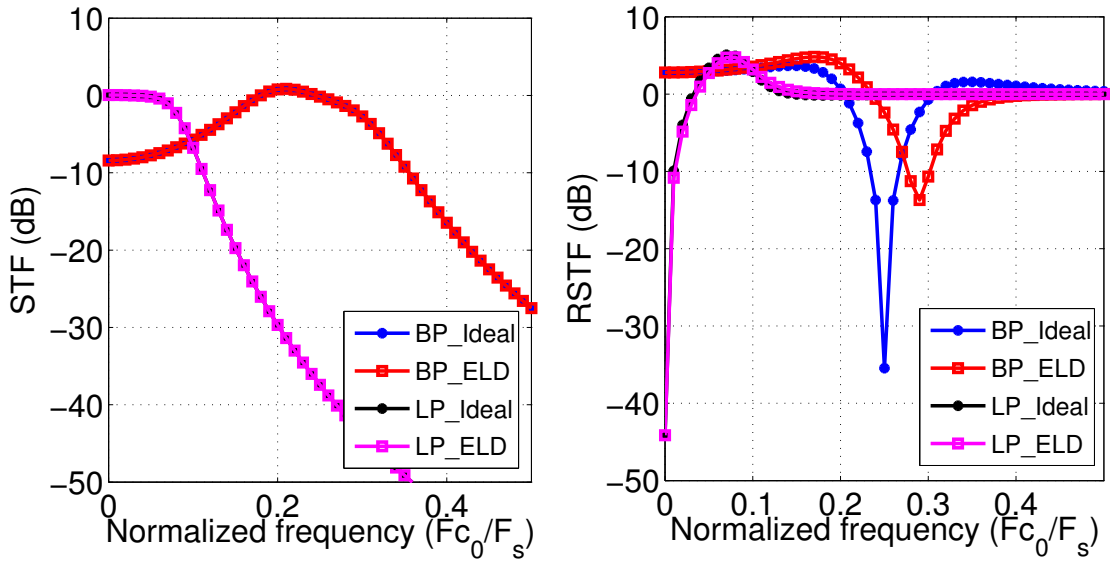


Figure III.16: ELD effect on RSTF

Mismatch between the I and Q path which will degrade the performance of DPD in the zero IF architecture. In addition to I/Q mismatch, flicker noise will have a

great impact on the Zero IF architecture compare to the Low IF one given that the frequency of the LIF is far from DC compared to ZIF frequencies.

Given the pros and cons of the ZIF and LIF architectures, the ZIF architecture is suitable for our application.

III.3.2 STF Choices

In Section III.1, the mode of operation of the MSNBC architecture is presented. However, for the sake of simplicity, all signal transfer functions were assumed to be equal to 1, and this not always the case, especially for CT systems. The choice of having a unity STF in the band of operation is thus a design choice for the modulator.

In the case of a CIFB modulator, a unitary STF in the band of operation can be obtained by choosing $b_i = a_i$ and $b(n+1) = 1$, where $1 \leq i \leq n$ and n is the modulator order. However, the STF has an out-of-band gain of 10 dB as shown in Figure III.17. This OOBG of the STF can saturate the quantizer in case of out of band signal.

By choosing the modulator coefficients such that ($b_1 = a_1$ et $b_{2:n+1} = 0$) a filtering STF is implemented. In this case, out of band signals are attenuated and the gain is unity in the band of operation. However, the cancellation of the main signal is degraded. Furthermore, in this case, in order to obtain the right noise suppression, the output of each modulator will have to be digitally processed. This is performed by Noise Cancellation Filters (NCF).

Designing $\Sigma\Delta_0$ with a filtering STF however degrades the RSTF. For instance, on Figure III.17 for an input signal at 2.5 MHz, the signal fed to the secondary modulator is attenuated by 26.3 dB when using a unitary STF and by 19.2 dB with a filtering STF.

ELD impact on the STF

We previously showed that excess loop delay affects the MSNBC performance. This is even more important as the MSNBC architecture relies on the RSTF. Several techniques to compensate for this delay exist [87], [88] , [89], [90]. Those techniques aim to create an unchanged noise transfer function as presented in Figure III.18.

However, when implementing those compensation techniques, the STF of the modulator is changed. This change should be taken into account in the calculation of the NCF to an optimal cancellation of the primary modulator noise in S_{1A}. Detailed calculation of NCFs in presence of ELD compensation are presented below:

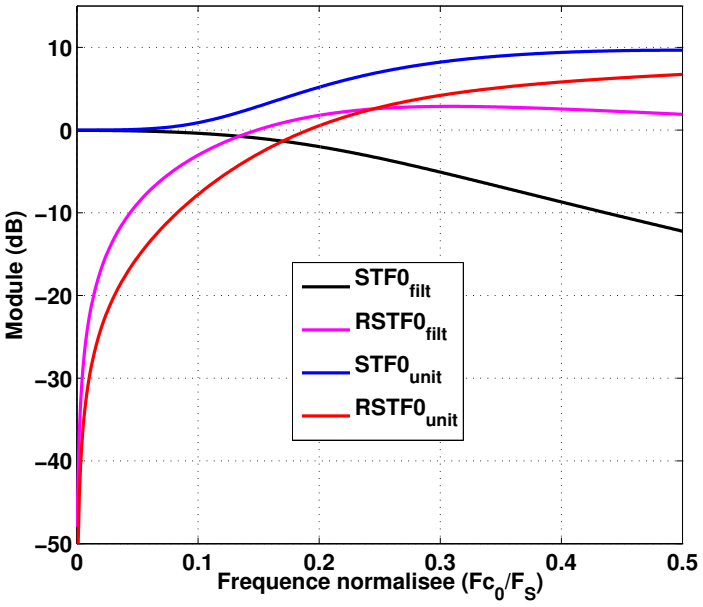


Figure III.17: STF and $RSTF$ comparison

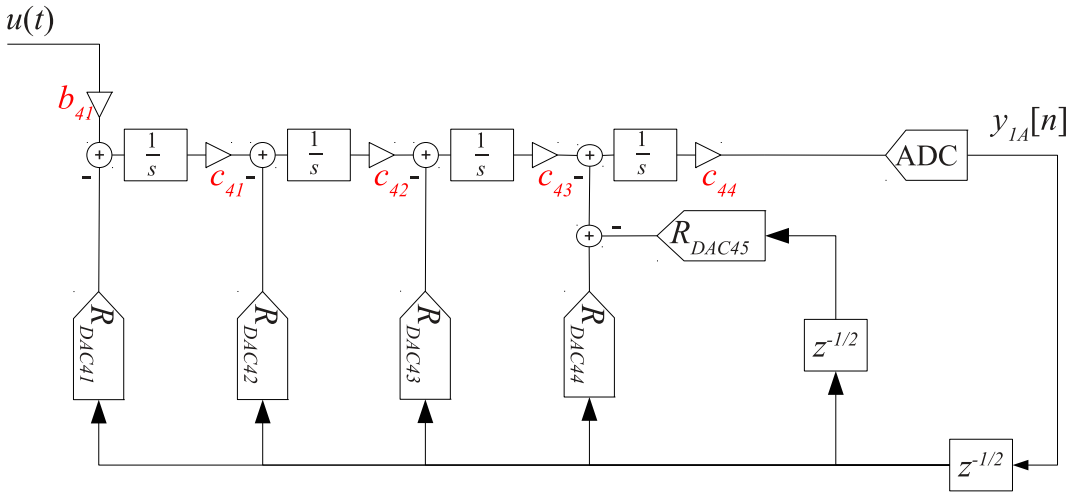


Figure III.18: Fourth order modulator with classical ELD compensation

Assuming a 4^{th} order CIFB modulator, with NRZ DACs and digital differentiator ELD compensation, the output $Y_{1A}(z)$ is expressed as :

$$Y_{1A}(z) = \frac{N_{1A}(z)}{1 + \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_4(s)\right\rangle_{|t=kT_S}\right] z^{-1/2} - \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle \mathcal{R}_{DAC_{45}}(s)G(s)\right\rangle_{|t=kT_S}\right] z^{-1}} + \frac{\mathcal{Z}\left[\mathcal{L}^{-1}\left\langle b_{41}c_{41}c_{42}c_{43}c_{44}G^4(s)U(s)\right\rangle_{|t=kT_S}\right]}{1 + \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle H_4(s)\right\rangle_{|t=kT_S}\right] z^{-1/2} - \mathcal{Z}\left[\mathcal{L}^{-1}\left\langle \mathcal{R}_{DAC_{45}}(s)G(s)\right\rangle_{|t=kT_S}\right] z^{-1}} \tag{III.16}$$

Where

$$U(s) = b_1 X(s) - \mathcal{R}_{DAC_{21}}(s) \cdot \mathcal{L}\left\langle y_{0[n]}\right\rangle(s) \cdot e^{sT_d/2} \tag{III.17}$$

$$H_4(s) = c_{41}c_{42}c_{43}c_{44}G^4(s)\mathcal{R}_{DAC_{41}}(s) + c_{42}c_{43}c_{44}G^3(s)\mathcal{R}_{DAC_{42}}(s) + c_{43}c_{44}G^2(s)\mathcal{R}_{DAC_{43}}(s) + c_{44}G(s)\mathcal{R}_{DAC_{44}}(s) \tag{III.18}$$

$$S_{1A}(z) = NCF_{1A}^{\tilde{D}}(z) \cdot Y_0(z) + NCF_{1A}^{\tilde{N}}(z) \cdot Y_{1A}(z) \tag{III.19}$$

Performance analysis of the reconstructed signal was done when the correct NCFs were not used. Figure III.19 compares the SNR in the adjacent channel after reconstruction and by using NCFs which take ELD into account. 2 cases are presented: in one case, NCFs estimated assuming no ELD are used to reconstruct the signal, in other cases NCFs calculated assuming ELD compensation are used.

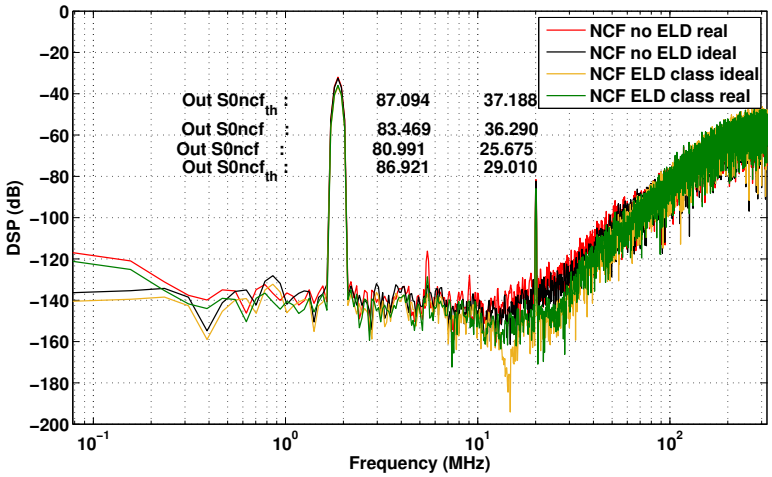


Figure III.19: Fourth order modulator with classical ELD compensation

We can see that using the NCFs improves the SNR in the adjacent channel. Furthermore the use of an accurate model leads to a better signal to noise ratio.

III.3.3 Signal Scaling

The quantizer of secondary modulators is important as well. As demonstrated in the mode of operation, the signal sent to the second modulator is the shaped quantization noise of the first modulator, which is in fact noise. This means that the amplitude of this signal is low compared to the amplitude of the input signal of the first modulator. Thus, two options are offered for adjacent modulators:

- On the one hand, the input signal can be scaled so that an identical quantizer as the one in the first modulator can be used. This means that a gain should be applied to the shaped quantization noise before being digitized by the adjacent modulator.

- On the other hand, the signal is not scaled, thus, the reference voltage of QTZ_{sec} is decreased.

We choose to scale the signal at the input of the second modulator and use the same quantizer in both modulator. However, the RSTF should be approximated carefully as a bad scaling will result in saturation of the adjacent modulator.

III.4 The MSNBC: Top level design

The MSNBC modulator has the feature to implement several DR specifications per band, hence relax adjacent ADCs requirements for signals with specific spectral composition. The shaped quantization noise of the primary modulator is removed by summing the outputs of $\Sigma\Delta_0$ and $\Sigma\Delta_{1A}$ and by using NCFs to compensate for non unitary STFs. Thus the SNR of the primary channel is improved in the main channel as well as the adjacent one.

III.4.1 Design Parameters

We proved in Chapter 1 that at least 50 and 12 dB SNR are required respectively for $\Sigma\Delta_0$ and $\Sigma\Delta_{1A}$/ $\Sigma\Delta_{1B}$ in order to maintain the ACPR as in an ideal feedback path. Nevertheless, it is important to include margins to those specifications to compensate for non-idealities and noise. As the signal to quantization noise (SQNR) is 10 dB under our noise budget, an extra 10 dB margin is added to previous requirements.

Several ADC parameters should be set according to the needed resolutions: the oversampling ratio, orders of modulators and quantizers number of bits. To estimate those parameters, continuous time simulations are done with Matlab and Cadence Spectre. A modified version of the Delta Sigma Toolbox [93] is used to generate the coefficients of $\Sigma\Delta$ modulators. Those values are extracted to simulate the schematic of the zero IF CT MSNBC modulator of Figure III.12. The modulator consists of ideal blocks implemented in VerilogA. Because the zero IF CT MSNBC modulator has two identical paths, only results of the in-phase path are presented. All $\Sigma\Delta$ modulators have the continuous time feedback cascaded form. The reason for this choice is to avoid a peak in the signal transfer function as in the feedforward form. The STF of all modulators is assumed to be 0 dB in bands of operation. Unitary STFs prevent using noise cancellation filters.

The test signal used is the sum of three sine waves representing the mono carrier 20 MHz LTE signal and non-linearities in each adjacent channel. A sine wave is used instead of a real 20 MHz LTE signal to simplify SNR calculations. In section III, the initial ACPR in 20 MHz bandwidth is 30 dBc. For the following simulations, the amplitude of first adjacent subband non-linearity is set to -50 dBc because the system is more stringent when non-linearity amplitudes are low. To meet requirements, 2^{nd}

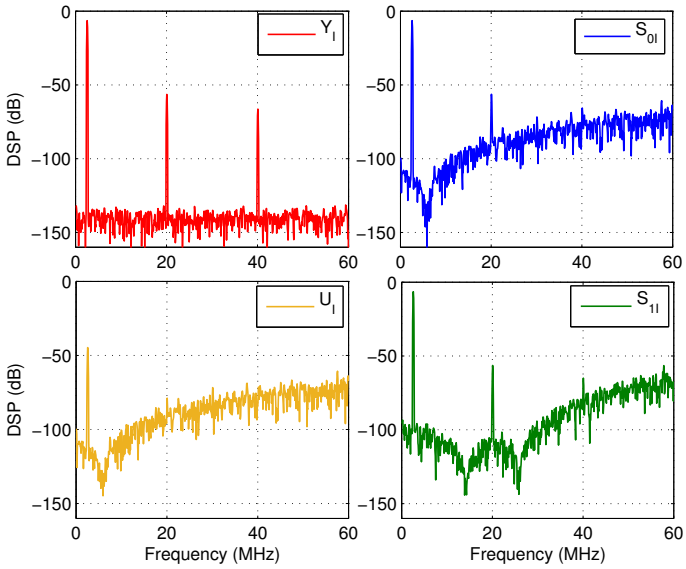


Figure III.20: MSNBC signals spectra

and 4^{th} order modulators with 4-bits quantizers are used, and the sampling frequency is 640 MHz. Figure III.20 presents the Power Spectrum Density (PSD) of signals versus the frequency. As expected, the main signal is not completely cancelled in U_I, but attenuated by 38 dB. This is because the output signal of the modulator is slightly delayed compared to the input signal. The SQNR of S_0 first subband is improved by 20 dB. The modulator achieves 86.7 dB SQNR in the main bandwidth and 30.5 dB in the first adjacent channel of S_{1I}.

III.4.2 2-4 MSNBC vs. 0-4 MSNBC

We saw in Chapter I that in order to perform a proper DPD, the feedback ADC should have 60 dB SNR in the main channel and 20 dB SNR in the adjacent channel. We need an ADC architecture that improves the SNR in adjacent channels. Two options are therefore possible with the MSNBC architecture.

We can have a high precision design of the primary modulator, and take the signal of the main bandwidth at the output of $\Sigma\Delta_0$. Another option, on the other hand, is to relax design constraints in the primary modulator and take the main signal after adding the outputs of both modulators. We can then have a 2-4 or a 0-4 MSNC as illustrated in Figure III.21. In the 0-4 MSNBC, the input signal is directly digitized by a 4-bit quantizer. The output signal of the quantizer is then converted in the analog domain with a DAC and subtracted to the input signal before being fed to the adjacent modulator.

A comparison of top level simulation results of the two MSNBC configurations

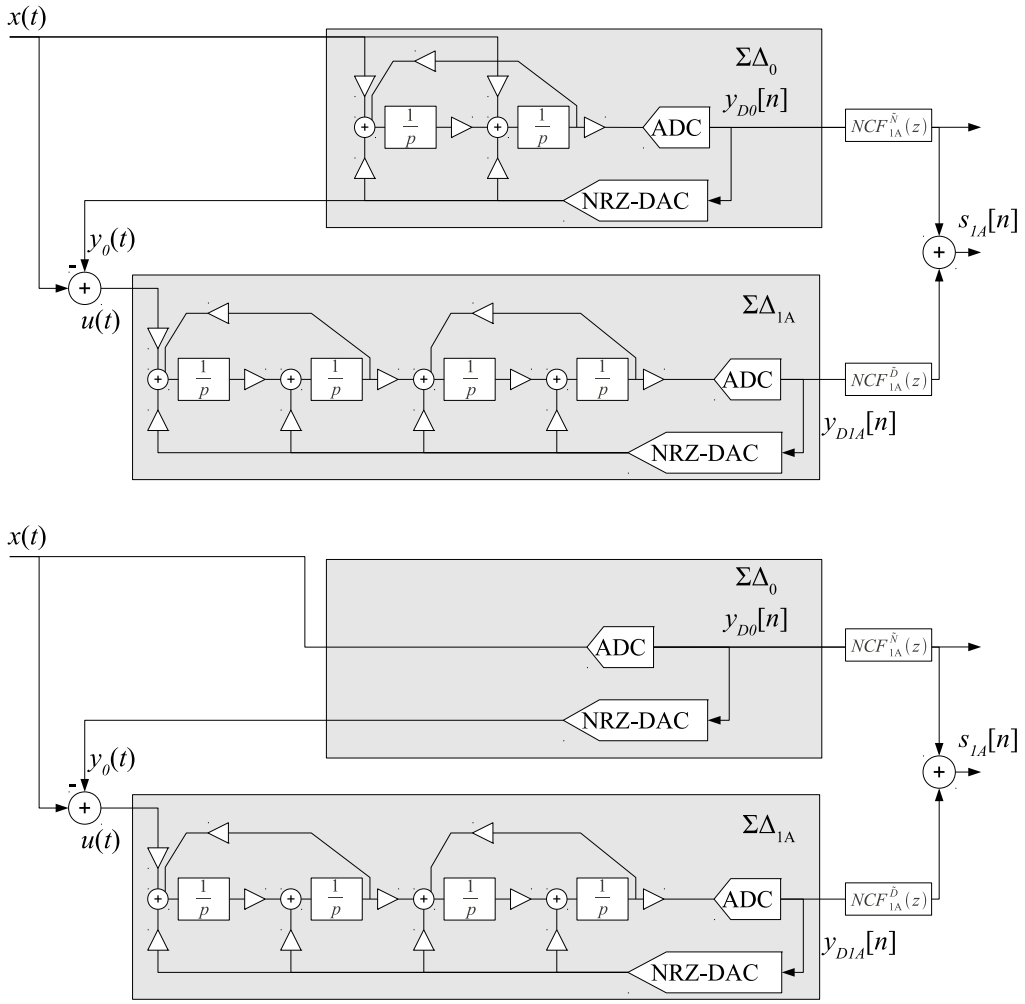


Figure III.21: 2-4 and 0-4 MSNBC schematics

is presented in Figure III.22. For those simulations the STFs of all modulators are unitary. Thus, no NCFs where used before summing $\Sigma\Delta_0$ and $\Sigma\Delta_1$'s outputs. The SNRs of $Y0_{24}$ and $Y0_{04}$ in the main channel are respectively 88 and 45 dB. However, after addition, $S1_{24}$ and $S1_{04}$ both have 73 dB in the main channel. The difference is however noticeable in the adjacent channel. Their performance are respectively 38.1 and 35.4 dB for $S1_{24}$ and $S1_{04}$.

As will be shown in Chapter IV, non-idealities of the primary modulator are compensated in the secondary modulator in the case where $\Sigma\Delta_1$ doesn't have a unitary STF and where NCFs are used. This option is however not available in the MASH architecture and will trade analog design constraints into digital filter design constraints. The MASH architecture requires a good matching of the NTF. This is achievable for Discrete Time modulators. For continuous time $\Sigma\Delta$ modulators,

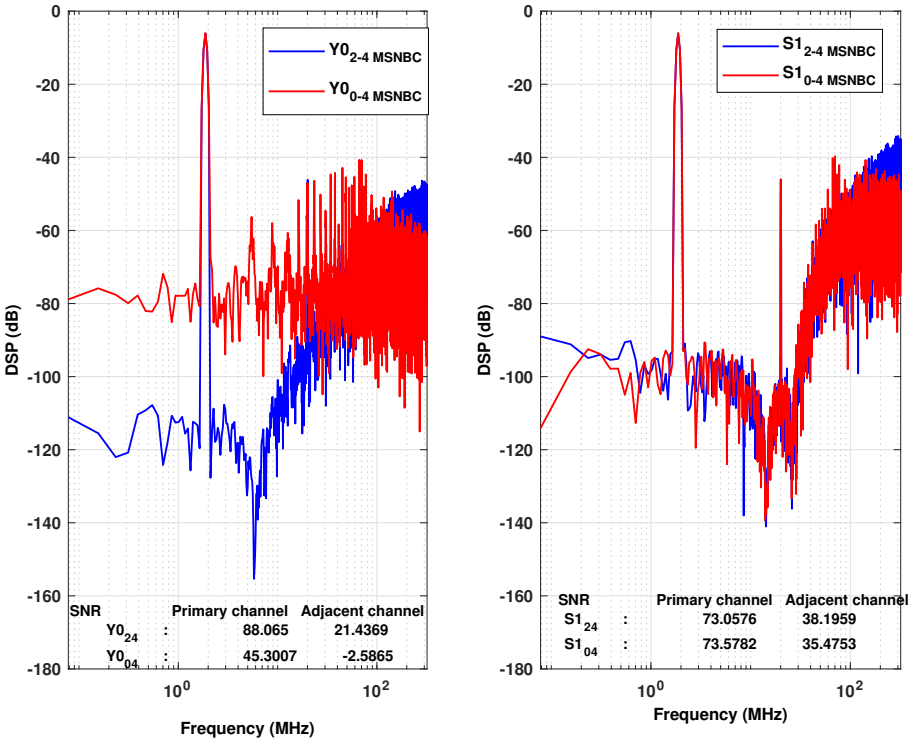


Figure III.22: 2-4 and 0-4 MSNBC top level simulation results

whereas some CT MASH ADCs exist, non-idealities make the matching of the NTF worse.

In order to compare the 2-4 and 0-4 MSNBC architectures, we have decided to implement both of them on silicon. A switch will be added to by-pass the first modulator and enable the change between the 2-4 and the 0-4 architectures.

III.5 Conclusion

In this chapter, we presented the mode of operation of the MSNBC ADC as well as top level design choices. The impact of non-idealities specific to the MSNBC were investigated. Our investigation leads us to design a flexible architecture where we can either choose to be on a 2-4 or a 0-4 topology. Thus, the first modulator can either be a second order continuous time Sigma Delta modulator with a 4-bit quantizer or a 0-order modulator with a 4-bit quantizer. The adjacent modulator is a 4^{th} order CT modulator with a 4-bit quantizer. Given that all modulators need a 4-bit quantizer, we decide to use the same quantizer and to scale the signal at the input of $\Sigma\Delta_1$. Integrators should have at least 40 dB gain and $2\pi F_s$ gain-bandwidth

product. Integrator capacitors are tuned to stay in a maximum of ±10% RC time constant variations. Classical ELD compensation of up to 0.5 T_s is implemented in each modulator. Both modulators will have filtering STFs and we will need to use NCFs to compensate for non unitary STF in the secondary modulator. DACs will have NRZ topology. Because the combination of ISI and DWA highly degrades SNR performance, we decided not to implement DWA. Mismatch will be taken care in the design by using large size components.

Chapter IV

MSNBC Transistor Level Design And Measurements

In Chapter III, we defined some system level parameters of the MSNBC. We saw as instance that our $\Sigma\Delta$ modulator will be implemented in continuous time with a CIFB form. Modulators will be made of RC integrators where amplifiers should have at least 40 dB DC gain and a Gain-bandwidth product at least equal to $4F_s$ in order to meet our performance requirements. Table IV.1 gathers key parameters of our modulators.

Parameter	$\Sigma\Delta_0$ modulator	$\Sigma\Delta_1$ modulator
OSR	16	32
Modulator order	2	4
Architecture	CIFB	
DAC pulse	Non-Return to Zero	
Quantizer	4 bits	

Table IV.1: CIFB parameters

The goal of this chapter is to go one level down in the design process and justify our transistor level design and layout choices, and present simulations and measurement results.

IV.1 Transistor Level Design

The 65nm CMOS bulk process of ST microelectronics is used to implement the MSNBC. This single poly process uses a type P substrate and offers several front-end options such as low threshold voltage transistors, MIM capacitors, high-sheet

resistors or deep N-well that are all free of charge through MPW runs. Deep N-well is extensively used in this design as it allows isolating the P-WELL of NMOS transistors from the substrate, which enables connecting the source terminal to the substrate of NMOS transistors to reduce modulation of the threshold voltage by the substrate noise. As PMOS transistors are realized within an N-well, they are inherently isolated from the substrate.

Modulators analog blocks are implemented with fully differential circuits to minimize the common mode noise and reduce even-order harmonic distortion. To save power consumption, analog circuits are powered with 1.2 V supply, whereas digital cells used 1 V supply voltage.

The mapping of modulators coefficients into resistors and capacitors value is now studied. In order to obtain this number, the thermal noise budget should be estimated.

$$SNR_{dB} = P_{signal_dB} - P_{noise_dB}$$

If $P_{signal_princ_dB}$ =-6 dB and $ACPR$ =50 dB. Then $P_{signal_adj_dB}$ =-56 dB. The target SNR of the primary modulator is :

$$SNR_{CIFB_2}{}^{1} = 60\,dB$$

The total power of noise is then:

$$P_{noise_CIFB_2} = -66\,dB$$

Which corresponds to:

$$P_{noise_CIFB_2} = 251.2\,nV^2$$

We then consider that thermal noise contribution is half the total noise. Thus,

$$P_{Thermal_noise_CIFB_2} = 125\,nV^2$$

Same calculations are done with the secondary modulator.

$$SNR_{CIFB_4} = 20\,dB$$

Assuming a perfect cancellation of the main signal at the input of the secondary modulator, the total noise power is:

$$P_{noise_CIFB_4} = -76\,dB$$

[1] Given that the primary modulator is a second order CIFB modulator, we call it CIFB2

$$P_{noise_CIFB_4} = 25.1\,nV^2$$

Again, we consider that thermal noise contributes to half the total noise. Then,

$$P_{Thermal_noise_CIFB_4} = 12.5\,nV^2 \tag{IV.1}$$

The thermal noise from the second modulator comes from the first operational amplifier, the first DAC and resistors R_1 and R_{g1}. Those resistors represent the input coefficients b_1 and g_1 of a CIFB modulator, as presented in Figure IV.1.

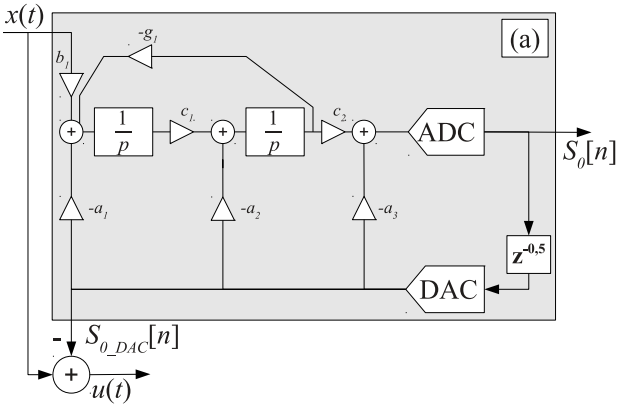


Figure IV.1: CIFB schematic

This is approximated with the following equation:

$$P_{thermal_noise} = BW(8KTR_{g1} + 8KTR_1 + \frac{8KT\gamma}{gm_{op}} + 16KT\gamma R_1\frac{V_{ref}}{V_{gtDAC}}) \tag{IV.2}$$

What we want is to meet the following requirement:

$$P_{thermal_noise} \leq 12.5\,nV^2$$

After simplification, we have:

$$R_{g1} + R_1 + \frac{\gamma}{gm_{op}} + \frac{2\gamma R_1 V_{ref}}{V_{gtDAC}} \leq 18.3K\Omega \tag{IV.3}$$

where BW is the signal bandwidth, K is Boltzman's constant, T is the absolute temperature, γ is the transistor thermal noise constant, gm_{op} is the transconductance of the input transistor of opamp1, V_{gtDAC} is the overdrive voltage of the first DAC and V_{ref} is the reference voltage of the quantizer.

Modulators coefficients are obtained with the relationship:

$$a_i = \frac{1}{R_i C_i F s} \tag{IV.4}$$

Thus, R_1 and R_{g1} expressions can be replaced in

$$\frac{1}{c_1 b_1 C_1 F s} + \frac{c_2}{c_1 g_1 C_1 F s} + \frac{\gamma}{g m_{op}} + \frac{2\gamma R_1 V_{ref}}{V_{gtDAC}} \leq 18.3 K\Omega$$

We obtain equations giving the maximum values of the first resistor and capacitor of the second modulator. However, as the noise requirement is more stringent for the secondary modulator, these are chosen as maximum values of input resistor and capacitor of both modulators of the MSNBC. We assume that,

- OTA $GBW = 4F_s$
- $DC_{gain} = 45\,dB$

and

$$GBW = \frac{g m_{op}}{2\pi C_1} \tag{IV.5}$$

We thus obtain:

$$\frac{1}{C_1 F s}\left(\frac{1}{c_1 b_1} + \frac{c_2}{c_1 g_1} + \frac{\gamma}{8\pi} + \frac{2\gamma V_{ref}}{c_1 b_1 V_{gtDAC}}\right) \leq Rmax \tag{IV.6}$$

$$\frac{1}{Rmax F s}\left(\frac{1}{c_1 b_1} + \frac{c_2}{c_1 g_1} + \frac{\gamma}{8\pi} + \frac{2\gamma V_{ref}}{c_1 b_1 V_{gtDAC}}\right) \leq C_1 \tag{IV.7}$$

The final MSNBC modulator consists of a second order CIFB modulator which is the primary modulator, a fourth order CIFB modulator as a secondary and biasing circuits to generate voltage and current references. Main sub-blocks of CIFB modulators are detailed below.

IV.1.1 Sub-blocks Design

Some existing blocks available in our research team were re-used and adapted for our proposed ADC. Thus, the design of this MSNBC is not optimized for a power consumption point of view as the first target is to have a silicon proof of concept.

Loop filter

The loop filters of each CIFB2 and CIFB4 are made of integrators are built around Operational Transconductance Amplifier (OTA)-RC rather than Gm-C cells, because they have higher linearity performance and better robustness over PVT variations. Furthermore, the virtual ground of the integrator provides a low impedance node that facilitates the connection of a current-steering DAC. Feed-in and feedback coefficients are implemented with resistance ratio. Passives that implement feed-in and feedforward coefficients are sized to meet the matching requirement of 1 %. The noise floor of the modulator is dominated by the thermal noise and the flicker noise of the front-end that is composed of the input resistors, OTA21 and the unitary current cells of the main DAC.

Thermal noise is set by the resistor value and a scaling factor whose value depends on the ratio of the reference voltage of the quantizer to the overdrive voltage of the current cells in the main DAC. In this design, the overdrive voltage of the current cells is set to 1/4 of the supply voltage to optimize noise and matching performance.

The finite GBW induced voltage swing at the virtual ground of the first OTA21 is the main source of distortion in the front end. Lowering the GBW increases the voltage swing at the virtual ground of OTA21. Moreover, even if the finite-GBW-induced phase shift through the loop filter is rigorously compensated by tuning components values, the robustness of the modulator stability against PVT variations cannot be guaranteed with a high yield.

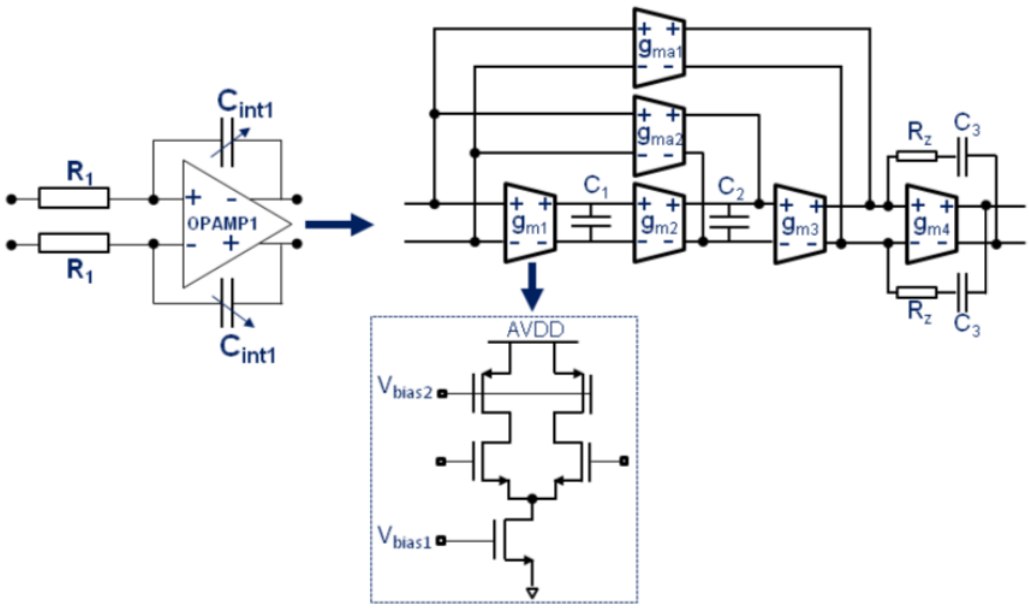


Figure IV.2: OTA schematic [94]

As shown in Figure IV.2, the main integrator embeds a 4-stage amplifier that achieves a GBW and a phase margin of 3.9 GHz and 88 ° respectively which ensures low-distortion and low phase-shift against PVT variations. Each transconductance stage has its own common-mode feedback circuit that ensures an optimal operating point for the differential path. The power consumption of the common-mode feedback circuits represent one-third of whole amplifier power budget. The last stage (gm4) uses minimum length devices to increase the phase margin while consuming low power. The OTA21 consumes 20 mA. OTA21 performance is summarized in Table IV.2.

Parameter	Value	Unit
DC Gain	45	dB
Open-loop GBW	2.56	GHz
Load capacitor	1508	fF
Phase margin	90	°
Input referred noise density		
@10 KHz	10	$nV/\sqrt{Hz}$
@10 MHz	3.2	$nV/\sqrt{Hz}$
Offset (3σ)	± 2	mV
Supply	1.2	V
Power consumption	24	mW

Table IV.2: First integrator parameters

RC calibration is used to compensate for the shifting of the RC time-constant that can vary by more than ± 35 % in this process. The feedback capacitor of each integrator are tuned to the ideal value with different accuracies.

In order to save design and layout time, OTA22, OTA41, OTA42, OTA43 and OTA44 are similar to OTA21. DC gain are mostly the same for all those integrators. However, given that the capacitive load varies, the unity gain bandwidth and phase margin are not the same for all integrators. Table IV.3 gathers the MSNBC component values.

R resistors are the one used to implement b_i and c_i coefficients of $\Sigma\Delta$ modulators. Rg allows to create NTF notches in the secondary modulator. However, they increase thermal noise when used at the input of the modulator. We decided not to have a notch in the primary modulator in order to meet our thermal noise requirement. As first integrators are critical, higher precision are used for their time constant calibration compared to other integrators.

	$\Sigma\Delta_0$		$\Sigma\Delta_1$			
Position	1	2	1	2	3	4
Rg (Ω)	-	-	21017	52552		
R (Ω)	2000	2109	2000	5937	2723.5	2723
Cap int (fF)	1508	477.5	2009.6	499.1	532.5	500.4
Cap fix (fF)	980.2	310.375	1306.2	324.4	346.1	325.3
Cap unit (fF)	16.7/22.1	22.2/22.1	22.3/22.1	23.3/22.1	24.8/22.1	23.3/22.1
Precision	6 bits	4 bits	6 bits	4 bits	4 bits	4 bits

Table IV.3: Component values

Quantizer

The quantizer is a 4-bit flash ADC. It consists of 15 comparators which convert the output of the loop filter into a thermometric code plus two comparators to detect saturation. A voltage buffer provides a copy of a voltage reference to a resistive ladder which generates the threshold voltages $V_{REF}[i]$ for the comparators. The schematic of one comparator slice is detailed in Figure IV.3

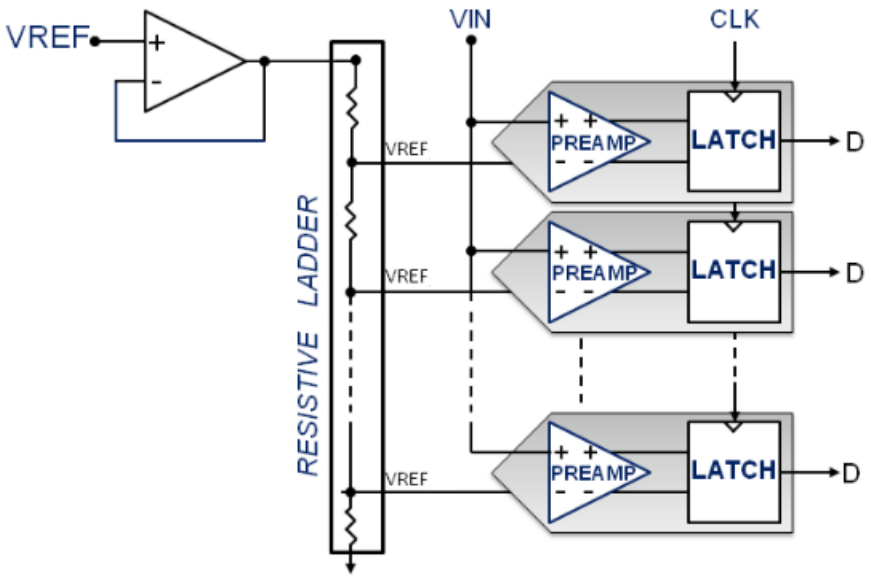


Figure IV.3: Comparator schematic [94]

A front-end CMOS switch disconnects each comparator from the loop filter during the offset calibration procedure that is done after the power-up of the ADC IC. In normal mode (calibration off) the on-state resistance of the switch, together with the input capacitance of the quantizer create a pole whose value is set well beyond

the sampling frequency of the modulator in order to preserve its stability. The noise and distortion requirement of the switch are greatly relaxed as they are shaped by the 5th-order loop filter preceding the quantizer. For each comparator, the offset value is estimated by a feedback loop which consists of a counter/integrator and a current-steering DAC. For each DAC code, the output of the comparator is integrated over several fractions of the clock period to reduce the influence of noise. When the mean value of the comparator output is equal to or greater than zero, then the counter stops and leaves the output current of the DAC at a value that compensates the offset voltage. After calibration, the residual offset is bounded within one DAC's LSB.

The preamplifier is a double-differential amplifier with a PMOS load and a resetting switch for faster overload recovery. It uses a non-switching load, which strongly minimizes the kickback noise on the loop filter output and the reference ladder.

Parameter	Value	Unit
Sampling Frequency	640	MHz
Full scale	0.8	V
Resolution	4	bits
Offset (3σ)		
Before calibration	80	mV
After calibration	≤ 5	mV
Supply		
Analog	1.2	V
Digital	1	V
Power consumption		
Analog	1.8	mW
Digital	2.3	mW

Table IV.4: Quantizer parameters

Design parameters of quantizers are gathered in Table IV.4.

DACs

Multi-bit feedback DACs are not inherently linear and generate errors due to the mismatch between the unit-DAC elements. As the feedback DACs are placed after the quantizer in a CT $\Sigma\Delta$ modulator, the non-linearity coming from the DACs is not shaped by the loop filter. Hence, it is directly reinserted in the main modulator path, increasing the in-band noise-floor and reducing the SNR.

The current steering architecture is widely used for high-speed DAC applications.

The main advantages of this architecture are the power efficient, an easy implementation (which requires only digital CMOS processes), a guaranteed monotonicity, a good matching, and the glitches that do not contribute to nonlinearity (when using thermometer coding). To minimize performance degradation, as presented in Chapter 2, feedback DAC element mismatch should at least be 2 %. The matching between each one of these current sources is primordial to assure good performance of the continuous-time ΣΔ modulator.

Pelgrom states mismatch as a "process that causes time-independent random variations in physical quantities of identically designed devices" [95]. For current-steering DAC applications, this denotes that each current source in the array produces a current that deviates slightly from the desired current, I_{ref} . Hence, to reach the required specifications, the current sources should be designed in such a way that random variations do not affect the performance of the current-steering DAC. From Pelgrom's matching estimation [95], it is possible to determine the minimum gate-area for the unit current source. For a (σI/I) of 2 %, the obtained (WL)min is about 6 μm^2.

The architecture of one of the 15 unit current cells of DAC21 is shown in Figure IV.4. It consists of a regulated cascode current source with a pair of NMOS. The boosting amplifier is a single-stage common-source amplifier whose GBW is optimized to boost the output impedance of the DAC over a wide frequency range.

The switches are sized small to minimize the delay and the output capacitance of the current cell. The gates of switches are driven by high-crossing point buffers that ensure that one transistor is always in the on-state and biased in saturation, allowing a double cascode configuration which further improves the output resistance of the DAC. A careful design of the clock distribution circuit and true single-phase clock (TSPC) flip-flops (FF) that drive DAC switches has led to an additive jitter value of only 137 fs rms. This value leaves enough margin for the jitter of the clock-source. The current cell drivers are implemented with only two PMOS transistors rather than four which reduce the propagation delay between the FF and the DAC output.

An impedance value higher than 400 MΩ is obtained up to the band edge (40 MHz) which makes the distortion mechanism due to finite GBW of opamp1 negligible within the signal bandwidth. Table IV.5 presents the parameters values used in this design.

The value of DACs currents reference are gathered in Table IV.6. DAC current cells are extracted using the following relationship for an RC-integrator:

$$a_i V_{REF} = \frac{I_{DAC} \times T_s}{C} \tag{IV.8}$$

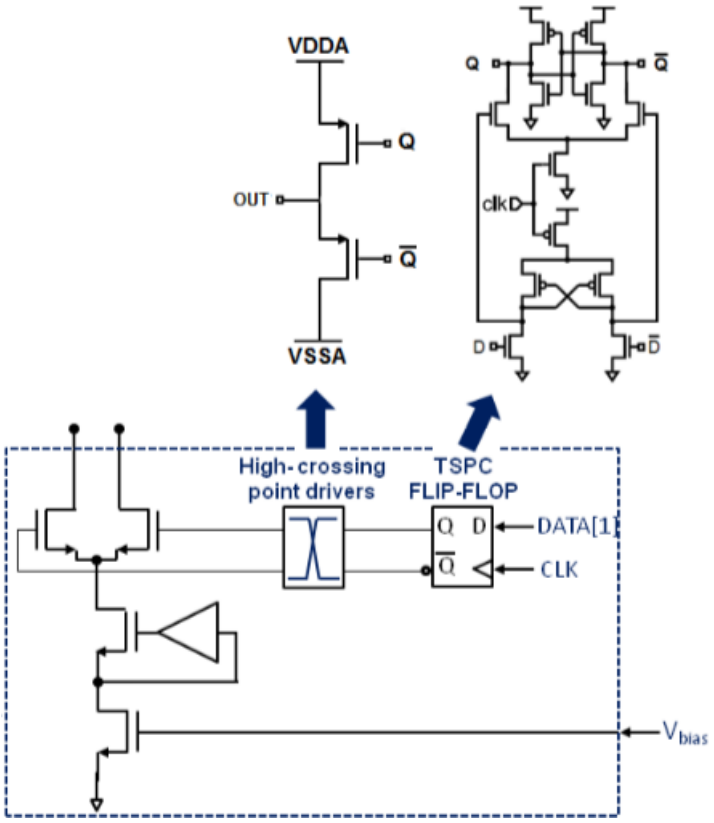


Figure IV.4: DAC unit current cell schematic [94]

Parameter	Value	Unit
Cell current	25	μA
Number of cells	15	V
Matching	2	%
Supply		
Analog	1.2	V
Digital	1	V
Power consumption		
Analog	0.18	mW
Digital	0.5	mW

Table IV.5: DAC parameters

with a_i the DAC feedback coefficient, T_s the sampling period, V_{REF} the reference voltage and C the capacitor. Except from DAC45, all DACs have the same architecture as DAC21. Given that the reference current changed, the ratio of the area is adjusted to meet the mismatch constraint previously obtained.

	$\Sigma\Delta_0$			$\Sigma\Delta_1$				
Position	1	2	3	1	2	3	4	5
Iref (μA)	25	49.99	23.45	10/3	10/3	10	40	18.71

Table IV.6: DAC parameters

Floorplan

To achieve a good resolution and linearity of the MSNBC, a great deal of caution should be taken in the layout design to reduce the effects of parasitics, mismatch and noise coupling from digital blocks to analog blocks.

The layout and chip micrograph of the MSNBC modulator are presented in Figure IV.5, which labels some major blocks.

The analog and digital blocks are separated to avoid disturbances. Main input pins are located at the left of chip, whereas output pins as well as output buffers are located at the right of the chip. Biasing voltages and currents are placed at the center of the chip, closed to integrators. DACs from the CIFB2 are located at the top of the chip, close to INT21 and 22. DACs 41, 42, 43, 44 and 45 are placed at the bottom of the circuit, close to CIFB4 integrators. DAC40 is placed close to DAC21 and INT21 to generate the shaped quantization noise and to avoid the impact of parasitics resistor in the RSTF. Given that quantizers of both modulators have the same reference voltage and the same resolution, they shared the same resistor ladder to save area.

The MSNBC prototype was fabricated in 65nm 1P7M CMOS process through the Multi Project Wafer program of the CMP. The active die area is 3.25mm^2 (1.804 mm x 1.804 mm). Digital blocks were isolated in a deep N-well to reduce the coupling with the analog blocks through the substrate.

The power supplies are routed in several metal layers to reduce the power lines equivalent resistance and consequently the voltage loss. To improve the isolation between analog and digital blocks, some design techniques such as shielding and guard ring were used. Also, the power supply lines of analog and digital blocks are physically separated. The circuit also includes a Serial-to-Parellel Interface (SPI) to generate static signals to control capacitors, calibration and to switch between the 2-4 and the 0-4 MSNBC modes.

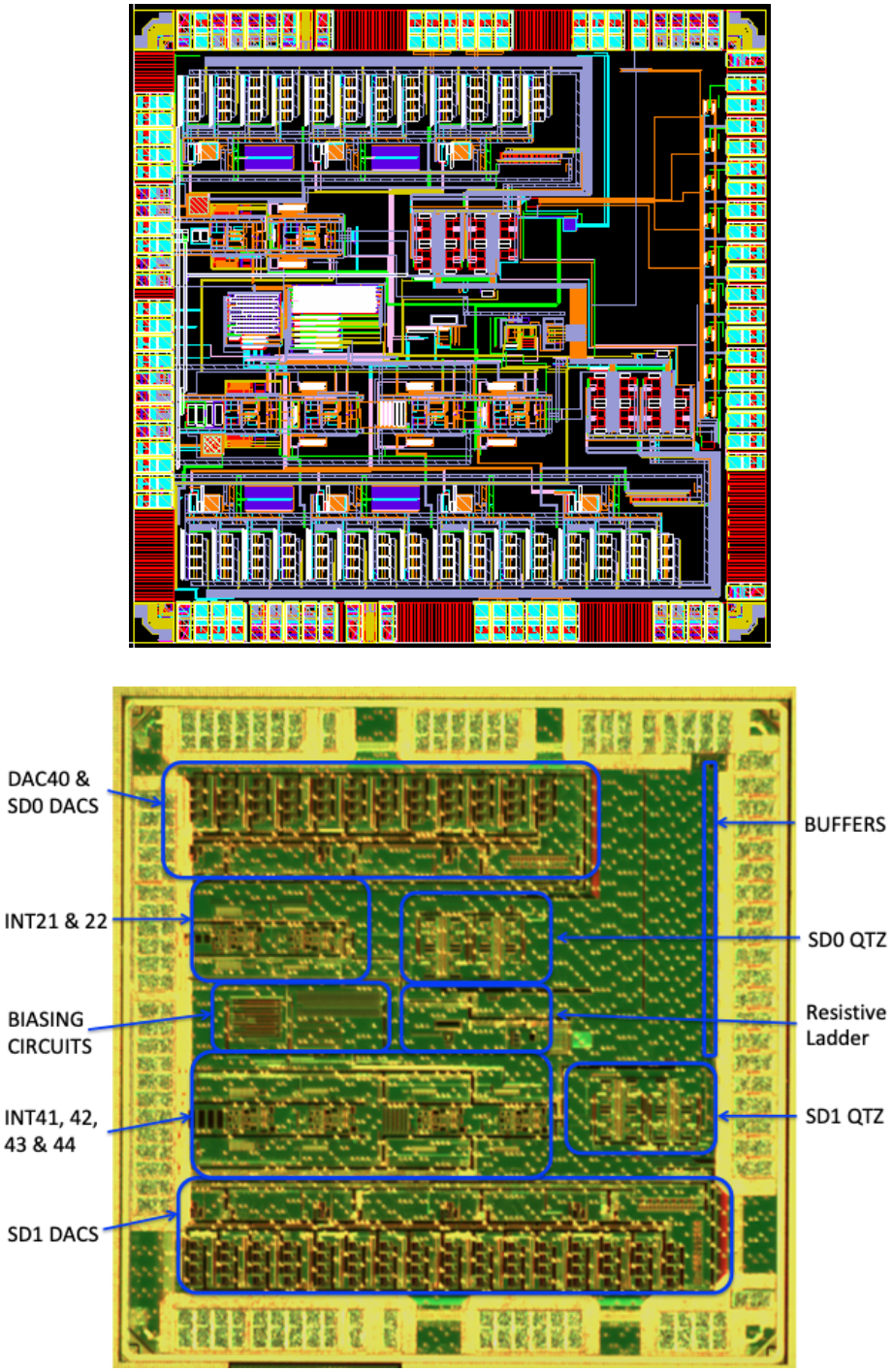


Figure IV.5: MSNBC Layout floor plan and die picture

IV.1.2 Simulation Results

Simulations of the MSNBC at the transistor level are performed in Cadence. The testbench consists of the 2-4 / 0-4 MSNBC circuits and output buffers.

The sum of two sine waves are used to represent the test signal: one at $Fin_1 =$

1.9 MHz with 0.67 V amplitude to represent the main signal, and a second sine wave at $Fin_2 = 20$ MHz to model the non-linearities at the output of the PA. The non-linearities amplitude are set to illustrate a system with 50 dBc ACPR. Thus the amplitude of those non-linearities are set to 3.1 mV. The sampling frequency is $Fs = 640$ MHz. Signal is assumed to be a 20 MHz LTE signal. Thus, $\Sigma\Delta_0$ linearizes 10 MHz bandwidth and $\Sigma\Delta_1$ 20 MHz. Each modulator implements a digital differentiator technique to compensate for ELD up to $0.5 \times T_s$. The reference voltage of the quantizer is 0.8 V, and both primary and secondary modulators have filtering STFs.

The primary and secondary modulators are first tested standalone by simulation to check their functionality. The same signal is applied at the input of both modulators. No scaling is performed at the input of the adjacent modulator. Results in Figure IV.6, show the output spectra of both modulators. Both results have non linearities that degrades their performance compare to high level simulations and DAC mismatch is not added in this simulation.

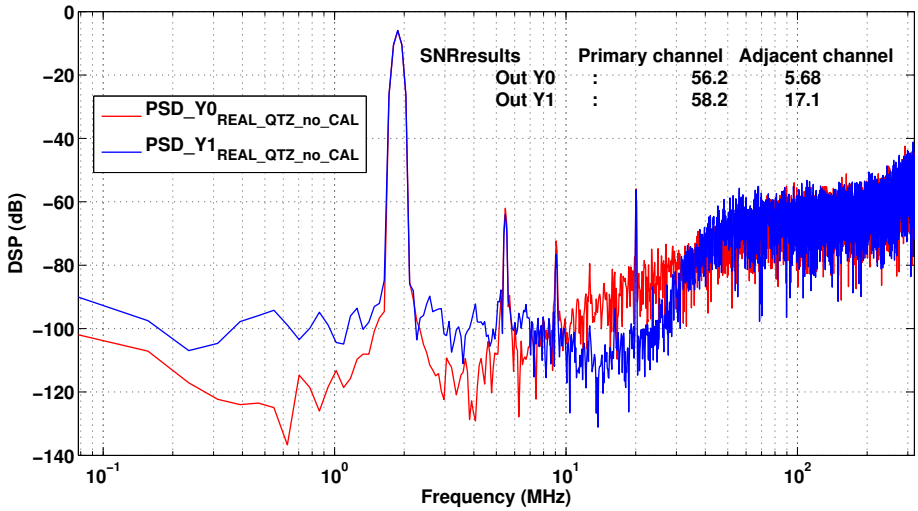


Figure IV.6: $CIFB_2$ and $CIFB_4$ results

The test signal is then applied to the MSNBC modulator. The output spectra of the ADC are presented in Figure IV.7. The black, green, blue and red curves respectively represent the output of the first modulator, the output of the second modulator the reconstructed signal without and with the NCFs. The output of the first modulator exhibits high odd orders non linearities. This is because the OTA used in the loop filter operates close to saturation. Because the input frequency of the signal is low, those non-linearities are in the band of interest. Thus, the SNR is 55 dB in the main channel and 6.3 dB in the adjacent channel.

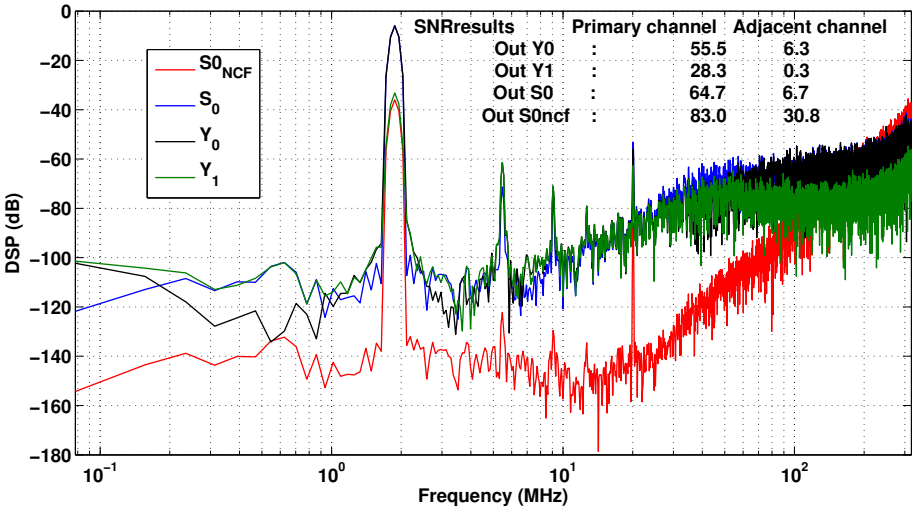


Figure IV.7: MSNBC performance results

The shaped quantization noise is thus scaled and applied to the second modulator. The SNR in the adjacent channel of $\Sigma\Delta_1$ is then 0.3 dB. Y_1 is scaled down to remove the scaling initially done at the input of the secondary modulator. After summing Y_0 and Y_1, performance is improved by 9 dB in the main band. The main channel has 64 dB SNR and the first subband 6.7 dB. We can then relax the design of the first modulator as non-linearities of the first modulator are compensated when using NCFs.

The 0-4 MSNBC was also simulated and transistor level simulation results are presented in Figure IV.8. We experienced a DC offset issue for this simulation which is under investigation. This might be caused by the fact that the signal is not attenuated by the same factor for a 0-order and a 2^{nd}-order modulator. Thus, the scaling and parameters used for a 2-4 MSNBC should not be the same as the one used for a 0-4 MSNBC.

Noise cancellation filters are applied in Matlab to the output signals of the MSNBC to generate the reconstructed the signal. When NCFs are used the cancellation of the shaped quantization noise is more effective in the reconstructed signal. The modulator achieves 83 dB SQNR in the main bandwidth and 30.8 dB in the first adjacent channel of S_1. The NCFs compensate for some non-linearity in the main channel of Y_0.

The NCFs used in this case do not take into account the excess loop delay. This demonstrates the robustness of our system. Figure IV.9 shows spectra before and after using noise cancellation filters.

For those simulations, the amplitude of input signal is decreased compared to

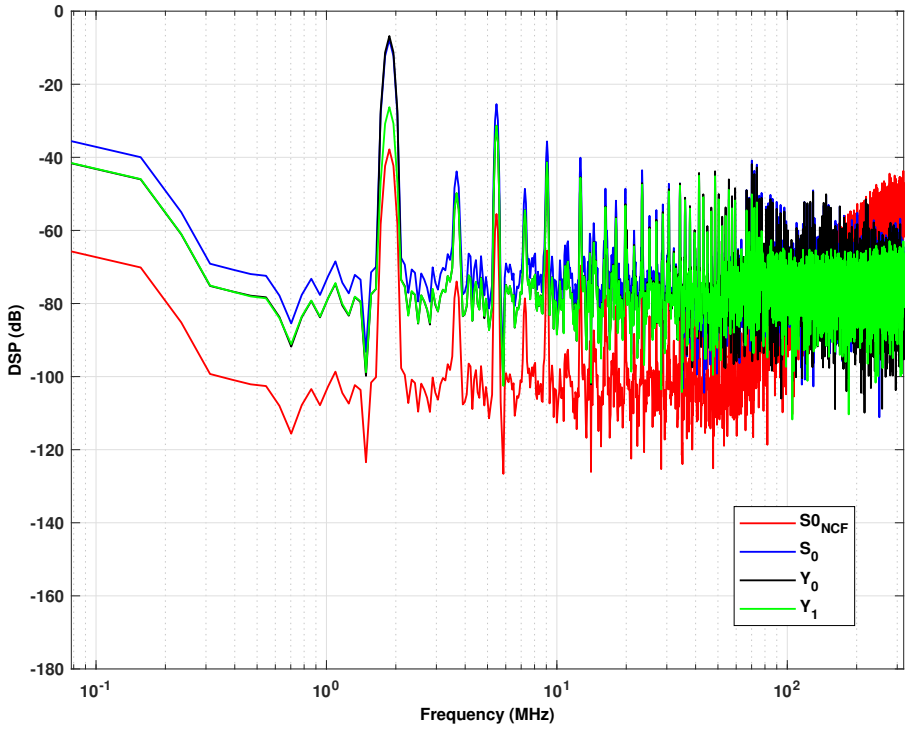


Figure IV.8: 0-4 MSNBC transistor level simulation results

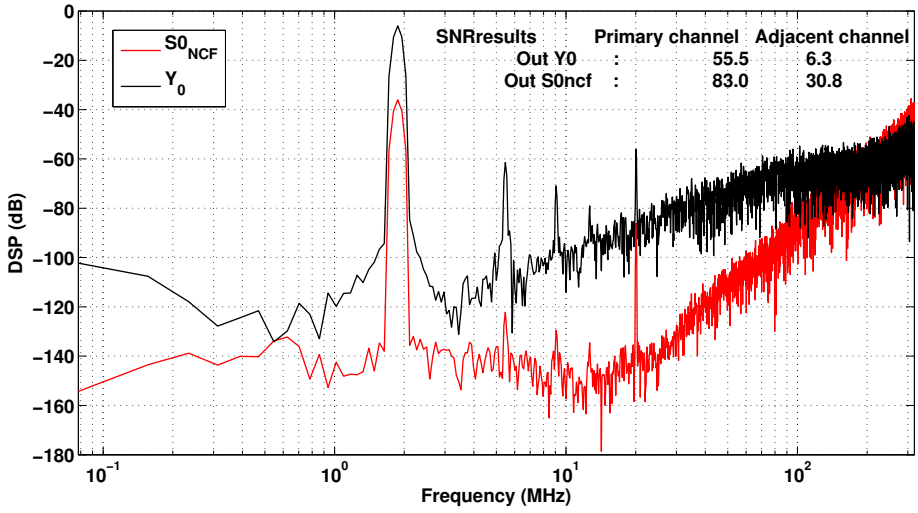


Figure IV.9: MSNBC spectra before and after using NCFs

the previous set of parameters. The purpose is to decrease the impact of OTAs non linearities. The process is changed but the temperature is the same. Simulation results are presented in Figure IV.10.

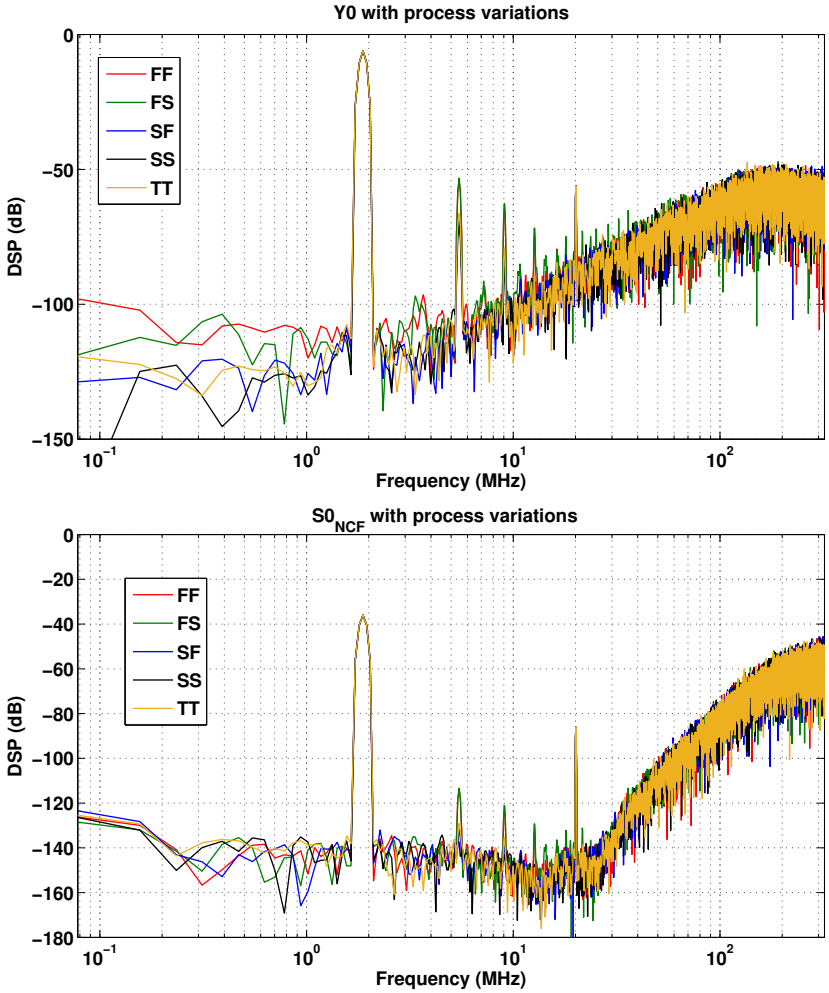


Figure IV.10: Output spectra of the 2-4 MSNBC at different process nodes

Decreasing the input amplitude improved the SNR performance in the main band of Y_0. Furthermore, the reconstructed signal also have better performance as the NCFs calculation takes into account ELD. Performance are showed in Table Table IV.7.

	FF	FS	SF	SS	TT
SNR Y_{0_princ} (dB)	47.4	46.7	61.5	64.8	60.1
SNR Y_{0_adj} (dB)	6.49	4.64	8.88	9.45	8.91
SNR $S_{0_NCF_princ}$ (dB)	76.6	76.4	85.1	86.2	85.3
SNR $S_{0_NCF_adj}$ (dB)	35.5	33.1	35.2	35.4	36.4

Table IV.7: Impact of process variation on the MSNBC

For the typical process, the reconstructed signal achieves 85.5 dB SQNR in the main bandwidth and 36.4 dB in the first subband. This performance is degraded

when NMOS transistors are in the Fast corner. The SNR in the main channel of S_0 drops by 9 dB. In the adjacent channel however, performance is almost unchanged across corners.

The designed MSNBC ADC performance thus meet initial specifications at the transistor level simulations. Those simulation results are then compared to measurement results of the chip.

IV.2 MSNBC Measurements

- Measurements results, test bench, power consumption
- Compare simulations and measurements
- Explain results

Conclusion

Digital predistortion is nowadays a common technique to cope with the linearity-efficiency trade-off of power amplifiers in base transceiver stations. This technique is highly preferred because of its efficiency, but also it takes advantage of the advance in digital signal processing. As the demand in bandwidth is always growing, the ADC in the feedback path becomes a bottleneck of DPD implementation. For a 100 MHz signal for example, the ADC should digitize up to 700 MHz to include PA non-linearities. Pipeline ADCs are commonly used for this application, but they tend to consume a lot of power. Subband DPD is a new technique to relax the feedback ADC design. The multi stage noise band cancellation architecture made of $\Sigma\Delta$ modulators is an excellent candidate to address the wide bandwidth high resolution and low power consumption trade-off of this application. The MSNBC architecture is particularly attractive as it relaxes dynamic range constraints per band.

A continuous time implementation of the MSNBC modulator is preferred to a discrete time implementation because of the high speed requirement. This is at the price of several considerations that need to be tackled before the design. A study of the MSNBC non-idealities leads to two possible implementations: a zero IF implementation, where the first modulator is a low pass type and its bandwidth constraint is halved, and a low IF implementation with a bandpass modulator as primary modulator. System level simulations results lead us to design an MSNBC made of two modulators:

- A second order CIFB modulator with 4-bit quantizer
- A fourth order CIFB modulator with 4-bit quantizer

Non-idealities related to continuous time $\Sigma\Delta$ modulators as well as imperfections specific to the MSNBC architecture were investigated. In order to test several configurations, the circuit is made reconfigurable. It can be setup to implement the initial 2-4 MSNBC but it can also implement a 0-4 MSNBC. The 0-4 topology is expected to consume less power and to require a smaller area but will require highly

accurate decimation filters, compared to a 2-4 MSNBC. Moreover, the fact that non-linearities of the primary modulator are compensated in the main bandwidth channel allows to relax design constraints in the primary modulator.

The purpose of this thesis is to demonstrate the feasibility of the MSNBC architecture that has so far only been studied at the system level. In order to save design time, some previously designed blocks have been re-used and adapted to our specifications. As a proof of concept, an MSNBC with two modulators was designed in a 65 nm CMOS technology. Transistor level simulations of the MSNBC show the signal attenuation at the input of the second modulator is effective but lower compared to systems level simulations. We obtained more than 20 dB attenuation of the main signal at the transistor level. Furthermore, the SNR in the adjacent channel has been improved by 24 dB, which means that the shaped quantization noise of the primary modulator has been cancelled in the adjacent channel. Results also proved that using the accurate NCFs leads to better SNR in the adjacent channel. Finally, simulations over process variations shows that performance in the subband are more robust compared to performance in the main channel.

Future work

This thesis, presents a proof of concept of this new type of converter. The logical steps that would follow this work should focus on an optimized implementation of the modulator in order to prove the saving in power consumption compared to ADC with same specifications and to make a final choice on the 2-4 and 0-4 architectures. The design of OTA should also be improved because non linearities of the OTAs degrades our performance in the main channel. The additional step forward is the design of decimation filter in order to have the overall ADC power consumption.

The current MSNBC is designed with two modulators. An area of improvement is to have a reconfigurable architecture of the MSNBC which will be made of adjacent modulators. Those adjacent modulators could be switched on and off depending on the highest non linearity order needed to characterize the power amplifier in DPD.

Finally, reconfigurability of the MSNBC can furthermore be achieved with modulators with variable center frequencies. The proposed future works should also take advantage of scaling technology nodes and be implemented in lowest technology nodes like 28nm FDSOI.

Bibliography

[1] Vincenzo Mancuso and Sara Alouf. Reducing costs and pollution in cellular networks. *IEEE Communications Magazine*, 49(8):63–71, 2011.

[2] Sesia Stefania, Toufik Issam, and Baker Matthew. LTE, the UMTS long term evolution: from theory to practice. *A John Wiley and Sons, Ltd*, 6:136–144, 2009.

[3] Guangyi Liu and Dajie Jiang. 5G: Vision and requirements for mobile communication system towards year 2020. *Chinese Journal of Engineering*, 2016, 2016.

[4] Angelos Chatzipapas, Sara Alouf, and Vincenzo Mancuso. On the minimization of power consumption in base stations using on/off power amplifiers. In *2011 IEEE Online Conference on Green Communications*, pages 18–23. IEEE, 2011.

[5] Minoru Etoh, Tomoyuki Ohya, and Yuji Nakayama. Energy consumption issues on mobile network systems. In *2008 International Symposium on Applications and the Internet*, pages 365–368. IEEE, 2008.

[6] Lei Guan and Anding Zhu. Green communications: Digital predistortion for wideband RF power amplifiers. *IEEE Microwave Magazine*, 15(7):84–99, 2014.

[7] D. Y. C. Lie, J. C. Mayeda, and J. Lopez. Highly efficient 5G linear power amplifiers (PA) design challenges. In *2017 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, pages 1–3, April 2017.

[8] Luis M Correia, Dietrich Zeller, Oliver Blume, Dieter Ferling, Ylva Jading, István Gódor, Gunther Auer, and Liesbet Van Der Perre. Challenges and enabling technologies for energy aware mobile radio networks. *IEEE Communications Magazine*, 48(11), 2010.

[9] George Koutitas and Panagiotis Demestichas. A review of energy efficiency in telecommunication networks. *Telfor journal*, 2(1):2–7, 2010.

[10] Bumman Kim, Jinsung Choi, Daehyun Kang, and Dongsu Kim. Envelope tracking technique for multimode PA operation. In *2009 European Microwave Conference (EuMC)*, pages 429–432. IEEE, 2009.

[11] Murat Eron, Bumman Kim, Frederick Raab, Robert Caverly, and Joseph Staudinger. The head of the class. *IEEE Microwave Magazine*, 12(7):S16–S33, 2011.

[12] Steve C Cripps. *RF Power Amplifiers for Wireless Communications, (Artech House Microwave Library (Hardcover))*. Artech House, Inc., 2006.

[13] Leonard R Kahn. Single-sideband transmission by envelope elimination and restoration. *Proceedings of the IRE*, 40(7):803–806, 1952.

[14] Zhancang Wang. *Envelope tracking power amplifiers for wireless communications*. Artech House, 2014.

[15] Peter Asbeck and Zoya Popovic. ET comes of age: Envelope tracking for higher-efficiency power amplifiers. *IEEE Microwave Magazine*, 17(3):16–25, 2016.

[16] Bumman Kim. Advanced linear PA architectures for handset applications. In *Wireless Symposium (IWS), 2013 IEEE International*, pages 1–1. IEEE, 2013.

[17] Kim Bumman, Moon Junghwan, and Kim Ildu. Efficiently amplified. *IEEE Microwave Magazine*, 11(5):87–100, 2010.

[18] Zhancang Wang. Demystifying envelope tracking: Use for high-efficiency power amplifiers for 4G and beyond. *IEEE microwave magazine*, 16(3):106–129, 2015.

[19] H Tango, T Hashinaga, K Totani, H Kuriyama, Y Hamada, and T Asaina. A 60% efficient envelope tracking power amplifier for 40W, 2.6 GHz LTE base station with in/output harmonic tuning. In *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, pages 1–4. IEEE, 2013.

[20] Youjiang Liu, Chan-Sei Yoo, John Fairbanks, Jonmei Yan, Donald Kimball, and Peter Asbeck. A 53% PAE envelope tracking GaN power amplifier for 20MHz bandwidth LTE signals at 880MHz. In *Power Amplifiers for Wireless and Radio Applications (PAWR), 2016 IEEE Topical Conference on*, pages 30–32. IEEE, 2016.

[21] Paul T Theilmann, Jonmei J Yan, Cuong Vu, Jeong-Sun Moon, Harris P Moyer, and Donald F Kimball. A 60MHz bandwidth high efficiency X-band envelope

tracking power amplifier. In *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2013 IEEE*, pages 1–4. IEEE, 2013.

[22] William H Doherty. A new high efficiency power amplifier for modulated waves. *Proceedings of the Institute of Radio Engineers*, 24(9):1163–1182, 1936.

[23] Raymond Pengelly, Christian Fager, and Mustafa Ozen. Doherty's legacy: a history of the Doherty power amplifier from 1936 to the present day. *IEEE Microwave Magazine*, 17(2):41–58, 2016.

[24] Frederick H Raab. Efficiency of Doherty RF power-amplifier systems. *IEEE transactions on Broadcasting*, pages 77–83, 1987.

[25] Masaya Iwamoto, Aracely Williams, Pin-Fan Chen, Andre G Metzger, Lawrence E Larson, and Peter M Asbeck. An extended Doherty amplifier with high efficiency over a wide power range. *IEEE Transactions on Microwave Theory and Techniques*, 49(12):2472–2479, 2001.

[26] Ildu Kim and Bumman Kim. A 2.655 GHz 3-stage Doherty power amplifier using envelope tracking technique. In *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, pages 1496–1499. IEEE, 2010.

[27] Mury Thian and Peter Gardner. Envelope-tracking-based Doherty power amplifier. *International Journal of Electronics*, 97(5):525–530, 2010.

[28] Chuanhui Ma, Wensheng Pan, Shihai Shao, Chaojin Qing, and Youxi Tang. A wideband Doherty power amplifier with 100 MHz instantaneous bandwidth for LTE-advanced applications. *IEEE Microwave and Wireless Components Letters*, 23(11):614–616, 2013.

[29] Khaled Bathich, Asdesach Z Markos, and Georg Boeck. A wideband GaN Doherty amplifier with 35% fractional bandwidth. In *Microwave Conference (EuMC), 2010 European*, pages 1006–1009. IEEE, 2010.

[30] AM Mahmoud Mohamed, Slim Boumaiza, and Raafat R Mansour. Reconfigurable Doherty power amplifier for multifrequency wireless radio systems. *IEEE Trans. Microw. Theory Techn*, 61(4):1588–1598, 2013.

[31] Xuan Anh Nghiem, Junqing Guan, Thomas Hone, and Renato Negra. Design of concurrent multiband Doherty power amplifiers for wireless applications. *IEEE transactions on Microwave Theory and Techniques*, 61(12):4559–4568, 2013.

[32] Andrei Grebennikov and Senad Bulja. High-efficiency Doherty power amplifiers: Historical aspect and modern trends. *Proceedings of the IEEE*, 100(12):3190–3219, 2012.

[33] Fadhel M Ghannouchi and Oualid Hammi. Behavioral modeling and predistortion. *IEEE Microwave Magazine*, 10(7):52–64, 2009.

[34] Yuelin Ma, Yasushi Yamao, Yoshihiko Akaiwa, and Koji Ishibashi. Wideband digital predistortion using spectral extrapolation of band-limited feedback signal. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(7):2088–2097, 2014.

[35] Haoyu Wang, Gang Li, Chongbin Zhou, Wei Tao, Falin Liu, and Anding Zhu. 1-bit observation for direct-learning-based digital predistortion of RF power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 65(7):2465–2475, 2017.

[36] Ying Liu, Xin Quan, Shihai Shao, and Youxi Tang. Digital predistortion architecture with reduced ADC dynamic range. *Electronics Letters*, 52(6):435–437, 2016.

[37] Chao Yu, Lei Guan, Erni Zhu, and Anding Zhu. Band-limited Volterra series-based digital predistortion for wideband RF power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 60(12):4198–4208, 2012.

[38] Lei Ding, Fernando Mujica, and Zigang Yang. Digital predistortion using direct learning with reduced bandwidth feedback. In *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, pages 1–3. IEEE, 2013.

[39] Oualid Hammi, Andrew Kwan, Souheil Bensmida, Kevin A Morris, and Fadhel M Ghannouchi. A digital predistortion system with extended correction bandwidth with application to LTE-A nonlinear power amplifiers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(12):3487–3495, 2014.

[40] M. Grimm, M. Allen, J. Marttila, M. Valkama, and R. Thoma. Joint Mitigation of Nonlinear RF and Baseband Distortions in Wideband Direct-Conversion Receivers. *IEEE Transactions on Microwave Theory and Techniques*, 62(1):166–182, Jan 2014.

[41] Lei Ding, G.T. Zhou, D.R. Morgan, Zhengxiang Ma, J.S. Kenney, Jaehyeong Kim, and C.R. Giardina. A robust digital baseband predistorter constructed

using memory polynomials. *IEEE Transactions on Communications*, 52(1):159–165, Jan 2004.

[42] 3GPP. *TS 36.104 - E-UTRA BS Radio Transmission and Reception.*

[43] S. Ho, Chi-Lun Lo, Jiayun Ru, and Jialin Zhao. A 23 mW, 73 dB Dynamic Range, 80 MHz BW Continuous-Time Delta-Sigma Modulator in 20 nm CMOS. *Solid-State Circuits, IEEE Journal of*, 50(4):908–919, April 2015.

[44] Robert H Walden. Analog-to-digital converter survey and analysis. *IEEE Journal on selected areas in communications*, 17(4):539–550, 1999.

[45] R. Schreier and R.C. Temes. Understanding Delta-Sigma Data Converters. In *Understanding Delta-Sigma Data Converters*, 2005.

[46] Michel Steyaert, Raf Roovers, and Jan Craninckx. A 100 MHz 8 bit CMOS interpolating A/D converter. In *Proceedings of IEEE Custom Integrated Circuits Conference-CICC'93*, pages 28–1. IEEE, 1993.

[47] Robert Taft, Chris Menkus, Maria Rosaria Tursi, Ols Hidri, and Valerie Pons. A 1.8 V 1.6 GS/s 8b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency. In *2004 IEEE International Solid-State Circuits Conference (IEEE Cat. No. 04CH37519)*, pages 252–526. IEEE, 2004.

[48] Brian P Ginsburg and Anantha P Chandrakasan. Dual time-interleaved successive approximation register ADCs for an ultra-wideband receiver. *IEEE Journal of Solid-State Circuits*, 42(2):247–257, 2007.

[49] Yun-Shiang Shu, Liang-Ting Kuo, and Tien-Yu Lo. An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS. *IEEE Journal of Solid-State Circuits*, 51(12):2928–2940, 2016.

[50] Dieter Draxelmayr. A 6b 600MHz 10mW ADC array in digital 90nm CMOS. In *2004 IEEE International Solid-State Circuits Conference (IEEE Cat. No. 04CH37519)*, pages 264–527. IEEE, 2004.

[51] Jian Lv, Longcheng Que, Linhai Wei, Zhijun Meng, and Yun Zhou. A low power and small area digital self-calibration technique for pipeline ADC. *AEU-International Journal of Electronics and Communications*, 83:52–57, 2018.

[52] Daihong Fu, Ken Dyer, S Lewis, and P Hurst. Digital background calibration of a 10 b 40 M sample/s parallel pipelined ADC. In *1998 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, ISSCC. First Edition (Cat. No. 98CH36156)*, pages 140–141. IEEE, 1998.

[53] Cormac SG Conroy, David W Cline, and Paul R Gray. An 8-b 85-MS/s parallel pipeline A/D converter in 1-μm CMOS. *IEEE Journal of Solid-State Circuits*, 28(4):447–454, 1993.

[54] Aria Eshraghi and Terri S Fiez. A comparative analysis of parallel delta-sigma ADC architectures. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 51(3):450–458, 2004.

[55] KC-H Chao, Shujaat Nadeem, Wai L Lee, and Charles G Sodini. A higher order topology for interpolative modulators for oversampling A/D converters. *IEEE Transactions on circuits and systems*, 37(3):309–318, 1990.

[56] James C Candy and Gabor C Temes. *Oversampling delta-sigma data converters: theory, design and simulation*. IEEE Press,, 1992.

[57] Richard Schreier. An empirical study of high-order single-bit delta-sigma modulators. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 40(8):461–466, 1993.

[58] L Risbo. Σ *Modulators-Stability and Design Optimization*. PhD thesis, PhD dissertation, Technical University of Denmark, 1994.

[59] Robert W Adams. Design and implementation of an audio 18-bit analog-to-digital converter using oversampling techniques. *Journal of the Audio Engineering Society*, 34(3):153–166, 1986.

[60] Max W Hauser. Circuits and technology considerations for MOS delta-sigma A/D converters. *IEEE Proc. ISCAS'86*, pages 1310–1315, 1986.

[61] Ian Galton. Why dynamic-element-matching DACs work. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 57(2):69–74, 2010.

[62] M. R. Miller and C. S. Petrie. A multibit sigma-delta ADC for multimode receivers. *IEEE Journal of Solid-State Circuits*, 38(3):475–482, March 2003.

[63] S. Lee and C. Cheng. A Low-Voltage and Low-Power Adaptive Switched-Current Sigma Delta ADC for Bio-Acquisition Microsystems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 53(12):2628–2636, Dec 2006.

[64] J. F. Jensen, G. Raghavan, A. E. Cosand, and R. H. Walden. A 3.2-GHz second-order delta-sigma modulator implemented in InP HBT technology. *IEEE Journal of Solid-State Circuits*, 30(10):1119–1127, Oct 1995.

[65] James A Cherry and W Martin Snelgrove. Excess loop delay in continuous-time delta-sigma modulators. *IEEE Transactions on Circuits and Systems II: analog and digital signal processing*, 46(4):376–389, 1999.

[66] A. Gharbiya and D. A. Johns. A 12-bit 3.125 MHz Bandwidth 0?3 MASH Delta-Sigma Modulator. *IEEE Journal of Solid-State Circuits*, 44(7):2010–2018, July 2009.

[67] V. Srinivasan, V. Wang, P. Satarzadeh, B. Haroun, and M. Corsi. A 20mW 61dB SNDR (60MHz BW) 1b 3rd-order continuous-time delta-sigma modulator clocked at 6GHz in 45nm CMOS. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pages 158–160, Feb 2012.

[68] J.G. Kauffman, Chao Chu, J. Becker, and M. Ortmanns. A 67dB DR 50MHz BW CT Delta Sigma modulator achieving 207 fJ/conv. In *Solid-State Circuits Conference (A-SSCC), 2013 IEEE Asian*, pages 401–404, Nov 2013.

[69] J.G. Kauffman, P. Witte, M. Lehmann, J. Becker, Y. Manoli, and M. Ortmanns. A 72 dB DR, CT $\Delta\Sigma$ Modulator Using Digitally Estimated, Auxiliary DAC Linearization Achieving 88 fJ/conv-step in a 25 MHz BW. *Solid-State Circuits, IEEE Journal of*, 49(2):392–404, Feb 2014.

[70] J. Harrison, M. Nesselroth, R. Mamuad, A. Behzad, A. Adams, and S. Avery. An LC bandpass $\Delta\Sigma$ ADC with 70dB SNDR over 20MHz bandwidth using CMOS DACs. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pages 146–148, Feb 2012.

[71] Hyungil Chae, Jaehun Jeong, G. Manganaro, and M.P. Flynn. A 12 mW Low Power Continuous-Time Bandpass $\Delta\Sigma$ Modulator With 58 dB SNDR and 24 MHz Bandwidth at 200 MHz IF. *Solid-State Circuits, IEEE Journal of*, 49(2):405–415, Feb 2014.

[72] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani. A 20-mW 640-MHz CMOS Continuous-Time $\Sigma\Delta$ ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB. *Solid-State Circuits, IEEE Journal of*, 41(12):2641–2649, Dec 2006.

[73] M. Bolatkale, L.J. Breems, R. Rutten, and K.A.A. Makinwa. A 4 GHz Continuous-Time $\Delta\Sigma$ ADC With 70 dB DR and - 74 dBFS THD in 125 MHz BW. *Solid-State Circuits, IEEE Journal of*, 46(12):2857–2868, Dec 2011.

[74] H. Shibata, R. Schreier, Wenhua Yang, A. Shaikh, D. Paterson, T.C. Caldwell, D. Alldred, and Ping Wing Lai. A DC-to-1 GHz Tunable RF $\Delta\Sigma$ ADC Achieving DR=74 dB and BW=150 MHz at f_0=450 MHz Using 550 mW. *Solid-State Circuits, IEEE Journal of*, 47(12):2888–2897, Dec 2012.

[75] Yunzhi Dong, W. Yang, R. Schreier, A. Sheikholeslami, and S. Korrapati. A Continuous-Time 0-3 MASH ADC Achieving 88 dB DR With 53 MHz BW in 28 nm CMOS. *Solid-State Circuits, IEEE Journal of*, 49(12):2868–2877, Dec 2014.

[76] Do-Yeon Yoon, S. Ho, and Hae-Seung Lee. A Continuous-Time Sturdy-MASH $\Delta\Sigma$ Modulator in 28 nm CMOS. *Solid-State Circuits, IEEE Journal of*, 50(12):2880–2890, Dec 2015.

[77] Nima Maghari, Sunwoo Kwon, and Un-Ku Moon. 74 dB SNDR multi-loop sturdy-MASH delta-sigma modulator using 35 dB open-loop opamp gain. *IEEE Journal of Solid-State Circuits*, 44(8):2212–2221, 2009.

[78] Ahmed Gharbiya and David A Johns. Combining multipath and single-path time-interleaved delta-sigma modulators. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 55(12):1224–1228, 2008.

[79] Mucahit Kozak and Izzet Kale. Novel topologies for time-interleaved delta-sigma modulators. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 47(7):639–654, 2000.

[80] Ramin Khoini-Poorfard, Lysander B Lim, and David A Johns. Time-interleaved oversampling A/D converters: Theory and practice. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 44(8):634–645, 1997.

[81] Kye-Shin Lee, Sunwoo Kwon, and Franco Maloberti. A power-efficient two-channel time-interleaved $\Sigma\Delta$ modulator for broadband applications. *IEEE Journal of Solid-State Circuits*, 42(6):1206–1215, 2007.

[82] RF Cormier, Terry L Sculley, and Roberto H Bamberger. Combining sub-band decomposition and sigma delta modulation for wideband A/D conver-

sion. In *Proceedings of IEEE International Symposium on Circuits and Systems-ISCAS'94*, volume 5, pages 357–360. IEEE, 1994.

[83] Philippe Benabes, Ali Beydoun, and Mohamad Javidan. Frequency-Band-Decomposition converters using continuous-time Sigma-Delta A/D modulators. In *2009 Joint IEEE North-East Workshop on Circuits and Systems and TAISA Conference*, pages 1–4. IEEE, 2009.

[84] Antoine Bonnetat, Han Le Duc, Ali Beydoun, Dominique Dallet, Guillaume Ferre, Jean-Michel Hode, Patricia Desgreys, and Chadi Jabbour. Time or Frequency Interleaved Analog-to-Digital Converters. In *Digitally Enhanced Mixed Signal Systems*, pages 181–235. The Institution of Engineering and Technology, 2019.

[85] D.-K.G. Pham, P. Desgreys, P. Loumeau, and T. Ridgers. Multi-stage noise band cancellation Sigma Delta modulator for digitisation of distorted signals. *Electronics Letters*, 48(10):560–562, 2012.

[86] Maurits Ortmanns and Friedel Gerfers. *Continuous-time sigma-delta A/D conversion: fundamentals, performance limits and robust implementations*. Springer, 2006.

[87] J.A. Cherry and W.M. Snelgrove. Excess loop delay in continuous-time delta-sigma modulators. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 46(4):376–389, Apr 1999.

[88] M. Vadipour, C. Chen, A. Yazdi, M. Nariman, T. Li, P. Kilcoyne, and H. Darabi. A 2.1mW/3.2mW delay-compensated GSM/WCDMA $\Delta\Sigma$ analog-digital converter. In *VLSI Circuits, 2008 IEEE Symposium on*, pages 180–181, June 2008.

[89] Chen-Yen Ho, Cong Liu, Chi-Lun Lo, Hung-Chieh Tsai, Tze-Chien Wang, and Yu-Hsin Lin. A 4.5mW CT self-coupled $\Delta\Sigma$ modulator with 2.2MHz BW and 90.4dB SNDR using residual ELD compensation. In *Solid- State Circuits Conference - (ISSCC), 2015 IEEE International*, pages 1–3, Feb 2015.

[90] P. Fontaine, A.N. Mohieldin, and A. Bellaouar. A low-noise low-voltage CT $\Delta\Sigma$ modulator with digital compensation of excess loop delay. In *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pages 498–613 Vol. 1, Feb 2005.

[91] Arindam Sanyal and Nan Sun. Dynamic Element Matching Techniques for Static and Dynamic Errors in Continuous-Time Multi-Bit $\Delta\Sigma$ Modulators. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 5(4):598–611, 2015.

[92] M. Keller, A. Buhmann, J. Sauerbrey, M. Ortmanns, and Y. Manoli. A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma Delta Modulators. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 55(11):3480–3487, Dec 2008.

[93] R. Schreier. The Delta-Sigma Toolbox v. 7.3, 2009.

[94] Hussein Fakhoury. *Conception de modulateurs Delta-Sigma Passe-bas à temps continu en technologie CMOS pour des applications large bande et haute résolution.* PhD thesis, Télécom ParisTech, 2014.

[95] Marcel JM Pelgrom, Aad CJ Duinmaijer, and Anton PG Welbers. Matching properties of MOS transistors. *IEEE Journal of solid-state circuits*, 24(5):1433–1439, 1989.

Titre : Conception d'un Convertisseur Analogique Numérique (CAN) large bande pour la linéarisation d'amplificateurs de puissance

Mots clés : CAN, Sigma Delta, MSNBC, Pré-distorsion, linéarisation, amplificateur

Résumé : De nos jours, la consommation d'énergie devient un des principaux défis à surmonter dans le développement des réseaux de communications mobiles. L'amplificateur de puissance est le composant le plus gourmand en énergie dans les stations de base. La cinquième génération de téléphonie mobile de part ses larges bandes de communication et ses modulations complexes augmente encore plus les contraintes sur l'amplificateur de puissance. Pour palier ce problème, il est courant de faire appel à des techniques de pré-distorsion. Une contrainte importante dans la mise en oeuvre de cette technique est la numérisation de la sortie de l'amplificateur qui, dû aux non-linéarités, s'étale sur un spectre significativement plus large que le signal utile, environ 5 fois en pratique voire plus.
Habituellement, pour cette opération de numérisation, un Convertisseur Analogique Numérique (CAN) du type pipeline est utilisé car il permet d'obtenir des résolutions supérieures à 10 bits sur une bande de plusieurs dizaines voire centaines de MHz. Cependant, sa consommation d'énergie élevée pousse à explorer d'autres pistes. L'architecture "Multi Stage Noise Band Cancellation" (MSNBC) à base de modulateurs Delta Sigma a l'avantage de réaliser des dynamiques différentes par sous bande et est ainsi un candidat de choix pour le CAN de la boucle de retour des techniques de pré-distortion.
L'objectif de ce travail est de démontrer la faisabilité de l'architecture MSNBC qui jusqu'à présent a été uniquement étudiée au niveau système. Ces études nous ont permis de proposer une architecture adaptée pour la numérisation d'un signal de bande RF 20 MHz avec des résolutions différentes par sous bande. Une architecture Zéro-IF temps continu avec un modulateur primaire du second ordre et un modulateur secondaire du quatrième ordre avec des quantificateurs 4 bits a été adoptée. Cette architecture a été implémentée en une technologie CMOS 65 nm. Les simulations électrique du MSNBC 2-4 avec un signal LTE ont permis d'obtenir 84.5 dB de SNDR dans la bande principale et 29.2 dB dans la bande adjacente contenant les produits d'intermodulation.

Title : Wideband Analog-to-Digital Converter Design For Power Amplifiers Linearization

Keywords : ADC, Sigma Delta, MSNBC, DPD, Linearization, Power amplifier

Summary : Power consumption is nowadays one of the main challenges to overcome in the development of mobile communications networks. The power amplifier (PA) is the most power hungry component in base transceiver stations. The upcoming fifth generation of mobile telephony with wider communication bands and complex modulations further increases the constraints on the PA. To overcome this problem, it is common to use predistortion techniques that enable the power amplifier to operate with greater linearity and efficiency. An important constraint in the implementation of this technique is the digitization of the output of the amplifier which, due to non-linearities, spreads over a significantly wider spectrum than the initial signal, about 5 times in practice or even more.
Pipeline Analog-to-Digital Converters (ADCs) are commonly used for this operation because it allows resolutions of greater than 10 bits to be obtained over a band of several tens or even hundreds of MHz. However, its high energy consumption pushes to find a better solution. The "Multi Stage Noise Band Cancellation" (MSNBC) architecture based on Delta Sigma modulators has the advantage of realizing different dynamics per subband and is thus a prime candidate for the feedback loop ADC of predistortion techniques.
The purpose of this work is to demonstrate the feasibility of the MSNBC architecture that has so far only been studied at the system level. Our investigations allowed us to propose a suitable architecture to digitize a 20 MHz RF band signal with different resolutions per subband. A continuous time Zero-IF architecture with a second-order primary modulator and a fourth-order secondary modulator with 4-bit quantizers was adopted. This architecture has been implemented in a 65 nm CMOS technology. Transistor level simulations of the 2-4 MSNBC architecture simulations with an LTE test signal resulted in 84.5 dB SNDR in the main band and 29.2 dB in the adjacent band which contains the intermodulation products.

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